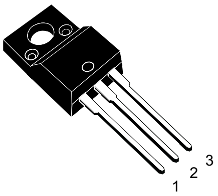
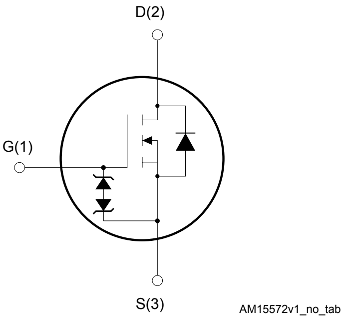
STF18N60DM2

Datasheet

N-channel 600 V, 0.260 Ω typ., 12 A MDmesh DM2 Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF18N60DM2	600 V	0.295 Ω	12 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status links
STF18N60DM2

Product summary	
Order code	STF18N60DM2
Marking	18N60DM2
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	12	A
I_D	Drain current (continuous) at T_{case}= 100 °C	7.6	A
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at T_{case} = 25 °C	25	W
dv/dt(2)	Peak diode recovery voltage slope	40	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	–55 to 150	°C
T_j	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. $I_{SD} \leq 12$, $di/dt \leq 400$ A/μs, $V_{DS(peak)} < V_{(BR)DSS}$, $V_{DD} = 400$ V
3. $V_{DS} \leq 480$ V

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.5	A
E_{AR}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	380	mJ

2 Electrical characteristics

(T_{case}= 25 °C unless otherwise specified)

Table 4. **Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.260	0.295	Ω

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	800	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	1.33	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, f = 1 MHz, V_{GS} = 0 V	-	80	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	5.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	20	-	nC
Q_{gs}	Gate-source charge		-	5.2	-	nC
Q_{gd}	Gate-drain charge		-	8.5	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 6 A R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13.5	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	9.5	-	ns
t_f	Fall time		-	32.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM} (1)	Source-drain current (pulsed)		-		48	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	125		ns
Q_{rr}	Reverse recovery charge		-	0.675		µC
I_{RRM}	Reverse recovery current		-	11		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	190		ns
Q_{rr}	Reverse recovery charge		-	1.225		µC
I_{RRM}	Reverse recovery current		-	13		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

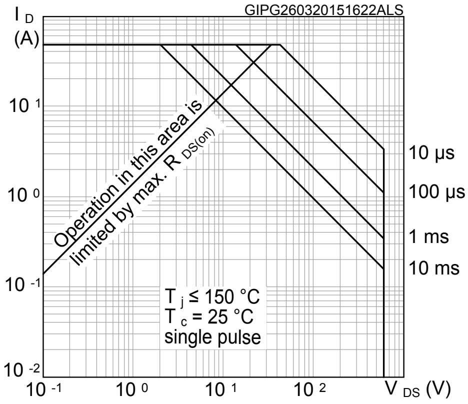


Figure 2. Thermal impedance

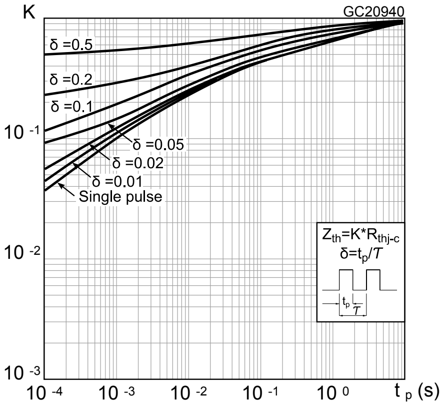


Figure 3. Output characteristics

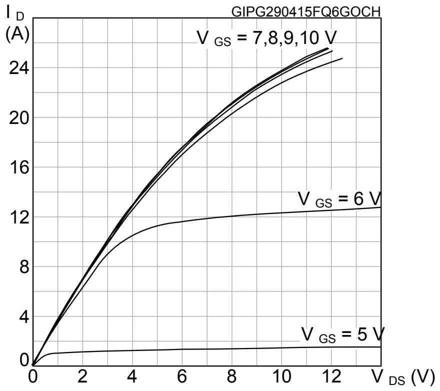


Figure 4. Transfer characteristics

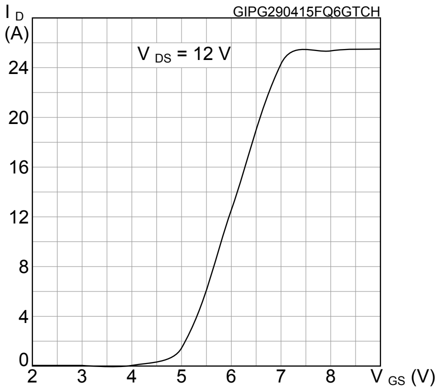


Figure 5. Gate charge vs gate-source voltage

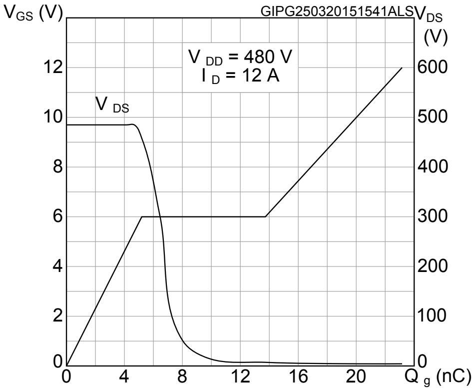


Figure 6. Static drain-source on-resistance

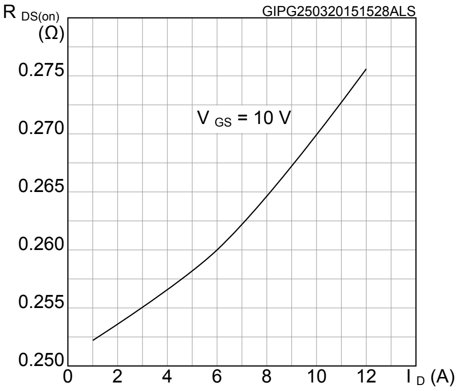


Figure 7. **Capacitance variations**

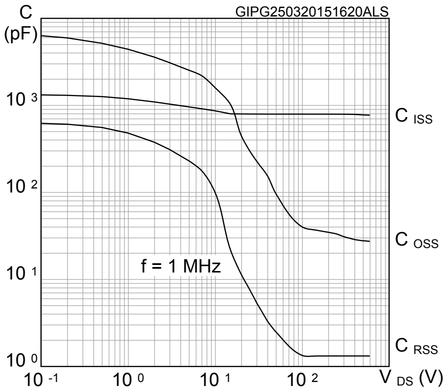


Figure 8. **Normalized gate threshold voltage vs temperature**

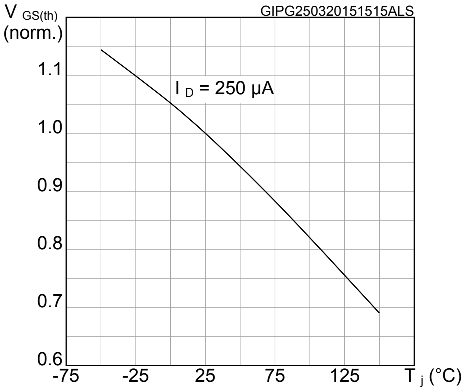


Figure 9. **Normalized on-resistance vs temperature**

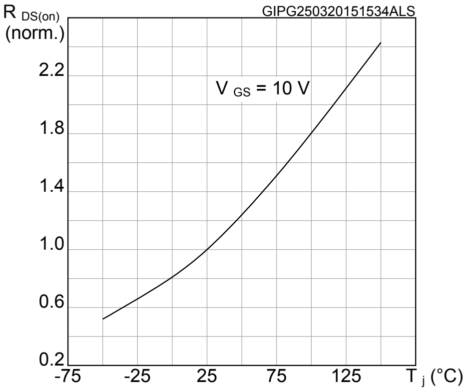


Figure 10. **Normalized $V_{(BR)DSS}$ vs temperature**

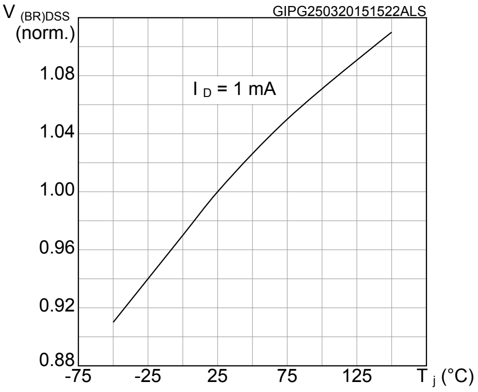


Figure 11. **Source-drain diode forward characteristics**

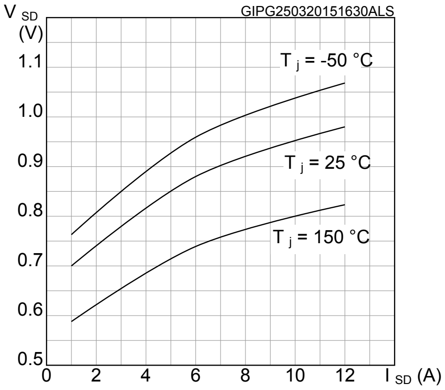
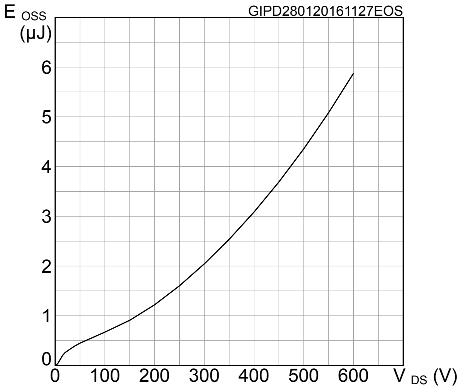


Figure 12. **Output capacitance stored energy**



3 Test circuits

Figure 13. Test circuit for resistive load switching times

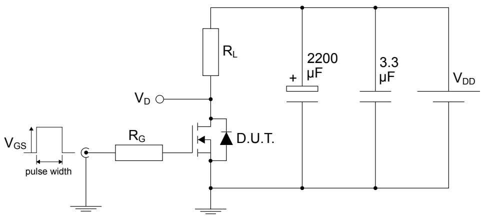


Figure 14. Test circuit for gate charge behavior

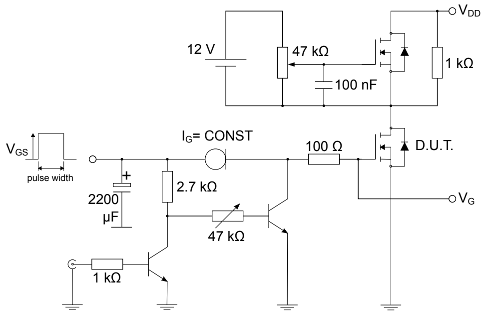


Figure 15. Test circuit for inductive load switching and diode recovery times

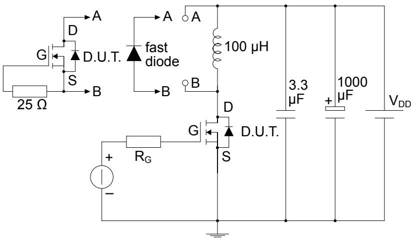


Figure 16. Unclamped inductive load test circuit

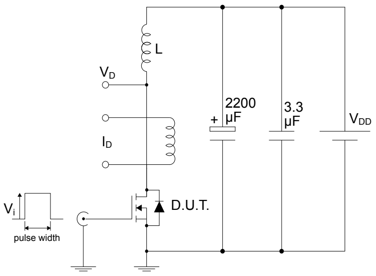


Figure 17. Unclamped inductive waveform

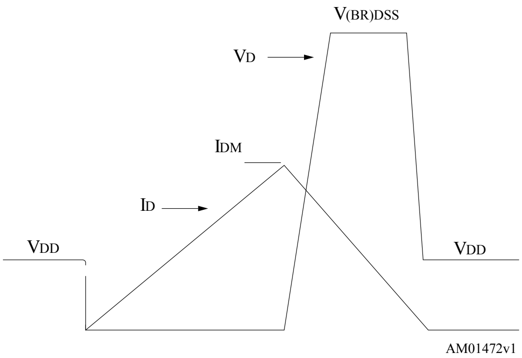
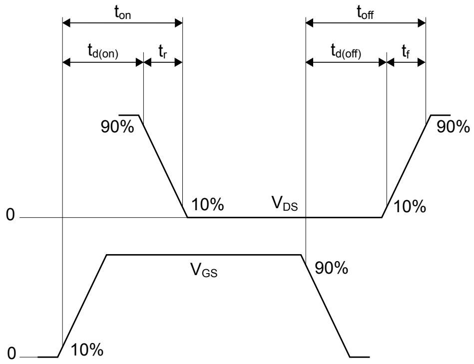


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP package information

Figure 19. TO-220FP package outline

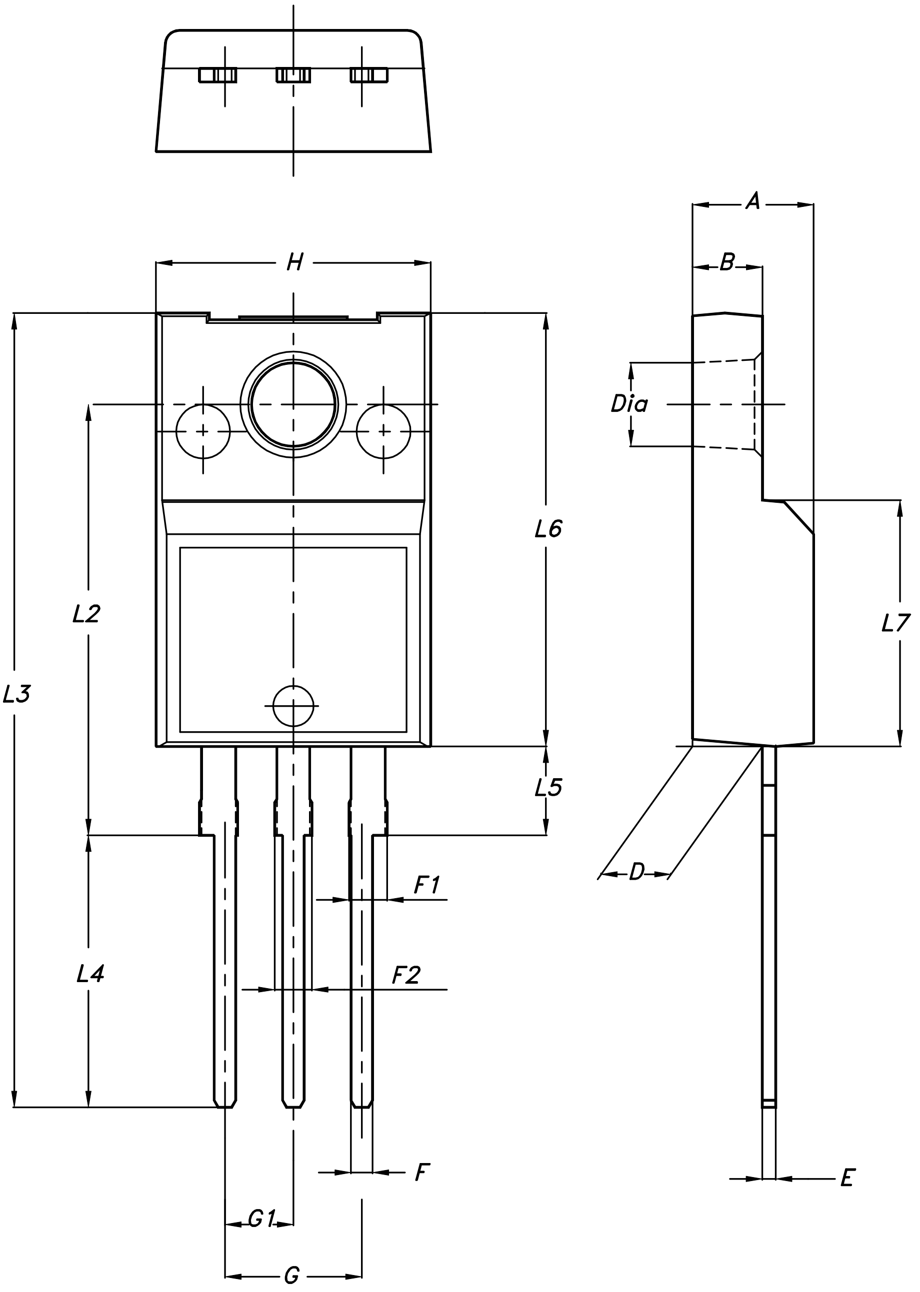


Table 8. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
01-Apr-2015	1	First release.
21-May-2015	2	Text edits throughout document In *Section 2.1 Electrical characteristics (curves)*: - updated *Figure 4: Output characteristics* - updated *Figure 5: Transfer characteristics*
02-Jul-2015	3	Updated title and I_D values in *features* and *Table 1*
28-Jan-2016	4	Updated *Section 2.1: "Electrical characteristics (curves)"*.
10-Jun-2019	5	Modified Table 1. Absolute maximum ratings, Table 2. Thermal data, Table 4. Static and Table 7. Source-drain diode. Minor text changes.

Contents

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