SDFS063A - D2932, MARCH 1987 - REVISED OCTOBER 1993

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

### description

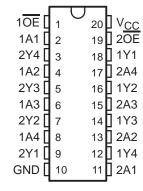
These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Taken together with the 'F240 and 'F241, these devices provide the choice of selected combinations of inverting and noninverting outputs, symmetrical  $\overline{OE}$  (active-low output-enable) inputs, and complementary  $\overline{OE}$  and  $\overline{OE}$  inputs.

The 'F244 is organized as two 4-bit buffers/line drivers with separate output enable  $(\overline{OE})$  inputs. When  $\overline{OE}$  is low, the device passes data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

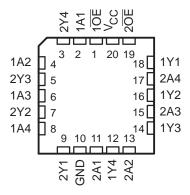
The SN74F244 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F244 is characterized for operation over the full military temperature range of  $-55^{\circ}$ C to 125°C. The SN74F244 is characterized for operation from 0°C to 70°C.

#### SN54F244 . . . J PACKAGE SN74F244 . . . DB, DW, OR N PACKAGE (TOP VIEW)



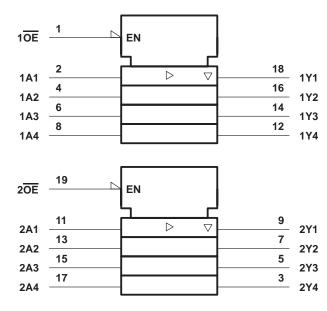
# SN54F244 . . . FK PACKAGE (TOP VIEW)



FUNCTION TABLE (each buffer)

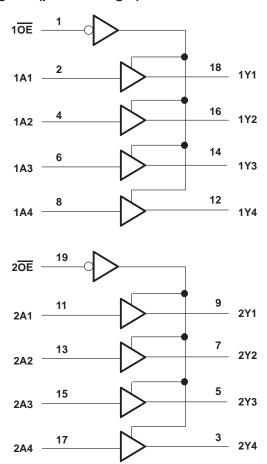
INP	JTS	OUTPUT
OE	Α	Υ
L	Н	Н
L	L	L
Н	Χ	Z

# logic symbol†



<sup>&</sup>lt;sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

# logic diagram (positive logic)



# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V <sub>CC</sub>		–1.2 V to 7 V
Voltage range applied to any output in		
Voltage range applied to any output in	•	
Current into any output in the low state	S .	90
, ,		128 mA
Operating free-air temperature range:		
	SN74F244	0°C to 70°C
Storage temperature range		–65°C to 150°C

<sup>‡</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

# recommended operating conditions

		SN54F2			SN74F244			LINUT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
VCC	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.8			8.0	V
liK	Input clamp current			-18			-18	mA
lOH	High-level output current			- 12			- 15	mA
loL	Low-level output current			48			64	mA
TA	Operating free-air temperature	-55		125	0		70	°C

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

BAB AMET		TEST CONDITIONS				S	N74F24	1		
PARAMETER	TES	ST CONDITIONS	MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK	V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = –18 mA			-1.2			-1.2	V	
		$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3			
V	V <sub>CC</sub> = 4.5 V	$I_{OH} = -12 \text{ mA}$	2	3.2					.,	
VOH		$I_{OH} = -15 \text{ mA}$				2	3.1		V	
	$V_{CC} = 4.75 \text{ V},$	IOH = -3  mA				2.7				
	V 45V	I <sub>OL</sub> = 48 mA		0.38	0.55				V	
V <sub>OL</sub>	$V_{CC} = 4.5 \text{ V}$	I <sub>OL</sub> = 64 mA					0.42	0.55	V	
lozh	V <sub>C</sub> C = 5.5 V,	V <sub>O</sub> = 2.7 V			50			50	μΑ	
lozL	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0.5 V			-50			-50	μΑ	
II	V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 7 V			0.1			0.1	mA	
I <sub>IH</sub>	$V_{CC} = 5.5 \text{ V},$	V <sub>I</sub> = 2.7 V			20			20	μΑ	
. OE	.,,				– 1			- 1		
I <sub>IL</sub> Any A	$V_{CC} = 5.5 \text{ V},$	$V_{  } = 0.5 V$		- 1.6					mA	
los <sup>‡</sup>	V <sub>CC</sub> = 5.5 V,	V <sub>O</sub> = 0	-100		-225	-100		-225	mA	
		Outputs high		40	60		40	60		
ICC	$V_{CC} = 5.5 \text{ V},$	Outputs low		60	90		60	90	mA	
	Outputs open	Outputs disabled		60	90		60	90		

<sup>†</sup> All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C. ‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

# SN54F244, SN74F244 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS SDFS063A – D2932, MARCH 1987 – REVISED OCTOBER 1993

# switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C <sub>i</sub> R <sub>i</sub>	$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			$V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 $\Omega$ , $T_A$ = MIN to MAX†			
			′F244			SN54		SN74F244		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> PLH	Α	Y	1.7	3.6	5.2	2	6.5	1.7	6.2	ns
<sup>t</sup> PHL	A	Y	1.7	3.6	5.2	2	7	1.7	6.5	
<sup>t</sup> PZH	ŌĒ	Y	1.2	3.9	5.7	2	7	1.2	6.7	
<sup>t</sup> PZL	OE	Y	1.2	5	7	2	8.5	1.2	8	ns
<sup>t</sup> PHZ	ŌĒ	V	1.2	4.1	6	2	7	1.2	7	ne
t <sub>PLZ</sub>	OE	Y	1.2	4.1	6	2	7.5	1.2	7	ns

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.







24-Jan-2013

### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
5962-9758601Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	-55 to 125	5962- 9758601Q2A SNJ54F 244FK	Samples
5962-9758601QRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Call TI	-55 to 125	5962-9758601QR A SNJ54F244J	Samples
5962-9758601QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	Call TI	-55 to 125	5962-9758601QS A SNJ54F244W	Samples
JM38510/33203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 33203B2A	Samples
JM38510/33203BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33203BRA	Samples
JM38510/33203BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 33203BSA	Samples
M38510/33203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 33203B2A	Samples
M38510/33203BRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 33203BRA	Samples
M38510/33203BSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	JM38510/ 33203BSA	Samples
SN54F244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54F244J	Samples
SN74F244DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
SN74F244DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Samples
SN74F244DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Samples
SN74F244DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Samples
SN74F244DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Samples
SN74F244DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Samples





www.ti.com 24-Jan-2013

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
SN74F244DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Sample
SN74F244DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F244	Sample
SN74F244N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F244N	Sample
SN74F244N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74F244NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F244N	Sample
SN74F244NSLE	OBSOLETE	SO	NS	20		TBD	Call TI	Call TI	0 to 70		
SN74F244NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74F244	Sample
SN74F244NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74F244	Sample
SN74F244NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74F244	Sample
SNJ54F244FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9758601Q2A SNJ54F 244FK	Sample
SNJ54F244J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9758601QR A SNJ54F244J	Sample
SNJ54F244W	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9758601QS A SNJ54F244W	Sample

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



# PACKAGE OPTION ADDENDUM

24-Jan-2013

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Only one of markings shown within the brackets will appear on the physical device.

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#### OTHER QUALIFIED VERSIONS OF SN54F244, SN74F244:

Catalog: SN74F244

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Military: SN54F244

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

www.ti.com 26-Mar-2013

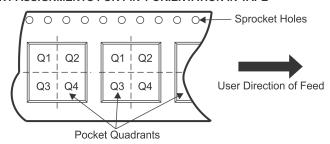
# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

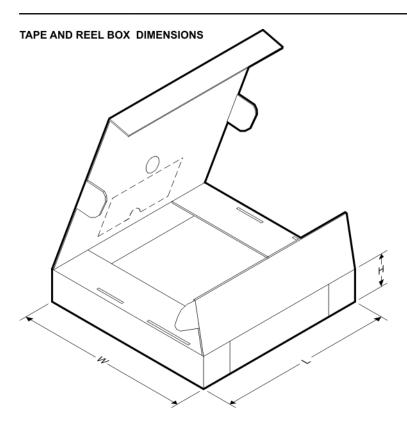
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F244DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74F244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74F244DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

www.ti.com 26-Mar-2013



#### \*All dimensions are nominal

7 til diritoriorio di o riorini di							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F244DBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74F244DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74F244DWR	SOIC	DW	20	2000	367.0	367.0	45.0

#### 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F20)

# CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



# FK (S-CQCC-N\*\*)

# LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



# N (R-PDIP-T\*\*)

# PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

# PLASTIC SMALL OUTLINE



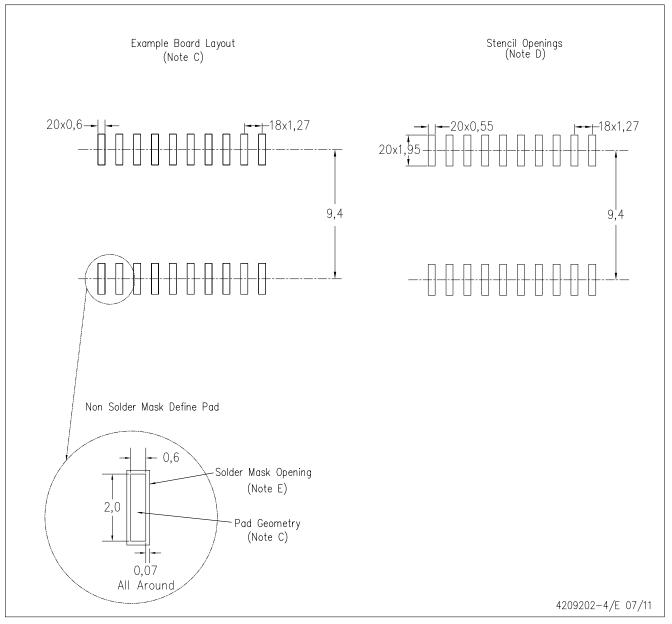
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# **MECHANICAL DATA**

# NS (R-PDSO-G\*\*)

# 14-PINS SHOWN

### PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



# DB (R-PDSO-G\*\*)

# PLASTIC SMALL-OUTLINE

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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DSP **Energy and Lighting** dsp.ti.com www.ti.com/energy Clocks and Timers www.ti.com/clocks Industrial www.ti.com/industrial Interface interface.ti.com Medical www.ti.com/medical logic.ti.com Logic Security www.ti.com/security

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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001:
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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