8th Generation Intel® Processor Family for S-Processor Platforms

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Revision History

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001	• Initial release	October 2017

§ §

1 Introduction

The 8th Generation Intel® Processor Family for S-Processor is built on 14-nanometer process technology.

The S-Processor Line is offered in a 2-Chip Platform. See Figure 1-1.

The following table describes the processor lines covered in this document.

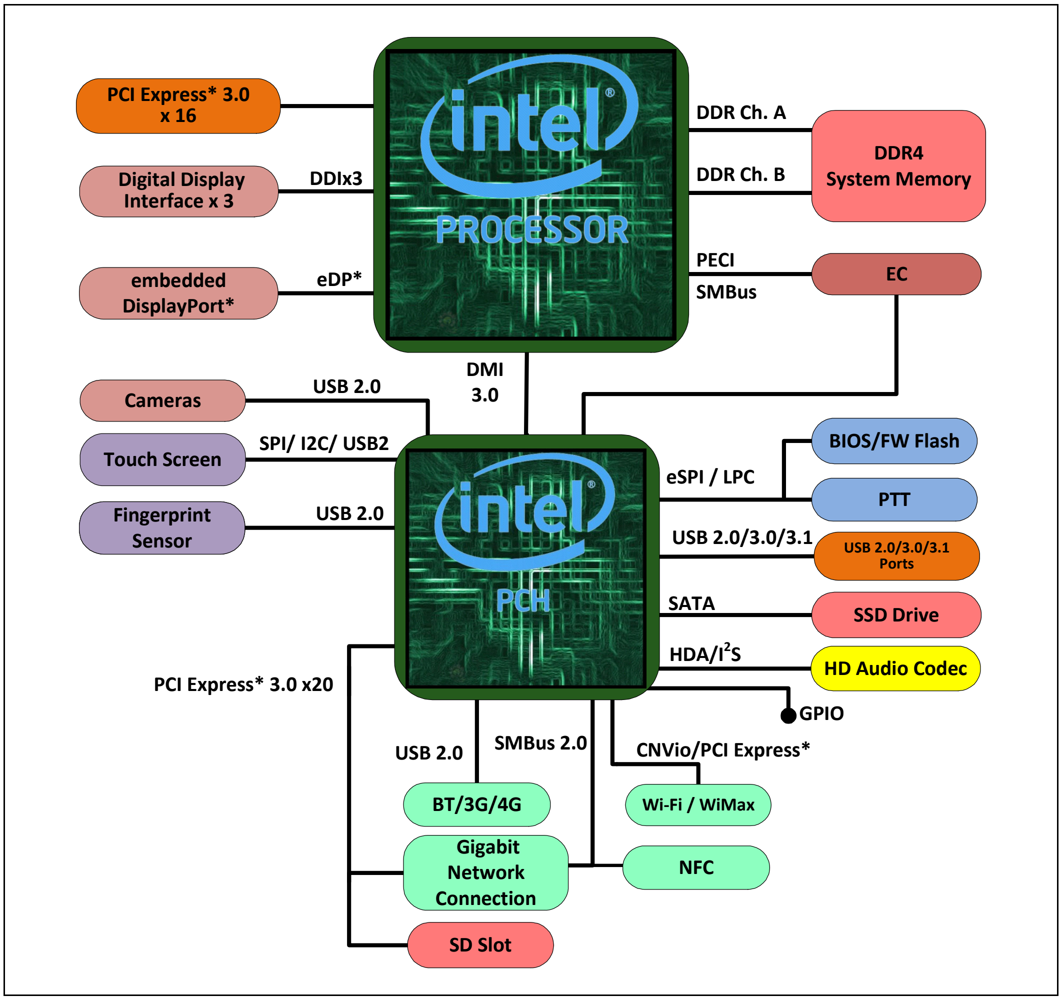
Table 1-1. Processor Lines

Processor Line[1]	Package	Base TDP	Processor IA Cores	Graphics Configuration	Platform Type
S-Processor Line (DT)	LGA1151	65W, 95W	6	GT2	2-Chip
			4	GT2	

Notes:
1. Processor Lines offering may change.
2. N/A
3. The S-Processor (DT) 65W & 95W TDP (6+2 & 4+2) SKUs are paired with the PCH-H Intel® Z370 chipset.

Throughout this document, the 8th Generation Intel® Processor Family for S-Processor family may be referred to simply as "processor". The Intel® Z370 Series Chipset Family Platform Controller Hub (PCH) may be referred to simply as "PCH".

Figure 1-1. S-Processor Line Platform



1.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT)
- Intel® Active Management Technology 11.0 (Intel® AMT 11.0)
- Intel® Trusted Execution Technology (Intel® TXT)
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® 64 Architecture
- Execute Disable Bit
- Intel® Turbo Boost Technology 2.0
- Intel® Advanced Vector Extensions 2 (Intel® AVX2)
- Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)
- PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction
- Intel® Secure Key
- Intel® Transactional Synchronization Extensions (Intel® TSX-NI)
- PAIR – Power Aware Interrupt Routing
- SMEP – Supervisor Mode Execution Protection
- Intel® Boot Guard
- Intel® Software Guard Extensions (Intel® SGX)
- Intel® Memory Protection Extensions (Intel® MPX)
- GMM Scoring Accelerator
- Intel® Processor Trace
- High Definition Content Protection (HDCP) 2.2

Note: The availability of the features may vary between processor SKUs.

Refer to Chapter 3 for more information.

1.2 Power Management Support

1.2.1 Processor Core Power Management

- Full support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3, C6, C7, C8
- Enhanced Intel SpeedStep® Technology

Note: Package C-states above C8 are not supported in S-Processor Line paired with Intel® Z370 Series Chipset PCH-H.

Refer to Section 4.2 for more information.

1.2.2 System Power Management

- S0/S0ix, S3, S4, S5

Refer to Chapter 4, “Power Management” for more information.

1.2.3 Memory Controller Power Management

- Disabling Unused System Memory Outputs
- DRAM Power Management and Initialization
- Initialization Role of CKE
- Conditional Self-Refresh
- Dynamic Power Down
- DRAM I/O Power Management
- DDR Electrical Power Gating (EPG)
- Power training

Refer to Section 4.3 for more information.

1.2.4 Processor Graphics Power Management

1.2.4.1 Memory Power Savings Technologies

- Intel Rapid Memory Power Management (Intel RMPM)
- Intel Smart 2D Display Technology (Intel S2DDT)

1.2.4.2 Display Power Savings Technologies

- Intel (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP port
- Intel Automatic Display Brightness
- Smooth Brightness
- Intel Display Power Saving Technology (Intel DPST 6)
- Panel Self-Refresh 2 (PSR 2)
- Low Power Single Pipe (LPSP)

1.2.4.3 Graphics Core Power Savings Technologies

- Intel Graphics Dynamic Frequency
- Intel Graphics Render Standby Technology (Intel GRST)
- Dynamic FPS (Intel DFPS)

Refer to Section 4.6 for more information.

1.3 Thermal Management Support

- Digital Thermal Sensor
- Intel Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Memory Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS
- Intel Turbo Boost Technology 2.0 Power Control

Refer to Chapter 5, “Thermal Management” for more information.

1.4 Package Support

- The processor is available in A 37.5 mm x 37.5 mm LGA package (LGA1151) for S-Processor Line

1.5 Ballout Information

The processor ball information is available in Chapter 9, “Processor Ball Information”.

1.6 Processor Testability

An XDP on-board connector is warmly recommended to enable full debug capabilities. For the processor SKUs, a merged XDP connector is highly recommended to enable lower C-state debug.

Note: When separate XDP connectors will be used at C8 state, the processor will need to be waked up using the PCH.

The processor includes boundary-scan for board and system level testability.

1.7 Terminology

Table 1-2. Terminology (Sheet 1 of 3)

Term	Description
4K	Ultra High Definition (UHD)
AES	Advanced Encryption Standard
AGC	Adaptive Gain Control
BLT	Block Level Transfer
BPP	Bits per pixel
CDR	Clock and Data Recovery

Table 1-2. Terminology (Sheet 2 of 3)

Term	Description
CTLE	Continuous Time Linear Equalizer
DDI	Digital Display Interface for DP or HDMI/DVI
DDR4/DDR4-RS	Fourth-Generation Double Data Rate SDRAM Memory Technology RS - Reduced Standby Power
DFE	decision feedback equalizer
DMA	Direct Memory Access
DMI	Direct Media Interface
DP	DisplayPort*
DTS	Digital Thermal Sensor
eDP*	embedded DisplayPort*
EU	Execution Unit in the Processor Graphics
GSA	Graphics in System Agent
HDCP	High-bandwidth Digital Content Protection
HDMI*	High Definition Multimedia Interface
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® DPST	Intel Display Power Saving Technology
Intel® PTT	Intel Platform Trust Technology
Intel® TSX-NI	Intel Transactional Synchronization Extensions
Intel® TXT	Intel Trusted Execution Technology
Intel® VT	Intel Virtualization Technology. Processor virtualization, when used in conjunction with Virtual Machine Monitor software, enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel Virtualization Technology (Intel VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
ISP	Image Signal Processor
LFM	Low Frequency Mode. corresponding to the Enhanced Intel SpeedStep® Technology's lowest voltage/frequency pair. It can be read at MSR CEh [47:40].
LLC	Last Level Cache
LPM	Low-Power Mode.The LPM Frequency is less than or equal to the LFM Frequency. The LPM TDP is lower than the LFM TDP as the LPM configuration limits the processor to single thread operation
LPSP	Low-Power Single Pipe
LSF	Lowest Supported Frequency.This frequency is the lowest frequency where manufacturing confirms logical functionality under the set of operating conditions.
MCP	Multi Chip Package - includes the processor and the PCH.
MFM	Minimum Frequency Mode. MFM is the minimum ratio supported by the processor and can be read from MSR CEh [55:48].
MLC	Mid-Level Cache
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved balls/lands, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PCH	Platform Controller Hub. The chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security, and storage features. The PCH may also be referred as "chipset".
PECI	Platform Environment Control Interface

Table 1-2. Terminology (Sheet 3 of 3)

Term	Description
PEG	PCI Express Graphics
PL1, PL2, PL3	Power Limit 1, Power Limit 2, Power Limit 3
Processor	The 64-bit multi-core component (package)
Processor Core	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the LLC.
Processor Graphics	Intel Processor Graphics
PSR	Panel Self-Refresh
Rank	A unit of DRAM corresponding to four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SODIMM.
SCI	System Control Interrupt. SCI is used in the ACPI protocol.
SDP	Scenario Design Power.
SGX	Software Guard Extension
SHA	Secure Hash Algorithm
SSC	Spread Spectrum Clock
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased, or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material), the processor should be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
STR	Suspend to RAM
TAC	Thermal Averaging Constant
TCC	Thermal Control Circuit
TDP	Thermal Design Power
TOB	Tolerance Budget
TTV TDP	Thermal Test Vehicle TDP
V_{CC}	Processor core power supply
V_{CCGT}	Processor Graphics Power Supply
V_{CCIO}	I/O Power Supply
V_{CCSA}	System Agent Power Supply
V_{CCST}	Vcc Sustain Power Supply
V_{DDQ}	DDR Power Supply
VLD	Variable Length Decoding
VPID	Virtual Processor ID
V_{SS}	Processor Ground

1.8 Related Documents

Table 1-3. Related Documents (Sheet 1 of 2)

Document	Document Number
8th Generation Intel® Processor Family for S-Processor Platform Datasheet Volume 2	336465
8th Generation Intel® Processor Family for S-Processor Platform Specification Update	336466
Advanced Configuration and Power Interface 3.0	http://www.acpi.info/
DDR4 Specification	http://www.jedec.org

Table 1-3. Related Documents (Sheet 2 of 2)

Document	Document Number
High Definition Multimedia Interface specification revision 1.4	http://www.hdmi.org/manufacturer/specification.aspx
Embedded DisplayPort* Specification revision 1.4	http://www.vesa.org/vesa.standards/
DisplayPort* Specification revision 1.2	http://www.vesa.org/vesa.standards/
PCI Express* Base Specification Revision 3.0	http://www.pcisig.com/specifications
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm

§ §

2 Interfaces

2.1 System Memory Interface

- Two channels of DDR4 memory with a maximum of two DIMMs per channel. DDR technologies, number of DIMMs per channel, number of ranks per channel are SKU dependent.
- UDIMM, SO-DIMM, and Memory Down support (based on SKU)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR4 I/O Voltage of 1.2V
- 64-bit wide channels
- Non-ECC UDIMM and SODIMM DDR4 support (based on SKU)
- Theoretical maximum memory bandwidth of:
    - 29.1 GB/s in dual-channel mode assuming 1866 MT/s
    - 33.3 GB/s in dual-channel mode assuming 2133 MT/s
    - 37.5 GB/s in dual-channel mode assuming 2400 MT/s
    - 41.6 GB/s in dual-channel mode assuming 2666 MT/s

Note: Memory down of all technologies (DDR4) should be implemented homogeneously, which means that all DRAM devices should be from the same vendor and have the same part number. Implementing a mix of DRAM devices may cause serious signal integrity and functional issues.

Note: If the S-Processor Line's memory interface is configured to one DIMM per Channel, the processor can use either of the DIMMs, DIMM0 or DIMM1, signals CTRL[1:0] or CTRL[3:2].

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR4 protocols with two independent, 64-bit wide channels.

Table 2-1. Processor DDR Memory Speed Support (Sheet 1 of 2)

Processor Line	DDR4 1DPC [MT/s]	DDR4 2DPC [MT/s]	LPDDR3 [MT/s]
S-Processor Line (AIO SODIMM)	2400[3]	2133[2]	N/A
S-Processor Line (DT UDIMM) 6+2	2666	2666[4]	N/A
S-Processor Line (DT UDIMM) 4+2	2400	2400	N/A

Table 2-1. Processor DDR Memory Speed Support (Sheet 2 of 2)

Processor Line	DDR4 1DPC [MT/s]	DDR4 2DPC [MT/s]	LPDDR3 [MT/s]

Notes:
1. 1DPC-refer to 1 DIMM per channel natively, means 1 DIMM Slot per channel and not refer to 1 DIMM populated at 2 DIMMs per channel.
   2DPC-refer to 2DIMMs per channel, fully populated or partially populated with 1 DIMM only.
2. S-Processor SO-DIMM 2DPC is limited to 2133 MT/s due to Daisy Chain topology.
3. DDR4 SODIMM 2666 MT/s is currently NOT POR, DDR4 SODIMM 2666MT/s enabling is pending silicon validation completion.
4. S-Processor 6+2 DDR4 2666 MT/s 2DPC UDIMM is supported when channel is populated with the same UDIMM part number.
5. DDR4 2666 MT/s support is limited to raw card versions A, C, E, D and G.

- DDR4 Data Transfer Rates:
  - 2133 MT/s (PC4-2133)
  - 2400 MT/s (PC4-2400)
  - 2666 MT/s (PC4-2666)
- UDIMM Modules:

  DDR4 SODIMM/UDIMM Modules:
  - Standard 4-Gb and 8-Gb technologies and addressing are supported for x8 and x16 devices.

  There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.
- DDR4 Memory Down: Single rank x8, x16 (based on SKU)

2.1.1.1 DDR4 Supported Memory Modules and Devices

Table 2-2. Supported DDR4 Non-ECC UDIMM Module Configurations

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	4GB	4Gb	512M x 8	8	1	15/10	16	8K
A	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
B	8GB	4Gb	512M x 8	16	2	15/10	16	8K
B	16GB	8Gb	1024M x 8	16	2	16/10	16	8K
C	2GB	4Gb	256M x 16	4	1	15/10	8	8K
C	4GB	8Gb	512M x 16	4	1	16/10	8	8K

Table 2-3. Supported DDR4 Non-ECC SODIMM Module Configurations (Sheet 1 of 2)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
A	4GB	4Gb	512M x 8	8	1	15/10	16	8K
A	8GB	8Gb	1024M x 8	8	1	16/10	16	8K
B	8GB	4Gb	512M x 8	16	2	15/10	16	8K
B	16GB	8Gb	1024M x 8	16	2	16/10	16	8K

Table 2-3. Supported DDR4 Non-ECC SODIMM Module Configurations (Sheet 2 of 2)

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
C	2GB	4Gb	256M x 16	4	1	15/10	8	8K
C	4GB	8Gb	512M x 16	4	1	16/10	8	8K
E	8GB	4Gb	512M x 8	16	2	15/10	16	8K
E	16GB	8Gb	1024M x 8	16	2	16/10	16	8K

2.1.2 System Memory Timing Support

The IMC supports the following DDR Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes:
  - 1N indicates a new DDR4 command may be issued every clock
  - 2N indicates a new DDR4 command may be issued every 2 clocks

Table 2-4. DRAM System Memory Timing Support

DRAM Device	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC (SODIMM Only)	CMD Mode
DDR4	2133	15/16	14/15/16	15/16	11/14/14	1 or 2	1N/2N
DDR4	2400	17	17	17	12/16/16	1 or 2	2N
DDR4	2666	19	19	19	9/10/11/12/14/16/18	1 or 2	2N

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the DDR Schema and DIMM Modules are populated in each memory channel, a number of different configurations can exist.

Single-Channel Mode

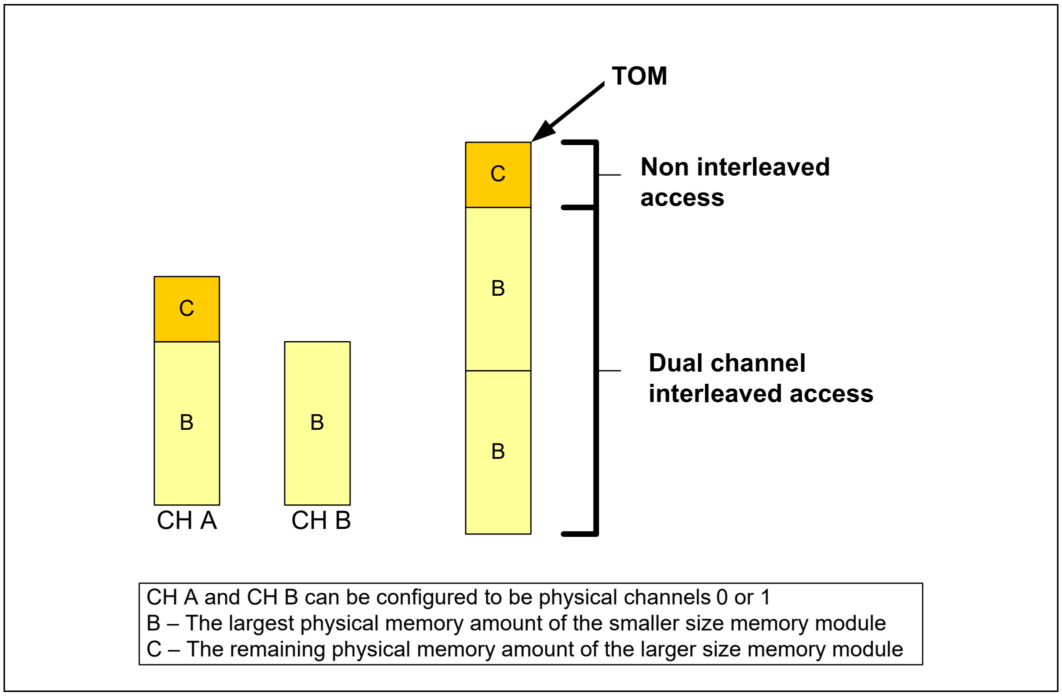
In this mode, all memory cycles are directed to a single channel. Single-Channel mode is used when either the Channel A or Channel B DIMM connectors are populated in any order, but not both.

Dual-Channel Mode – Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. Memory is divided into a symmetric and asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa. However, channel A size should be greater or equal to channel B size.

Figure 2-1. Intel® Flex Memory Technology Operations



CH A and CH B can be configured to be physical channels 0 or 1
B – The largest physical memory amount of the smaller size memory module
C – The remaining physical memory amount of the larger size memory module

Dual-Channel Symmetric Mode (Interleaved Mode)

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.1.4 System Memory Frequency

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For Dual-Channel modes both channels should have a DIMM connector populated. For Single-Channel mode, only a single channel can have a DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 Data Scrambling

The system memory controller incorporates a Data Scrambling feature to minimize the impact of excessive di/dt on the platform system memory VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result, the system memory controller uses a data scrambling feature to create pseudo-random patterns on the system memory data bus to reduce the impact of any excessive di/dt.

2.1.7 DDR I/O Interleaving

The processor supports I/O interleaving, which has the ability to swap DDR bytes for routing considerations. BIOS configures the I/O interleaving mode before DDR training.There are 2 supported modes:

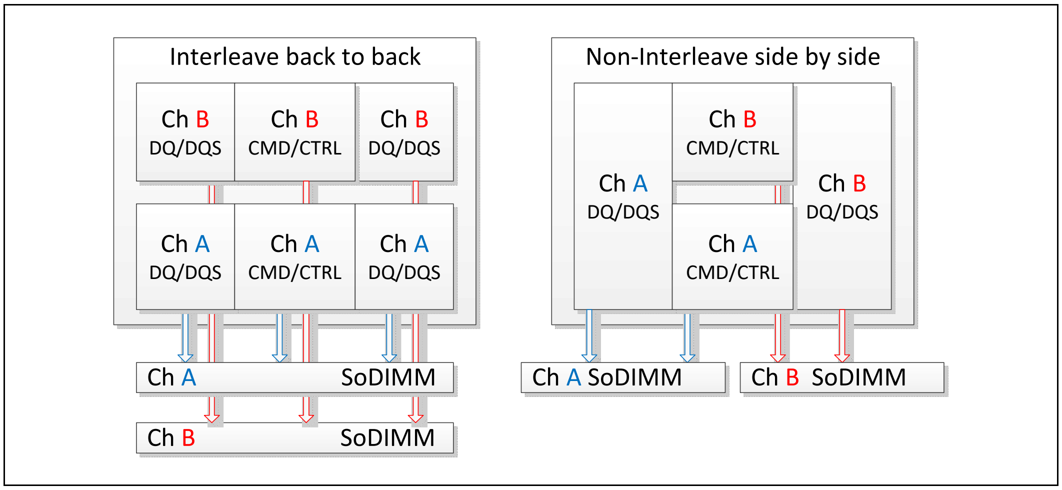
- Interleave (IL)
- Non-Interleave (NIL)

The following table and figure describe the pin mapping between the IL and NIL modes.

Table 2-5. Interleave (IL) and Non-Interleave (NIL) Modes Pin Mapping

IL (DDR4)		**NIL (DDR4**	
Channel	**Byte**	**Channel**	**Byte**
DDR0	Byte0	DDR0	Byte0
DDR0	Byte1	DDR0	Byte1
DDR0	Byte2	DDR0	Byte4
DDR0	Byte3	DDR0	Byte5
DDR0	Byte4	DDR1	Byte0
DDR0	Byte5	DDR1	Byte1
DDR0	Byte6	DDR1	Byte4
DDR0	Byte7	DDR1	Byte5
DDR1	Byte0	DDR0	Byte2
DDR1	Byte1	DDR0	Byte3
DDR1	Byte2	DDR0	Byte6
DDR1	Byte3	DDR0	Byte7
DDR1	Byte4	DDR1	Byte2
DDR1	Byte5	DDR1	Byte3
DDR1	Byte6	DDR1	Byte6
DDR1	Byte7	DDR1	Byte7

Figure 2-2. Interleave (IL) and Non-Interleave (NIL) Modes Mapping



2.1.8 Data Swapping

By default, the processor supports on-board data swapping in two manners (for all segments and DRAM technologies):

- byte (DQ+DQS) swapping between bytes in the same channel.
- bit swapping within specific byte.

2.1.9 DRAM Clock Generation

Every supported rank has a differential clock pair. There are a total of four clock pairs driven directly by the processor to DRAM.

2.1.10 DRAM Reference Voltage Generation

The memory controller has the capability of generating the DDR4 Reference Voltage (VREF) internally for both read and write operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced training procedures in order to provide the best voltage to achieve the best signal margins.

2.1.11 Data Swizzling

All Processor Lines does not have die-to-package DDR swizzling.

2.2 PCI Express* Graphics Interface (PEG)

This section describes the PCI Express* interface capabilities of the processor.

2.2.1 PCI Express* Support

The processor's PCI Express* interface is a 16-lane (x16) port that can also be configured as multiple ports at narrower widths (see Table 2-6, Table 2-7).

The processor supports the configurations shown in the following table.

Table 2-6. PCI Express* Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes															
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	1	1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 **Reversed**	x16	N/A	N/A	1	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1x8+2x4	x8	x4	x4	0	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
1x8+2x4 **Reversed**	x8	x4	x4	0	0	0	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. For CFG bus details, refer to Section 6.4.
2. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
3. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   - — Connect lane 0 of 1st device to lane 0.
   - — Connect lane 0 of 2nd device to lane 8.
   - — Connect lane 0 of 3rd device to lane 12.

   For example:
   a. When using 1x8 + 2x4, the 8 lane device should use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device should use lanes 0:3, and other 2 lanes device should use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device should use lanes 0:3, two lane device should use lanes 8:9, one lane device should use lane 12.
4. for reversal lanes, for example:
   When using 1x8, the 8 lane device should use lanes 8:15, so lane 15 will be connected to lane 0 of the Device.

The processor supports the following:

- Hierarchical PCI-compliant configuration mechanism for downstream devices
- Traditional PCI style traffic (asynchronous snooped, PCI ordering)
- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express* Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion
- Automatic discovery, negotiation, and training of link out of reset.
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0: DMI -> PCI Express* Port 0
- 64-bit downstream address format, but the processor never generates an address above 512 GB (Bits 63:39 will always be zeros)
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 512 GB (addresses where any of Bits 63:39 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 512 GB will be dropped.
- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status
- PCI Express* reference clock is 100-MHz differential clock

- Power Management Event (PME) functions
- Dynamic width capability
- Message Signaled Interrupt (MSI and MSI-X) messages
- Lane reversal
- Full Advance Error Reporting (AER) and control capabilities are supported only on Server SKUs.

The following table summarizes the transfer rates and theoretical bandwidth of PCI Express* link.

Table 2-7. PCI Express* Maximum Transfer Rates and Theoretical Bandwidth

PCI Express* Generation	Encoding	Maximum Transfer Rate [GT/s]	Theoretical Bandwidth [GB/s]				
			x1	x2	x4	x8	x16
Gen 1	8b/10b	2.5	0.25	0.5	1.0	2.0	4.0
Gen 2	8b/10b	5	0.5	1.0	2.0	4.0	8.0
Gen 3	128b/130b	8	1.0	2.0	3.9	7.9	15.8

Note: The processor has limited support for Hot-Plug. For details, refer to Section 4.4.

2.2.2 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express* configuration uses standard mechanisms as defined in the PCI Plug and-Play specification. The processor PCI Express* ports support Gen 3.
At 8 GT/s, Gen3 operation results in twice as much bandwidth per lane as compared to Gen 2 operation. The 16 lanes port can operate at 2.5 GT/s, 5 GT/s, or 8 GT/s.

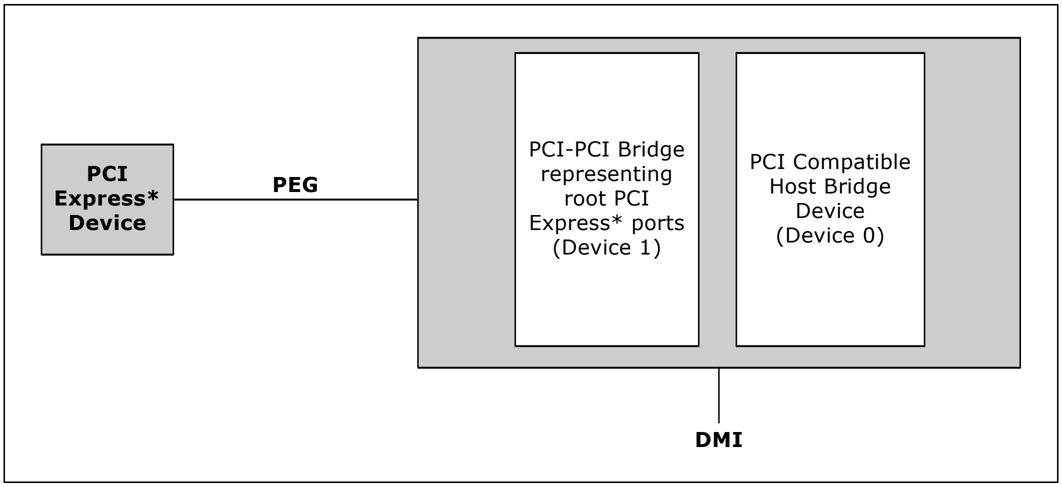
Gen 3 PCI Express* uses a 128b/130b encoding which is about 23% more efficient than the 8b/10b encoding used in Gen 1 and Gen 2.

The PCI Express* architecture is specified in three layers – Transaction Layer, Data Link Layer, and Physical Layer. See the *PCI Express Base Specification 3.0* for details of PCI Express* architecture.

2.2.3 PCI Express* Configuration Mechanism

The PCI Express* (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 2-3. PCI Express* Related Register Structures in the Processor



PCI Express* extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the conventional PCI specification. PCI Express* configuration space is divided into a PCI-compatible region (that consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express* region (that consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express* configuration access mechanism described in the PCI Express* Enhanced Configuration Mechanism section.

The PCI Express* Host Bridge is required to translate the memory-mapped PCI Express* configuration space accesses from the host processor to PCI Express* configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the PCI Express Base Specification for details of both the PCI-compatible and PCI Express* Enhanced configuration mechanisms and transaction rules.

2.2.4 PCI Express* Equalization Methodology

Link equalization requires equalization for both TX and RX sides for the processor and for the End point device.

Adjusting transmitter and receiver of the lanes is done to improve signal reception quality and for improving link robustness and electrical margin.

The link timing margins and voltage margins are strongly dependent on equalization of the link.

The processor supports the following:

- Full TX Equalization: Three Taps Linear Equalization (Pre, Current and Post cursors), with FS/LF (Full Swing /Low Frequency) 24/8 values respectively.

- Full RX Equalization and acquisition for: AGC (Adaptive Gain Control), CDR (Clock and Data Recovery), adaptive DFE (decision feedback equalizer) and adaptive CTLE peaking (continuous time linear equalizer).
- Full adaptive phase 3 EQ compliant with PCI Express* Gen 3 specification

See the *PCI Express* Base Specification 3.0* for details on PCI Express* equalization.

2.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) connects the processor and the PCH.

Main characteristics:

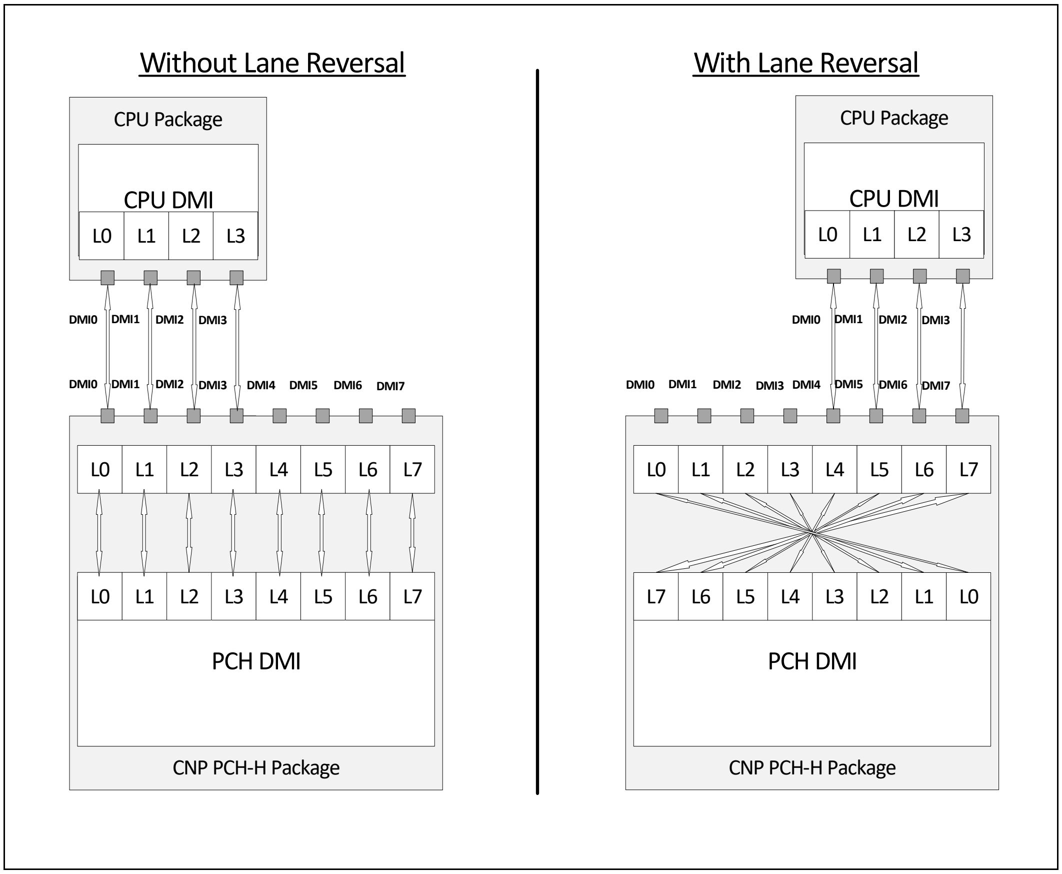
- 4 lanes Gen 3 DMI support
- 8 GT/s point-to-point DMI interface to PCH
- DC coupling - no capacitors between the processor and the PCH
- PCH end-to-end lane reversal across the link
- Half-Swing support (low-power/low-voltage)

Note: Only DMI x4 configuration is supported.

2.3.1 DMI Lane Reversal and Polarity Inversion

Note: Polarity Inversion and Lane Reversal on DMI Link are not allowed in S-Processor Line paired with Intel® Z370 Series Chipset PCH-H.

Figure 2-4. Example for DMI Lane Reversal Connection



2.3.2 DMI Error Flow

DMI can only generate SERR in response to errors; never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.3 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This link behavior is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Processor Graphics

The processor graphics is based on Gen 9 LP (generation 9 Low Power) graphics core architecture that enables substantial gains in performance and lower-power consumption over prior generations.

The processor graphics architecture delivers high dynamic range of scaling to address segments spanning low power to high power, increased performance per watt, support for next generation of APIs. Gen 9 LP scalable architecture is partitioned by usage domains along Render/Geometry, Media, and Display. The architecture also delivers very low-power video playback and next generation analytic and filters for imaging-related applications. The new Graphics Architecture includes 3D compute elements, Multi-format HW assisted decode/encode pipeline, and Mid-Level Cache (MLC) for superior high definition playback, video quality, and improved 3D performance and media.

The Display Engine handles delivering the pixels to the screen. GSA (Graphics in System Agent) is the primary channel interface for display memory accesses and PCI-like traffic in and out.

The display engine supports the latest display standards such as eDP* 1.4, DP* 1.2, HDMI* 1.4, HW support for blend, scale, rotate, compress, high PPI support, and advanced SRD2 display power management.

2.4.1 Operating Systems Support

Windows* 10 x64,OS X, Linux* OS, Chrome* OS.

Note: The processor supports only 64-bit operating systems.

2.4.2 API Support (Windows*)

- Direct3D* 2015, Direct3D 11.2, Direct3D 11.1, Direct3D 9, Direct3D 10, Direct2D
- OpenGL* 4.5
- OpenCL* 2.1, OpenCL 2.0, OpenCL 1.2

DirectX* extensions:

- PixelSync, InstantAccess, Conservative Rasterization, Render Target Reads, Floating-point De-norms, Shared Virtual memory, Floating Point atomics, MSAA sample-indexing, Fast Sampling (Coarse LOD), Quilted Textures, GPU Enqueue Kernels, GPU Signals processing unit. Other enhancements include color compression.

Gen 9 LP architecture delivers hardware acceleration of Direct X* 11 Render pipeline comprising the following stages: Vertex Fetch, Vertex Shader, Hull Shader, Tessellation, Domain Shader, Geometry Shader, Rasterizer, Pixel Shader, Pixel Output.

2.4.3 Media Support (Intel® QuickSync & Clear Video Technology HD)

Gen 9 LP implements multiple media video codecs in hardware as well as a rich set of image processing algorithms.

Note: All supported media codecs operate on 8 bpc, YCbCr 4:2:0 video profiles.

2.4.3.1 Hardware Accelerated Video Decode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW decode is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2)
- Direct3D11 Video API
- Intel Media SDK
- MFT (Media Foundation Transform) filters.

Gen 9 LP supports full HW accelerated video decoding for AVC/VC1/MPEG2/HEVC/VP8/JPEG.

Table 2-8. Hardware Accelerated Video Decoding

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	Main High	1080p
VC1/WMV9	Advanced Main Simple	L3 High Simple	3840x3840
AVC/H264	High Main MVC & stereo	L5.1	2160p(4K)
VP8	0	Unified level	1080p
JPEG/MJPEG	Baseline	Unified level	16k x16k
HEVC/H265 (8 bits)	Main	L5.1	2160(4K)
HEVC/H265 (10 bits)	Main BT2020, isolate Dec	L5.1	2160(4K)
VP9	0 (4:2:0 Chroma 8-bit)	Unified level	2160(4K)

Expected performance:

- More than 16 simultaneous decode streams @ 1080p.

Note: Actual performance depends on the processor SKU, content bit rate, and memory frequency. Hardware decode for H264 SVC is not supported.

2.4.3.2 Hardware Accelerated Video Encode

Gen 9 LP implements a high-performance and low-power HW acceleration for video decoding operations for multiple video codecs.

The HW encode is exposed by the graphics driver using the following APIs:

- Intel Media SDK
- MFT (Media Foundation Transform) filters

Gen 9 LP supports full HW accelerated video encoding for AVC/MPEG2/HEVC/VP8/JPEG.

Table 2-9. Hardware Accelerated Video Encode

Codec	Profile	Level	Maximum Resolution
MPEG2	Main	High	1080p
AVC/H264	High Main	L5.1	2160p(4K)
VP8	Unified profile	Unified level	—
JPEG	Baseline	—	16Kx16K
HEVC/H265	Main	L5.1	2160p(4K)
VP9	Support 8 bits 4:2:0 BT2020 may be obtained the pre/post processing	—	—

Note: Hardware encode for H264 SVC is not supported.

2.4.3.3 Hardware Accelerated Video Processing

There is hardware support for image processing functions such as De-interlacing, Film cadence detection, Advanced Video Scaler (AVS), detail enhancement, image stabilization, gamut compression, HD adaptive contrast enhancement, skin tone enhancement, total color control, Chroma de-noise, SFC pipe (Scalar and Format Conversion), memory compression, Localized Adaptive Contrast Enhancement (LACE), spatial de-noise, Out-Of-Loop De-blocking (from AVC decoder), 16 bpc support for de-noise/de-mosaic.

There is support for Hardware assisted Motion Estimation engine for AVC/MPEG2 encode, True Motion, and Image stabilization applications.

The HW video processing is exposed by the graphics driver using the following APIs:

- Direct3D* 9 Video API (DXVA2).
- Direct3D 11 Video API.
- Intel Media SDK.
- MFT (Media Foundation Transform) filters.
- Intel CUI SDK.

Note: Not all features are supported by all the above APIs. Refer to the relevant documentation for more details.

2.4.3.4 Hardware Accelerated Transcoding

Transcoding is a combination of decode video processing (optional) and encode. Using the above hardware capabilities can accomplish a high-performance transcode pipeline. There is not a dedicated API for transcoding.

The processor graphics supports the following transcoding features:

- Low-power and low-latency AVC encoder for video conferencing and Wireless Display applications.
- Lossless memory compression for media engine to reduce media power.
- HW assisted Advanced Video Scaler.
- Low power Scaler and Format Converter.

Expected performance:

- S-Processor Line: 18x 1080p30 RT (same as previous generation).

Note: Actual performance depends on Processor Line, video processing algorithms used, content bit rate, and memory frequency.

2.4.4 Switchable/Hybrid Graphics

The processor supports Switchable/Hybrid graphics.

Switchable graphics: The Switchable Graphics feature allows the user to switch between using the Intel integrated graphics and a discrete graphics card. The Intel Integrated Graphics driver will control the switching between the modes. In most cases it will operate as follows: when connected to AC power - Discrete graphic card; when connected to DC (battery) - Intel integrated GFX

Hybrid graphics: Intel integrated graphics and a discrete graphics card work cooperatively to achieve enhanced power and performance.

Table 2-10. Switchable/Hybrid Graphics Support

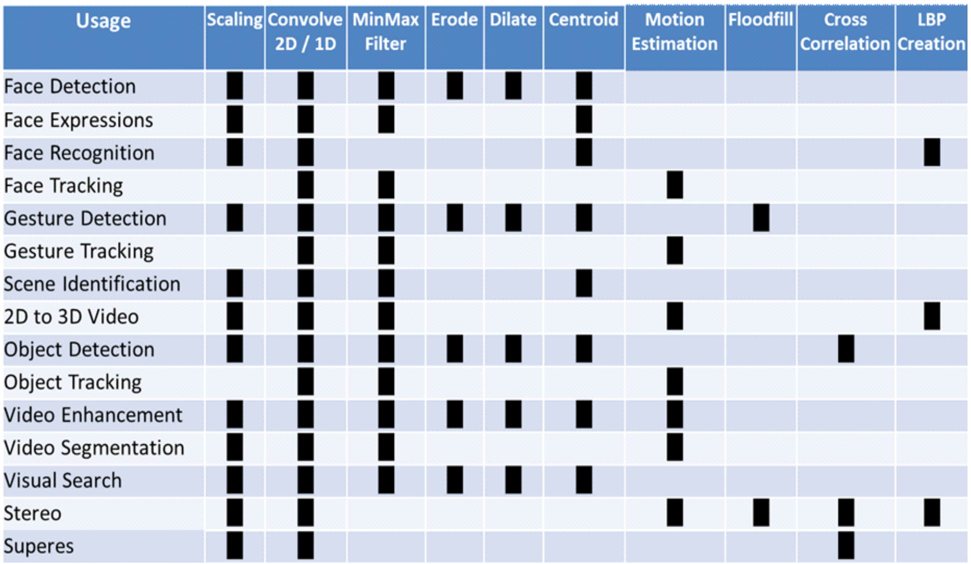
Operating System	Hybrid Graphics	Switchable Graphics[2]
Windows* 10 (64 bit)	Yes[1]	N/A

Note:
1. Contact your graphics vendor to check for support.
2. Intel does not validate any SG configurations on Windows* 8.1 or Windows* 10.

2.4.5 Gen 9 LP Video Analytics

There is HW assist for video analytics filters such as scaling, convolve 2D/1D, minmax, 1P filter, erode, dilate, centroid, motion estimation, flood fill, cross correlation, Local Binary Pattern (LBP).

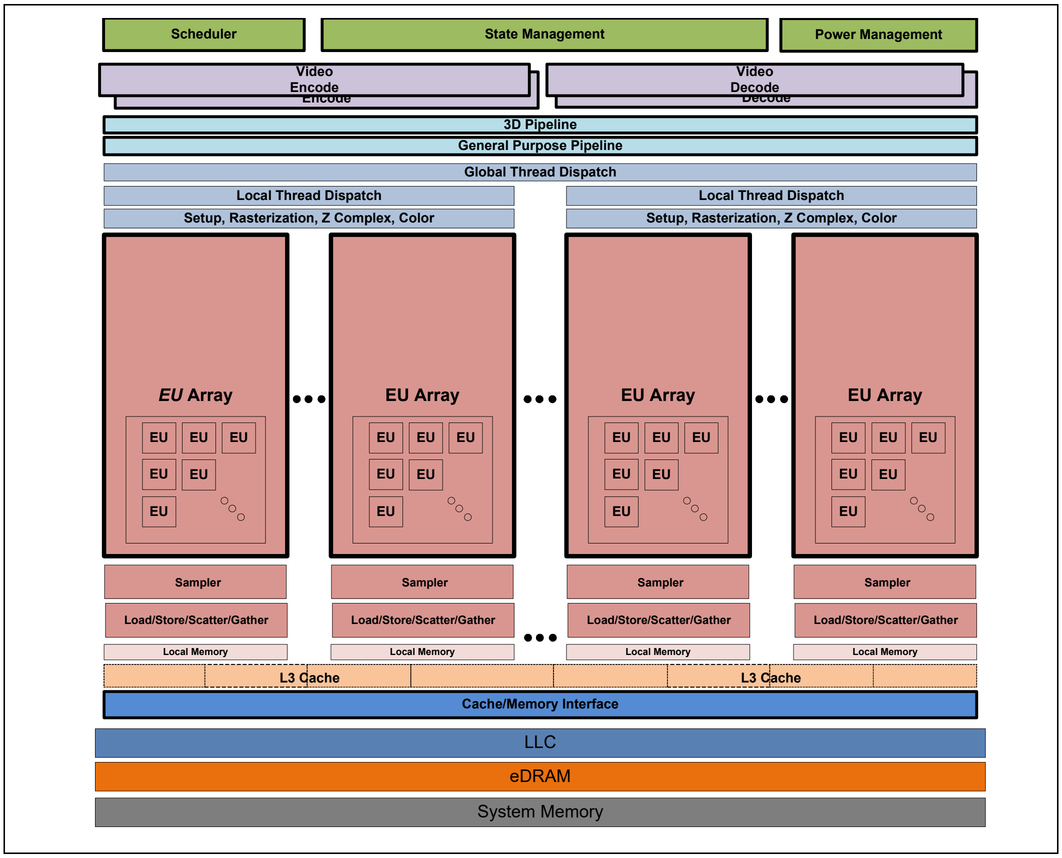
Figure 2-5. Video Analytics Common Use Cases



Usage	Scaling	Convolve 2D / 1D	MinMax Filter	Erode	Dilate	Centroid	Motion Estimation	Floodfill	Cross Correlation	LBP Creation
Face Detection	■	■	■	■	■	■				
Face Expressions	■	■	■			■				
Face Recognition	■	■				■				■
Face Tracking		■	■				■			
Gesture Detection	■	■	■	■	■	■		■		
Gesture Tracking		■	■				■			
Scene Identification	■	■	■			■				
2D to 3D Video	■	■	■				■			■
Object Detection	■	■	■	■	■	■			■	
Object Tracking		■	■				■			
Video Enhancement	■	■	■	■	■	■	■			
Video Segmentation	■	■	■				■			
Visual Search	■	■	■	■	■	■				
Stereo	■	■					■	■	■	■
Superes	■	■							■	

2.4.6 Gen 9 LP (9th Generation Low Power) Block Diagram

Figure 2-6. Gen 9 LP Block Diagram



2.4.7 GT2 Graphic Frequency

Table 2-11. GT2 Graphics Frequency (S-Processor Line)

Segment	GT Unslice	GT Unslice + 1 GT Slice	GT Unslice + 2 GT Slice
S-Processor Line - Hexa Core with GT2	GT Max Dynamic frequency	[GT Unslice only] - (1or2)BIN	—

2.5 Display Interfaces

2.5.1 DDI Configuration

The processor supports single eDP* interface and 2 or 3 DDI interfaces (depends on segment).

Table 2-12. DDI Ports Availability

Ports	Port name in VBT	S-Processor Line[2,3]
DDI0 - eDP	Port A	Yes
DDI1	Port B	Yes
DDI2	Port C	Yes
DDI3	Port D	Yes
DDI4 - eDP/VGA	Port E	Yes[1]

Notes:
1. For more information, see Section 2.5.2, "eDP* Bifurcation"
2. 3xDDC (DDPB, DDPC, DDPD) are valid for all the processor SKUs .
3. 5xHPD (PCH) inputs (eDP_HPD, DDPB_HPD0, DDPC_HPD1, DDPD_HPD2, DDPE_HPD3) are valid for all processor SKUs.
4. VBT provides a configuration option to select the four AUX channels A/B/C/D for a given port, based on how the aux channel lines are connected physically on the board.

- DDI interface can be configured as DisplayPort* or HDMI*.
- Each DDI can support dual mode (DP++).
- Each DDI can support DVI (DVI max resolution is 1920x1200 @ 60 Hz).
- The DisplayPort* can be configured to use 1, 2, or 4 lanes depending on the bandwidth requirements and link data rate.
- DDI ports notated as: DDI B, C, D.
- S-Processor Line processors supports eDP and up to 3 DDI supporting DP/HDMI.
- AUX/DDC signals are valid for each DDI Port. (three for S-Processor Lines)
- Total Five dedicated HPD (Hot plug detect signals) are valid for all processor SKUs.

Note: SSC is supported in eDP*/DP for all Processor Lines.

Note: The processor platform supports DP Type-C implementation with additional discrete components.

2.5.2 eDP* Bifurcation

Table 2-13. VGA and Embedded DisplayPort* (eDP*) Bifurcation Summary

Port	S-Processor Line
eDP - DDIA (eDP lower x2 lanes, [1:0])	Yes
VGA - DDIE[2] (DP upper x2 lanes, [3:2])	Yes[1]

Notes:
1. Requires a DP to VGA converter.
2. DP-to-VGA converter on the processor ports is supported using external dongle only, display driver software for VGA dongles which configures the VGA port as a DP branch device.
3. For example, DT SKUs can use eDP_AUX for VGA converter which is available as free Design but HPD should be used as DDPE_HPD3.

2.5.3 Display Technologies

Table 2-14. Display Technologies Support

Technology	Standard
eDP* 1.4	VESA* Embedded DisplayPort* Standard 1.4
DisplayPort* 1.2	VESA DisplayPort* Standard 1.2 VESA DisplayPort* PHY Compliance Test Specification 1.2 VESA DisplayPort* Link Layer Compliance Test Specification 1.2
HDMI* 1.4[1]	High-Definition Multimedia Interface Specification Version 1.4

Notes:
1. HDMI* 2.0/2.0a support is possible using LS-Pcon converter chip connected to the DP port. The LS-Pcon supports 2 modes:
   a. Level shifter for HDMI 1.4 resolutions.
   b. DP-HDMI 2.0 protocol converter for HDMI 2.0 resolutions.

- The HDMI* interface supports HDMI with 3D, 4Kx2K @ 24 Hz, Deep Color, and x.v.Color.
- The processor supports High-bandwidth Digital Content Protection (HDCP) for high definition content playback over digital interfaces. HDCP is not supported for eDP.
- The processor supports eDP display authentication: Alternate Scrambler Seed Reset (ASSR).
- The processor supports Multi-Stream Transport (MST), enabling multiple monitors to be used via a single DisplayPort connector.

The maximum MST DP supported resolution for S-Processors is shown in the following table.

Table 2-15. Display Resolutions and Link Bandwidth for Multi-Stream Transport calculations (Sheet 1 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
640	480	60	25.2	0.76
800	600	60	40	1.20
1024	768	60	65	1.95

Table 2-15. Display Resolutions and Link Bandwidth for Multi-Stream Transport calculations (Sheet 2 of 2)

Pixels per line	Lines	Refresh Rate [Hz]	Pixel Clock [MHz]	Link Bandwidth [Gbps]
1280	720	60	74.25	2.23
1280	768	60	68.25	2.05
1360	768	60	85.5	2.57
1280	1024	60	108	3.24
1400	1050	60	101	3.03
1680	1050	60	119	3.57
1920	1080	60	148.5	4.46
1920	1200	60	154	4.62
2048	1152	60	156.75	4.70
2048	1280	60	174.25	5.23
2048	1536	60	209.25	6.28
2304	1440	60	218.75	6.56
2560	1440	60	241.5	7.25
3840	2160	30	262.75	7.88
2560	1600	60	268.5	8.06
2880	1800	60	337.5	10.13
3200	2400	60	497.75	14.93
3840	2160	60	533.25	16.00
4096	2160	60	556.75	16.70
4096	2304	60	605	18.15

Notes:

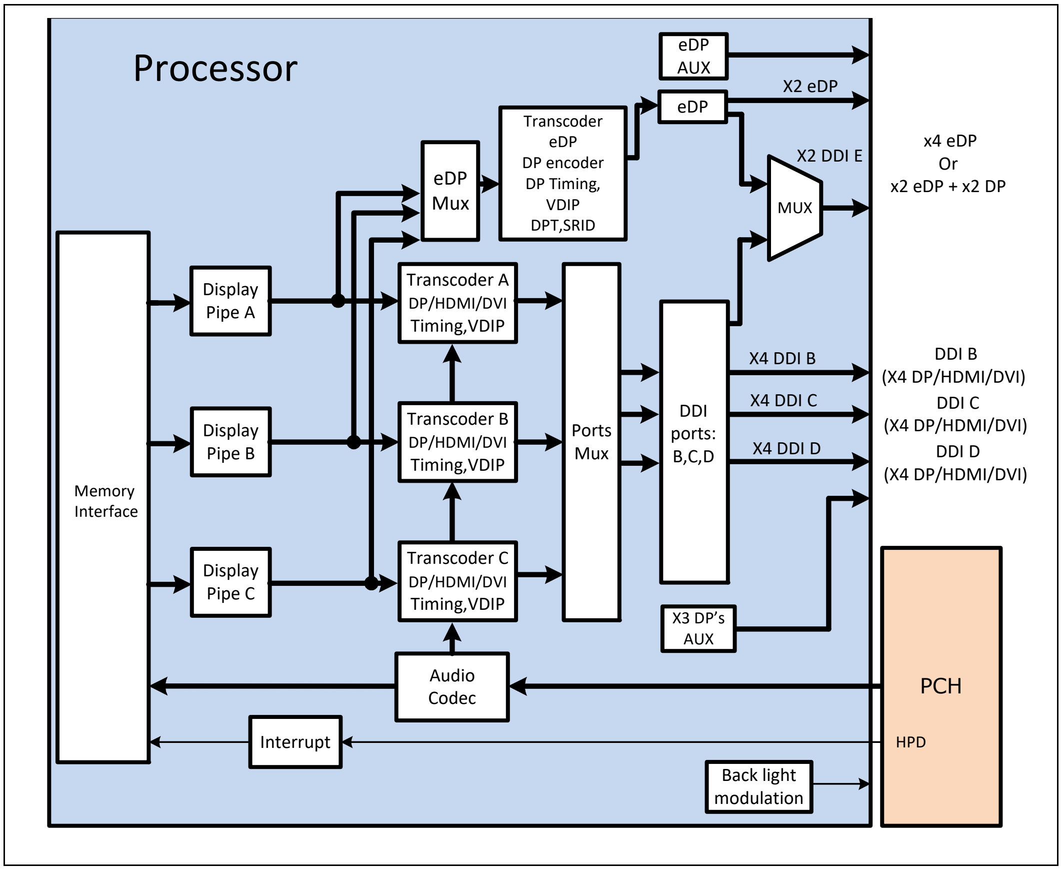
1. All above is related to bit depth of 24.
2. The data rate for a given video mode can be calculated as: Data Rate = Pixel Frequency * Bit Depth.
3. The bandwidth requirements for a given video mode can be calculated as:
   Bandwidth = Data Rate * 1.25 (for 8B/10B coding overhead).
4. The Table above is partial List of the common Display resolutions, just for example.
   The Link Bandwidth depends if the standards is Reduced Blanking or not.
   If the Standard is Not reduced blanking - the expected Bandwidth will be higher.
   For more details, refer to VESA and Industry Standards and Guidelines for Computer Display Monitor Timing (DMT), Version 1.0, Rev. 13 February 8, 2013
5. To calculate the resolutions that can be supported in MST configurations, follow the below guidelines:
   a. Identify what is the Link Bandwidth (column right) according the requested Display resolution.
   b. Summarize the Bandwidth for Two of three Displays accordingly, and make sure the final result is below 21.6Gbps. (for HBR2, four lanes)
   c. For special cases when x2 lanes are used or HBR or RBR used, refer to the tables in Section 2.5.14 accordingly.

   For examples:
   a. Docking Two displays: 3840x2160 @ 60 Hz + 1920x1200 @ 60 Hz = 16 + 4.62 = 20.62 Gbps [Supported]
   b. Docking Three Displays: 3840x2160 @ 30 Hz + 3840x2160 @ 30 Hz + 1920x1080 @ 60 Hz = 7.88 + 7.88 + 4.16 = 19.92 Gbps [Supported]
6. Consider also the supported resolutions as mentioned in Section 2.5.9 and Section 2.5.10.

- The processor supports only 3 streaming independent and simultaneous display combinations of DisplayPort*/eDP*/HDMI/DVI monitors. In the case where 4 monitors are plugged in, the software policy will determine which 3 will be used.
- Three High Definition Audio streams over the digital display interfaces are supported.

- For display resolutions driving capability see Table 2-17, "Maximum Display Resolution".
- DisplayPort* Aux CH supported by the processor, while DDC channel, Panel power sequencing, and HPD are supported through the PCH.

Figure 2-7. Processor Display Architecture (with 3 DDI ports as an example)



Display is the presentation stage of graphics. This involves:

- Pulling rendered data from memory
- Converting raw data into pixels
- Blending surfaces into a frame
- Organizing pixels into frames
- Optionally scaling the image to the desired size
- Re-timing data for the intended target
- Formatting data according to the port output standard

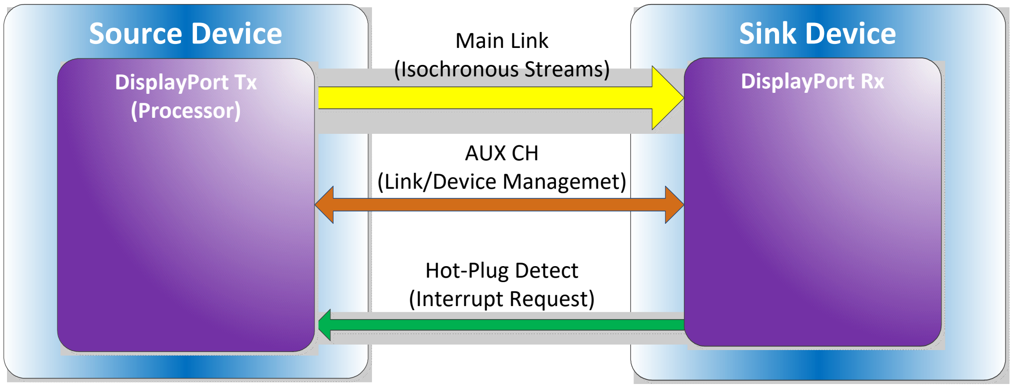
2.5.4 DisplayPort*

The DisplayPort* is a digital communication interface that uses differential signaling to achieve a high-bandwidth bus interface designed to support connections between PCs and monitors, projectors, and TV displays.

A DisplayPort* consists of a Main Link, Auxiliary channel, and a Hot-Plug Detect signal. The Main Link is a unidirectional, high-bandwidth, and low-latency channel used for transport of isochronous data streams such as uncompressed video and audio. The Auxiliary Channel (AUX CH) is a half-duplex bidirectional channel used for link management and device control. The Hot-Plug Detect (HPD) signal serves as an interrupt request for the sink device.

The processor is designed in accordance to VESA* DisplayPort* specification. Refer to Table 2-14.

Figure 2-8. DisplayPort* Overview



2.5.5 High-Definition Multimedia Interface (HDMI*)

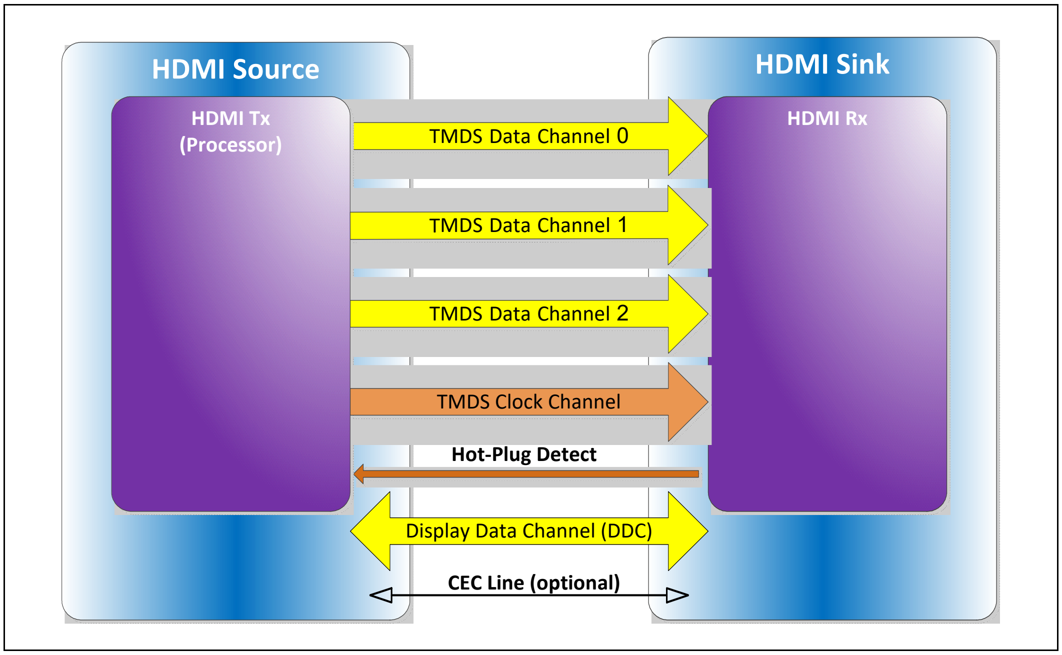
The High-Definition Multimedia Interface (HDMI*) is provided for transmitting uncompressed digital audio and video signals from DVD players, set-top boxes, and other audio-visual sources to television sets, projectors, and other video displays. It can carry high-quality multi-channel audio data and all standard and high-definition consumer electronics video formats. The HDMI display interface connecting the processor and display devices uses transition minimized differential signaling (TMDS) to carry audiovisual information through the same HDMI cable.

HDMI includes three separate communications channels: TMDS, DDC, and the optional CEC (consumer electronics control). CEC is not supported on the processor. As shown in the following figure, the HDMI cable carries four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC. The DDC is used by an HDMI Source to determine the capabilities and characteristics of the Sink.

Audio, video, and auxiliary (control/status) data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver for data recovery on the three data channels. The digital display data signals driven natively through the PCH are AC coupled and needs level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

The processor HDMI interface is designed in accordance with the High-Definition Multimedia Interface.

Figure 2-9. HDMI* Overview



2.5.6 Digital Video Interface (DVI)

The processor Digital Ports can be configured to drive DVI-D. DVI uses TMDS for transmitting data from the transmitter to the receiver, which is similar to the HDMI protocol except for the audio and CEC. Refer to the HDMI section for more information on the signals and data transmission. The digital display data signals driven natively through the processor are AC coupled and need level shifting to convert the AC coupled signals to the HDMI compliant digital signals.

2.5.7 embedded DisplayPort* (eDP*)

The embedded DisplayPort* (eDP*) is an embedded version of the DisplayPort standard oriented towards applications such as notebook and All-In-One PCs. Like DisplayPort, embedded DisplayPort* also consists of a Main Link, Auxiliary channel, and an optional Hot-Plug Detect signal. eDP* can be bifurcated in order to support VGA display.

2.5.8 Integrated Audio

- HDMI* and display port interfaces carry audio along with video.
- The processor supports 3 High Definition audio streams on 3 digital ports simultaneously (the DMA controllers are in PCH).
- The integrated audio processing (DSP) is performed by the PCH, and delivered to the processor using the AUDIO_SDI and AUDIO_CLK inputs pins.
- AUDIO_SDO output pin is used to carry responses back to the PCH
- Supports only the internal HDMI and DP CODECs.

Table 2-16. Processor Supported Audio Formats over HDMI and DisplayPort*

Audio Formats	HDMI*	DisplayPort*
AC-3 Dolby* Digital	Yes	Yes
Dolby Digital Plus	Yes	Yes
DTS-HD*	Yes	Yes
LPCM, 192 kHz/24 bit, 8 Channel	Yes	Yes
Dolby TrueHD, DTS-HD Master Audio* (Lossless Blu-Ray Disc* Audio Format)	Yes	Yes

The processor will continue to support Silent stream. Silent stream is an integrated audio feature that enables short audio streams, such as system events to be heard over the HDMI* and DisplayPort* monitors. The processor supports silent streams over the HDMI and DisplayPort interfaces at 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz sampling rates.

2.5.9 Multiple Display Configurations (Dual Channel DDR)

The following multiple display configuration modes are supported (with appropriate driver software):

- Single Display is a mode with one display port activated to display the output to one display device.
- Intel Display Clone is a mode with up to three display ports activated to drive the display content of same color depth setting but potentially different refresh rate and resolution settings to all the active display devices connected.
- Extended Desktop is a mode with up to three display ports activated to drive the content with potentially different color depth, refresh rate, and resolution settings on each of the active display devices connected.

The digital ports on the processor can be configured to support DisplayPort/HDMI/DVI. The following table shows examples of valid three display configurations through the processor.

Table 2-17. Maximum Display Resolution (Sheet 1 of 2)

Standard	S-Processor Line	Notes
eDP*	4096x2304 @ 60Hz, 24bpp	1,2,3,7
DP*	4096x2304 @ 60Hz, 24bpp	1,2,3,7
HDMI* 1.4 (native)	4096x2160 @ 24 Hz, 24 bpp	1,2,3
HDMI 2.0 (Via LS-Pcon)	4096x2160 @ 60Hz, 24bpp	1,2,3,6

Table 2-17. Maximum Display Resolution (Sheet 2 of 2)

Standard	S-Processor Line	Notes

Notes:
1. Maximum resolution is based on implementation of 4 lanes with HBR2 link data rate.
2. bpp - bit per pixel.
3. S-Processor Line support up to 4 displays, but only three can be active at the same time.
4. The resolutions are assumed at max VCC_{SA}.
5. In the case of connecting more than one active display port, the processor frequency may be lower than base frequency at thermally limited scenario.
6. HDMI2.0 implemented using LSPCON device. Only one LSPCON with HDCP2.2 support is supported per platform.
7. Display resolution of 5120x2880@60Hz can be supported with 5K panels displays which have two ports. (with the GFX driver accordingly).

2.5.10 Multiple Display Configurations (Single Channel DDR)

Table 2-18. S -Processor Line Display Resolution Configuration

Minimum DDR speed [MT/s]	Maximum Resolution (Clone/ Extended mode)		
	eDP @60Hz (Primary)	DP @60Hz / HDMI @30Hz (Secondary 1)	DP @60Hz / HDMI @30Hz (Secondary 2)
1866	2560 x 1440	4096 x 2304	4096 x 2304
2133	3840 x 2160	4096 x 2304	4096 x 2304
2400	3840 x 2160	4096 x 2304	4096 x 2304

2.5.11 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high-definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, and so on) and the sink (panels, monitor, and TVs). The processor supports HDCP 2.2 for 4k Premium content protection over wired displays (HDMI*, DVI, and DisplayPort*).

The HDCP 2.2 keys are integrated into the processor and customers are not required to physically configure or handle the keys. HDCP2.2 for HDMI2.0 is covered by the LSPCON platform device.

Some minor difference will be between Integrated HDCP2.2 over HDMI1.4 compared to the HDCP2.2 over LSPCON in HDMI1.4 Mode. Also, LSPCON is needed for HDMI 2.0a which defines HDR over HDMI.

The HDCP 1.4 keys are integrated into the processor and customers are not required to physically configure or handle the keys.

Table 2-19. HDCP Display supported Implications Table (Sheet 1 of 2)

Topic	HDCP Revision	Maximum Resolution	HDR[1]	HDCP Solution[2]	BPC[3]	Comments
DP	HDCP1.4	4K@60	No	iHDCP	10 bit	Legacy Integrated for HDCP1.4
	HDCP2.2	4K@60	Yes	iHDCP	10 bit	New Integrated for HDCP2.2

Table 2-19. HDCP Display supported Implications Table (Sheet 2 of 2)

Topic	HDCP Revision	Maximum Resolution	HDR[1]	HDCP Solution[2]	BPC[3]	Comments
HDMI1.4	HDCP1.4	4K@30	No	iHDCP	8 bit	Legacy Integrated for HDCP1.4
	HDCP2.2	4K@30	No	LSPCON	8 bit	LSPCON HDCP2.2 required
	HDCP2.2	4K@30	No	iHDCP[4]	8 bit	New Integrated for HDCP2.2
HDMI2.0	HDCP2.2	4K@60	No	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required
HDMI2.0a	HDCP2.2	4K@60	Yes	LSPCON	12 bit (YUV 420)	LSPCON HDCP2.2 required

Notes:
1. HDR - High Dynamic range feature expands the range of both contrast and color significantly, HDR will be supported on DP and HDMI2.0a configuration only.
2. HDCP Solutions:
   a. iHDCP - Intel Silicon Integrated HDCP
   b. LSPCon - 3rd Party motherboard soldered down solution
3. BPC - Bits Per Channel.
4. HDMI1.4 with the Integrated HDCP2.2 solution will replace the LSPCON Solution at a later time.

2.5.12 Display Link Data Rate Support

Table 2-20. Display Link Data Rate Support

Technology	Link Data Rate
eDP*	RBR (1.62 GT/s) 2.16 GT/s 2.43 GT/s HBR (2.7 GT/s) 3.24 GT/s 4.32 GT/s HBR2 (5.4 GT/s)
DisplayPort*	RBR (1.62 GT/s) HBR (2.7 GT/s) HBR2 (5.4 GT/s)
HDMI*	1.65 Gb/s 2.97 Gb/s

Table 2-21. Display Resolution and Link Rate Support

Resolution	Link Rate Support	High Definition
4096x2304	5.4 (HBR2)	UHD (4K)
3840x2160	5.4 (HBR2)	UHD (4K)
3200x2000	5.4 (HBR2)	QHD+
3200x1800	5.4 (HBR2)	QHD+
2880x1800	2.7 (HBR)	QHD
2880x1620	2.7 (HBR)	QHD
2560x1600	2.7 (HBR)	QHD
2560x1440	2.7 (HBR)	QHD
1920x1080	1.62 (RBR)	FHD

2.5.13 Display Bit Per Pixel (BPP) Support

Table 2-22. Display Bit Per Pixel (BPP) Support

Technology	Bit Per Pixel (bpp)
eDP*	24,30,36
DisplayPort*	24,30,36
HDMI*	24,36

2.5.14 Display Resolution per Link Width

Table 2-23. Supported Resolutions[1] for HBR (2.7 Gbps) by Link Width

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	S-Processor Lines
4 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp
2 lanes	5.4	180	2048x1280 @ 60 Hz, 24bpp
1 lane	2.7	90	1280x960 @ 60 Hz, 24bpp

Notes:
1. The examples assumed 60 Hz refresh rate and 24 bpp.

Table 2-24. Supported Resolutions[1] for HBR2 (5.4 Gbps) by Link Width

Link Width	Max Link Bandwidth [Gbps]	Max Pixel Clock (theoretical) [MHz]	S-Processor Lines
4 lanes	21.6	720	See “Maximum Display Resolutions” table
2 lanes	10.8	360	2880x1800 @ 60 Hz, 24bpp
1 lane	5.4	180	2048x1280 @ 60 Hz, 24bpp

Notes:
1. The examples assumed 60 Hz refresh rate and 24 bpp.

2.6 Platform Environmental Control Interface (PECI)

Note: PECI is an Intel proprietary interface that provides a communication channel between Intel processors and external components like Super IO (SIO) and Embedded Controllers (EC) to provide processor temperature, Turbo, Configurable TDP, and memory throttling control mechanisms and many other services. PECI is used for platform thermal management and real time control and configuration of processor features and performance.

2.6.1 PECI Bus Architecture

The PECI architecture is based on a wired OR bus that the clients (as processor PECI) can pull up (with strong drive).

The idle state on the bus is near zero.

The following figures demonstrate PECI design and connectivity:

- PECI Host-Clients Connection: While the host/originator can be third party PECI host and one of the PECI client is a processor PECI device.

- PECI EC Connection.

Figure 2-10. Example for PECI Host-Clients Connection

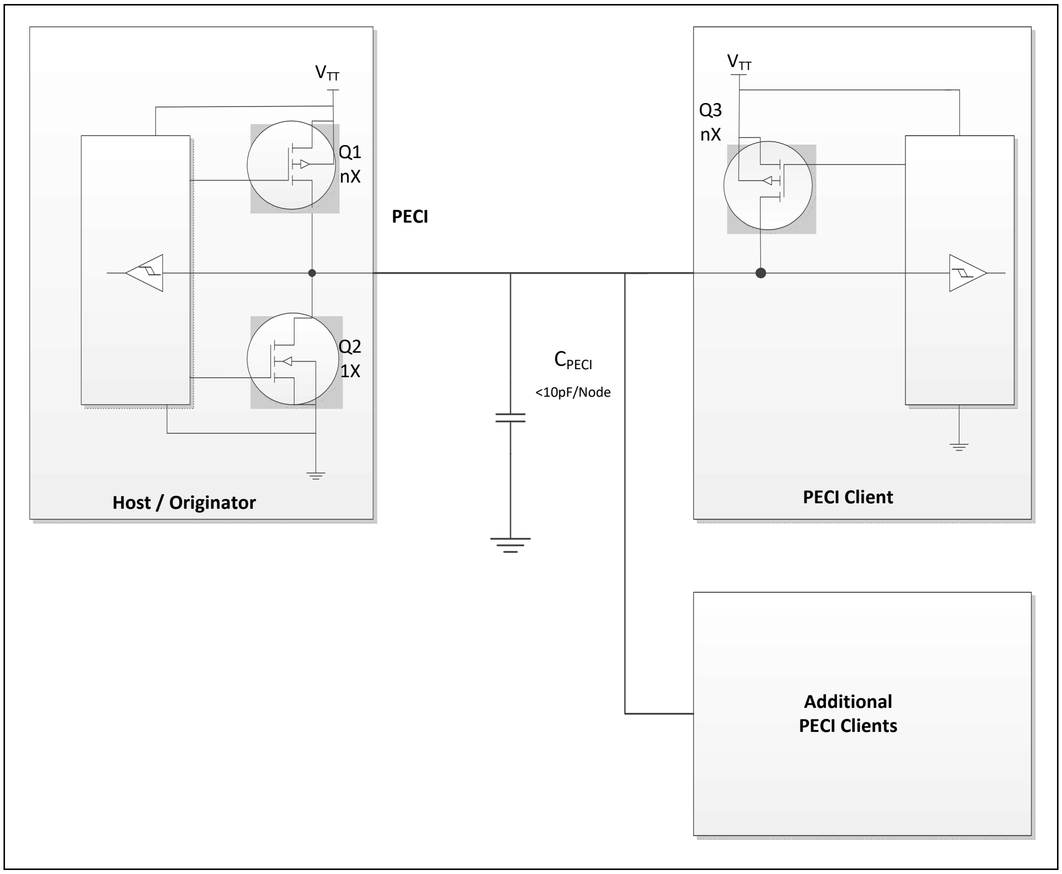
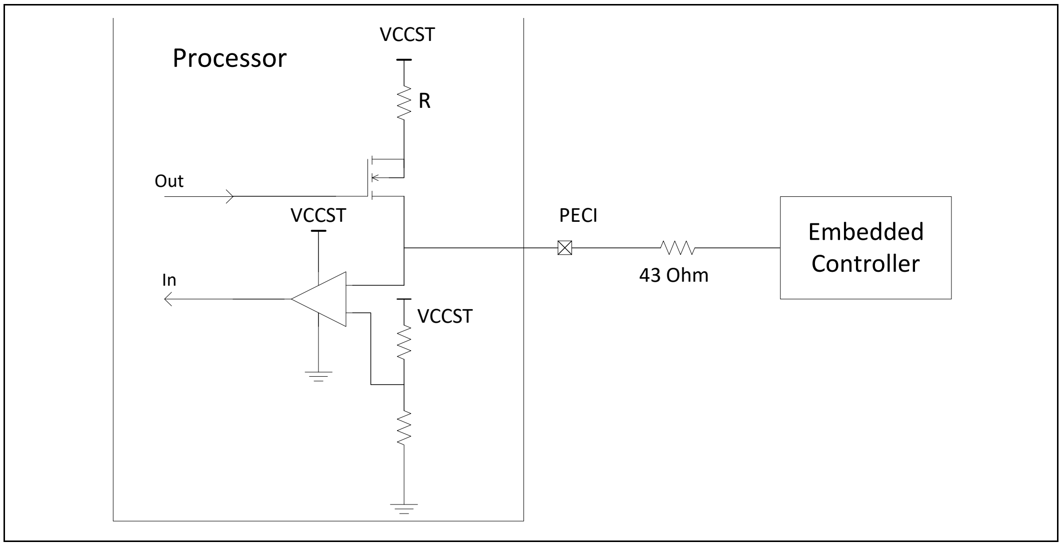


Figure 2-11. Example for PECI EC Connection



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3 Technologies

This chapter provides a high-level description of Intel technologies implemented in the processor.

The implementation of the features may vary between the processor SKUs.

Details on the different technologies of Intel processors and other relevant external notes are located at the Intel technology web site: http://www.intel.com/technology/

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

Intel Virtualization Technology (Intel VT) for IA-32, Intel 64 and Intel Architecture (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) extends Intel VT-x by adding hardware assisted support to improve I/O device virtualization performance.

Intel VT-x specifications and functional descriptions are included in the *Intel 64 and IA-32 Architectures Software Developer's Manual, Volume 3*. Available at:

http://www.intel.com/products/processor/manuals/index.htm

The Intel VT-d specification and other VT documents can be referenced at:

http://www.intel.com/technology/virtualization/index.htm

https://sharedspaces.intel.com/sites/PCDC/SitePages/Ingredients/ingredient.aspx?ing=VT

3.1.1 Intel® Virtualization Technology (Intel® VT) for IA-32, Intel® 64 and Intel® Architecture (Intel® VT-X)

Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide an improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that VMMs will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.

- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

Intel® VT-x Key Features

The processor supports the following added new Intel VT-x features:

- Extended Page Table (EPT) Accessed and Dirty Bits
  - — EPT A/D bits enabled VMMs to efficiently implement memory management and page classification algorithms to optimize VM memory operations, such as de-fragmentation, paging, live migration, and check-pointing. Without hardware support for EPT A/D bits, VMMs may need to emulate A/D bits by marking EPT paging-structures as not-present or read-only, and incur the overhead of EPT page-fault VM exits and associated software processing.
- EPTP (EPT pointer) switching
  - — EPTP switching is a specific VM function. EPTP switching allows guest software (in VMX non-root operation, supported by EPT) to request a different EPT paging-structure hierarchy. This is a feature by which software in VMX non-root operation can request a change of EPTP without a VM exit. Software will be able to choose among a set of potential EPTP values determined in advance by software in VMX root operation.
- Pause loop exiting
  - — Support VMM schedulers seeking to determine when a virtual processor of a multiprocessor virtual machine is not performing useful work. This situation may occur when not all virtual processors of the virtual machine are currently scheduled and when the virtual processor in question is in a loop involving the PAUSE instruction. The new feature allows detection of such loops and is thus called PAUSE-loop exiting.

The processor IA core supports the following Intel VT-x features:

- **Mode based (XU/XS) EPT execute control - New Feature for this processor**
  - — A new mode of EPT operation which enables different controls for executability of GPA based on Guest specified mode (User/Supervisor) of linear address translating to the GPA. When the mode is enabled, the executability of a GPA is defined by two bits in EPT entry. One bit for accesses to user pages and other one for accesses to supervisor pages.
  - — The new mode requires changes in VMCS, and EPT entries. VMCS includes a bit “mode based EPT execute control” which is used to enable/disable the mode. An additional bit in EPT entry is defined as “supervisor-execute access”; the original execute control bit is considered as “user-execute access”. If the “mode based EPT execute control” is disabled the additional bit is ignored and the system works with one bit execute control for both user pages and supervisor pages.
  - — Behavioral changes - Behavioral changes are across three areas:
    - **Access to GPA-** If the “mode-based EPT execute control” VM-execution control is 1, treatment of guest-physical accesses by instruction fetches depends on the linear address from which an instruction is being fetched
      1. If the translation of the linear address specifies user mode (the S bit was set in every paging structure entry used to translate the linear address), the resulting guest-physical address is executable under EPT only if the XU bit (at position 2) is set in every EPT paging-structure entry used to translate the guest-physical address.
      2. If the translation of the linear address specifies supervisor mode (the S bit was clear in at least one of the paging-structure entries used to

translate the linear address), the resulting guest-physical address is executable under EPT only if the XS bit is set in every EPT paging-structure entry used to translate the guest-physical address

—The XU and XS bits are used only when translating linear addresses for guest code fetches. They do not apply to guest page walks, data accesses, or A/D-bit updates

- **VMEntry -** If the "activate secondary controls" and "mode-based EPT execute control" VM-execution controls are both 1, VM entries ensure that the "enable EPT" VM-execution control is 1. VM entry fails if this check fails. When such a failure occurs, control is passed to the next instruction,
- **VMExit** - The exit qualification due to EPT violation reports clearly whether the violation was due to User mode access or supervisor mode access.

— Capability Querying: IA32_VMX_PROCBASED_CTLS2 has bit to indicate the capability, RDMSR can be used to read and query whether the processor supports the capability or not.

- Extended Page Tables (EPT)
  - — EPT is hardware assisted page table virtualization
  - — It eliminates VM exits from guest OS to the VMM for shadow page-table maintenance
- Virtual Processor IDs (VPID)
  - — Ability to assign a VM ID to tag processor IA core hardware structures (such as TLBs)
  - — This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - — Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest
  - — The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees
- Descriptor-Table Exiting
  - — Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - — A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

3.1.2 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

Intel® VT-d Objectives

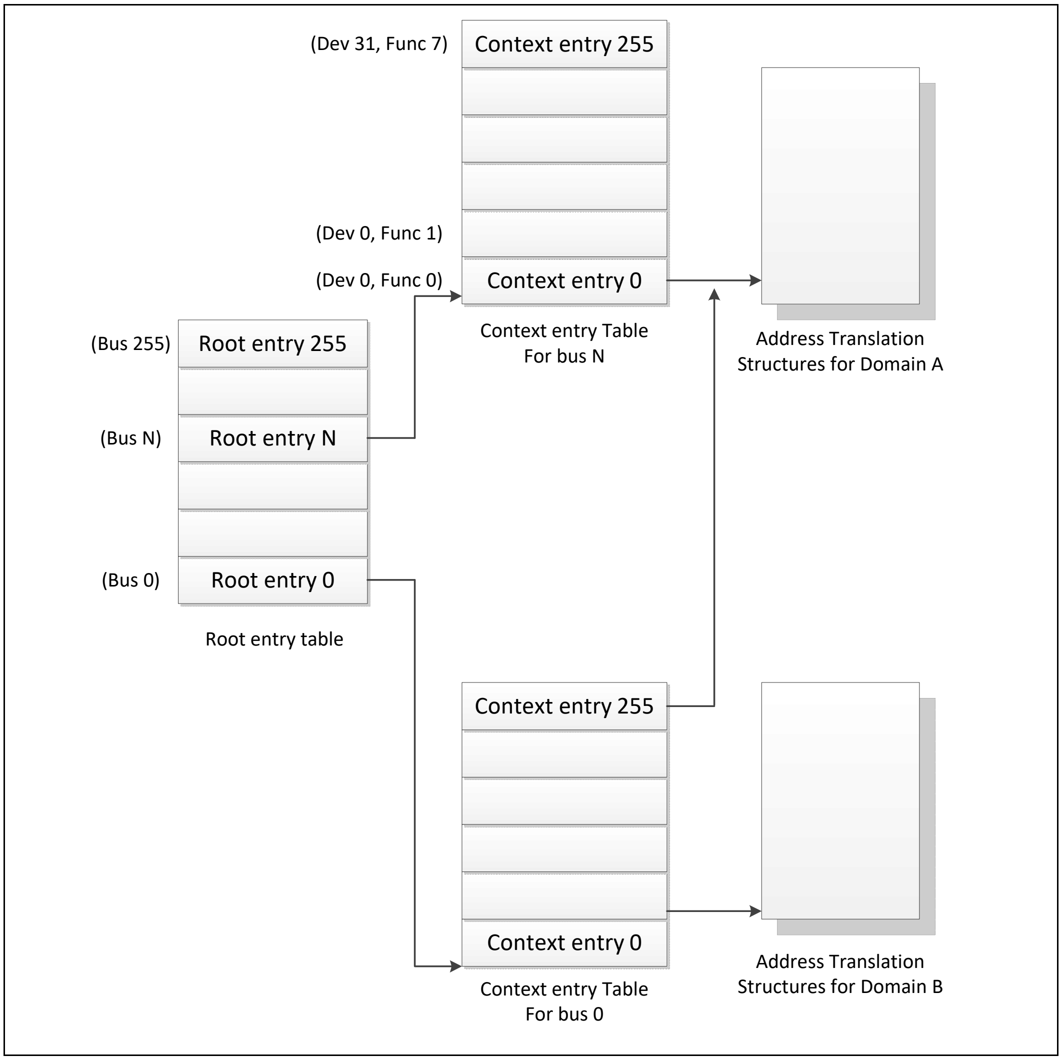
The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Intel VT-d provides accelerated I/O performance for a virtualized platform and provides software with the following capabilities:

- I/O device assignment and security: for flexibly assigning I/O devices to VMs and extending the protection and isolation properties of VMs for I/O operations.

- DMA remapping: for supporting independent address translations for Direct Memory Accesses (DMA) from devices.
- Interrupt remapping: for supporting isolation and routing of interrupts from devices and external interrupt controllers to appropriate VMs.
- Reliability: for recording and reporting to system software DMA and interrupt errors that may otherwise corrupt memory or impact VM isolation.

Intel VT-d accomplishes address translation by associating transaction from a given I/O device to a translation table associated with the Guest to which the device is assigned. It does this by means of the data structure in the following illustration. This table creates an association between the device's PCI Express* Bus/Device/Function (B/D/F) number and the base address of a translation table. This data structure is populated by a VMM to map devices to translation tables in accordance with the device assignment restrictions above, and to include a multi-level translation table (VT-d Table) that contains Guest specific address translations.

Figure 3-1. Device to Domain Mapping Structures



Intel VT-d functionality, often referred to as an Intel VT-d Engine, has typically been implemented at or near a PCI Express* host bridge component of a computer system. This might be in a chipset component or in the PCI Express functionality of a processor with integrated I/O. When one such VT-d engine receives a PCI Express transaction from a PCI Express bus, it uses the B/D/F number associated with the transaction to search for an Intel VT-d translation table. In doing so, it uses the B/D/F number to traverse the data structure shown in the above figure. If it finds a valid Intel VT-d table in this data structure, it uses that table to translate the address provided on the PCI Express bus. If it does not find a valid translation table for a given translation, this results in an Intel VT-d fault. If Intel VT-d translation is required, the Intel VT-d engine performs an N-level table walk.

For more information, refer to *Intel Virtualization Technology for Directed I/O Architecture Specification* http://www.intel.com/content/dam/www/public/us/en/documents/product-specifications/vt-directed-io-spec.pdf

Intel® VT-d Key Features

The processor supports the following Intel VT-d features:

- Memory controller and processor graphics comply with the Intel VT-d 2.1 Specification.
- Two Intel VT-d DMA remap engines.
    - iGFX DMA remap engine
    - Default DMA remap engine (covers all devices except iGFX)
- Support for root entry, context entry, and default context
- 39-bit guest physical address and host physical address widths
- Support for 4K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
- Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads, on IOTLB invalidation
- Support for Global, Domain specific and Page specific IOTLB invalidation
- MSI cycles (MemWr to address FEEx_xxxxh) not translated
    - Translation faults result in cycle forwarding to VBIOS region (byte enables masked for writes). Returned data may be bogus for internal agents, PEG/DMI interfaces return unsupported request status
- Interrupt Remapping is supported
- Queued invalidation is supported
- Intel VT-d translation bypass address range is supported (Pass Through)

The processor supports the following added new Intel VT-d features:

- 4-level Intel VT-d Page walk – both default Intel VT-d engine as well as the IGD VT-d engine are upgraded to support 4-level Intel VT-d tables (adjusted guest address width of 48 bits)

- Intel VT-d superpage – support of Intel VT-d superpage (2 MB, 1 GB) for default Intel VT-d engine (that covers all devices except IGD)

  IGD Intel VT-d engine does not support superpage and BIOS should disable superpage in default Intel VT-d engine when iGfx is enabled.

Note: Intel VT-d Technology may not be available on all SKUs.

3.2 Security Technologies

3.2.1 Intel® Trusted Execution Technology (Intel® TXT)

Intel® Trusted Execution Technology (Intel® TXT) defines platform-level enhancements that provide the building blocks for creating trusted platforms.

The Intel TXT platform helps to provide the authenticity of the controlling environment such that those wishing to rely on the platform can make an appropriate trust decision. The Intel TXT platform determines the identity of the controlling environment by accurately measuring and verifying the controlling software.

Another aspect of the trust decision is the ability of the platform to resist attempts to change the controlling environment. The Intel TXT platform will resist attempts by software processes to change the controlling environment or bypass the bounds set by the controlling environment.

Intel TXT is a set of extensions designed to provide a measured and controlled launch of system software that will then establish a protected environment for itself and any additional software that it may execute.

These extensions enhance two areas:

- The launching of the Measured Launched Environment (MLE).
- The protection of the MLE from potential corruption.

The enhanced platform provides these launch and control interfaces using Safer Mode Extensions (SMX).

The SMX interface includes the following functions:

- Measured/Verified launch of the MLE.
- Mechanisms to ensure the above measurement is protected and stored in a secure location.
- Protection mechanisms that allow the MLE to control attempts to modify itself.

The processor also offers additional enhancements to System Management Mode (SMM) architecture for enhanced security and performance. The processor provides new MSRs to:

- Enable a second SMM range
- Enable SMM code execution range checking
- Select whether SMM Save State is to be written to legacy SMRAM or to MSRs
- Determine if a thread is going to be delayed entering SMM
- Determine if a thread is blocked from entering SMM
- Targeted SMI, enable/disable threads from responding to SMIs, both VLWs and IPI

For the above features, BIOS should test the associated capability bit before attempting to access any of the above registers.

For more information, refer to the *Intel® Trusted Execution Technology Measured Launched Environment Programming Guide*

Note: Intel TXT Technology may not be available on all SKUs.

3.2.2 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)

The processor supports Intel Advanced Encryption Standard New Instructions (Intel AES-NI) that are a set of Single Instruction Multiple Data (SIMD) instructions that enable fast and secure data encryption and decryption based on the Advanced Encryption Standard (AES). Intel AES-NI are valuable for a wide range of cryptographic applications, such as applications that perform bulk encryption/decryption, authentication, random number generation, and authenticated encryption. AES is broadly accepted as the standard for both government and industry applications, and is widely deployed in various protocols.

Intel AES-NI consists of six Intel SSE instructions. Four instructions, AESENC, AESENCLAST, AESDEC, and AESDELAST facilitate high performance AES encryption and decryption. The other two, AESIMC and AESKEYGENASSIST, support the AES key expansion procedure. Together, these instructions provide full hardware for supporting AES; offering security, high performance, and a great deal of flexibility.

Note: Intel AES-NI Technology may not be available on all SKUs.

3.2.3 PCLMULQDQ (Perform Carry-Less Multiplication Quad word) Instruction

The processor supports the carry-less multiplication instruction, PCLMULQDQ. PCLMULQDQ is a Single Instruction Multiple Data (SIMD) instruction that computes the 128-bit carry-less multiplication of two 64-bit operands without generating and propagating carries. Carry-less multiplication is an essential processing component of several cryptographic systems and standards. Hence, accelerating carry-less multiplication can significantly contribute to achieving high speed secure computing and communication.

3.2.4 Intel® Secure Key

The processor supports Intel Secure Key (formerly known as Digital Random Number Generator (DRNG)), a software visible random number generation mechanism supported by a high quality entropy source. This capability is available to programmers through the RDRAND instruction. The resultant random number generation capability is designed to comply with existing industry standards in this regard (ANSI X9.82 and NIST SP 800-90).

Some possible usages of the RDRAND instruction include cryptographic key generation as used in a variety of applications, including communication, digital signatures, secure storage, and so on.

3.2.5 Execute Disable Bit

The Execute Disable Bit allows memory to be marked as non executable when combined with a supporting operating system. If code attempts to run in non-executable memory, the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can, thus, help improve the overall security of the system.

See the *Intel 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.

3.2.6 Boot Guard Technology

Boot Guard technology is a part of boot integrity protection technology. Boot Guard can help protect the platform boot integrity by preventing execution of unauthorized boot blocks. With Boot Guard, platform manufacturers can create boot policies such that invocation of an unauthorized (or untrusted) boot block will trigger the platform protection per the manufacturer's defined policy.

With verification based in the hardware, Boot Guard extends the trust boundary of the platform boot process down to the hardware level.

Boot Guard accomplishes this by:

- Providing of hardware-based Static Root of Trust for Measurement (S-RTM) and the Root of Trust for Verification (RTV) using Intel architectural components.
- Providing of architectural definition for platform manufacturer Boot Policy.
- Enforcing of manufacture provided Boot Policy using Intel architectural components.

Benefits of this protection is that Boot Guard can help maintain platform integrity by preventing re-purposing of the manufacturer’s hardware to run an unauthorized software stack.

3.2.7 Intel® Supervisor Mode Execution Protection (SMEP)

Intel® Supervisor Mode Execution Protection (SMEP) is a mechanism that provides the next level of system protection by blocking malicious software attacks from user mode code when the system is running in the highest privilege level. This technology helps to protect from virus attacks and unwanted code from harming the system. For more information, refer to *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A* at: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.8 Intel® Supervisor Mode Access Protection (SMAP)

Intel® Supervisor Mode Access Protection (SMAP) is a mechanism that provides next level of system protection by blocking a malicious user from tricking the operating system into branching off user data. This technology shuts down very popular attack vectors against operating systems.

For more information, refer to the *Intel ® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*: http://www.intel.com/Assets/PDF/manual/253668.pdf

3.2.9 Intel® Memory Protection Extensions (Intel® MPX)

Intel® MPX provides hardware accelerated mechanism for memory testing (heap and stack) buffer boundaries in order to identify buffer overflow attacks.

An Intel MPX enabled compiler inserts new instructions that tests memory boundaries prior to a buffer access. Other Intel MPX commands are used to modify a database of memory regions used by the boundary checker instructions.

The Intel MPX ISA is designed for backward compatibility and will be treated as no-operation instructions (NOPs) on older processors.

Intel MPX can be used for:

- Efficient runtime memory boundary checks for security-sensitive portions of the application.
- As part of a memory checker tool for finding difficult memory access errors. Intel MPX is significantly of magnitude faster than software implementations.

Intel MPX emulation (without hardware acceleration) is available with the Intel C++ Compiler 13.0 or newer.

For more information, refer to the Intel MPX documentation.

3.2.10 Intel® Software Guard Extensions (Intel® SGX)

Intel® Software Guard Extensions (Intel® SGX) is a processor enhancement designed to help protect application integrity and confidentiality of secrets and withstands software and certain hardware attacks.

Intel® Software Guard Extensions (Intel® SGX) architecture provides the capability to create isolated execution environments named Enclaves that operate from a protected region of memory.

Enclave code can be accessed using new special ISA commands that jump into per Enclave predefined addresses. Data within an Enclave can only be accessed from that same Enclave code.

The latter security statements hold under all privilege levels including supervisor mode (ring-0), System Management Mode (SMM) and other Enclaves.

Intel® SGX features a memory encryption engine that both encrypt Enclave memory as well as protect it from corruption and replay attacks.

Intel® SGX benefits over alternative Trusted Execution Environments (TEEs) are:

- Enclaves are written using C/C++ using industry standard build tools.
- High processing power as they run on the processor.
- Large amount of memory are available as well as non-volatile storage (such as disk drives).
- Simple to maintain and debug using standard IDEs (Integrated Development Environment)
- Scalable to a larger number of applications and vendors running concurrently
- Allow Launch Enclaves other than the one currently provided by Intel.

- Supported protected memory sizes:
  - Supports 32, 64 and 128MB.

For more information, refer to the Intel® SGX website at:

https://software.intel.com/en-us/sgx

Intel® SGX specifications and functional descriptions are included in the *Intel® 64 Architectures Software Developer's Manual, Volume 3*. Available at:

http://www.intel.com/products/processor/manuals

3.2.11 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)

Refer to Section 3.1.2 Intel VT-d for detail.

3.3 Power and Performance Technologies

3.3.1 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution processor IA core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature should be enabled using the BIOS and requires operating system support.

Note: Intel HT Technology may not be available on all SKUs.

3.3.2 Intel® Turbo Boost Technology 2.0

The Intel® Turbo Boost Technology 2.0 allows the processor IA core / processor graphics core to opportunistically and automatically run faster than the processor IA core base frequency / processor graphics base frequency if it is operating below power, temperature, and current limits. The Intel Turbo Boost Technology 2.0 feature is designed to increase performance of both multi-threaded and single-threaded workloads.

Compared with previous generation products, Intel Turbo Boost Technology 2.0 will increase the ratio of application power towards TDP and also allows to increase power above TDP as high as PL2 for short periods of time. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time.

Note: Intel Turbo Boost Technology 2.0 may not be available on all SKUs.

3.3.2.1 Intel® Turbo Boost Technology 2.0 Frequency

To determine the highest performance frequency amongst active processor IA cores, the processor takes the following into consideration:

- The number of processor IA cores operating in the C0 state.
- The estimated processor IA core current consumption and I_{CCMax} register settings.
- The estimated package prior and present power consumption and turbo power limits.
- The package temperature.
- Sustained turbo residencies at high voltages and temperature.

Any of these factors can affect the maximum frequency for a given workload. If the power, current, Voltage or thermal limit is reached, the processor will automatically reduce the frequency to stay within the PL1 value. Turbo processor frequencies are only active if the operating system is requesting the P0 state. If turbo frequencies are limited the cause is logged in IA_PERF_LIMIT_REASONS register. For more information on P-states and C-states, refer Chapter 4, “Power Management”.

3.3.3 Intel® Advanced Vector Extensions 2 (Intel® AVX2)

Intel® Advanced Vector Extensions 2.0 (Intel® AVX2) is the latest expansion of the Intel instruction set. Intel AVX2 extends the Intel Advanced Vector Extensions (Intel AVX) with 256-bit integer instructions, floating-point fused multiply add (FMA) instructions, and gather operations. The 256-bit integer vectors benefit math, codec, image, and digital signal processing software. FMA improves performance in face detection, professional imaging, and high performance computing. Gather operations increase vectorization opportunities for many applications. In addition to the vector extensions, this generation of Intel processors adds new bit manipulation instructions useful in compression, encryption, and general purpose software.
For more information on Intel AVX, see http://www.intel.com/software/avx

Intel Advanced Vector Extensions (Intel AVX) are designed to achieve higher throughput to certain integer and floating point operation. Due to varying processor power characteristics, utilizing AVX instructions may cause a) parts to operate below the base frequency b) some parts with Intel Turbo Boost Technology 2.0 to not achieve any or maximum turbo frequencies. Performance varies depending on hardware, software and system configuration and you should consult your system manufacturer for more information. Intel Advanced Vector Extensions refers to Intel AVX, Intel AVX2 or Intel AVX-512.
For more information on Intel AVX, see http://www-ssl.intel.com/content/www/us/en/architecture-and-technology/turbo-boost/turbo-boost-technology.html

Note: Intel AVX2 Technology may not be available on all SKUs.

3.3.4 Intel® 64 Architecture x2APIC

The x2APIC architecture extends the xAPIC architecture that provides key mechanisms for interrupt delivery. This extension is primarily intended to increase processor addressability.

Specifically, x2APIC:

- Retains all key elements of compatibility to the xAPIC architecture:
  - Delivery modes
  - Interrupt and processor priorities
  - Interrupt sources
  - Interrupt destination types
- Provides extensions to scale processor addressability for both the logical and physical destination modes
- Adds new features to enhance performance of interrupt delivery
- Reduces complexity of logical destination mode interrupt delivery on link based architectures

The key enhancements provided by the x2APIC architecture over xAPIC are the following:

- Support for two modes of operation to provide backward compatibility and extensibility for future platform innovations:
  - In xAPIC compatibility mode, APIC registers are accessed through memory mapped interface to a 4K-Byte page, identical to the xAPIC architecture.
  - In x2APIC mode, APIC registers are accessed through Model Specific Register (MSR) interfaces. In this mode, the x2APIC architecture provides significantly increased processor addressability and some enhancements on interrupt delivery.
- Increased range of processor addressability in x2APIC mode:
  - Physical xAPIC ID field increases from 8 bits to 32 bits, allowing for interrupt processor addressability up to 4G-1 processors in physical destination mode. A processor implementation of x2APIC architecture can support fewer than 32-bits in a software transparent fashion.
  - Logical xAPIC ID field increases from 8 bits to 32 bits. The 32-bit logical x2APIC ID is partitioned into two sub-fields – a 16-bit cluster ID and a 16-bit logical ID within the cluster. Consequently, ((2^20) - 16) processors can be addressed in logical destination mode. Processor implementations can support fewer than 16 bits in the cluster ID sub-field and logical ID sub-field in a software agnostic fashion.
- More efficient MSR interface to access APIC registers:
  - To enhance inter-processor and self-directed interrupt delivery as well as the ability to virtualize the local APIC, the APIC register set can be accessed only through MSR-based interfaces in x2APIC mode. The Memory Mapped IO (MMIO) interface used by xAPIC is not supported in x2APIC mode.
- The semantics for accessing APIC registers have been revised to simplify the programming of frequently-used APIC registers by system software. Specifically, the software semantics for using the Interrupt Command Register (ICR) and End Of Interrupt (EOI) registers have been modified to allow for more efficient delivery and dispatching of interrupts.

- The x2APIC extensions are made available to system software by enabling the local x2APIC unit in the "x2APIC" mode. To benefit from x2APIC capabilities, a new operating system and a new BIOS are both needed, with special support for x2APIC mode.
- The x2APIC architecture provides backward compatibility to the xAPIC architecture and forward extendible for future Intel platform innovations.

Note: Intel x2APIC Technology may not be available on all SKUs.

For more information, see the Intel® *64 Architecture x2APIC Specification* at http://www.intel.com/products/processor/manuals/.

3.3.5 Power Aware Interrupt Routing (PAIR)

The processor includes enhanced power-performance technology that routes interrupts to threads or processor IA cores based on their sleep states. As an example, for energy savings, it routes the interrupt to the active processor IA cores without waking the deep idle processor IA cores. For performance, it routes the interrupt to the idle (C1) processor IA cores without interrupting the already heavily loaded processor IA cores. This enhancement is mostly beneficial for high-interrupt scenarios like Gigabit LAN, WLAN peripherals, and so on.

3.3.6 Intel® Transactional Synchronization Extensions (Intel® TSX-NI)

Intel® Transactional Synchronization Extensions (Intel® TSX-NI) provides a set of instruction set extensions that allow programmers to specify regions of code for transactional synchronization. Programmers can use these extensions to achieve the performance of fine-grain locking while actually programming using coarse-grain locks. Details on Intel TSX-NI may be found in *Intel® Architecture Instruction Set Extensions Programming Reference.*

Note: Intel TSX-NI may not be available on all SKUs.

3.4 Debug Technologies

3.4.1 Intel® Processor Trace

Intel® Processor Trace (Intel® PT) is a new tracing capability added to Intel Architecture, for use in software debug and profiling. Intel PT provides the capability for more precise software control flow and timing information, with limited impact to software execution. This provides enhanced ability to debug software crashes, hangs, or other anomalies, as well as responsiveness and short-duration performance issues.

Intel VTune™ Amplifier for Systems and the Intel System Debugger are part of Intel System Studio 2015, which includes updates for new debug and trace features on this latest platform, including Intel PT and Intel Trace Hub.

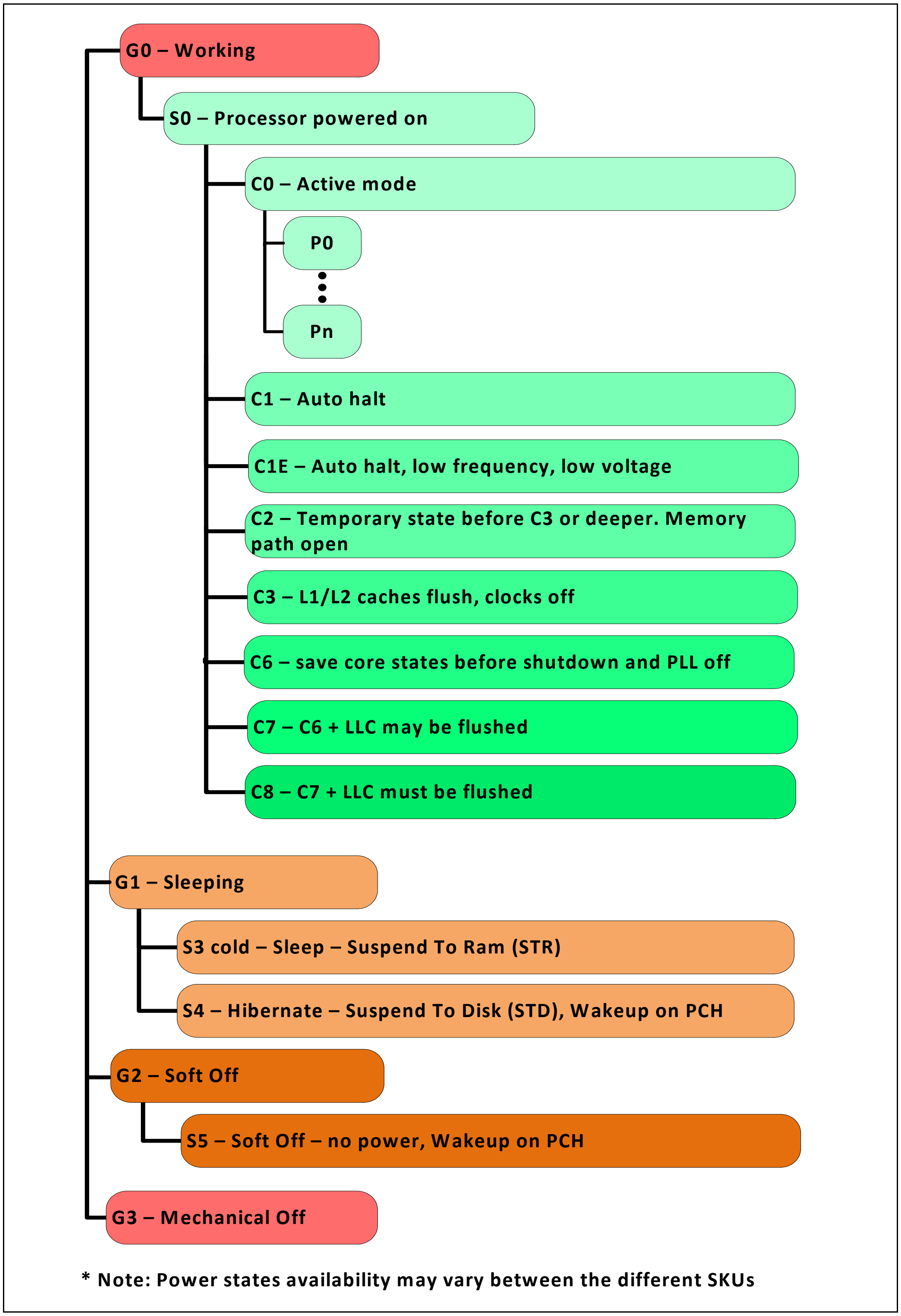
§ §

4 Power Management

This chapter provides information on the following power management topics:

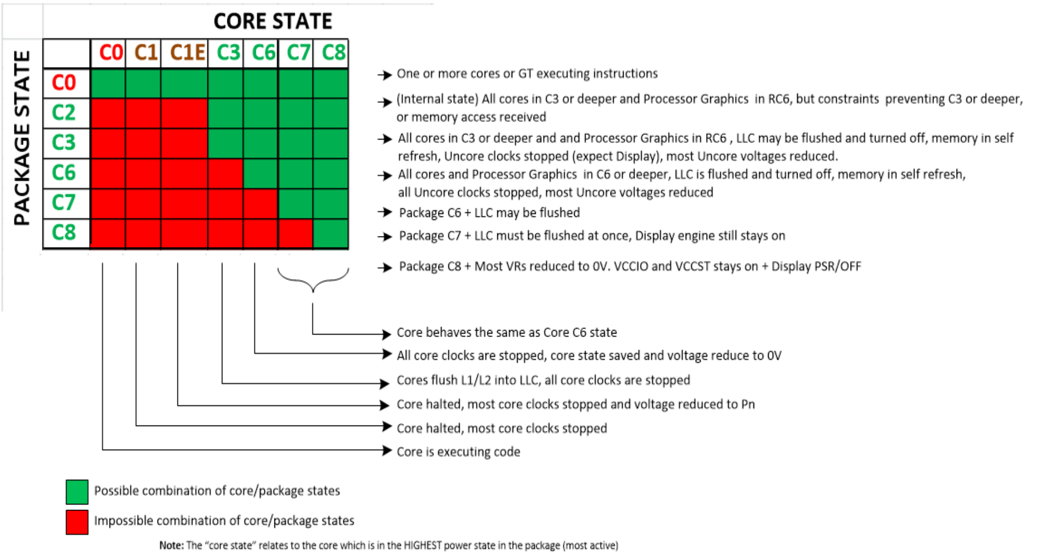
- Advanced Configuration and Power Interface (ACPI) States
- Processor IA Core Power Management
- Integrated Memory Controller (IMC) Power Management
- PCI Express* Power Management
- Direct Media Interface (DMI) Power Management
- Processor Graphics Power Management

Figure 4-1. Processor Power States



* Note: Power states availability may vary between the different SKUs

Figure 4-2. Processor Package and IA Core C-States



CORE STATE

PACKAGE STATE	C0	C1	C1E	C3	C6	C7	C8
C0	🟩	🟩	🟩	🟩	🟩	🟩	🟩
C2	🟥	🟥	🟥	🟩	🟩	🟩	🟩
C3	🟥	🟥	🟥	🟩	🟩	🟩	🟩
C6	🟥	🟥	🟥	🟥	🟩	🟩	🟩
C7	🟥	🟥	🟥	🟥	🟥	🟩	🟩
C8	🟥	🟥	🟥	🟥	🟥	🟥	🟩

→ One or more cores or GT executing instructions

→ (Internal state) All cores in C3 or deeper and Processor Graphics in RC6, but constraints preventing C3 or deeper, or memory access received

→ All cores in C3 or deeper and and Processor Graphics in RC6 , LLC may be flushed and turned off, memory in self refresh, Uncore clocks stopped (expect Display), most Uncore voltages reduced.

→ All cores and Processor Graphics in C6 or deeper, LLC is flushed and turned off, memory in self refresh, all Uncore clocks stopped, most Uncore voltages reduced

→ Package C6 + LLC may be flushed

→ Package C7 + LLC must be flushed at once, Display engine still stays on

→ Package C8 + Most VRs reduced to 0V. VCCIO and VCCST stays on + Display PSR/OFF

→ Core behaves the same as Core C6 state

→ All core clocks are stopped, core state saved and voltage reduce to 0V

→ Cores flush L1/L2 into LLC, all core clocks are stopped

→ Core halted, most core clocks stopped and voltage reduced to Pn

→ Core halted, most core clocks stopped

→ Core is executing code

🟩 Possible combination of core/package states

🟥 Impossible combination of core/package states

Note: The “core state” relates to the core which is in the HIGHEST power state in the package (most active)

4.1 Advanced Configuration and Power Interface (ACPI) States Supported

This section describes the ACPI states supported by the processor.

Table 4-1. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wake-up on PCH).
G2/S5	Soft off. All power lost (except wake-up on PCH). Total reboot.
G3	Mechanical off. All power removed from system.

Table 4-2. Processor IA Core / Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT processor IA core state (package C0 state).
C1E	AutoHALT processor IA core state with lowest frequency and voltage operating point (package C0 state).
C2	All processor IA cores in C3 or deeper. Memory path open. Temporary state before Package C3 or deeper.
C3	Processor IA execution cores in C3 or deeper, flush their L1 instruction cache, L1 data cache, and L2 cache to the LLC shared cache. LLC may be flushed. Clocks are shut off to each core.
C6	Processor IA execution cores in this state save their architectural state before removing core voltage. BCLK is off.
C7	Processor IA execution cores in this state behave similarly to the C6 state. If all execution cores request C7, LLC ways may be flushed until it is cleared. If the entire LLC is flushed, voltage will be removed from the LLC.
C8	C7 plus LLC should be flushed.

Table 4-3. Integrated Memory Controller (IMC) States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE de-asserted (not self-refresh) with all banks closed.
Active Power down	CKE de-asserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE de-asserted using device self-refresh.

Table 4-4. PCI Express* Link States

State	Description
L0	Full on – Active transfer state.
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-5. Direct Media Interface (DMI) States

State	Description
L0	Full on – Active transfer state
L1	Lowest Active Power Management – Longer exit latency
L3	Lowest power state (power-off) – Longest exit latency

Table 4-6. G, S, and C Interface State Combinations

Global (G) State	Sleep (S) State	Processor Package (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6/C7	Deep Power Down	On	Deep Power Down
G0	S0	C8	Off	On	Deeper Power Down
G1	S3	Power off	Off	Off, except RTC	Suspend to RAM
G1	S4	Power off	Off	Off, except RTC	Suspend to Disk
G2	S5	Power off	Off	Off, except RTC	Soft Off
G3	N/A	Power off	Off	Power off	Hard off

4.2 Processor IA Core Power Management

While executing code, Enhanced Intel SpeedStep Technology and Intel Speed Shift® Technology optimizes the processor’s IA core frequency and voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, deeper power C-states have longer entry and exit latencies.

4.2.1 OS/HW controlled P-states

4.2.1.1 Enhanced Intel® SpeedStep® Technology

Enhanced Intel® SpeedStep® Technology enables OS to control and select P-state. The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor IA cores.
    - Once the voltage is established, the PLL locks on to the target frequency.
    - All active processor IA cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested among all active IA cores is selected.
    - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.1.2 Intel® Speed Shift Technology

Intel Speed Shift Technology is an energy efficient method of frequency control by the hardware rather than relying on OS control. OS is aware of available hardware P-states and request a desired P-state or it can let Hardware determine the P-state. The OS request is based on its workload requirements and awareness of processor capabilities. Processor decision is based on the different system constraints for example: Workload demand, thermal limits while taking into consideration the minimum and maximum levels and activity window of performance requested by the operating system.

For more details, refer to the following document (see related documents section):

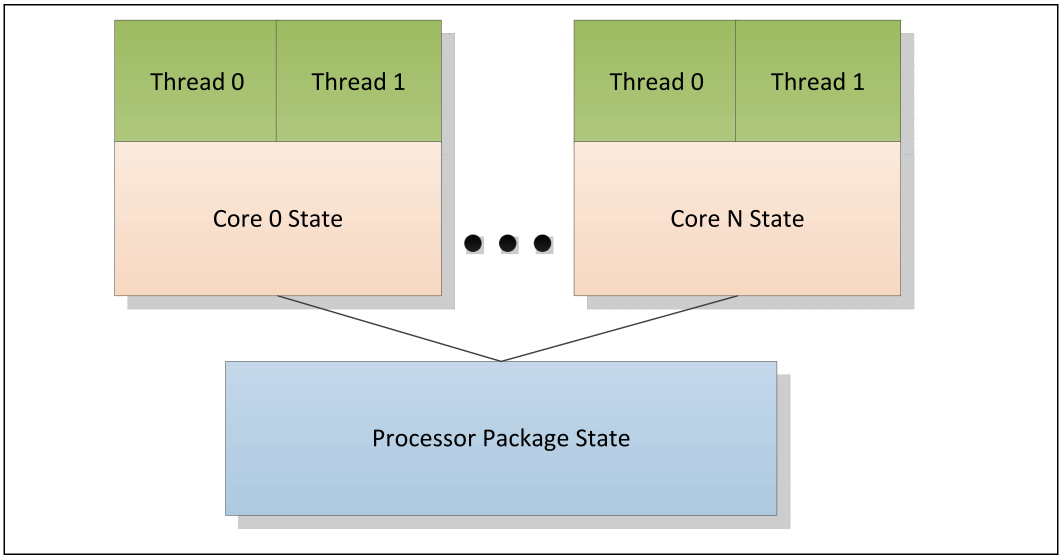
- Intel® 64 and IA-32 Architectures Software Developer's Manual (SDM), Volume 3B.

4.2.2 Low-Power Idle States

When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, deeper C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor IA core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Caution: Long term reliability cannot be assured unless all the Low-Power Idle States are enabled.

Figure 4-3. Idle Power Management Breakdown of the Processor IA Cores



While individual threads can request low-power C-states, power saving actions only take place once the processor IA core C-state is resolved. processor IA core C-states are automatically resolved by the processor. For thread and processor IA core C-states, a transition to and from C0 state is required before entering any other C-state.

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low-power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions using I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, should be enabled in the BIOS.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range do not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

When P_LVLx I/O instructions are used, MWAIT sub-states cannot be defined. The MWAIT sub-state is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF’ feature that triggers a wake up on an interrupt, even if interrupts are masked by EFLAGS.IF.

4.2.4 Processor IA Core C-State Rules

The following are general rules for all processor IA core C-states, unless specified otherwise:

- A processor IA core C-State is determined by the lowest numerical thread state (such as Thread 0 requests C1E while Thread 1 requests C3 state, resulting in a processor IA core C1E state). Refer Table 4-6, “G, S, and C Interface State Combinations”.
- A processor IA core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered using an MWAIT/Timed MWAIT instruction
  - The deadline corresponding to the Timed MWAIT instruction expires
- An interrupt directed toward a single thread wakes up only that thread.
- If any thread in a processor IA core is active (in C0 state), the core’s C-state will resolve to C0.
- Any interrupt coming into the processor package may wake any processor IA core.
- A system reset re-initializes all processor IA cores.

processor IA core C0 State

The normal operating state of a processor IA core where code is being executed.

processor IA core C1/C1E State

C1/C1E is a low-power state entered when all threads within a processor IA core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel 64 and IA-32 Architectures Software Developer's Manual* for more information.

While a processor IA core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see Section 4.2.5.

processor IA core C3 State

Individual threads of a processor IA core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A processor IA core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared LLC, while maintaining its architectural state. All processor IA core clocks are stopped at this point. Because the processor IA core's caches are flushed, the processor does not wake any processor IA core that is in the C3 state when either a snoop is detected or when another processor IA core accesses cacheable memory.

processor IA core C6 State

Individual threads of a processor IA core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering processor IA core C6 state, the processor IA core will save its architectural state to a dedicated SRAM. Once complete, a processor IA core will have its voltage reduced to zero volts. During exit, the processor IA core is powered on and its architectural state is restored.

processor IA core C7-C8 States

Individual threads of a processor IA core can enter the C7 orC8 state by initiating a P_LVL4, P_LVL5, P_LVL6, P_LVL7 I/O read (respectively) to the P_BLK or by an MWAIT(C7/C8/C9/C10) instruction. The processor IA core C7-C8 state exhibits the same behavior as the processor IA core C6 state.

C-State Auto-Demotion

In general, deeper C-states, such as C6 or C7, have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore, incorrect or inefficient usage of deeper C-states have a negative impact on battery life and idle power. To increase residency and improve battery life and idle power in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C7/C6 to C3
- C7/C6/C3 To C1

The decision to demote a processor IA core from C6/C7 to C3 or C3/C6/C7 to C1 is based on each processor IA core's immediate residency history. Upon each processor IA core C6/C7 request, the processor IA core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a processor IA core is allowed to go into C3/C6 or C7. Each option can be run concurrently or individually. If the interrupt rate experienced on a processor IA core is high and the processor IA core is rarely in a deep C-state between such interrupts, the processor IA core can be demoted to a C3 or C1 state. A higher interrupt pattern is required to demote a processor IA core to C1 as compared to C3.

This feature is disabled by default. BIOS should enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register.

4.2.5 Package C-States

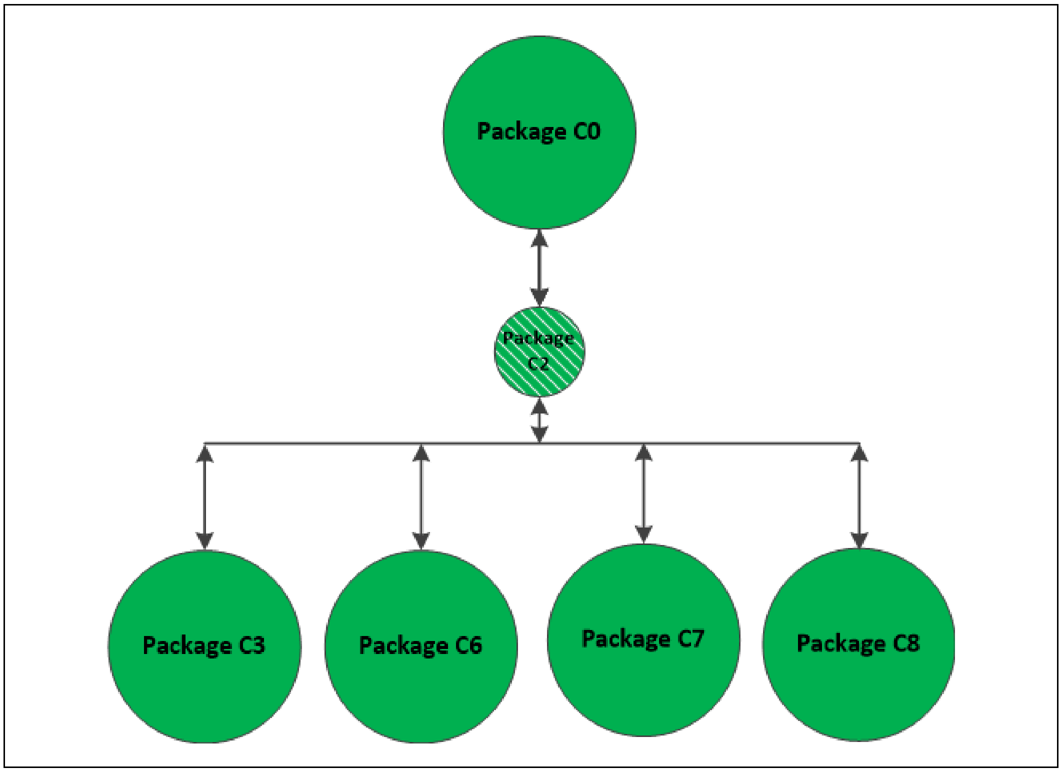
The processor supports C0, C2, C3, C6, C7, and C8 package states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states, unless specified otherwise:

- A package C-state request is determined by the lowest numerical processor IA core C-state amongst all processor IA cores.
- A package C-state is automatically resolved by the processor depending on the processor IA core idle power states and the status of the platform components.
    - Each processor IA core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
    - The platform may allow additional power savings to be realized in the processor.
    - For package C-states, the processor is not required to enter C0 before entering any other C-state.
    - Entry into a package C-state may be subject to auto-demotion – that is, the processor may keep the package in a deeper package C-state then requested by the operating system if the processor determines, using heuristics, that the deeper C-state results in better power/performance.

The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a processor IA core break event is received, the target processor IA core is activated and the break event message is forwarded to the target processor IA core.
    - If the break event is not masked, the target processor IA core enters the processor IA core C0 state and the processor enters package C0.
    - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request,
    - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
    - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

Figure 4-4. Package C-State Entry and Exit



Package C0

This is the normal operating state for the processor. The processor remains in the normal state when at least one of its processor IA cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low-power state. Individual processor IA cores may be in deeper power idle states while the package is in C0 state.

Package C2 State

Package C2 state is an internal processor state that cannot be explicitly requested by software. A processor enters Package C2 state when either:

- All processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6, but constraints (LTR, programmed timer events in the near future, and so forth) prevent entry to any state deeper than C2 state.
- Or, all processor IA cores have requested a C3 or deeper power state and all graphics processor IA cores requested are in RC6 and a memory access request is received. Upon completion of all outstanding memory requests, the processor transitions back into a deeper package C-state.

Package C3 State

A processor enters the package C3 low-power state when:

- At least one processor IA core is in the C3 state.

- The other processor IA cores are in a C3 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6/C7 state or deeper state but has allowed a package C3 state.

In package C3-state, the LLC shared cache is valid.

Package C6 State

A processor enters the package C6 low-power state when:

- At least one processor IA core is in the C6 state.
- The other processor IA cores are in a C6 or deeper power state, and the processor has been granted permission by the platform.
- The platform has not granted a package C7 or deeper request but has allowed a C6 package state.

In package C6 state, all processor IA cores have saved their architectural state and have had their voltages reduced to zero volts. It is possible the LLC shared cache is flushed and turned off in package C6 state.

Package C7 State

The processor enters the package C7 low-power state when all processor IA cores are in the C7 or deeper state and the operating system may request that the LLC will be flushed.

Processor IA core break events are handled the same way as in package C3 or C6.

Upon exit of the package C7 state, the LLC will be partially enabled once a processor IA core wakes up if it was fully flushed, and will be fully enabled once the processor has stayed out of C7 for a preset amount of time. Power is saved since this prevents the LLC from being re-populated only to be immediately flushed again. Some VRs are reduce to 0V.

Package C8 State

The processor enters C8 states when the processor IA cores lower numerical state is C8.

The C8 state is similar to C7 state, but in addition, the LLC is flushed in a single step, Vcc and Vcc_{GT} are reduced to 0V. The display engine stays on.

InstantGo

InstantGo is a platform state. On display time out the OS requests the processor to enter package C10 and platform devices at RTD3 (or disabled) in order to attain low power in idle.

Dynamic LLC Sizing

When all processor IA cores request C7 or deeper C-state, internal heuristics dynamically flushes the LLC. Once the processor IA cores enter a deep C-state, depending on their MWAIT sub-state request, the LLC is either gradually flushed N-ways at a time or flushed all at once. Upon the processor IA cores exiting to C0 state, the LLC is gradually expanded based on internal heuristics.

4.2.6 Package C-States and Display Resolutions

The integrated graphics engine has the frame buffer located in system memory. When the display is updated, the graphics engine fetches display data from system memory. Different screen resolutions and refresh rates have different memory latency requirements. These requirements may limit the deepest Package C-state the processor can enter. Other elements that may affect the deepest Package C-state available are the following:

- Display is on or off
- Single or multiple displays
- Native or non-native resolution
- Panel Self Refresh (PSR) technology

Note: Display resolution is not the only factor influencing the deepest Package C-state the processor can get into. Device latencies, interrupt response latencies, and core C-states are among other factors that influence the final package C-state the processor can enter.

The following table lists display resolutions and deepest available package C-State.The display resolutions are examples using common values for blanking and pixel rate. Actual results will vary. The table shows the deepest possible Package C-state.System workload, system idle, and AC or DC power also affect the deepest possible Package C-state.

Table 4-7. Deepest Package C-State Available

S Processor Line
PSR Disabled
PC8

Notes:
1. All Deep states are with Display ON.
2. The deepest package C-state dependents on various factors, including Platform devices, HW configuration and peripheral software.

4.3 Integrated Memory Controller (IMC) Power Management

The main memory is power managed during normal operation and in low-power ACPI C-states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory in which it is not connected to any actual memory devices (such as SODIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding control signals (CLK_P/CLK_N/CKE/ODT/CS) are not driven.

At reset, all rows should be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tri-stated with a DRAMs present, the DRAMs are not ensured to maintain data integrity. CKE tri-state should be enabled by BIOS where appropriate, since at reset all rows should be assumed to be populated.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the memory interface.Each channel drives 4 CKE pins, one per rank.

The CKE is one of the power-saving means. When CKE is off, the internal DDR clock is disabled and the DDR power is reduced. The power-saving differs according to the selected mode and the DDR type used. For more information, refer to the IDD table in the DDR specification.

The processor supports four different types of power-down modes in package C0 state. The different power-down modes can be enabled through configuring PM PDWN configuration register. The type of CKE power-down can be configured through PDWN_mode (bits 15:12) and the idle timer can be configured through PDWN_idle_counter (bits 11:0). The different power-down modes supported are:

- **No power-down** (CKE disable)
- **Active power-down (APD):** This mode is entered if there are open pages when de-asserting CKE. In this mode the open pages are retained. Power-saving in this mode is the lowest. Power consumption of DDR is defined by IDD3P. Exiting this mode is fined by tXP – small number of cycles. For this mode, DRAM DLL should be on.
- **PPD/DLL-off:** In this mode the data-in DLLs on DDR are off. Power-saving in this mode is the best among all power modes. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP, but also tXPDLL (10–20 according to DDR type) cycles until first data transfer is allowed. For this mode, DRAM DLL should be off.
- **Precharged power-down (PPD):** This mode is entered if all banks in DDR are precharged when de-asserting CKE. Power-saving in this mode is intermediate – better than APD, but less than DLL-off. Power consumption is defined by IDD2P. Exiting this mode is defined by tXP. The difference from APD mode is that when waking-up, all page-buffers are empty.) The LPDDR does not have a DLL. As a result, the power savings are as good as PPD/DDL-off but will have lower exit latency and higher performance.

The CKE is determined per rank, whenever it is inactive. Each rank has an idle counter. The idle-counter starts counting as soon as the rank has no accesses, and if it expires, the rank may enter power-down while no new transactions to the rank arrives to queues. The idle-counter begins counting at the last incoming transaction arrival.

It is important to understand that since the power-down decision is per rank, the IMC can find many opportunities to power down ranks, even while running memory intensive applications; the savings are significant (may be few Watts, according to DDR specification). This is significant when each channel is populated with more ranks.

Selection of power modes should be according to power-performance or thermal trade-off of a given system:

- When trying to achieve maximum performance and power or thermal consideration is not an issue: use no power-down
- In a system which tries to minimize power-consumption, try using the deepest power-down mode possible – PPD/DLL-off with a low idle timer value
- In high-performance systems with dense packaging (that is, tricky thermal design) the power-down mode should be considered in order to reduce the heating and avoid DDR throttling caused by the heating.

The default value that BIOS configures in PM PDWN configuration register is 6080 – that is, PPD/DLL-off mode with idle timer of 0x80, or 128 DCLKs. This is a balanced setting with deep power-down mode and moderate idle timer value.

The idle timer expiration count defines the # of DCLKs that a rank is idle that causes entry to the selected power mode. As this timer is set to a shorter time the IMC will have more opportunities to put the DDR in power-down. There is no BIOS hook to set this register. Customers choosing to change the value of this register can do it by changing it in the BIOS. For experiments, this register can be modified in real time if BIOS does not lock the IMC registers.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level recognized (other than the reset pin) once power is applied. It should be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is ensured to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

During S0 idle state, system memory may be conditionally placed into self-refresh state when the processor is in package C3 or deeper power state. Refer to Section 4.6.1.1 for more details on conditional self-refresh with Intel HD Graphics enabled.

When entering the S3 – Suspend-to-RAM (STR) state or S0 conditional self-refresh, the processor IA core flushes pending cycles and then enters SDRAM ranks that are not used by the processor graphics into self-refresh. The CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for package C3 or deeper power states as long as there are no memory requests to service.

Table 4-8. Targeted Memory State Conditions (Sheet 1 of 2)

State	Memory State with Processor Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power-down based on idle conditions.	Dynamic memory rank power-down based on idle conditions.
C3, C6, C7 or deeper	If the processor graphics engine is idle and there are no pending display requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power-down based on idle conditions.

Table 4-8. Targeted Memory State Conditions (Sheet 2 of 2)

State	Memory State with Processor Graphics	Memory State with External Graphics
S3	Self-Refresh Mode	Self-Refresh Mode
S4	Memory power-down (contents lost)	Memory power-down (contents lost)

4.3.2.3 Dynamic Power-Down

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power-down state. The processor IA core controller can be configured to put the devices in active power-down (CKE de-assertion with open pages) or precharge power-down (CKE de-assertion with all pages closed). Precharge power-down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power-down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks, CKE, ODT and CS signals are controlled per DIMM rank and will be powered down for unused ranks.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path should be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.3.3 DDR Electrical Power Gating (EPG)

The DDR I/O of the processor supports Electrical Power Gating (DDR-EPG) while the processor is at C3 or deeper power state.

In C3 or deeper power state, the processor internally gates VDDQ for the majority of the logic to reduce idle power while keeping all critical DDR pins such as CKE and VREF in the appropriate state.

In C7 or deeper power state, the processor internally gates V_{CCIO} for all non-critical state to reduce idle power.

In S3 or C-state transitions, the DDR does not go through training mode and will restore the previous training information.

4.3.4 Power Training

BIOS MRC performing Power Training steps to reduce DDR I/O power while keeping reasonable operational margins, still ensuring platform operation. The algorithms attempt to weaken ODT, driver strength and the related buffers parameters both on the MC and the DRAM side and find the best possible trade-off between the total I/O power and the operational margins using advanced mathematical models.

4.4 PCI Express* Power Management

- Active power management support using L1 state.
- All inputs and outputs disabled in L2/L3 Ready state.

Note: Processor PEG-PCIe interface does not support Hot-Plug.

Hot Plug like* is only supported at Processor PEG-PCIe using Thunderbolt Device.

* Turning Thunderbolt™ power on and Off electrically RTD3 Like

Table 4-9. Package C-States with PCIe* Link States Dependencies

PEG/DMI	L-State	Description	Package C-State
DMI	L1	Higher latency, lower power "standby" state	PC6-PC8
PEG	L1, L2, Disabled, NDA (no device attached)	L1- Higher latency, lower power "standby" state L2 – Auxiliary-powered Link, deep-energy-saving state. Disabled - The intent of the Disabled state is to allow a configured Link to be disabled until directed or Electrical Idle is exited (i.e., due to a hot removal and insertion) after entering Disabled. NDA- no physical device is attached on PEG port	PC6-PC7
PEG	L2, Disabled, NDA (no device attached)	L2 – Auxiliary-powered Link, deep-energy-saving state. Disabled - The intent of the Disabled state is to allow a configured Link to be disabled until directed or Electrical Idle is exited (i.e., due to a hot removal and insertion) after entering Disabled. NDA- no physical device is attached on PEG port	PC8

4.5 Direct Media Interface (DMI) Power Management

Note: Active power management support using L1 state.

4.6 Processor Graphics Power Management

4.6.1 Memory Power Savings Technologies

4.6.1.1 Intel® Rapid Memory Power Management (Intel® RMPM)

Intel® Rapid Memory Power Management (Intel® RMPM) conditionally places memory into self-refresh when the processor is in package C3 or deeper power state to allow the system to remain in the deeper power states longer for memory not reserved for graphics memory. Intel RMPM functionality depends on graphics/display state (relevant only when processor graphics is being used), as well as memory traffic patterns generated by other connected I/O devices.

4.6.1.2 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC. Intel S2DDT is only enabled in single pipe mode.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, and so on. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, processor benchmarks, and so on, or conditions when the processor is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.6.2 Display Power Savings Technologies

4.6.2.1 Intel® (Seamless & Static) Display Refresh Rate Switching (DRRS) with eDP* Port

Intel DRRS provides a mechanism where the monitor is placed in a slower refresh rate (the rate at which the display is updated). The system is smart enough to know that the user is not displaying either 3D or media like a movie where specific refresh rates are required. The technology is very useful in an environment such as a plane where the user is in battery mode doing E-mail, or other standard office applications. It is also useful where the user may be viewing web pages or social media sites while in battery mode.

4.6.2.2 Intel® Automatic Display Brightness

Intel Automatic Display Brightness feature dynamically adjusts the backlight brightness based upon the current ambient light environment. This feature requires an additional sensor to be on the panel front. The sensor receives the changing ambient light conditions and sends the interrupts to the Intel Graphics driver. As per the change in Lux, (current ambient light illuminance), the new backlight setting can be adjusted through BLC. The converse applies for a brightly lit environment. Intel Automatic Display Brightness increases the backlight setting.

4.6.2.3 Smooth Brightness

The Smooth Brightness feature is the ability to make fine grained changes to the screen brightness. All Windows* 10 system that support brightness control are required to support Smooth Brightness control and it should be supporting 101 levels of brightness control. Apart from the Graphics driver changes, there may be few System BIOS changes required to make this feature functional.

4.6.2.4 Intel® Display Power Saving Technology (Intel® DPST) 6.0

The Intel DPST technique achieves backlight power savings while maintaining a good visual experience. This is accomplished by adaptively enhancing the displayed image while decreasing the backlight brightness simultaneously. The goal of this technique is to provide equivalent end-user-perceived image quality at a decreased backlight power level.

1. The original (input) image produced by the operating system or application is analyzed by the Intel DPST subsystem. An interrupt to Intel DPST software is generated whenever a meaningful change in the image attributes is detected. (A meaningful change is when the Intel DPST software algorithm determines that enough brightness, contrast, or color change has occurred to the displaying images that the image enhancement and backlight control needs to be altered.)

2. Intel DPST subsystem applies an image-specific enhancement to increase image contrast, brightness, and other attributes.
3. A corresponding decrease to the backlight brightness is applied simultaneously to produce an image with similar user-perceived quality (such as brightness) as the original image.

Intel DPST 6.0 has improved the software algorithms and has minor hardware changes to better handle backlight phase-in and ensures the documented and validated method to interrupt hardware phase-in.

4.6.2.5 Panel Self-Refresh 2 (PSR 2)

Panel Self-Refresh feature allows the Processor Graphics core to enter low-power state when the frame buffer content is not changing constantly. This feature is available on panels capable of supporting Panel Self-Refresh. Apart from being able to support, the eDP* panel should be eDP 1.4 compliant. PSR 2 adds partial frame updates and requires an eDP 1.4 compliant panel.
PSR2 is limited to 3200x2000@60 Maximum display resolution.

4.6.2.6 Low-Power Single Pipe (LPSP)

Low-power single pipe is a power conservation feature that helps save power by keeping the inactive pipes powered OFF. This feature is enabled only in a single display configuration without any scaling functionalities. This feature is supported from 4th Generation Intel® Core™ processor family onwards. LPSP is achieved by keeping a single pipe enabled during eDP* only with minimal display pipeline support. This feature is panel independent and works with any eDP panel (port A) in single display mode.

4.6.3 Processor Graphics Core Power Savings Technologies

4.6.3.1 Intel® Graphics Dynamic Frequency

Intel Turbo Boost Technology 2.0 is the ability of the processor IA cores and graphics (Graphics Dynamic Frequency) cores to opportunistically increase frequency and/or voltage above the guaranteed processor and graphics frequency for the given part. Intel Graphics Dynamic Frequency is a performance feature that makes use of unused package power and thermals to increase application performance. The increase in frequency is determined by how much power and thermal budget is available in the package, and the application demand for additional processor or graphics performance. The processor IA core control is maintained by an embedded controller. The graphics driver dynamically adjusts between P-States to maintain optimal performance, power, and thermals. The graphics driver will always place the graphics engine in its lowest possible P-State. Intel Graphics Dynamic Frequency requires BIOS support. Additional power and thermal budget should be available.

4.6.3.2 Intel® Graphics Render Standby Technology (Intel® GRST)

The final power savings technology from Intel happens while the system is asleep. This is another technology where the voltage is adjusted down. For RC6, the voltage is adjusted very low, or very close to zero, what may reduced power by over 1000.

4.6.3.3 Dynamic FPS (DFPS)

Dynamic FPS (DFPS) or dynamic frame-rate control is a runtime feature for improving power-efficiency for 3D workloads. Its purpose is to limit the frame-rate of full screen 3D applications without compromising on user experience. By limiting the frame rate, the load on the graphics engine is reduced, giving an opportunity to run the Processor Graphics at lower speeds, resulting in power savings. This feature works in both AC/DC modes.

4.7 Voltage Optimization

Voltage Optimization opportunistically provides reduction in power consumption, that is, a boost in performance at a given PL1. Over time the benefit is reduced. There is no change to base frequency or turbo frequency. During system validation and tuning, this feature should be disabled to reflect processor power and performance that is expected over time.

This feature is available on selected SKUs.

§ §

5 Thermal Management

5.1 Processor Thermal Management

The thermal solution provides both component-level and system-level thermal management. To allow optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Bare Die Parts: Remains below the maximum junction temperature (Tj_{MAX}) specification at the maximum thermal design power (TDP).
- Lidded Parts: Remains below the maximum case temperature (Tcmax) specification at the maximum thermal design power.
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1.1 Thermal Considerations

The processor TDP is the maximum sustained power that should be used for design of the processor thermal solution. TDP is a power dissipation and component temperature operating condition limit, specified in this document, that is validated during manufacturing for the base configuration when executing a near worst case commercially available workload as specified by Intel for the SKU segment. TDP may be exceeded for short periods of time or if running a very high power workload.

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum component temperature specifications. For lidded parts, the appropriate case temperature (TCASE) specifications is defined by the applicable thermal profile. For bare die parts the component temperature specification is the applicable Tj_max.

Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The processor integrates multiple processing IA cores, graphics cores and for some SKUs a PCH, or a PCH and EDRAM, on a single package.This may result in power distribution differences across the package and should be considered when designing the thermal solution.

Intel Turbo Boost Technology 2.0 allows processor IA cores to run faster than the base frequency. It is invoked opportunistically and automatically as long as the processor is conforming to its temperature, voltage, power delivery and current control limits. When Intel Turbo Boost Technology 2.0 is enabled:

- Applications are expected to run closer to TDP more often as the processor will attempt to maximize performance by taking advantage of estimated available energy budget in the processor package.

- The processor may exceed the TDP for short durations to utilize any available thermal capacitance within the thermal solution. The duration and time of such operation can be limited by platform runtime configurable registers within the processor.
- Graphics peak frequency operation is based on the assumption of only one of the graphics domains (GT) being active. This definition is similar to the IA core Turbo concept, where peak turbo frequency can be achieved when only one IA core is active. Depending on the workload being applied and the distribution across the graphics domains the user may not observe peak graphics frequency for a given workload or benchmark.
- Thermal solutions and platform cooling that are designed to less than thermal design guidance may experience thermal and performance issues.

Note: Intel Turbo Boost Technology 2.0 availability may vary between the different SKUs.

5.1.2 Intel® Turbo Boost Technology 2.0 Power Monitoring

When operating in turbo mode, the processor monitors its own power and adjusts the processor and graphics frequencies to maintain the average power within limits over a thermally significant time period. The processor estimates the package power for all components on package. In the event that a workload causes the temperature to exceed program temperature limits, the processor will protect itself using the Adaptive Thermal Monitor.

5.1.3 Intel® Turbo Boost Technology 2.0 Power Control

Illustration of Intel® Turbo Boost Technology 2.0 power control is shown in the following sections and figures. Multiple controls operate simultaneously allowing customization for multiple system thermal and power limitations. These controls allow for turbo optimizations within system constraints and are accessible using MSR, MMIO, or PECI interfaces.

5.1.3.1 Package Power Control

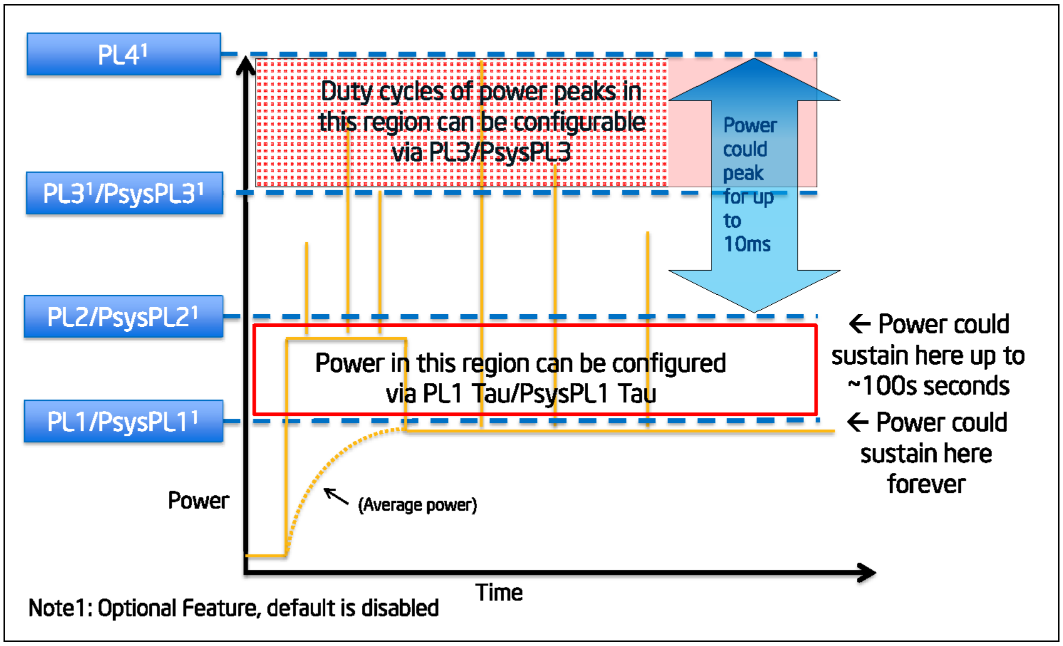
The package power control settings of PL1, PL2, PL3, PL4 and Tau allow the designer to configure Intel Turbo Boost Technology 2.0 to match the platform power delivery and package thermal solution limitations.

- Power Limit 1 (PL1): A threshold for average power that will not exceed - recommend to set to equal TDP power. PL1 should not be set higher than thermal solution cooling limits.
- Power Limit 2 (PL2): A threshold that if exceeded, the PL2 rapid power limiting algorithms will attempt to limit the spike above PL2.
- Power Limit 3 (PL3): A threshold that if exceeded, the PL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PL3 by reactively limiting frequency. This is an optional setting
- Power Limit 4 (PL4): A limit that will not be exceeded, the PL4 power limiting algorithms will preemptively limit frequency to prevent spikes above PL4.
- Turbo Time Parameter (Tau): An averaging constant used for PL1 exponential weighted moving average (EWMA) power calculation.

Note: Implementation of Intel Turbo Boost Technology 2.0 only requires configuring PL1, PL1 Tau, and PL2.

Note: PL3 and PL4 are disabled by default.

Figure 5-1. Package Power Control



5.1.3.2 Platform Power Control

The processor supports Psys (Platform Power) to enhance processor power management. The Psys signal needs to be sourced from a compatible charger circuit and routed to the IMVP8 (voltage regulator). This signal will provide the total thermally relevant platform power consumption (processor and rest of platform) via SVID to the processor.

When the Psys signal is properly implemented, the system designer can utilize the package power control settings of PsysPL1/Tau, PsysPL2 and PsysPL3 for additional manageability to match the platform power delivery and platform thermal solution limitations for Intel Turbo Boost Technology 2.0. The operation of the PsysPL1/tau, PsysPL2 and PsysPL3 is analogous to the processor power limits described in Section 5.1.3.1.

- Platform Power Limit 1 (PsysPL1): A threshold for average platform power that will not be exceeded - recommend to set to equal platform thermal capability.
- Platform Power Limit 2 (PsysPL2): A threshold that if exceeded, the PsysPL2 rapid power limiting algorithms will attempt to limit the spikes above PsysPL2.
- Platform Power Limit 3 (PsysPL3): A threshold that if exceeded, the PsysPL3 rapid power limiting algorithms will attempt to limit the duty cycle of spikes above PsysPL3 by reactively limiting frequency.
- PsysPL1 Tau: An averaging constant used for PsysPL1 exponential weighted moving average (EWMA) power calculation.

- The Psys signal and associated power limits / Tau are optional for the system designer and disabled by default.
- The Psys data will not include power consumption for charging.

5.1.3.3 Turbo Time Parameter (Tau)

Turbo Time Parameter (Tau) is a mathematical parameter (units of seconds) that controls the Intel Turbo Boost Technology 2.0 algorithm. During a maximum power turbo event, the processor could sustain PL2 for a duration longer than the Turbo Time Parameter. If the power value and/or Turbo Time Parameter is changed during runtime, it may take some time based on the new Turbo Time Parameter level for the algorithm to settle at the new control limits. The time varies depending on the magnitude of the change, power limits, and other factors. There is an individual Turbo Time Parameter associated with Package Power Control and Platform Power Control.

5.1.4 Configurable TDP (cTDP) and Low-Power Mode

Configurable TDP (cTDP) and Low-Power Mode (LPM) form a design option where the processor's behavior and package TDP are dynamically adjusted to a desired system performance and power envelope. Configurable TDP and Low-Power Mode technologies offer opportunities to differentiate system design while running active workloads on select processor SKUs through scalability, configuration and adaptability. The scenarios or methods by which each technology is used are customizable but typically involve changes to PL1 and associated frequencies for the scenario with a resultant change in performance depending on system's usage. Either technology can be triggered by (but are not limited to) changes in OS power policies or hardware events such as docking a system, flipping a switch or pressing a button. cTDP and LPM are designed to be configured dynamically and do not require an operating system reboot.

Note: Configurable TDP and Low-Power Mode technologies are not battery life improvement technologies.

5.1.4.1 Configurable TDP

Note: Configurable TDP availability may vary between the different SKUs.

With cTDP, the processor is now capable of altering the maximum sustained power with an alternate processor IA core base frequency. Configurable TDP allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. Configurable TDP can be enabled using Intel's DPTF driver or through HW/EC firmware. Enabling cTDP using the DPTF driver is recommended as Intel does not provide specific application or EC source code.

cTDP consists of three modes as shown in the following table.

Table 5-1. Configurable TDP Modes (Sheet 1 of 2)

Mode	Description
Base	The average power dissipation and junction temperature operating condition limit, specified in Table 5-2 for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.

Table 5-1. Configurable TDP Modes (Sheet 2 of 2)

Mode	Description
TDP-Up	The SKU-specific processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Up configuration in Table 5-2. The Configurable TDP-Up Frequency and corresponding TDP is higher than the processor IA core Base Frequency and SKU Segment Base TDP.
TDP-Down	The processor IA core frequency where manufacturing confirms logical functionality within the set of operating condition limits specified for the SKU segment and Configurable TDP-Down configuration in Table 5-2. The Configurable TDP-Down Frequency and corresponding TDP is lower than the processor IA core Base Frequency and SKU Segment Base TDP.

In each mode, the Intel Turbo Boost Technology 2.0 power limits are reprogrammed along with a new OS controlled frequency range. The DPTF driver assists in all these operations. The cTDP mode does not change the max per-processor IA core turbo frequency.

5.1.4.2 Low-Power Mode

Low-Power Mode (LPM) can provide cooler and quieter system operation. By combining several active power limiting techniques, the processor can consume less power while running at equivalent low frequencies. Active power is defined as processor power consumed while a workload is running and does not refer to the power consumed during idle modes of operation. LPM is only available using the Intel DPTF driver.

Through the DPTF driver, LPM can be configured to use each of the following methods to reduce active power:

- Restricting package power control limits and Intel Turbo Boost Technology availability Off-Lining processor IA core activity (Move processor traffic to a subset of cores)
- Placing a processor IA Core at LFM or LSF (Lowest Supported Frequency) Utilizing IA clock modulation.

LPM power as listed in the TDP Specifications table is defined at point which processor IA core working at LSF, GT = RPn and 1 IA core active.

Off-lining processor IA core activity is the ability to dynamically scale a workload to a limited subset of cores in conjunction with a lower turbo power limit. It is one of the main vectors available to reduce active power. However, not all processor activity is ensured to be able to shift to a subset of cores. Shifting a workload to a limited subset of cores allows other processor IA cores to remain idle and save power. Therefore, when LPM is enabled, less power is consumed at equivalent frequencies.

Minimum Frequency Mode MFM of operation, which is the lowest supported frequency (LSF) at the LFM voltage, has been made available for use under LPM for further reduction in active power beyond LFM capability to enable cooler and quieter modes of operation.

5.1.5 Thermal Management Features

Occasionally the processor may operate in conditions that are near to its maximum operating temperature. This can be due to internal overheating or overheating within the platform. In order to protect the processor and the platform from thermal failure, several thermal management features exist to reduce package power consumption and thereby temperature in order to remain within normal operating limits. Furthermore, the processor supports several methods to reduce memory power.

5.1.5.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor IA core power consumption and temperature until it operates below its maximum operating temperature. Processor IA core power reduction is achieved by:

- Adjusting the operating frequency (using the processor IA core ratio multiplier) and voltage.
- Modulating (starting and stopping) the internal processor IA core clocks (duty cycle).

The Adaptive Thermal Monitor can be activated when the package temperature, monitored by any digital thermal sensor (DTS), meets its maximum operating temperature. The maximum operating temperature implies maximum junction temperature Tj_{MAX}.

Reaching the maximum operating temperature activates the Thermal Control Circuit (TCC). When activated the TCC causes both the processor IA core and graphics core to reduce frequency and voltage adaptively. The Adaptive Thermal Monitor will remain active as long as the package temperature remains at its specified limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the package frequency and voltage until the TCC is de-activated.

Tj_{MAX} is factory calibrated and is not user configurable. The default value is software visible in the TEMPERATURE_TARGET (0x1A2) MSR, bits [23:16].

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. It is not intended as a mechanism to maintain processor thermal control to PL1 = TDP. The system design should provide a thermal solution that can maintain normal operation when PL1 = TDP within the intended usage range.

Adaptive Thermal Monitor protection is always enabled.

5.1.5.1.1 TCC Activation Offset

TCC Activation Offset can be set as an offset from the maximum allowed component temperature to lower the onset of TCC and Adaptive Thermal Monitor. In addition, the processor has added an optional time window (Tau) to manage processor performance at the TCC Activation offset value via an EWMA (Exponential Weighted Moving Average) of temperature.

TCC Activation Offset with Tau=0

An offset (degrees Celsius) can be written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], the offset value will be subtracted from the value found in bits [23:16]. When the time window (Tau) is set to zero, there will be no averaging. The offset will be subtracted from the Tj_{MAX} value and used as a new max temperature set point for Adaptive Thermal Monitoring. This will have the same behavior as in prior products to have TCC activation and Adaptive Thermal Monitor to occur at this lower target silicon temperature.

If enabled, the offset should be set lower than any other passive protection such as ACPI _PSV trip points

TCC Activation Offset with Tau

To manage the processor with the EWMA (Exponential Weighted Moving Average) of temperature, an offset (degrees Celsius) is written to the TEMPERATURE_TARGET (0x1A2) MSR, bits [29:24], and the time window (Tau) is written to the TEMPERATURE_TARGET (0x1A2) MSR [6:0]. The Offset value will be subtracted from the value found in bits [23:16] and be the temperature.

The processor will manage to this average temperature by adjusting the frequency of the various domains. The instantaneous Tj can briefly exceed the average temperature. The magnitude and duration of the overshoot is managed by the time window value (Tau).

This averaged temperature thermal management mechanism is in addition, and not instead of Tj_{MAX} thermal management. That is, whether the TCC activation offset is 0 or not, TCC Activation will occur at Tj_{MAX}.

5.1.5.1.2 Frequency / Voltage Control

Upon Adaptive Thermal Monitor activation, the processor attempts to dynamically reduce processor temperature by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor IA core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor IA core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the processor IA core bus ratio and number of processor IA cores in deep C-states.
- The processor IA core power and temperature are reduced while minimizing performance degradation.

Once the temperature has dropped below the trigger temperature, the operating frequency and voltage will transition back to the normal system operating point.

Once a target frequency/bus ratio is resolved, the processor IA core will transition to the new target automatically.

- On an upward operating point transition the voltage transition precedes the frequency transition.
- On a downward transition the frequency transition precedes the voltage transition.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor IA core optimized target frequency, the P-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor IA core optimized target frequency, the processor will transition to the P-state operating point.

5.1.5.1.3 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 25% on and 75% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the Adaptive Thermal Monitor is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the Adaptive Thermal Monitor goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the Adaptive Thermal Monitor activation when the frequency/voltage targets are at their minimum settings. Processor performance will be decreased when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the Adaptive Thermal Monitor is active.

Clock modulation will not be activated by the Package average temperature control mechanism.

5.1.5.2 Digital Thermal Sensor

Each processor has multiple on-die Digital Thermal Sensor (DTS) that detects the processor IA, GT and other areas of interest instantaneous temperature.

Temperature values from the DTS can be retrieved through:

- A software interface using processor Model Specific Register (MSR).
- A processor hardware interface as described in Platform Environmental Control Interface (PECI).

When temperature is retrieved by the processor MSR, it is the instantaneous temperature of the given DTS. When temperature is retrieved using PECI, it is the average of the highest DTS temperature in the package over a 256 ms time window. Intel recommends using the PECI reported temperature for platform thermal control that benefits from averaging, such as fan speed control. The average DTS temperature may not be a good indicator of package Adaptive Thermal Monitor activation or rapid increases in temperature that triggers the Out of Specification status bit within the PACKAGE_THERM_STATUS MSR 1B1h and IA32_THERM_STATUS MSR 19Ch.

Code execution is halted in C1 or deeper C- states. Package temperature can still be monitored through PECI in lower C-states.

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (Tj_{MAX}), regardless of TCC activation offset. It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in the TEMPERATURE_TARGET MSR 1A2h. The temperature returned by the DTS is an implied negative integer indicating the relative offset from Tj_{MAX}. The DTS does not report temperatures greater than Tj_{MAX}. The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a package DTS indicates that it has reached the TCC activation (a reading of 0x0, except when the TCC activation offset is changed), the TCC will activate and indicate an Adaptive Thermal Monitor event. A TCC activation will lower both processor IA core and graphics core frequency, voltage, or both. Changes to the temperature can be detected using two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts using the processor IA core's local APIC.

5.1.5.2.1 Digital Thermal Sensor Accuracy (Taccuracy)

The error associated with DTS measurements will not exceed ±5 °C within the entire operating range.

5.1.5.2.2 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability before the DTS reading reaches Tj_{MAX}.

5.1.5.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted by the processor when the TCC is active. Only a single PROCHOT# pin exists at a package level. When any DTS temperature reaches the TCC activation temperature, the PROCHOT# signal will be asserted. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

5.1.5.4 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is set to input only. When configured as an input or bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The processor package will remain at the lowest supported P-state until the system de-asserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and de-assertion of the PROCHOT# signal.

When PROCHOT# is configured as a bi-directional signal and PROCHOT# is asserted by the processor, it is impossible for the processor to detect a system assertion of PROCHOT#. The system assertion will have to wait until the processor de-asserts PROCHOT# before PROCHOT# action can occur due to the system assertion. While the processor is hot and asserting PROCHOT#, the power is reduced but the reduction rate is slower than the system PROCHOT# response of < 100 us. The processor thermal control is staged in smaller increments over many milliseconds. This may cause several milliseconds of delay to a system assertion of PROCHOT# while the output function is asserted.

5.1.5.5 Voltage Regulator Protection using PROCHOT#

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and assert PROCHOT# and, if enabled, activate the TCC when the temperature limit of the VR is reached. When PROCHOT# is configured as a bi-directional or input only signal, if the system assertion of PROCHOT# is recognized by the processor, it will result in an immediate transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.1.5.6 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss.
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor.
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations).

5.1.5.7 Low-Power States and PROCHOT# Behavior

Depending on package power levels during package C-states, outbound PROCHOT# may de-assert while the processor is idle as power is removed from the signal. Upon wake up, if the processor is still hot, the PROCHOT# will re-assert. Although, typically package idle state residency should resolve any thermal issues. The PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor IA core and package thermals even during idle states by regularly polling for thermal data over PECI.

5.1.5.8 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the package will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the product. At this point, the THERMTRIP# signal will go active.

5.1.5.9 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the package temperature. This feature is intended for graceful shutdown before the THERMTRIP# is activated. However, the processor execution is not guaranteed between critical temperature and THERMTRIP#. If the Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the PACKAGE_THERM_STATUS MSR 1B1h and the condition also generates a thermal interrupt, if enabled. For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer’s Manual*.

5.1.5.10 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption using clock modulation. This mechanism is referred to as “On-Demand” mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. The processor platforms should not rely on software usage of this mechanism to limit the processor temperature. On-Demand

Mode can be accomplished using processor MSR or chipset I/O emulation. On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode.

5.1.5.11 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to 1, the processor will immediately reduce its power consumption using modulation of the internal processor IA core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable using bits [3:1] of the same IA32_CLOCK_MODULATION MSR. In this mode, the duty cycle can be programmed in either 12.5% or 6.25% increments (discoverable using CPUID). Thermal throttling using this method will modulate each processor IA core's clock independently.

5.1.5.12 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor IA cores simultaneously.

5.1.6 Intel® Memory Thermal Management

The processor provides thermal protection for system memory by throttling memory traffic when using either DIMM modules or a memory down implementation. Two levels of throttling are supported by the processor, either a warm threshold or hot threshold that is customizable through memory mapped I/O registers. Throttling based on the warm threshold should be an intermediate level of throttling. Throttling based on the hot threshold should be the most severe. The amount of throttling is dynamically controlled by the processor.

Memory temperature can be acquired through an on-board thermal sensor (TS-on-Board), retrieved by an embedded controller and reports to the processor through the PECI 3.1 interface. This methodology is known as PECI injected temperatures, this is a method of Closed Loop Thermal Management (CLTM). CLTM requires the use of a physical thermal sensor. EXTTS# is another method of CLTM but it is only capable of reporting memory thermal status to the processor. EXTTS# consists of two GPIO pins on the PCH, where the state of the pins is communicated internally to the processor.

When a physical thermal sensor is not available to report temperature, the processor supports Open Loop Thermal Management (OLTM) that estimates the power consumed per rank of the memory using the processor's DRAM power meter. A per rank power is associated with the warm and hot thresholds that, when exceeded, may trigger memory thermal throttling.

5.2 All-Processor Line Thermal and Power Specifications

The following notes apply only to Table 5-2, Table 5-3 and Table 5-4.

Note	Definition
1	The TDP and Configurable TDP values are the average power dissipation in junction temperature operating condition limit, for the SKU Segment and Configuration, for which the processor is validated during manufacturing when executing an associated Intel-specified high-complexity workload at the processor IA core frequency corresponding to the configuration and SKU.
2	TDP workload may consist of a combination of processor IA core intensive and graphics core intensive applications.
3	Can be modified at runtime by MSR writes, with MMIO and with PECI commands.
4	'Turbo Time Parameter' is a mathematical parameter (units of seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds. refer to Section 5.1.3.2 for further information.
5	Shown limit is a time averaged power, based upon the Turbo Time Parameter. Absolute product power may exceed the set limits for short durations or under virus or uncharacterized workloads.
6	Processor will be controlled to specified power limit as described in Section 5.1.2. If the power value and/or 'Turbo Time Parameter' is changed during runtime, it may take a short period of time (approximately 3 to 5 times the 'Turbo Time Parameter') for the algorithm to settle at the new control limits.
7	This is a hardware default setting and not a behavioral characteristic of the part. The reference BIOS code may override the hardware default power limit values to optimize performance
8	For controllable turbo workloads, the PL2 limit may be exceeded for up to 10 ms.
9	Refer to Table 5-1 for the definitions of 'base', 'TDP-Up' and 'TDP-Down'.
10	LPM power level is an opportunistic power and is not a guaranteed value as usages and implementations may vary.
11	Power limits may vary depending on if the product supports the 'TDP-up' and/or 'TDP-down' modes. Default power limits can be found in the PKG_PWR_SKU MSR (614h).
12	N/A
13	cTDP down power is based on GT2 equivalent graphics configuration. cTDP down does not decrease the number of active Processor Graphics EUs, but relies on Power Budget Management (PL1) to achieve the specified power level.
14	May vary based on SKU, Not all SKUs have cTDP up/down, each SKU has a different base Frequency and cTDP frequency respective.
15	Sustained residencies at high voltages and temperatures may temporarily limit turbo frequency.

Note: The ~ sign stands for approximation.

5.3 S-Processor Line Thermal and Power Specifications

Table 5-2. TDP Specifications (S-Processor Line)

Segment and Package	Processor IA Cores, Graphics Configuration and TDP	Configuration	Processor IA Core Frequency	Graphics core Frequency	Thermal Design Power (TDP) [w]	Notes
S-Processor Line LGA	Hexa Core GT2 95W	Base	3.2 GHz to 3.7 GHz	1.0 GHz to 1.2 GHz	95	1,9,10, 11,12, 15
		LPM	0.8 GHz	0.35 GHz	N/A	
	Quad Core GT2 95W	Base	4.0 GHz	1.15 GHz	95	1,9,10, 11,12, 15
		LPM	0.8 GHz	0.35 GHz	N/A	
	Hexa Core GT2 65W	Base	2.8 GHz to 3.3 GHz	1.0 GHz to 1.2 GHz	65	1,9,10, 11,12, 15
		LPM	0.8 GHz	0.35 GHz	N/A	
	Quad Core GT2 65W	Base	3.6 GHz	1.1 GHz	65	1,9,10, 11,12, 15
		LPM	0.8 GHz	0.35 GHz	N/A	

Table 5-3. Low Power and TTV Specifications (S-Processor Line)

Processor IA Cores, Graphics Configuration and TDP	PCG[7]	Max Power Package C7 (W) [1,4,5]	Max Power Package C8 (W) [1,4,5]	TTV TDP (W) [6,7]	Min T_{CASE} (°C)	Max TTV T_{CASE} (°C)
Hexa Core GT2 95W	2015D	N/A	N/A	95	0	64.5
Hexa Core GT2 65W	2015C	N/A	N/A	65	0	71.4
Quad Core GT2 62W	2015C	N/A	N/A	62	0	69.9

Notes:

1. The package C-state power is the worst case power in the system configured as follows:
   a. Memory configured for DDR4 2400 and populated with two DIMMs per channel.
   b. DMI and PCIe links are at L1
2. Specification at DTS = 50 °C and minimum voltage loadline.
3. Specification at DTS = 35 °C and minimum voltage loadline.
4. These DTS values in Notes 2 - 3 are based on the TCC Activation MSR having a value of 100, see Section 5.1.5, "Thermal Management Features".
5. These values are specified at VCC_MAX and VNOM for all other voltage rails for all processor frequencies. Systems should be designed to ensure the processor is not to be subjected to any static VCC and ICC combination wherein VCCP exceeds VCCP_MAX at specified ICCP. See the loadline specifications.
6. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at DTS = -1.TDP is achieved with the Memory configured for DDR4 2400 and 2 DIMMs per channel.
7. Platform Compatibility Guide (PCG) (previously known as FMB) provides a design target for meeting all planned processor frequency requirements.
8. Not 100% tested. Specified by design characterization.

Table 5-4. $T_{CONTROL}$ Offset Configuration (S-Processor Line - Client) (Sheet 1 of 2)

Segment	Hexa Core GT2			Quad Core GT2	
TDP [W]	95	65	35	62	35
TEMP_TARGET ($T_{CONTROL}$) [ºC]	18	18	6	20	7

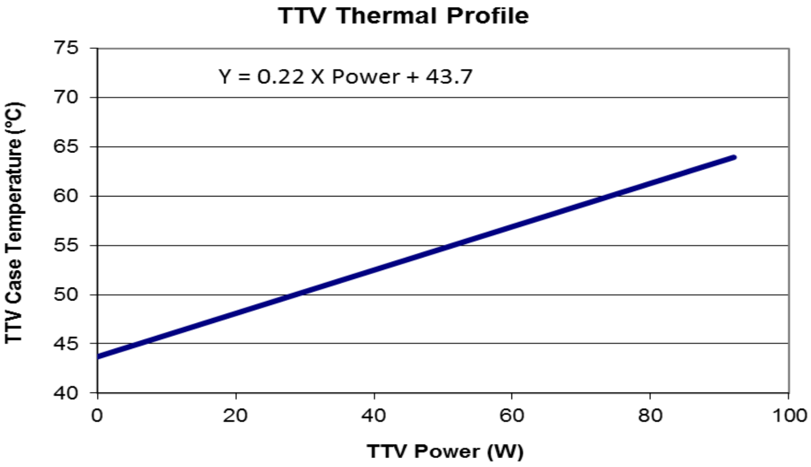
Table 5-4. $T_{CONTROL}$ Offset Configuration (S-Processor Line - Client) (Sheet 2 of 2)

Segment	Hexa Core GT2	Quad Core GT2

Notes:
1. Digital Thermal Sensor (DTS) based fan speed control is recommended to achieve optimal thermal performance.
2. Intel recommends full cooling capability at approximately the DTS value of -1, to minimize TCC activation risk.
3. For example, if $T_{CONTROL}$ = 20 ºC, Fan acceleration operation will start at 80 ºC (100 ºC - 20 ºC).

5.3.1 Thermal Profile for PCG 2015D Processor

Figure 5-2. Thermal Test Vehicle Thermal Profile for PCG 2015D Processor



Notes:
1. Refer to Table 5-5 for discrete points that constitute the thermal profile.

Table 5-5. Thermal Test Vehicle Thermal Profile for PCG 2015D Processor (Sheet 1 of 2)

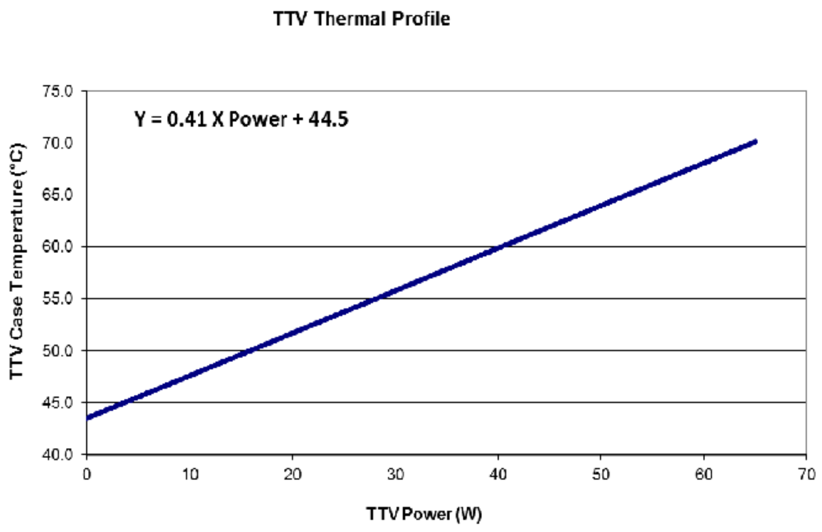
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	43.7	46	53.8
2	44.1	48	54.3
4	44.6	50	54.7
6	45.0	52	55.1
8	45.6	54	55.6
10	45.9	56	56.0
12	46.3	58	56.5
14	46.8	60	56.9
16	47.2	62	57.3
18	47.7	64	57.8
20	48.1	66	58.2
22	48.5	68	58.7
24	49.0	70	59.1
26	49.4	72	59.5
28	49.9	74	60.0
30	50.3	76	60.4

Table 5-5. Thermal Test Vehicle Thermal Profile for PCG 2015D Processor (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
32	50.7	78	60.9
34	51.2	80	61.3
36	51.6	82	61.7
38	52.1	84	62.2
40	52.5	86	62.6
42	52.9	88	63.1
44	53.4	90	63.5
46	53.8	92	63.9

5.3.2 Thermal Profile for PCG 2015C Processor

Figure 5-3. Thermal Test Vehicle Thermal Profile for PCG 2015C Processor



Notes:
1. Refer to Table 5-6 for discrete points that constitute the thermal profile.

Table 5-6. Thermal Test Vehicle Thermal Profile for PCG 2015C Processor (Sheet 1 of 2)

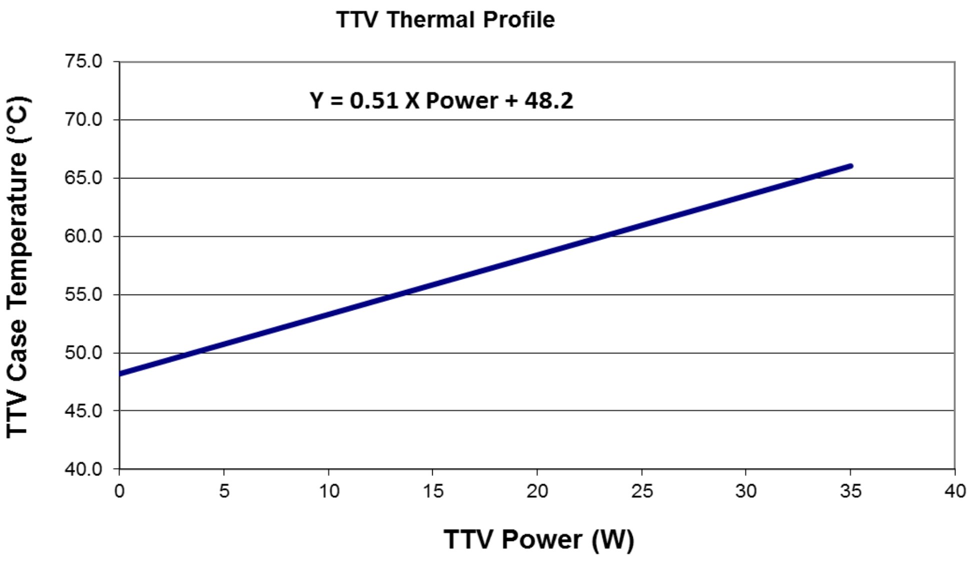
Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	44.5	34	57.4
2	44.3	36	58.3
4	45.1	38	59.1
6	46.0	40	59.9
8	46.8	42	60.7
10	47.6	44	61.5
12	48.4	46	62.4
14	49.2	48	63.2
16	50.1	50	64.0
18	50.9	52	64.8

Table 5-6. Thermal Test Vehicle Thermal Profile for PCG 2015C Processor (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
20	51.7	53	65.2
22	52.5	54	65.6
24	53.3	56	66.5
26	54.2	58	67.3
28	55.0	60	68.1
30	55.8	62	68.9
32	56.6	64	69.7
34	57.4	65	70.2

5.3.3 Thermal Profile for PCG 2015B Processor

Figure 5-4. Thermal Test Vehicle Thermal Profile for PCG 2015B Processor



Notes:
1. Refer to Table 5-7 for discrete points that constitute the thermal profile.

Table 5-7. Thermal Test Vehicle Thermal Profile for PCG 2015B Processor (Sheet 1 of 2)

Power (W)	T_{CASE_MAX} (°C)	Power (W)	T_{CASE_MAX} (°C)
0	48.2	20	58.4
2	49.2	22	59.4
4	50.2	24	60.4
6	51.3	26	61.5
8	52.3	28	62.5
10	53.3	30	63.5
12	54.3	32	64.5

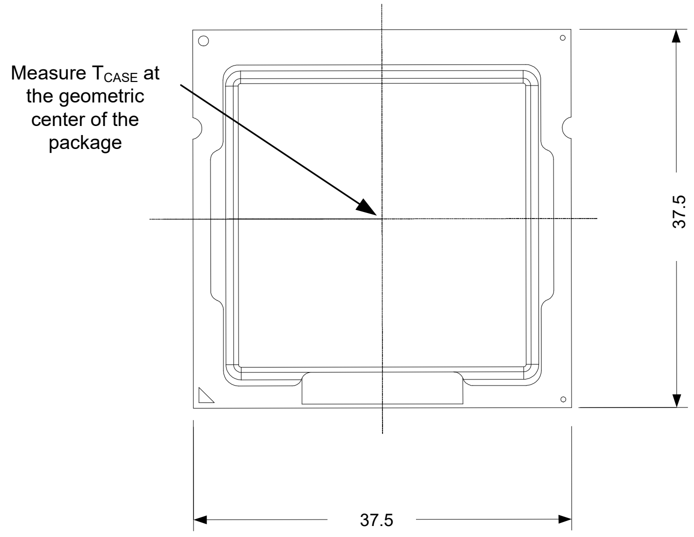
Table 5-7. Thermal Test Vehicle Thermal Profile for PCG 2015B Processor (Sheet 2 of 2)

Power (W)	T_{CASE_MAX} (°C)
14	55.3
16	56.4
18	57.4
34	65.5
35	66.1

5.3.4 Thermal Metrology

The maximum TTV case temperatures ($T_{CASE-MAX}$) can be derived from the data in the appropriate TTV thermal profile earlier in this chapter. The TTV T_{CASE} is measured at the geometric top center of the TTV integrated heat spreader (IHS). Figure 5-5 illustrates the location where T_{CASE} temperature measurements should be made.

Figure 5-5. Thermal Test Vehicle (TTV) Case Temperature (T_{CASE}) Measurement Location



The following supplier can machine the groove and attach a thermocouple to the IHS. The following supplier is listed as a convenience to Intel's general customers and may be subject to change without notice. THERM-X OF CALIFORNIA, 3200 Investment Blvd, Hayward, Ca 94544. George Landis +1-510-441-7566 Ext. 368 george@therm-x.com. The vendor part number is XTMS1565.

5.3.5 Fan Speed Control Scheme with Digital Thermal Sensor (DTS) 1.1

To correctly use DTS 1.1, the designer must first select a worst case scenario $T_{AMBIENT}$, and ensure that the Fan Speed Control (FSC) can provide a Ψ_{CA} that is equivalent or greater than the Ψ_{CA} specification.

The DTS 1.1 implementation consists of two points: a Ψ_{CA} at $T_{CONTROL}$ and a Ψ_{CA} at DTS = -1.

The Ψ_{CA} point at DTS = -1 defines the minimum Ψ_{CA} required at TDP considering the worst case system design $T_{AMBIENT}$ design point:

$$\Psi_{CA} = (T_{CASE-MAX} - T_{AMBIENT-TARGET}) / TDP$$

For example, for a 91 W TDP part, the T_{CASE} maximum is 63.7 °C and at a worst case design point of 40 °C local ambient this will result in:

$$\Psi_{CA} = (63.7 - 40) / 91 = 0.26\ °C/W$$

Similarly for a system with a design target of 45 °C ambient, the Ψ_{CA} at DTS = -1 needed will be 0.21 °C/W.

The second point defines the thermal solution performance (Ψ_{CA}) at $T_{CONTROL}$. The following table lists the required Ψ_{CA} for the various TDP processors.

These two points define the operational limits for the processor for DTS 1.1 implementation. At $T_{CONTROL}$ the fan speed must be programmed such that the resulting Ψ_{CA} is better than or equivalent to the required Ψ_{CA} listed in the following table. Similarly, the fan speed should be set at DTS = -1 such that the thermal solution performance is better than or equivalent to the ΨCA requirements at $T_{AMBIENT\text{-}MAX}$.

The fan speed controller must linearly ramp the fan speed from processor DTS = $T_{CONTROL}$ to processor DTS = -1.

Figure 5-6. Digital Thermal Sensor (DTS) 1.1 Definition Points

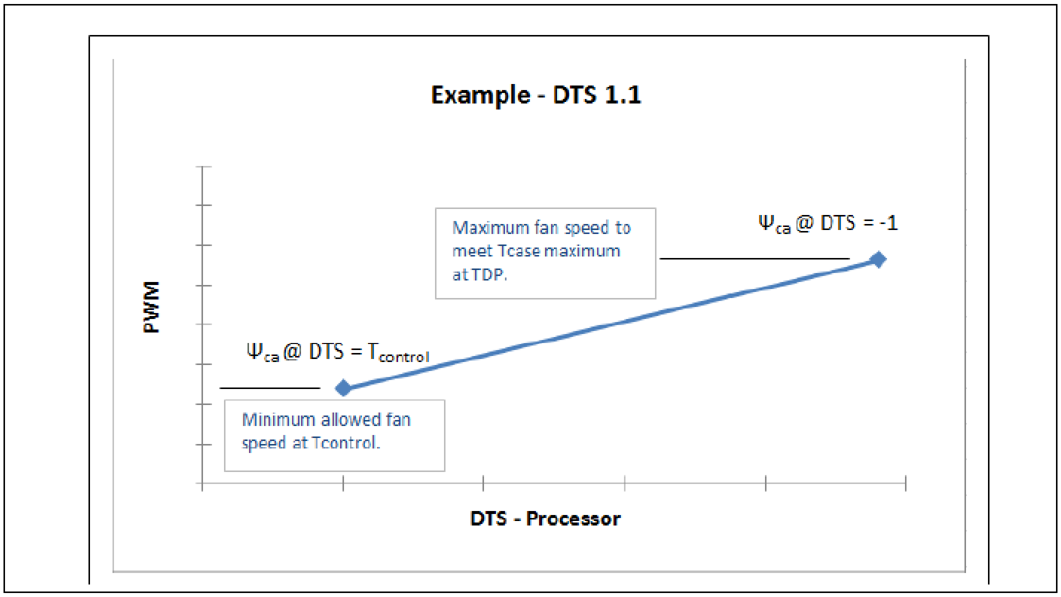


Table 5-8. Digital Thermal Sensor (DTS) 1.1 Thermal Solution Performance Above $T_{CONTROL}$

Processor		Ψ_{CA} at DTS = $T_{CONTROL}$ [1, 2] At System $T_{AMBIENT\_MAX}$ = 30 °C	Ψ_{CA} at DTS = -1 At System $T_{AMBIENT\_MAX}$ = 40 °C	Ψ_{CA} at DTS = -1 At System $T_{AMBIENT\_MAX}$ = 45 °C	Ψ_{CA} at DTS = -1 At System $T_{AMBIENT\_MAX}$ = 50 °C
Hexa Core GT2	95W	0.44	0.247	0.195	0.142
Hexa Core GT2	65W	0.763	0.477	0.4	0.323
Quad Core GT2	62W	0.775	0.49	0.41	0.329

Notes:

1. Ψ_{CA} at "DTS = $T_{CONTROL}$" is applicable to systems that have an internal T_{RISE} (T_{ROOM} temperature to Processor cooling fan inlet) of less than 10 °C. In case the expected T_{RISE} is greater than 10 °C, a correction factor should be used as explained below. For each 1 °C T_{RISE} above 10 °C, the correction factor (CF) is defined as CF = 1.7 / (processor TDP)
2. Example: A chassis T_{RISE} assumption is 12 °C for a 91 W TDP processor: CF = 1.7 / 91 W = 0.019 /W For T_{RISE} > 10 °C Ψ_{CA} at $T_{CONTROL}$ = (Value provide in Column 2) – (T_{RISE} – 10) * CF Ψ_{CA} = 0.45 – (12 – 10) 0.019 = 0.41 °C/W In this case, the fan speed should be set slightly higher, equivalent to Ψ_{CA} = 0.41 °C/W

5.3.6 Fan Speed Control Scheme with Digital Thermal Sensor (DTS) 2.0

To simplify processor thermal specification compliance, the processor calculates the DTS Thermal Profile from $T_{CONTROL}$ Offset, TCC Activation Temperature, TDP, and the Thermal Margin Slope provided in the following table.

Note: TCC Activation Offset is 0 for the processors.

Using the DTS Thermal Profile, the processor can calculate and report the Thermal Margin, where a value less than 0 indicates that the processor needs additional cooling, and a value greater than 0 indicates that the processor is sufficiently cooled.

Figure 5-7. Digital Thermal Sensor (DTS) 2.0 Definition Points

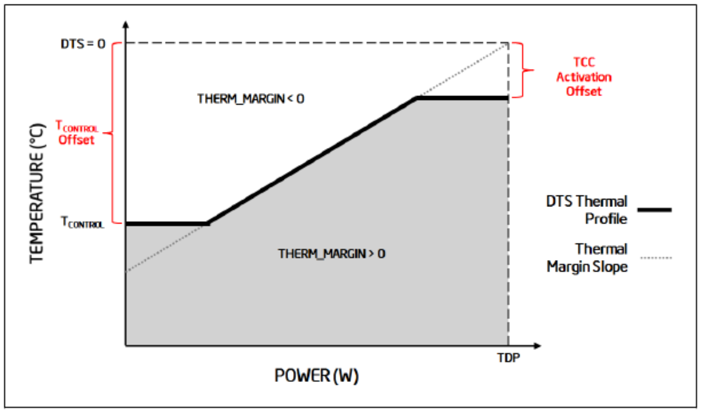


Table 5-9. Thermal Margin Slope

PCG	Die Configuration (Cores/GT)	TDP [W]	TCC Activation [°C]	Temperature Control Offset	Thermal Margin Slope [°C/W]
2015D	Hexa Core GT2	95	100	18	0.516
2015C	Hexa Core GT2	65	100	18	0.713
	Quad Core GT2	62	100	20	0.889

§ §

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The notations in the following table are used to describe the signal type.

The signal description also includes the type of buffer used for the particular signal (see the following table).

Table 6-1. Signal Tables Terminology

Notation	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin
SE	Single Ended Link
Diff	Differential Link
CMOS	CMOS buffers. 1.05V- tolerant
OD	Open Drain buffer
DDR4	DDR4 buffers: 1.2V-tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Availability	Signal Availability condition - based on segment, SKU, platform type or any other factor
Asynchronous [1]	Signal has no timing relationship with any reference clock.
Note: 1. Qualifier for a buffer type.	

6.1 System Memory Interface

Table 6-2. DDR4 Memory Interface (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_DQ[63:0] DDR1_DQ[63:0]	**Data Buses:** Data signals interface to the SDRAM data buses.	I/O	DDR4	SE	All Processor Lines
DDR0_DQSP[7:0] DDR0_DQSN[7:0] DDR1_DQSP[7:0] DDR1_DQSN[7:0]	**Data Strobes:** Differential data strobe pairs. The data is captured at the crossing point of DQS during read and write transactions.	I/O	DDR4	Diff	All Processor Lines
DDR0_CKN[3:0] DDR0_CKP[3:0] DDR1_CKN[3:0] DDR1_CKP[3:0]	**SDRAM Differential Clock:** Differential clocks signal pairs, pair per rank. The crossing of the positive edge of DDR0_CKP/DDR1_CKP and the negative edge of their complement DDR0_CKN / DDR1_CKN are used to sample the command and control signals on the SDRAM.	O	DDR4	Diff	[1:0] applicable for All Processor Lines. [3:2] applicable only in S Processor Line

Table 6-2. DDR4 Memory Interface (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR0_CKE[3:0] DDR1_CKE[3:0]	**Clock Enable:** (1 per rank). These signals are used to: • Initialize the SDRAMs during power-up. • Power-down SDRAM ranks. • Place all SDRAM ranks into and out of self-refresh during STR (Suspend to RAM).	O	DDR4	SE	[1:0] applicable for All Processor Lines. [3:2] applicable only in S Processor Line .
DDR0_CS#[3:0] DDR1_CS#[3:0]	**Chip Select:** (1 per rank). These signals are used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O	DDR4	SE	[1:0] applicable for All Processor Lines. [3:2] applicable only in S Processor Line
DDR0_ODT[3:0] DDR1_ODT[3:0]	**On Die Termination:** (1 per rank). Active SDRAM Termination Control.	O	DDR4	SE	[0,1] applicable for All Processor Lines. [3:2] applicable only in S Processor Line
DDR0_MA[16:0] DDR1_MA[16:0]	**Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. • A[16:14] use also as command signals, see ACT# signal description. • A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. HIGH: Autoprecharge; LOW: no Autoprecharge). • A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. • A12 is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. HIGH, no burst chop; LOW: burst chopped).	O	DDR4	SE	All Processor Lines
DDR0_ACT# DDR1_ACT#	**Activation Command:** ACT# HIGH along with CS# determines that the signals addresses below have command functionality. A16 use as RAS# signal A15 use as CAS# signal A14 use as WE# signal	O	DDR4	SE	All Processor Lines
DDR0_BG[1:0] DDR1_BG[1:0]	**Bank Group:** BG[0:1] define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All processor lines SO-DIMM, x8 DRAMs, x16 DDP DRAMs devices use BG[1:0]. x16 SDP DRAMs devices use BG[0]
DDR0_BA[1:0] DDR1_BA[1:0]	**Bank Address:** BA[1:0] define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.	O	DDR4	SE	All Processor Lines
DDR0_ALERT# DDR1_ALERT#	**Alert:** This signal is used at command training only. It is getting the Command and Address Parity error flag during training. CRC feature is not supported.	I	DDR4	SE	All Processor Lines
DDR0_PAR DDR1_PAR	**Command and Address Parity:** These signals are used for parity check.	O	DDR4	SE	All Processor Lines
DDR1_VREF_DQ	**Memory Reference Voltage for DQ:**	O	A	SE	All -Processor Line
DDR_VREF_CA	**Memory Reference Voltage for Command & Address:**	O	A	SE	All Processor Lines

Table 6-3. System Memory Reference and Compensation Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDR_VTT_CNTL	**System Memory Power Gate Control:** When signal is high – platform memory VTT regulator is enable, output high. When signal is low - Disables the platform memory VTT regulator in C8 and deeper and S3.	O	CMOS	SE	All Processor Lines

6.2 PCI Express* Graphics (PEG) Signals

Table 6-4. PCI Express* Interface

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PEG_RCOMP	Resistance Compensation for PCI Express channels PEG and DMI.	N/A	A	SE	S-Processor Line
PEG_RXP[15:0] PEG_RXN[15:0]	PCI Express Receive Differential Pairs.	I	PCI Express*	Diff	
PEG_TXP[15:0] PEG_TXN[15:0]	PCI Express Transmit Differential Pairs.	O	PCI Express*	Diff	

6.3 Direct Media Interface (DMI) Signals

Table 6-5. DMI Interface Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DMI_RXP[3:0] DMI_RXN[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pairs.	I	DMI	Diff	S-Processor Line
DMI_TXP[3:0] DMI_TXN[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pairs.	O	DMI	Diff	

6.4 Reset and Miscellaneous Signals

Table 6-6. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Intel recommends placing test points on the board for CFG pins. • **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]**: Reserved configuration lane. • **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]**: PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for S-Processor Line only and test point may be placed on the board for them.
CFG_RCOMP	**Configuration Resistance Compensation**	N/A	N/A	SE	All Processor Lines
RESET#	Platform Reset pin driven by the PCH.	I	CMOS	SE	S-Processor Line
PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for this processor.			N/A	S-Processor Line
PROC_TRIGIN	Debug pin	I	CMOS	SE	S-Processor Line
PROC_TRIGOUT	Debug pin	O	CMOS	SE	S-Processor Line
PROC_AUDIO_SDI	**Processor Audio Serial Data Input:** This signal is an input to the processor from the PCH.	I	AUD	SE	S-Processor Line
PROC_AUDIO_SDO	**Processor Audio Serial Data Output:** This signal is an output from the processor to the PCH.	O	AUD	SE	
PROC_AUDIO_CLK	**Processor Audio Clock**	I	AUD	SE	

6.5 embedded DisplayPort* (eDP*) Signals

Table 6-7. embedded DisplayPort* Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
eDP_TXP[3:0] eDP_TXN[3:0]	**embedded DisplayPort Transmit:** differential pair	O	eDP	Diff	All Processor Lines
eDP_AUXP eDP_AUXN	**embedded DisplayPort Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair.	O	eDP	Diff	All Processor Lines

Table 6-7. embedded DisplayPort* Signals (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DISP_UTILS	**embedded DisplayPort Utility:** Output control signal used for brightness correction of embedded LCD displays with backlight modulation. This pin will co-exist with functionality similar to existing BKLTCTL pin on PCH	O	Async CMOS	SE	All Processor Lines
DISP_RCOMP	**DDI IO Compensation resistor, supporting DP*, eDP* and HDMI* channels.**	N/A	A	SE	All Processor Lines

Note:
1. When using eDP bifurcation:
   - — x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
   - — x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])

6.6 Display Interface Signals

Table 6-8. Display Interface Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
DDI1_TXP[3:0] DDI1_TXN[3:0] DDI2_TXP[3:0] DDI2_TXN[3:0] DDI3_TXP[3:0] DDI3_TXN[3:0]	**Digital Display Interface Transmit:** Differential Pairs	O	DP/ HDMI*	Diff	All Processor Lines. DDI3_TXP[3:0] DDI3_TXN[3:0] DDI3_AUXP DDI3_AUXN are present in S-Processor Line.
DDI1_AUXP DDI1_AUXN DDI2_AUXP DDI2_AUXN DDI3_AUXP DDI3_AUXN	**Digital Display Interface Display Port Auxiliary:** Half-duplex, bidirectional channel consist of one differential pair for each channel.	O	DP/ HDMI*	Diff	

6.7 Processor Clocking Signals

Table 6-9. Processor Clocking Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		Diff	
PCI_BCLKP PCI_BCLKN	100 MHz Clock for PCI Express* logic	I		Diff	

6.8 Testability Signals

Table 6-10. Testability Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BPM#[3:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O	GTL	SE	All Processor Lines
PROC_PRDY#	**Probe Mode Ready:** PROC_PRDY# is a processor output used by debug tools to determine processor debug readiness.	O	OD	SE	All Processor Lines
PROC_PREQ#	**Probe Mode Request:** PROC_PREQ# is used by debug tools to request debug operation of the processor.	I	GTL	SE	All Processor Lines
PROC_TCK	**Test Clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). This signal should be driven low or allowed to float during power on Reset.	I	GTL	SE	All Processor Lines
PROC_TDI	**Test Data In:** This signal transfers serial test data into the processor. This signal provides the serial input needed for JTAG specification support.	I	GTL	SE	All Processor Lines
PROC_TDO	**Test Data Out:** This signal transfers serial test data out of the processor. This signal provides the serial output needed for JTAG specification support.	O	OD	SE	All Processor Lines
PROC_TMS	**Test Mode Select:** A JTAG specification support signal used by debug tools.	I	GTL	SE	All Processor Lines
PROC_TRST#	**Test Reset:** Resets the Test Access Port (TAP) logic. This signal should be driven low during power on Reset.	I	GTL	SE	All Processor Lines

6.9 Error and Thermal Protection Signals

Table 6-11. Error and Thermal Protection Signals (Sheet 1 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this signal for non-recoverable machine check errors or other unrecoverable internal errors. CATERR# is used for signaling the following types of errors: Legacy MCERRs, CATERR# is asserted for 16 BCLKs. Legacy IERRs, CATERR# remains asserted until warm or cold reset.	O	OD	SE	All Processor Lines
PECI	**Platform Environment Control Interface:** A serial sideband interface to the processor. It is used primarily for thermal, power, and error management.	I/O	PECI, Async	SE	All Processor Lines
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O	GTL I OD O	SE	All Processor Lines

Table 6-11. Error and Thermal Protection Signals (Sheet 2 of 2)

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130 °C. This is signaled to the system by the THERMTRIP# pin.	O	OD	SE	All Processor Lines

6.10 Power Sequencing Signals

Table 6-12. Power Sequencing Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
PROCPWRGD	**Processor Power Good:** The processor requires this input signal to be a clean indication that the V_{CC} and V_{DDQ} power supplies are stable and within specifications. This requirement applies regardless of the S-state of the processor. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	I	CMOS	SE	All Processor Lines
VCCST_PWRGD	**VCCST Power Good:** The processor requires this input signal to be a clean indication that the VCCST and VDDQ power supplies are stable and within specifications. This signal should have a valid level during both S0 and S3 power states. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal should then transition monotonically to a high state.	I	CMOS	SE	All Processor Lines
PROC_DETECT# /SKTOCC#	**Processor Detect / Socket Occupied:** Pulled down directly (0 Ohms) on the processor package to the ground. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	N/A	N/A	SE	All Processor Lines
VIDSOUT VIDSCK VIDALERT#	**VIDSOUT, VIDSCK, VIDALERT#:** These signals comprise a three-signal serial synchronous interface used to transfer power management information between the processor and the voltage regulator controllers.	I/O O I	I:GTL/O:OD OD CMOS	SE	All Processor Lines
PM_SYNC	**Power Management Sync:** A sideband signal to communicate power management status from the PCH to the processor. PCH report EXTTS#/EVENT# status to the processor.	I	CMOS	SE	S-Processor Line
PM_DOWN	**Power Management Down:** Sideband to PCH. Indicates processor wake up event EXTTS# on PCH. The processor combines the pin status into the OLTM/CLTM.	O	CMOS	SE	S-Processor Line

6.11 Processor Power Rails

Table 6-13. Processor Power Rails Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
Vcc	Processor IA cores power rail	I	Power	—	All Processor Lines
Vcc_{GT}	Processor Graphics power rail	I	Power	—	All Processor Lines
V_{DDQ}	System Memory power rail	I	Power	—	All Processor Lines
Vcc_{SA}	Processor System Agent power rail	I	Power	—	All Processor Lines
Vcc_{IO}	Processor I/O power rail. Consists of V_{CCIO} and Vcc_{IO_DDR}. V_{CCIO} and V_{CCIO_DDR} should be isolated from each other.	I	Power	—	All Processor Lines
Vcc_{ST}	Sustain voltage for processor standby modes	I	Power	—	All Processor Lines
Vcc_{PLL}	Processor PLLs power rails	I	Power	—	All Processor Lines
Vcc_{PLL_OC}	Processor PLLs power rails	I	Power	—	All Processor Lines
Vcc_SENSE Vss_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{GT}_SENSE Vss_{GT}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{IO}_SENSE Vss_{IO}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines
Vcc_{SA}_SENSE Vss_{SA}_SENSE	Isolated, low impedance voltage sense pins. They can be used to sense or measure voltage near the silicon.	N/A	Power	—	All Processor Lines

6.12 Ground, Reserved and Non-Critical to Function (NCTF) Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

Arbitrary connection of these signals to VCC, VDDQ, VSS, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Table 6-14.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing and prevent boundary scan testing. A resistor should be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, the resistor can also be used for system testability.

Table 6-14. GND, RSVD, and NCTF Signals

Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF should be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

6.13 Processor Internal Pull-Up / Pull-Down Terminations

Table 6-15. Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up / Pull Down	Vcc_{IO}	16-60 ohms
PREQ#	Pull Up	Vcc_{ST}	3 kohms
PROC_TDI	Pull Up	Vcc_{STG}[1]	3 kohms
PROC_TMS	Pull Up	Vcc_{STG}[1]	3 kohms
PROC_TRSN#	Pull Down	-	3 kohms
CFG[19:0]	Pull Up	Vcc_{IO}	3 kohms

Note:
1. For S-Processor Line, it should be Vcc_{ST}

§ §

7 Electrical Specifications

7.1 Processor Power Rails

Table 7-1. Processor Power Rails

Power Rail	Description	Control	Availability
V_{CC}	Processor IA Cores Power Rail	SVID	All Processor Lines
Vcc_{GT}	Processor Graphics Power Rails	SVID	All Processor Lines
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)	All Processor Lines
Vcc_{IO}	IO Power Rail	Fixed	All Processor Lines
Vcc_{ST}	Sustain Power Rail	Fixed	All Processor Lines
Vcc_{PLL}[5]	Processor PLLs power Rail	Fixed	All Processor Lines
Vcc_{PLL_OC}[3]	Processor PLLs OC power Rail	Fixed	All Processor Lines
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)	All Processor Lines

Notes:
1. N/A
2. N/A
3. Vcc_{PLL_OC} power rail should be sourced from the VDDQ VR. The connection can be direct or through a load switch, depending desired power optimization. In case of direct connection (Vcc_{PLL_OC} is shorted to V_{DDQ}, no load switch), platform should ensure that Vcc_{ST} is ON (high) while Vcc_{PLL_OC} is ON (high).
4. Vcc_{STG} power rail should be sourced from the VR as V_{CCST}. The connection can be direct or through a load switch, depending on desired power optimization.
5. Add 1 MHz LPF to reduce noise on power rail.

7.1.1 Power and Ground Pins

All power pins should be connected to their respective processor power planes, while all VSS pins should be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop.

7.1.2 V_{CC} Voltage Identification (VID)

The processor uses three signals for the **S**erial **V**oltage **ID**entification (SVID) interface to support automatic selection of voltages. The following table specifies the voltage level corresponding to the 8-bit VID value transmitted over serial VID. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator should disable itself. VID signals are CMOS push/pull drivers. See Table 7-14 for the DC specifications for these signals. The VID codes will change due to temperature and/or current load changes in order to minimize the power of the part. A voltage range is provided in Section 7.2. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same processor IA core frequency may have different default VID settings. This is shown in the VID range values in Section 7.2. The processor provides the ability to operate while transitionally to an adjacent VID and its associated voltage. This will represent a DC shift in the loadline.

7.2 DC Specifications

The processor DC specifications in this section are defined at the processor signal pins, unless noted otherwise.

- The DC specifications for the DDR4 signals are listed in the *Voltage and Current Specifications* section.
- The *Voltage and Current Specifications* section lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Read all notes associated with each parameter.
- AC tolerances for all DC rails include dynamic load currents at switching frequencies up to 1 MHz.

7.2.1 Processor Power Rails DC Specifications

7.2.1.1 Vcc DC Specifications

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max			Unit	Note[1]
Operating Voltage	Voltage Range for Processor Operating Modes	All	0	—	1.52			V	1, 2, 3, 7
Icc_{MAX} (S-Processors)	Maximum Processor IA Core I_{CC}	S-Processor Line (65W) - Quad Core GT2	—	—	79			A	4, 6, 7
		S-Processor Line (95W) - Quad Core GT2	—	—	100				
		S-Processor Line (65W) - Hexa Core GT2	—	—	133				
		S-Processor Line (95W) - Hexa Core GT2	—	—	138				
TOB_{VCC}	Voltage Tolerance	PS0, PS1	—	—	±20			mV	3, 6, 8
		PS2, PS3	—	—	±20				
Ripple	Ripple Tolerance				$I_L \le 0.5$	$0.5<I_L<Icc_{TDC}$	$Icc_{TDC}<I_L<Icc_{MAX}$	mV	3, 6, 8
		PS0	—	—	+30/-10	±10	±15		
		PS1	—	—	+30/-10	±15	±15		
		PS2	—	—	+30/-10	+30/-10	+30/-10		
		PS3	—	—	+30/-10	+30/-10	+30/-10		
DC_LL (S-Processors)	Loadline slope within the VR regulation loop capability	S-Processor Line - Hexa Core GT2	—	—	2.1			mΩ	10, 13, 14
		S-Processor Line - Quad Core GT2	—	—	2.1			mΩ	10, 13, 14
AC_LL (S-Processors)	AC Loadline	S-Processor Lines	—	—	Same as Max DC_LL (up to 400 KHz)			mΩ	10, 13, 14
T_OVS_TDP_MAX	Max Overshoot time **TDP/virus mode**	—	—	—	10/30			µs	
V_OVS TDP_MAX/ virus_MAX	Max Overshoot at **TDP/virus mode**	—	—	—	70/200			mV	

Table 7-2. Processor IA core (Vcc) Active and Idle Mode DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]

Notes:

1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID) that is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_SENSE and Vss_SENSE as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. Processor IA core VR to be designed to electrically support this current.
5. Processor IA core VR to be designed to thermally support this current indefinitely.
6. Long term reliability cannot be assured if tolerance, ripple, and core noise parameters are violated.
7. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
8. PSx refers to the voltage regulator power state as set by the SVID protocol.
9. N/A
10. LL measured at sense points.
11. Typ column represents Icc_{MAX} for commercial application it is NOT a specification - it is a characterization of limited samples using limited set of benchmarks that can be exceeded.
12. Operating voltage range in steady state.
13. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
14. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly via the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.

7.2.1.2 Vcc_{GT} DC Specifications

Table 7-3. Processor Graphics (Vcc_{GT}) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Segment</th><th>Min</th><th>Typ</th><th colspan="3">Max</th><th>Unit</th><th>Note[1]</th></tr>
<tr><td>Operating voltage</td><td>Active voltage Range for Vcc_{GT}</td><td>All</td><td>0.55</td><td>—</td><td colspan="3">1.52</td><td>V</td><td>2, 3, 6, 8</td></tr>
<tr><td>Idle voltage</td><td>Processor Graphics core idle voltage</td><td>All</td><td>0</td><td>—</td><td colspan="3">0.55</td><td>V</td><td>3</td></tr>
<tr><td rowspan="4">Icc_{MAX_GT} (S-Processors)</td><td rowspan="4">Max. Current for Processor Graphics Rail</td><td>S-Processor Line (65W) - Quad Core GT2</td><td>—</td><td>—</td><td colspan="3">45</td><td rowspan="4">A</td><td rowspan="4">6</td></tr>
<tr><td>S-Processor Line (95W) - Quad Core GT2</td><td>—</td><td>—</td><td colspan="3">45</td></tr>
<tr><td>S-Processor Line (65W) - Hexa Core GT2</td><td>—</td><td>—</td><td colspan="3">45</td></tr>
<tr><td>S-Processor Line (95W) - Hexa Core GT2</td><td>—</td><td>—</td><td colspan="3">45</td></tr>
<tr><td rowspan="2">TOB_{GT}</td><td rowspan="2">Vcc_{GT} Tolerance</td><td>PS0, PS1</td><td>—</td><td>—</td><td colspan="3">±20</td><td>mV</td><td>3, 4</td></tr>
<tr><td>PS2, PS3</td><td>—</td><td>—</td><td colspan="3">±20</td><td>mV</td><td>3, 4</td></tr>
<tr><td rowspan="5">Ripple</td><td rowspan="5">Ripple Tolerance</td><td colspan="3">—</td><td>$I_L \le 0.5$</td><td>$0.5 < I_L < Icc_{TDC}$</td><td>$Icc_{TDC} < I_L < Icc_{MAX}$</td><td rowspan="5">mV</td><td rowspan="5">3, 4</td></tr>
<tr><td>PS0</td><td>—</td><td>—</td><td>+30/-10</td><td>±10</td><td>±15</td></tr>
<tr><td>PS1</td><td>—</td><td>—</td><td>+30/-10</td><td>±15</td><td>±15</td></tr>
<tr><td>PS2</td><td>—</td><td>—</td><td>+30/-10</td><td>+30/-10</td><td>+30/-10</td></tr>
<tr><td>PS3</td><td>—</td><td>—</td><td>+30/-10</td><td>+30/-10</td><td>+30/-10</td></tr>
</table>

Table 7-3. Processor Graphics (Vcc_{GT}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
DC_LL	Vcc_{GT} Loadline slope	S-Quad Core GT2 S-Hexa Core GT2	— —	— —	3.1 3.1	mΩ	7, 9, 10
AC_LL (S-Processors)	AC Loadline	S-Processor Line	—	—	Same as Max DC_LL (up to 400 KHz)	mΩ	7, 9, 10
T_OVS_MAX	Max Overshoot time	—	—	—	10	µs	
V_OVS_MAX	Max Overshoot	—	—	—	70	mV	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
3. The voltage specification requirements are measured across Vcc_{GT_SENSE} and Vss_{GT_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. This differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or low-power states).
6. N/A
7. LL measured at sense points.
8. Operating voltage range in steady state.
9. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
10. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly via the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.

7.2.1.3 V_{DDQ} DC Specifications

Table 7-4. Memory Controller (V_{DDQ}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note[1]
V_{DDQ} (DDR4)	Processor I/O supply voltage for DDR4	All	Typ-5%	1.20	Typ+5%	V	3, 4, 5
TOB_{VDDQ}	VDDQ Tolerance	All	AC+DC:± 5			%	3, 4, 6
Icc_{MAX_VDDQ} (DDR4)	Max Current for V_{DDQ} Rail (DDR4)	S	—	—		A	2

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. The current supplied to the DIMM modules is not included in this specification.
3. Includes AC and DC error, where the AC noise is bandwidth limited to under 100 MHz, measured on package pins.
4. No requirement on the breakdown of AC versus DC noise.
5. The voltage specification requirements are measured as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
6. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.4 Vcc$_{SA}$ DC Specifications

Table 7-5. System Agent (Vcc$_{SA}$) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note^{1,2}
Vcc$_{SA}$	Voltage for the System Agent	S-Processor Line (fixed voltage)	—	1.05	—	V	3,5
TOB$_{VCCSA}$	Vcc$_{SA}$ Tolerance	S-Processor Line			±5(DC+AC+ripple)	%	8
I$_{CCMAX\_VCCSA}$	Max Current for V$_{CCSA}$ Rail	S-Processor Lines Quad core GT2 S-Processor Lines Hexa Core GT2			11.1 11.1	A	
DC_LL	Vcc$_{SA}$ Loadline	S-Processor Line			10.3	mΩ	6,7
T_OVS_MAX	Max Overshoot time	—	—	—	10	µs	
V_OVS_MAX	Max Overshoot	—	—	—	70	mV	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc$_{SA\text{—}SENSE}$ and Vss$_{SA\text{—}SENSE}$ as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. PSx refers to the voltage regulator power state as set by the SVID protocol.
5. Vcc$_{SA}$ voltage during boot (Vboot)1.05V for a duration of 2 seconds.
6. LL measured at sense points.
7. LL specification values should not be exceeded. If exceeded, power, performance and reliability penalty are expected.
8. Load Line (AC/DC) should be measured by the VRTT tool and programmed accordingly via the BIOS Load Line override setup options. AC/DC Load Line BIOS programming directly affects operating voltages (AC) and power measurements (DC). A superior board design with a shallower AC Load Line can improve on power, performance, and thermals compared to boards designed for POR impedance.
9. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.5 Vcc$_{IO}$ DC Specifications

Table 7-6. Processor I/O (Vcc$_{IO}$) Supply DC Voltage and Current Specifications (Sheet 1 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note^{1,2}
Vcc$_{IO}$	Voltage for the memory controller and shared cache	S	—	0.95	—	V	3,4,5
TOB$_{VCCIO}$	Vcc$_{IO}$ Tolerance	All	AC+DC:± 5			%	3,7
Icc$_{MAX\_VCCIO}$	Max Current for V$_{CCIO}$ Rail	S	—	—	6.4	A	
T_OVS_MAX	Max Overshoot time	All	—	—	150	µS	6
V_OVS_MAX	Max Overshoot at TDP	All	—	—	30	mV	6

Table 7-6. Processor I/O (Vcc_{IO}) Supply DC Voltage and Current Specifications (Sheet 2 of 2)

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note^{1,2}

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured across Vcc_{IO_SENSE} and Vss_{IO_SENSE} as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For low BW bus connection between processor and PCH -> Vcc_{IO}=0.85V.
5. For high BW bus connection between processor and PCH -> Vcc_{IO}=0.95V.
6. OS occurs during power on only, **not** during normal operation
7. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.6 Vcc_{ST} DC Specifications

Table 7-7. Vcc Sustain (Vcc_{ST}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Units	Notes ^{1,2}
Vcc_{ST}	Processor Vcc Sustain supply voltage	S with PCH Z370	—	1.0	—	V	3
TOB_{ST}	Vcc_{ST} Tolerance	All	AC+DC:± 5			%	3,4
Icc_{MAX_ST}	Max Current for Vcc_{ST}	S-Processor Lines	—	—	80	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For Voltage less than 1V, TOB will be 50 mV.

7.2.1.7 Vcc_{PLL} DC Specifications

Table 7-8. Processor PLL (Vcc_{PLL}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes^{1,2}
Vcc_{PLL}	PLL supply voltage (DC + AC specification)	S with PCH Z370	—	1.0	—	V	3
TOB_{CCPLL}	Vcc_{PLL} Tolerance	All	AC+DC:± 5			%	3,4
Icc_{MAX_VCCPLL}	Max Current for Vcc_{PLL} Rail	S-Processor Lines	—	—	150	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For Voltage less than 1V, TOB will be 50 mV.

Table 7-9. Processor PLL_OC (Vcc_{PLL_OC}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes[1,2]
Vcc_{PLL_OC}	PLL_OC supply voltage (DC + AC specification)	All	—	V_{DDQ}	—	V	3
TOB_{CCPLL_OC}	Vcc_{PLL_OC} Tolerance	All	AC+DC:± 5			%	3,4
$Icc_{MAX\_VCCPLL\_OC}$	Max Current for Vcc_{PLL_OC} Rail	S-Processor Line - Quad Core GT2 S-Processor Line - Hexa Core GT2	—	—	130 130	mA	

Notes:
1. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Long term reliability cannot be assured in conditions above or below Max/Min functional limits.
3. The voltage specification requirements are measured on package pins as near as possible to the processor with an oscilloscope set to 100-MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the oscilloscope probe.
4. For Voltage less than 1V, TOB will be 50 mV.

7.2.2 Processor Interfaces DC Specifications

7.2.2.1 DDR4 DC Specifications

Table 7-10. DDR4 Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	US-Processor Line			Units	Notes[1]
		Min	Typ	Max		
V_{IL}	Input Low Voltage	—	—	VREF(INT) - 0.07*VDDQ	V	2, 4, 8, 9, 13
V_{IH}	Input High Voltage	VREF(INT) + 0.07*VDDQ	—	—	V	3, 4, 8, 9, 13
$R_{ON\_UP/DN(DQ)}$	DDR4 Data Buffer pull-up/ down Resistance	Trainable			Ω	11
$R_{ODT(DQ)}$	DDR4 On-die termination equivalent resistance for data signals	Trainable			Ω	11
$V_{ODT(DC)}$	DDR4 On-die termination DC working point (driver set to receive mode)	$0.45*V_{DDQ}$	$0.5*V_{DDQ}$	$0.55*V_{DDQ}$	V	9
$R_{ON\_UP/DN(CK)}$	DDR4 Clock Buffer pull-up/ down Resistance	0.8*Typ	26	1.2*Typ	Ω	5, 11
$R_{ON\_UP/DN(CMD)}$	DDR4 Command Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	11
$R_{ON\_UP/DN(CTL)}$	DDR4 Control Buffer pull-up/ down Resistance	0.8*Typ	20	1.2*Typ	Ω	5, 11
$R_{ON\_UP/DN}$ (DDR_VTT_CNTL)	System Memory Power Gate Control Buffer Pull-Up/ down Resistance	40	—	140	Ω	-
I_{LI}	Input Leakage Current (DQ, CK) 0 V $0.2*V_{DDQ}$ $0.8*V_{DDQ}$	—	—	1	mA	-
DDR0_VREF_DQ DDR1_VREF_DQ DDR_VREF_CA	VREF output voltage	$V_{DDQ}/2-0.06$	$V_{DDQ}/2$	$V_{DDQ}/2+0.06$	V	12,14, 15

Table 7-10. DDR4 Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	US-Processor Line			Units	Notes[1]
		Min	Typ	Max		
DDR_RCOMP[0]	ODT resistance compensation	RCOMP values are memory topology dependent.			Ω	6
DDR_RCOMP[1]	Data resistance compensation				Ω	6
DDR_RCOMP[2]	Command resistance compensation				Ω	6

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{IL} may experience excursions above V_{DDQ}. However, input signal drivers should comply with the signal quality specifications.
5. This is the pull up/down driver resistance after compensation. Note that BIOS power training may change these values significantly based on margin/power trade-off. See processor I/O Buffer Models for I/V characteristics.
6. DDR_RCOMP resistors are installed on the package.
7. DDR_VREF is defined as $V_{DDQ}/2$ for DDR4
8. R_{ON} tolerance is preliminary and might be subject to change.
9. The value will be set during the MRC boot training within the specified range.
10. Processor may be damaged if V_{IH} exceeds the maximum voltage for extended periods.
11. Final value determined by BIOS power training, values might vary between bytes and/or units.
12. VREF values determined by BIOS training, values might vary between units.
13. VREF(INT) is a trainable parameter whose value is determined by BIOS for margin optimization.
14. DDR1_Vref_DQ connected to Channel 1 VREF_CA.
15. DDR_Vref_CA connected to Channel 0 VREF_CA.

7.2.2.2 PCI Express* Graphics (PEG) DC Specifications

Table 7-11. PCI Express* Graphics (PEG) Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential Tx Impedance	80	100	120	Ω	1, 5
$Z_{RX\text{-}DC}$	DC Common Mode Rx Impedance	40	50	60	Ω	1, 4
$Z_{RX\text{-}DIFF\text{-}DC}$	DC Differential Rx Impedance	80	—	120	Ω	1
PEG_RCOMP	resistance compensation	24.75	25	25.25	Ω	2, 3

Notes:
1. Refer to the PCI Express Base Specification for more details.
2. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.
3. PEG_RCOMP resistance should be provided on the system board with 1% resistors. COMP resistors are to V_{CCIO}.
   PEG_RCOMP - Intel allows using 24.9 Ω 1% resistors.
4. DC impedance limits are needed to ensure Receiver detect.
5. The Rx DC Common Mode Impedance should be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly.Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) should be within the specified range by the time Detect is entered.

7.2.2.3 Digital Display Interface (DDI) DC Specifications

Table 7-12. Digital Display Interface Group DC Specifications (DP/HDMI) (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
V_{OL}	DDIB_TXC[3:0] Output Low Voltage DDIC_TXC[3:0] Output Low Voltage DDID_TXC[3:0] Output Low Voltage	—	—	$0.25*V_{CCIO}$	V	1,2
V_{OH}	DDIB_TXC[3:0] Output High Voltage DDIC_TXC[3:0] Output High Voltage DDID_TXC[3:0] Output High Voltage	$0.75*V_{CCIO}$	—	—	V	1,2
ZTX-DIFF-DC	DC Differential Tx Impedance	80	100	120	Ω	

Table 7-12. Digital Display Interface Group DC Specifications (DP/HDMI) (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]

Notes:
1. Vcc_{IO} depends on segment.
2. V_{OL} and V_{OH} levels depends on the level chosen by the Platform.

7.2.2.4 embedded DisplayPort* (eDP*) DC Specification

Table 7-13. embedded DisplayPort* (eDP*) Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Units
V_{OL}	eDP_DISP_UTIL Output Low Voltage	—	—	$0.1*V_{CCIO}$	V
V_{OH}	eDP_DISP_UTIL Output High Voltage	$0.9*Vcc_{IO}$	—	—	V
R_{UP}	eDP_DISP_UTIL Internal pull-up	100	—	—	Ω
R_{DOWN}	eDP_DISP_UTIL Internal pull-down	100	—	—	Ω
eDP_RCOMP	eDP resistance compensation	24.75	25	25.25	Ω
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω

Notes:
1. COMP resistance is to VCOMP_OUT.
2. eDP_RCOMP resistor should be provided on the system board.

7.2.2.5 CMOS DC Specifications

Table 7-14. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	—	Vcc * 0.3	V	2, 5
V_{IH}	Input High Voltage	Vcc * 0.7	—	V	2, 4, 5
V_{OL}	Output Low Voltage	—	Vcc * 0.1	V	2
V_{OH}	Output High Voltage	Vcc * 0.9	—	V	2, 4
R_{ON}	Buffer on Resistance	23	73	Ω	-
I_{LI}	Input Leakage Current	—	±150	μA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The Vcc referred to in these specifications refers to instantaneous Vcc levels.
3. For VIN between "0" V and Vcc Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above Vcc. However, input signal drivers should comply with the signal quality specifications.
5. N/A

7.2.2.6 GTL and OD DC Specifications

Table 7-15. GTL Signal Group and Open Drain Signal Group DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage (TAP, except PROC_TCK, PROC_TRST#)	—	Vcc * 0.6	V	2, 5, 6
V_{IH}	Input High Voltage (TAP, except PROC_TCK, PROC_TRST#)	Vcc * 0.72	—	V	2, 4, 5, 6

Table 7-15. GTL Signal Group and Open Drain Signal Group DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes[1]
V_{IL}	Input Low Voltage (PROC_TCK,PROC_TRST#)	—	Vcc * 0.3	V	2, 5, 6
V_{IH}	Input High Voltage (PROC_TCK,PROC_TRST#)	Vcc * 0.3	—	V	2, 4, 5, 6
$V_{HYSTERESIS}$	Hysteresis Voltage	Vcc * 0.2	—	V	-
R_{ON}	Buffer on Resistance (TDO)	7	17	Ω	-
V_{IL}	Input Low Voltage (other GTL)	—	Vcc * 0.6	V	2, 5, 6
V_{IH}	Input High Voltage (other GTL)	Vcc * 0.72	—	V	2, 4, 5, 6
R_{ON}	Buffer on Resistance (CFG/BPM)	16	24	Ω	-
R_{ON}	Buffer on Resistance (other GTL)	12	28	Ω	-
I_{LI}	Input Leakage Current	—	±150	μA	3

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The Vcc_{ST} referred to in these specifications refers to instantaneous $Vcc_{ST/IO}$.
3. For V_{IN} between 0 V and Vcc_{ST}. Measured when the driver is tri-stated.
4. V_{IH} and V_{OH} may experience excursions above Vcc_{ST}. However, input signal drivers should comply with the signal quality specifications.
5. N/A
6. Those V_{IL}/V_{IH} values are based on ODT disabled (ODT Pull-up not exist).

7.2.2.7 PECI DC Characteristics

The PECI interface operates at a nominal voltage set by Vcc_{ST}. The set of DC electrical specifications shown in the following table is used with devices normally operating from a Vcc_{ST} interface supply.

Vcc_{ST} nominal levels will vary between processor families. All PECI devices will operate at the Vcc_{ST} level determined by the processor installed in the system.

Table 7-16. PECI DC Electrical Limits

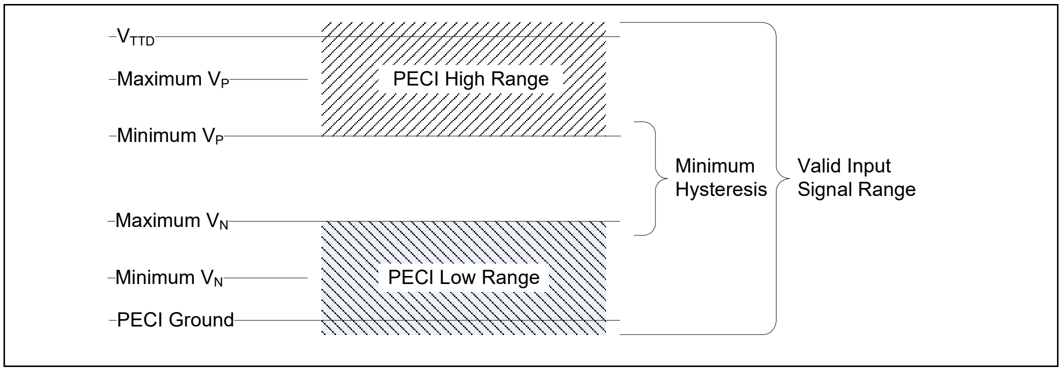
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
R_{up}	Internal pull up resistance	15	45	Ω	3
V_{IN}	Input Voltage Range	-0.15	Vcc_{ST} + 0.15	V	-
$V_{Hysteresis}$	Hysteresis	0.15 * Vcc_{ST}	—	V	-
V_{IL}	Input Voltage Low- Edge Threshold Voltage	—	0.3 * Vcc_{ST}	V	-
V_{IH}	Input Voltage High-Edge Threshold Voltage	0.7 * Vcc_{ST}	—	V	-
C_{bus}	Bus Capacitance per Node	N/A	10	pF	-
C_{pad}	Pad Capacitance	0.7	1.8	pF	-
Ileak000	leakage current @ 0V	—	0.6	mA	-
Ileak025	leakage current @ 0.25* Vcc_{ST}	—	0.4	mA	-
Ileak050	leakage current @ 0.50* Vcc_{ST}	—	0.2	mA	-
Ileak075	leakage current @ 0.75* Vcc_{ST}	—	0.13	mA	-
Ileak100	leakage current @ Vcc_{ST}	—	0.10	mA	-

Notes:
1. Vcc_{ST} supplies the PECI interface. PECI behavior does not affect Vcc_{ST} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. The PECI buffer internal pull up resistance measured at 0.75* Vcc_{ST}.

Input Device Hysteresis

The input buffers in both client and host models should use a Schmitt-triggered input design for improved noise immunity. Use the following figure as a guide for input buffer design.

Figure 7-1. Input Device Hysteresis



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8 Package Mechanical Specifications

8.1 Package Mechanical Attributes

The S-Processor Line uses a Flip Chip technology available in Land Grid Array (LGA). The following table provides an overview of the mechanical attributes of the package.

Table 8-1. Package Mechanical Attributes

Package	Parameter	S-Processor Line	
		Hexa Core / Quad Core GT2	
Package Technology	Package Type	Flip Chip Land Grid Array	
	Interconnect	Land Grid Array (LGA)	
	Lead Free	N/A	
	Halogenated Flame Retardant Free	Yes	
Package Configuration	Solder Ball Composition	N/A	
	Ball/Pin Count	1151	
	Grid Array Pattern	Grid Array	
	Land Side Capacitors	Yes	
	Die Side Capacitors	Yes	Yes
	Die Configuration	1 Die Single-Chip Package with IHS	
Package Dimensions	Nominal Package Size	37.5x37.5 mm	
	Min Ball/Pin pitch	0.914 mm	

8.2 Package Storage Specifications

Table 8-2. Package Storage Specifications (Sheet 1 of 2)

Parameter	Description	Min	Max	Notes
$T_{ABSOLUTE\ STORAGE}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time in Intel Original sealed moisture barrier bag.	-25 °C	125 °C	1, 2, 3
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for the sustained period of time as specified below in Intel Original sealed moisture barrier bag.	-5 °C	40 °C	1, 2, 3

Table 8-2. Package Storage Specifications (Sheet 2 of 2)

Parameter	Description	Min	Max	Notes
$RH_{\text{SUSTAINED STORAGE}}$	The maximum device storage relative humidity for the sustained period of time as specified below in Intel Original sealed moisture barrier bag.	60% @ 24 °C		1, 2, 3
$TIME_{\text{SUSTAINED STORAGE}}$	A prolonged or extended period of time: associated with customer shelf life in Intel Original sealed moisture barrier bag.	0 months	6 months	1, 2, 3

Notes:

1. $T_{\text{ABSOLUTE STORAGE}}$ applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.
2. Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
3. Post board attach storage temperature limits are not specified. Consult your board manufacturer for storage specifications.

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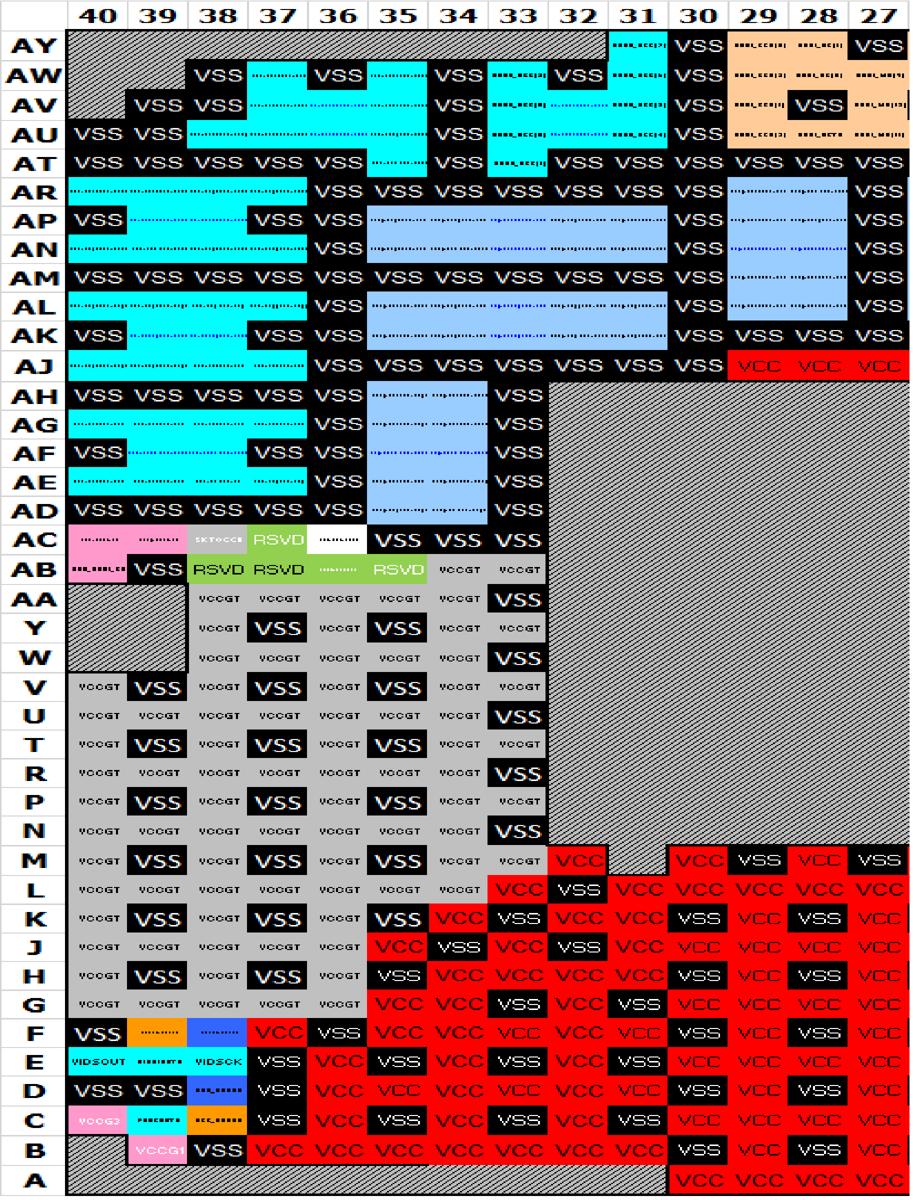
9 Processor Ball Information

The processor is available in the LGA package (LGA1151). This chapter provides the top view of the Ball map. Table 9-1 provides the Ball Listing.

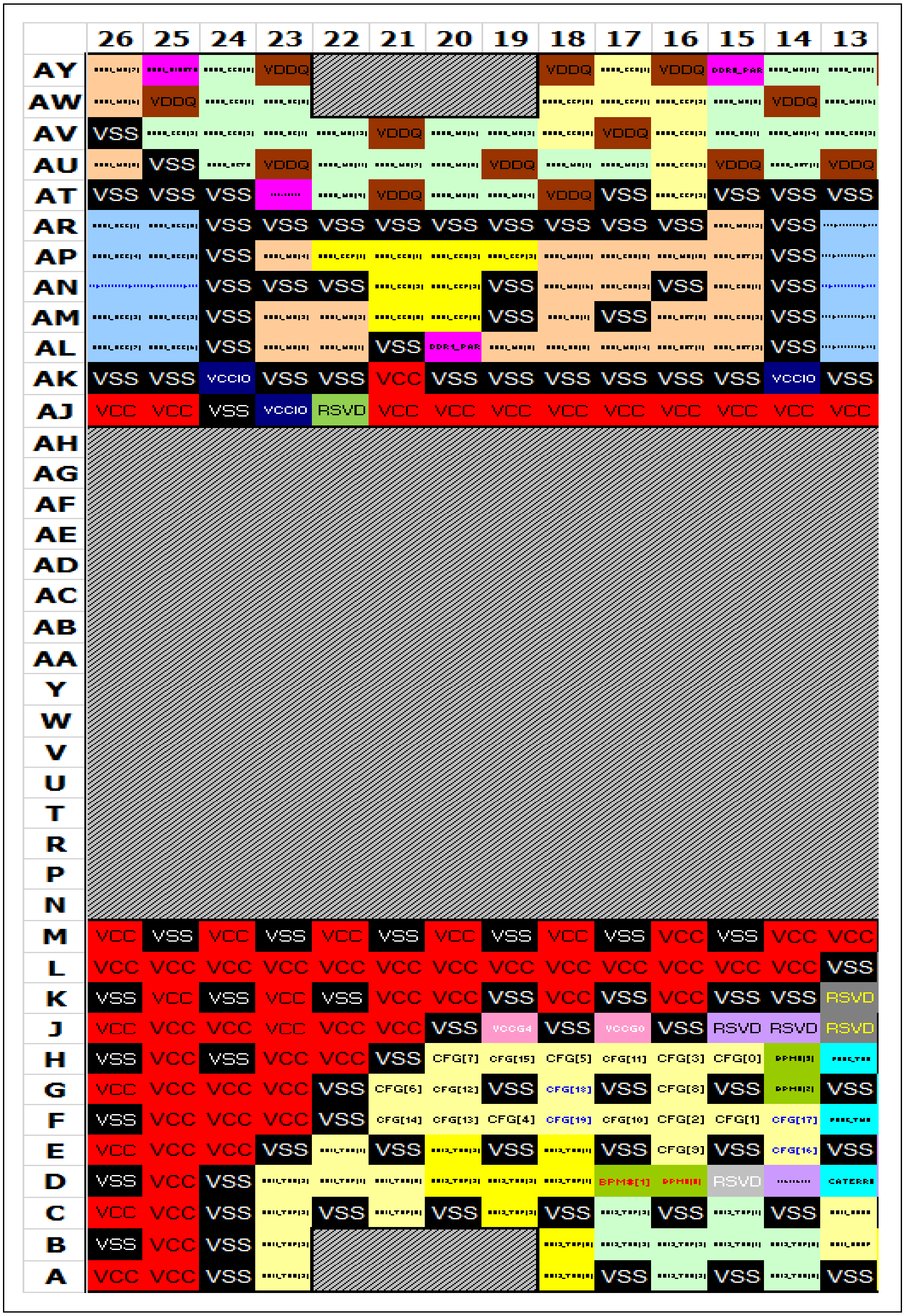
9.1 Ball Map

Figure 9-1. Ball Map Left (40-27)



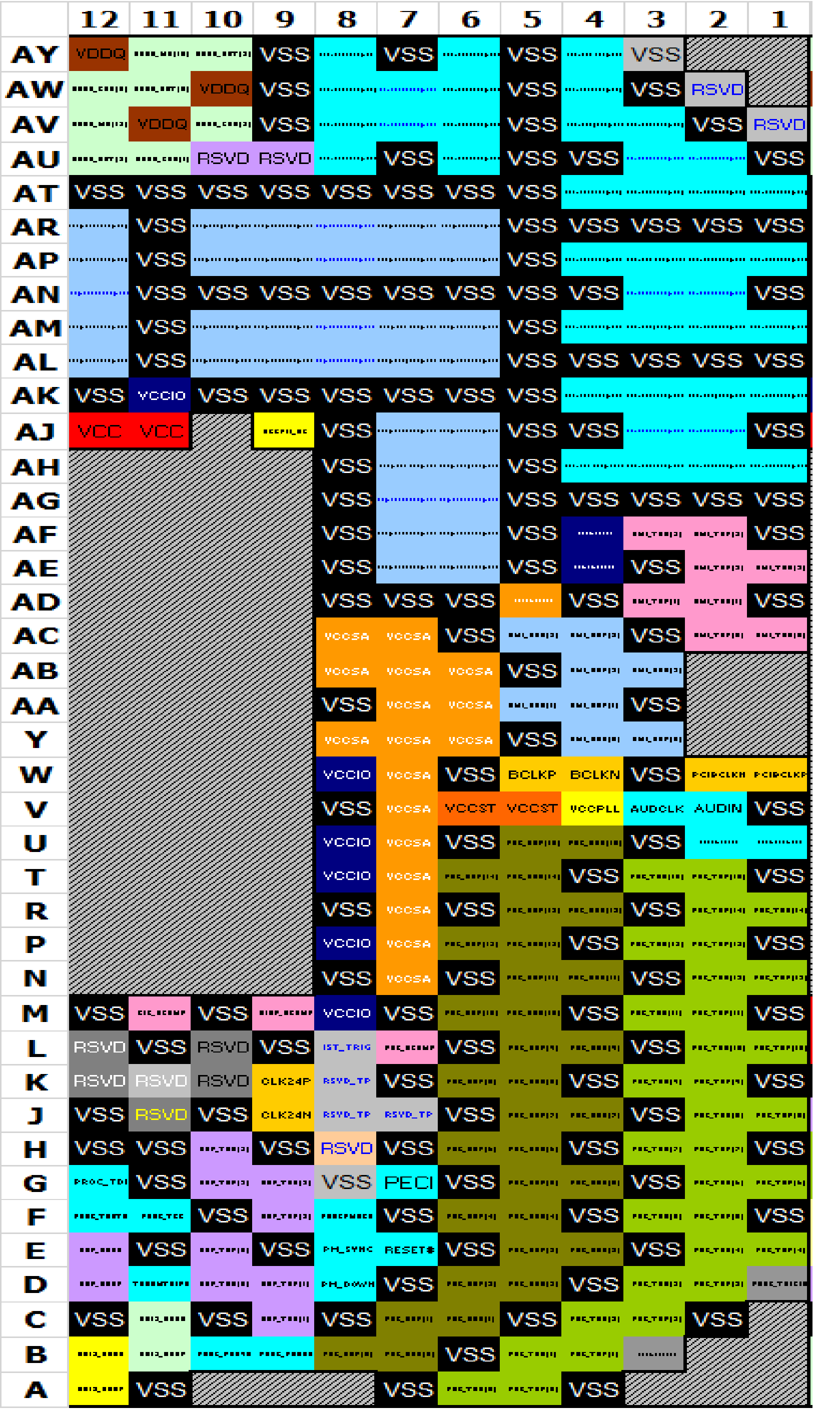
	40	39	38	37	36	35	34	33	32	31	30	29	28	27
AY										[illegible]	VSS	[illegible]	[illegible]	VSS
AW			VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	[illegible]	[illegible]
AV		VSS	VSS	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	VSS	[illegible]	VSS	[illegible]
AU	VSS	VSS	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]
AT	VSS	VSS	VSS	VSS	VSS	[illegible]	VSS	[illegible]	VSS	VSS	VSS	VSS	VSS	VSS
AR	[illegible]	[illegible]	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	VSS
AP	VSS	[illegible]	[illegible]	VSS	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
AN	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
AM	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	VSS
AL	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
AK	VSS	[illegible]	[illegible]	VSS	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	VSS	VSS	VSS
AJ	[illegible]	[illegible]	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VCC	VCC	VCC
AH	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	VSS						
AG	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS						
AF	VSS	[illegible]	[illegible]	VSS	VSS	[illegible]	[illegible]	VSS						
AE	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS						
AD	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	VSS						
AC	[illegible]	[illegible]	[illegible]	RSVD	[illegible]	VSS	VSS	VSS						
AB	[illegible]	VSS	RSVD	RSVD	[illegible]	RSVD	VCCGT	VCCGT						
AA			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VSS						
Y			VCCGT	VSS	VCCGT	VSS	VCCGT	VCCGT						
W			VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VSS						
V	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCCGT	VCCGT						
U	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VSS						
T	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCCGT	VCCGT						
R	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VSS						
P	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCCGT	VCCGT						
N	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VSS						
M	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCCGT	VCCGT	VCC		VCC	VSS	VCC	VSS
L	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCC	VSS	VCC	VCC	VCC	VCC	VCC
K	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	VCC
J	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC	VCC
H	VCCGT	VSS	VCCGT	VSS	VCCGT	VSS	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC
G	VCCGT	VCCGT	VCCGT	VCCGT	VCCGT	VCC	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC
F	VSS	[illegible]	[illegible]	VCC	VSS	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC
E	VIDSOUT	[illegible]	VIDSCK	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC
D	VSS	VSS	[illegible]	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC
C	VCCG3	[illegible]	[illegible]	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC	VCC
B		VCCG1	VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCC	VSS	VCC
A											VCC	VCC	VCC	VCC

Figure 9-2. Ball Map Center (26-13)



	26	25	24	23	22	21	20	19	18	17	16	15	14	13
AY	[illegible]	[illegible]	[illegible]	VDDQ					VDDQ	[illegible]	VDDQ	[illegible]	[illegible]	[illegible]
AW	[illegible]	VDDQ	[illegible]	[illegible]					[illegible]	[illegible]	[illegible]	[illegible]	VDDQ	[illegible]
AV	VSS	[illegible]	[illegible]	[illegible]	[illegible]	VDDQ	[illegible]	[illegible]	[illegible]	VDDQ	[illegible]	[illegible]	[illegible]	[illegible]
AU	[illegible]	VSS	[illegible]	VDDQ	[illegible]	[illegible]	[illegible]	VDDQ	[illegible]	[illegible]	[illegible]	VDDQ	[illegible]	VDDQ
AT	VSS	VSS	VSS	[illegible]	[illegible]	VDDQ	[illegible]	[illegible]	VDDQ	VSS	[illegible]	VSS	VSS	VSS
AR	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	VSS	[illegible]
AP	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]
AN	[illegible]	[illegible]	VSS	VSS	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]	VSS	[illegible]
AM	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]
AL	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	DDR1_PAR	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]
AK	VSS	VSS	VCCIO	VSS	VSS	VCC	VSS	VSS	VSS	VSS	VSS	VSS	VCCIO	VSS
AJ	VCC	VCC	VSS	VCCIO	RSVD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC
AH														
AG														
AF														
AE														
AD														
AC														
AB														
AA														
Y														
W														
V														
U														
T														
R														
P														
N														
M	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC
L	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS
K	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VSS	RSVD
J	VCC	VCC	VCC	VCC	VCC	VCC	VSS	VCCG4	VSS	VCCG0	VSS	RSVD	RSVD	RSVD
H	VSS	VCC	VSS	VCC	VCC	VSS	CFG[7]	CFG[15]	CFG[5]	CFG[11]	CFG[3]	CFG[0]	[illegible]	[illegible]
G	VCC	VCC	VCC	VCC	VSS	CFG[6]	CFG[12]	VSS	CFG[18]	VSS	CFG[8]	VSS	[illegible]	VSS
F	VSS	VCC	VCC	VCC	VSS	CFG[14]	CFG[13]	CFG[4]	CFG[19]	CFG[10]	CFG[2]	CFG[1]	CFG[17]	[illegible]
E	VCC	VCC	VCC	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	CFG[9]	VSS	CFG[16]	VSS
D	VSS	VCC	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	BPM#[1]	[illegible]	RSVD	[illegible]	CATERR#
C	VCC	VCC	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]
B	VSS	VCC	VSS	[illegible]					[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
A	VCC	VCC	VSS	[illegible]					[illegible]	VSS	[illegible]	VSS	[illegible]	VSS

Figure 9-3. Ball Map Right (12-1)



	12	11	10	9	8	7	6	5	4	3	2	1
AY	VDDQ	[illegible]	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	VSS		
AW	[illegible]	[illegible]	VDDQ	VSS	[illegible]	[illegible]	[illegible]	VSS	[illegible]	VSS	RSVD	
AV	[illegible]	VDDQ	[illegible]	VSS	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	RSVD
AU	[illegible]	[illegible]	RSVD	RSVD	[illegible]	VSS	[illegible]	VSS	VSS	[illegible]	[illegible]	VSS
AT	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	[illegible]	[illegible]
AR	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS
AP	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]
AN	[illegible]	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	VSS
AM	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]
AL	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS
AK	VSS	VCCIO	VSS	VSS	VSS	VSS	VSS	VSS	[illegible]	[illegible]	[illegible]	[illegible]
AJ	VCC	VCC		[illegible]	VSS	[illegible]	[illegible]	VSS	VSS	[illegible]	[illegible]	VSS
AH					VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	[illegible]
AG					VSS	[illegible]	[illegible]	VSS	VSS	VSS	VSS	VSS
AF					VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]	VSS
AE					VSS	[illegible]	[illegible]	VSS	[illegible]	VSS	[illegible]	[illegible]
AD					VSS	VSS	VSS	[illegible]	VSS	[illegible]	[illegible]	VSS
AC					VCCSA	VCCSA	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
AB					VCCSA	VCCSA	VCCSA	VSS	[illegible]	[illegible]		
AA					VSS	VCCSA	VCCSA	[illegible]	[illegible]	VSS		
Y					VCCSA	VCCSA	VCCSA	VSS	[illegible]	[illegible]		
W					VCCIO	VCCSA	VSS	BCLKP	BCLKN	VSS	PCIECLKN	PCIECLKP
V					VSS	VCCSA	VCCST	VCCST	VCCPLL	AUDCLK	AUDIN	VSS
U					VCCIO	VCCSA	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
T					VCCIO	VCCSA	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
R					VSS	VCCSA	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
P					VCCIO	VCCSA	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
N					VSS	VCCSA	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
M	VSS	[illegible]	VSS	[illegible]	VCCIO	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
L	RSVD	VSS	RSVD	VSS	IST_TRIG	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
K	RSVD	RSVD	RSVD	CLK24P	RSVD_TP	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
J	VSS	RSVD	VSS	CLK24N	RSVD_TP	RSVD_TP	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
H	VSS	VSS	[illegible]	VSS	RSVD	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
G	PROC_TDI	VSS	[illegible]	[illegible]	VSS	PECI	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
F	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS
E	[illegible]	VSS	[illegible]	VSS	PM_SYNC	RESET#	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]
D	[illegible]	[illegible]	[illegible]	[illegible]	PM_DOWN	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]
C	VSS	[illegible]	VSS	[illegible]	VSS	[illegible]	[illegible]	VSS	[illegible]	[illegible]	VSS	
B	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	VSS	[illegible]	[illegible]	[illegible]		
A	[illegible]	VSS				VSS	[illegible]	[illegible]	VSS			

9.2 Ball Listing

Table 9-1. Ball Listing (Sheet 1 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
V3	PROC_AUDIO_CLK	I	16002	-2286
V2	PROC_AUDIO_SDI	I	16916.4	-2286
U1	PROC_AUDIO_SDO	O	17830.8	-3200.4
W4	BCLKN	I	15087.6	-1371.6
W5	BCLKP	I	14173.2	-1371.6
D13	CATERR#	O	6858	-15087.6
J9	CLK24N	I	10515.6	-10515.6
K9	CLK24P	I	10515.6	-9601.2
G8	VSS	GND	11430	-12344.4
AY3	VSS	GND	16002	17830.8
F11	PROC_TCK	I	8686.8	-13258.8
G12	PROC_TDI	I	7772.4	-12344.4
H13	PROC_TDO	I	6858	-11430
F13	PROC_TMS	I	6858	-13258.8
F12	PROC_TRST#	I	7772.4	-13258.8
D1	PROC_TRIGIN	I	17830.8	-15087.6
B3	PROC_TRIGOUT	I	16002	-16916.4
F8	PROCPWRGD	I	11430	-13258.8
C13	DDI1_AUXN	O	6858	-16002
B13	DDI1_AUXP	O	6858	-16916.4
D21	DDI1_TXN[0]	O	-457.2	-15087.6
E22	DDI1_TXN[1]	O	-1371.6	-14173.2
A23	DDI1_TXN[2]	O	-2286	-17830.8
D23	DDI1_TXN[3]	O	-2286	-15087.6
C21	DDI1_TXP[0]	O	-457.2	-16002
D22	DDI1_TXP[1]	O	-1371.6	-15087.6
B23	DDI1_TXP[2]	O	-2286	-16916.4
C23	DDI1_TXP[3]	O	-2286	-16002
B12	DDI2_AUXN	O	7772.4	-16916.4
A12	DDI2_AUXP	O	7772.4	-17830.8
A18	DDI2_TXN[0]	O	2286	-17830.8
E18	DDI2_TXN[1]	O	2286	-14173.2
D19	DDI2_TXN[2]	O	1371.6	-15087.6
E20	DDI2_TXN[3]	O	457.2	-14173.2
B18	DDI2_TXP[0]	O	2286	-16916.4
D18	DDI2_TXP[1]	O	2286	-15087.6

Table 9-1. Ball Listing (Sheet 2 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
C19	DDI2_TXP[2]	O	1371.6	-16002
D20	DDI2_TXP[3]	O	457.2	-15087.6
C11	DDI3_AUXN	O	8686.8	-16002
B11	DDI3_AUXP	O	8686.8	-16916.4
A14	DDI3_TXN[0]	O	5943.6	-17830.8
B15	DDI3_TXN[1]	O	5029.2	-16916.4
A16	DDI3_TXN[2]	O	4114.8	-17830.8
B17	DDI3_TXN[3]	O	3200.4	-16916.4
B14	DDI3_TXP[0]	O	5943.6	-16916.4
C15	DDI3_TXP[1]	O	5029.2	-16002
B16	DDI3_TXP[2]	O	4114.8	-16916.4
C17	DDI3_TXP[3]	O	3200.4	-16002
Y4	DMI_RXN[0]	I	15087.6	-457.2
AA5	DMI_RXN[1]	I	14173.2	457.2
AB3	DMI_RXN[2]	I	16002	1371.6
AC5	DMI_RXN[3]	I	14173.2	2286
Y3	DMI_RXP[0]	I	16002	-457.2
AA4	DMI_RXP[1]	I	15087.6	457.2
AB4	DMI_RXP[2]	I	15087.6	1371.6
AC4	DMI_RXP[3]	I	15087.6	2286
AC1	DMI_TXN[0]	O	17830.8	2286
AD2	DMI_TXN[1]	O	16916.4	3200.4
AE1	DMI_TXN[2]	O	17830.8	4114.8
AF3	DMI_TXN[3]	O	16002	5029.2
AC2	DMI_TXP[0]	O	16916.4	2286
AD3	DMI_TXP[1]	O	16002	3200.4
AE2	DMI_TXP[2]	O	16916.4	4114.8
AF2	DMI_TXP[3]	O	16916.4	5029.2
M9	DISP_RCOMP	N/A	10515.6	-7772.4
E12	EDP_AUXN	O	7772.4	-14173.2
D12	EDP_AUXP	O	7772.4	-15087.6
D14	EDP_DISP_UTIL	O	5943.6	-15087.6
D10	EDP_TXN[0]	O	9601.2	-15087.6
C9	EDP_TXN[1]	O	10515.6	-16002
H10	EDP_TXN[2]	O	9601.2	-11430
G9	EDP_TXN[3]	O	10515.6	-12344.4
E10	EDP_TXP[0]	O	9601.2	-14173.2
D9	EDP_TXP[1]	O	10515.6	-15087.6
G10	EDP_TXP[2]	O	9601.2	-12344.4

Table 9-1. Ball Listing (Sheet 3 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
F9	EDP_TXP[3]	O	10515.6	-13258.8
H8	RSVD	N/A	11430	-11430
K10	RSVD	N/A	9601.2	-9601.2
L10	RSVD	N/A	9601.2	-8686.8
K12	RSVD	N/A	7772.4	-9601.2
L12	RSVD	N/A	7772.4	-8686.8
J13	RSVD	N/A	6858	-10515.6
K13	RSVD	N/A	6858	-9601.2
J11	RSVD	N/A	8686.8	-10515.6
D16	BPM#[0]	I/O	4114.8	-15087.6
D17	BPM#[1]	I/O	3200.4	-15087.6
G14	BPM#[2]	I/O	5943.6	-12344.4
H14	BPM#[3]	I/O	5943.6	-11430
H15	CFG[0]	I	5029.2	-11430
F15	CFG[1]	I	5029.2	-13258.8
F17	CFG[10]	I	3200.4	-13258.8
H17	CFG[11]	I	3200.4	-11430
G20	CFG[12]	I	457.2	-12344.4
F20	CFG[13]	I	457.2	-13258.8
F21	CFG[14]	I	-457.2	-13258.8
H19	CFG[15]	I	1371.6	-11430
F16	CFG[2]	I	4114.8	-13258.8
H16	CFG[3]	I	4114.8	-11430
F19	CFG[4]	I	1371.6	-13258.8
H18	CFG[5]	I	2286	-11430
G21	CFG[6]	I	-457.2	-12344.4
H20	CFG[7]	I	457.2	-11430
G16	CFG[8]	I	4114.8	-12344.4
E16	CFG[9]	I	4114.8	-14173.2
M11	CFG_RCOMP	N/A	8686.8	-7772.4
E14	CFG[16]	I	5943.6	-14173.2
G18	CFG[18]	I	2286	-12344.4
F14	CFG[17]	I	5943.6	-13258.8
F18	CFG[19]	I	2286	-13258.8
W2	PCI_BCLKN	I	16916.4	-1371.6
W1	PCI_BCLKP	I	17830.8	-1371.6
G7	PECI	I/O	12344.4	-12344.4
L7	PEG_RCOMP	N/A	12344.4	-8686.8
B7	PEG_RXN[0]	I	12344.4	-16916.4

Table 9-1. Ball Listing (Sheet 4 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
C6	PEG_RXN[1]	I	13258.8	-16002
M5	PEG_RXN[10]	I	14173.2	-7772.4
N4	PEG_RXN[11]	I	15087.6	-6858
P5	PEG_RXN[12]	I	14173.2	-5943.6
R4	PEG_RXN[13]	I	15087.6	-5029.2
T5	PEG_RXN[14]	I	14173.2	-4114.8
U4	PEG_RXN[15]	I	15087.6	-3200.4
D5	PEG_RXN[2]	I	14173.2	-15087.6
E4	PEG_RXN[3]	I	15087.6	-14173.2
F5	PEG_RXN[4]	I	14173.2	-13258.8
G4	PEG_RXN[5]	I	15087.6	-12344.4
H5	PEG_RXN[6]	I	14173.2	-11430
J4	PEG_RXN[7]	I	15087.6	-10515.6
K5	PEG_RXN[8]	I	14173.2	-9601.2
L4	PEG_RXN[9]	I	15087.6	-8686.8
B8	PEG_RXP[0]	I	11430	-16916.4
C7	PEG_RXP[1]	I	12344.4	-16002
M6	PEG_RXP[10]	I	13258.8	-7772.4
N5	PEG_RXP[11]	I	14173.2	-6858
P6	PEG_RXP[12]	I	13258.8	-5943.6
R5	PEG_RXP[13]	I	14173.2	-5029.2
T6	PEG_RXP[14]	I	13258.8	-4114.8
U5	PEG_RXP[15]	I	14173.2	-3200.4
D6	PEG_RXP[2]	I	13258.8	-15087.6
E5	PEG_RXP[3]	I	14173.2	-14173.2
F6	PEG_RXP[4]	I	13258.8	-13258.8
G5	PEG_RXP[5]	I	14173.2	-12344.4
H6	PEG_RXP[6]	I	13258.8	-11430
J5	PEG_RXP[7]	I	14173.2	-10515.6
K6	PEG_RXP[8]	I	13258.8	-9601.2
L5	PEG_RXP[9]	I	14173.2	-8686.8
A6	PEG_TXN[0]	O	13258.8	-17830.8
B5	PEG_TXN[1]	O	14173.2	-16916.4
L2	PEG_TXN[10]	O	16916.4	-8686.8
M3	PEG_TXN[11]	O	16002	-7772.4
N2	PEG_TXN[12]	O	16916.4	-6858
P3	PEG_TXN[13]	O	16002	-5943.6
R1	PEG_TXN[14]	O	17830.8	-5029.2
T3	PEG_TXN[15]	O	16002	-4114.8

Table 9-1. Ball Listing (Sheet 5 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
C4	PEG_TXN[2]	O	15087.6	-16002
D3	PEG_TXN[3]	O	16002	-15087.6
E2	PEG_TXN[4]	O	16916.4	-14173.2
F3	PEG_TXN[5]	O	16002	-13258.8
G2	PEG_TXN[6]	O	16916.4	-12344.4
H3	PEG_TXN[7]	O	16002	-11430
J2	PEG_TXN[8]	O	16916.4	-10515.6
K3	PEG_TXN[9]	O	16002	-9601.2
A5	PEG_TXP[0]	O	14173.2	-17830.8
B4	PEG_TXP[1]	O	15087.6	-16916.4
L1	PEG_TXP[10]	O	17830.8	-8686.8
M2	PEG_TXP[11]	O	16916.4	-7772.4
N1	PEG_TXP[12]	O	17830.8	-6858
P2	PEG_TXP[13]	O	16916.4	-5943.6
R2	PEG_TXP[14]	O	16916.4	-5029.2
T2	PEG_TXP[15]	O	16916.4	-4114.8
C3	PEG_TXP[2]	O	16002	-16002
D2	PEG_TXP[3]	O	16916.4	-15087.6
E1	PEG_TXP[4]	O	17830.8	-14173.2
F2	PEG_TXP[5]	O	16916.4	-13258.8
G1	PEG_TXP[6]	O	17830.8	-12344.4
H2	PEG_TXP[7]	O	16916.4	-11430
J1	PEG_TXP[8]	O	17830.8	-10515.6
K2	PEG_TXP[9]	O	16916.4	-9601.2
J8	RSVD_TP	N/A	11430	-10515.6
J7	RSVD_TP	N/A	12344.4	-10515.6
L8	IST_TRIG	N/A	11430	-8686.8
K8	RSVD_TP	N/A	11430	-9601.2
D8	PM_DOWN	O	11430	-15087.6
E8	PM_SYNC	I	11430	-14173.2
B10	PROC_PRDY#	O	9601.2	-16916.4
B9	PROC_PREQ#	I	10515.6	-16916.4
C39	PROCHOT#	I/O	-16916.4	-16002
E7	RESET#	I	12344.4	-14173.2
AB35	RSVD	N/A	-13258.8	1371.6
AB37	RSVD	N/A	-15087.6	1371.6
AB38	RSVD	N/A	-16002	1371.6
AC37	RSVD	N/A	-15087.6	2286
AJ22	RSVD	N/A	-1371.6	7772.4

Table 9-1. Ball Listing (Sheet 6 of 31)

Ball#	Ball Name	Default	X Location (μm)	Y Location (μm)
D15	RSVD	N/A	5029.2	-15087.6
K11	RSVD	N/A	8686.8	-9601.2
AB36	PROC_SELECT#	N/A	-14173.2	1371.6
AC38	SKTOCC#	N/A	-16002	2286
J15	RSVD	N/A	5029.2	-10515.6
AU9	RSVD	N/A	10515.6	15087.6
J14	RSVD	N/A	5943.6	-10515.6
AU10	RSVD	N/A	9601.2	15087.6
D11	THERMTRIP#	O	8686.8	-15087.6
A25	VCC	PWR	-4114.8	-17830.8
A26	VCC	PWR	-5029.2	-17830.8
A27	VCC	PWR	-5943.6	-17830.8
A28	VCC	PWR	-6858	-17830.8
A29	VCC	PWR	-7772.4	-17830.8
A30	VCC	PWR	-8686.8	-17830.8
AJ11	VCC	PWR	8686.8	7772.4
AJ12	VCC	PWR	7772.4	7772.4
AJ13	VCC	PWR	6858	7772.4
AJ14	VCC	PWR	5943.6	7772.4
AJ15	VCC	PWR	5029.2	7772.4
AJ16	VCC	PWR	4114.8	7772.4
AJ17	VCC	PWR	3200.4	7772.4
AJ18	VCC	PWR	2286	7772.4
AJ19	VCC	PWR	1371.6	7772.4
AJ20	VCC	PWR	457.2	7772.4
AJ21	VCC	PWR	-457.2	7772.4
AJ25	VCC	PWR	-4114.8	7772.4
AJ26	VCC	PWR	-5029.2	7772.4
AJ27	VCC	PWR	-5943.6	7772.4
AJ28	VCC	PWR	-6858	7772.4
AJ29	VCC	PWR	-7772.4	7772.4
AK21	VCC	PWR	-457.2	8686.8
B25	VCC	PWR	-4114.8	-16916.4
B27	VCC	PWR	-5943.6	-16916.4
B29	VCC	PWR	-7772.4	-16916.4
B31	VCC	PWR	-9601.2	-16916.4
B32	VCC	PWR	-10515.6	-16916.4
B33	VCC	PWR	-11430	-16916.4
B34	VCC	PWR	-12344.4	-16916.4

Table 9-1. Ball Listing (Sheet 7 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
B35	VCC	PWR	-13258.8	-16916.4
B36	VCC	PWR	-14173.2	-16916.4
B37	VCC	PWR	-15087.6	-16916.4
C25	VCC	PWR	-4114.8	-16002
C26	VCC	PWR	-5029.2	-16002
C27	VCC	PWR	-5943.6	-16002
C28	VCC	PWR	-6858	-16002
C29	VCC	PWR	-7772.4	-16002
C30	VCC	PWR	-8686.8	-16002
C32	VCC	PWR	-10515.6	-16002
C34	VCC	PWR	-12344.4	-16002
C36	VCC	PWR	-14173.2	-16002
D25	VCC	PWR	-4114.8	-15087.6
D27	VCC	PWR	-5943.6	-15087.6
D29	VCC	PWR	-7772.4	-15087.6
D31	VCC	PWR	-9601.2	-15087.6
D32	VCC	PWR	-10515.6	-15087.6
D33	VCC	PWR	-11430	-15087.6
D34	VCC	PWR	-12344.4	-15087.6
D35	VCC	PWR	-13258.8	-15087.6
D36	VCC	PWR	-14173.2	-15087.6
E24	VCC	PWR	-3200.4	-14173.2
E25	VCC	PWR	-4114.8	-14173.2
E26	VCC	PWR	-5029.2	-14173.2
E27	VCC	PWR	-5943.6	-14173.2
E28	VCC	PWR	-6858	-14173.2
E29	VCC	PWR	-7772.4	-14173.2
E30	VCC	PWR	-8686.8	-14173.2
E32	VCC	PWR	-10515.6	-14173.2
E34	VCC	PWR	-12344.4	-14173.2
E36	VCC	PWR	-14173.2	-14173.2
F23	VCC	PWR	-2286	-13258.8
F24	VCC	PWR	-3200.4	-13258.8
F25	VCC	PWR	-4114.8	-13258.8
F27	VCC	PWR	-5943.6	-13258.8
F29	VCC	PWR	-7772.4	-13258.8
F31	VCC	PWR	-9601.2	-13258.8
F32	VCC	PWR	-10515.6	-13258.8
F33	VCC	PWR	-11430	-13258.8

Table 9-1. Ball Listing (Sheet 8 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
F34	VCC	PWR	-12344.4	-13258.8
F35	VCC	PWR	-13258.8	-13258.8
F37	VCC	PWR	-15087.6	-13258.8
G23	VCC	PWR	-2286	-12344.4
G24	VCC	PWR	-3200.4	-12344.4
G25	VCC	PWR	-4114.8	-12344.4
G26	VCC	PWR	-5029.2	-12344.4
G27	VCC	PWR	-5943.6	-12344.4
G28	VCC	PWR	-6858	-12344.4
G29	VCC	PWR	-7772.4	-12344.4
G30	VCC	PWR	-8686.8	-12344.4
G32	VCC	PWR	-10515.6	-12344.4
G34	VCC	PWR	-12344.4	-12344.4
G35	VCC	PWR	-13258.8	-12344.4
H22	VCC	PWR	-1371.6	-11430
H23	VCC	PWR	-2286	-11430
H25	VCC	PWR	-4114.8	-11430
H27	VCC	PWR	-5943.6	-11430
H29	VCC	PWR	-7772.4	-11430
H31	VCC	PWR	-9601.2	-11430
H32	VCC	PWR	-10515.6	-11430
H33	VCC	PWR	-11430	-11430
H34	VCC	PWR	-12344.4	-11430
J21	VCC	PWR	-457.2	-10515.6
J22	VCC	PWR	-1371.6	-10515.6
J23	VCC	PWR	-2286	-10515.6
J24	VCC	PWR	-3200.4	-10515.6
J25	VCC	PWR	-4114.8	-10515.6
J26	VCC	PWR	-5029.2	-10515.6
J27	VCC	PWR	-5943.6	-10515.6
J28	VCC	PWR	-6858	-10515.6
J29	VCC	PWR	-7772.4	-10515.6
J30	VCC	PWR	-8686.8	-10515.6
J31	VCC	PWR	-9601.2	-10515.6
J33	VCC	PWR	-11430	-10515.6
J35	VCC	PWR	-13258.8	-10515.6
K16	VCC	PWR	4114.8	-9601.2
K18	VCC	PWR	2286	-9601.2
K20	VCC	PWR	457.2	-9601.2

Table 9-1. Ball Listing (Sheet 9 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
K21	VCC	PWR	-457.2	-9601.2
K23	VCC	PWR	-2286	-9601.2
K25	VCC	PWR	-4114.8	-9601.2
K27	VCC	PWR	-5943.6	-9601.2
K29	VCC	PWR	-7772.4	-9601.2
K31	VCC	PWR	-9601.2	-9601.2
K32	VCC	PWR	-10515.6	-9601.2
K34	VCC	PWR	-12344.4	-9601.2
L14	VCC	PWR	5943.6	-8686.8
L15	VCC	PWR	5029.2	-8686.8
L16	VCC	PWR	4114.8	-8686.8
L17	VCC	PWR	3200.4	-8686.8
L18	VCC	PWR	2286	-8686.8
L19	VCC	PWR	1371.6	-8686.8
L20	VCC	PWR	457.2	-8686.8
L21	VCC	PWR	-457.2	-8686.8
L22	VCC	PWR	-1371.6	-8686.8
L23	VCC	PWR	-2286	-8686.8
L24	VCC	PWR	-3200.4	-8686.8
L25	VCC	PWR	-4114.8	-8686.8
L26	VCC	PWR	-5029.2	-8686.8
L27	VCC	PWR	-5943.6	-8686.8
L28	VCC	PWR	-6858	-8686.8
L29	VCC	PWR	-7772.4	-8686.8
L30	VCC	PWR	-8686.8	-8686.8
L31	VCC	PWR	-9601.2	-8686.8
L33	VCC	PWR	-11430	-8686.8
M13	VCC	PWR	6858	-7772.4
M14	VCC	PWR	5943.6	-7772.4
M16	VCC	PWR	4114.8	-7772.4
M18	VCC	PWR	2286	-7772.4
M20	VCC	PWR	457.2	-7772.4
M22	VCC	PWR	-1371.6	-7772.4
M24	VCC	PWR	-3200.4	-7772.4
M26	VCC	PWR	-5029.2	-7772.4
M28	VCC	PWR	-6858	-7772.4
M30	VCC	PWR	-8686.8	-7772.4
M32	VCC	PWR	-10515.6	-7772.4
C38	VCC_SENSE	PWR_SENSE	-16002	-16002

Table 9-1. Ball Listing (Sheet 10 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
J17	RSVD	N/A	3200.4	-10515.6
B39	RSVD	N/A	-16916.4	-16916.4
C40	RSVD	N/A	-17830.8	-16002
J19	RSVD	N/A	1371.6	-10515.6
AT18	VDDQ	PWR	2286	14173.2
AT21	VDDQ	PWR	-457.2	14173.2
AU13	VDDQ	PWR	6858	15087.6
AU15	VDDQ	PWR	5029.2	15087.6
AU19	VDDQ	PWR	1371.6	15087.6
AU23	VDDQ	PWR	-2286	15087.6
AV11	VDDQ	PWR	8686.8	16002
AV17	VDDQ	PWR	3200.4	16002
AV21	VDDQ	PWR	-457.2	16002
AW10	VDDQ	PWR	9601.2	16916.4
AW14	VDDQ	PWR	5943.6	16916.4
AW25	VDDQ	PWR	-4114.8	16916.4
AY12	VDDQ	PWR	7772.4	17830.8
AY16	VDDQ	PWR	4114.8	17830.8
AY18	VDDQ	PWR	2286	17830.8
AY23	VDDQ	PWR	-2286	17830.8
V6	VCCST	PWR	13258.8	-2286
AA34	VCCGT	PWR	-12344.4	457.2
AA35	VCCGT	PWR	-13258.8	457.2
AA36	VCCGT	PWR	-14173.2	457.2
AA37	VCCGT	PWR	-15087.6	457.2
AA38	VCCGT	PWR	-16002	457.2
AB33	VCCGT	PWR	-11430	1371.6
AB34	VCCGT	PWR	-12344.4	1371.6
G36	VCCGT	PWR	-14173.2	-12344.4
G37	VCCGT	PWR	-15087.6	-12344.4
G38	VCCGT	PWR	-16002	-12344.4
G39	VCCGT	PWR	-16916.4	-12344.4
G40	VCCGT	PWR	-17830.8	-12344.4
H36	VCCGT	PWR	-14173.2	-11430
H38	VCCGT	PWR	-16002	-11430
H40	VCCGT	PWR	-17830.8	-11430
J36	VCCGT	PWR	-14173.2	-10515.6
J37	VCCGT	PWR	-15087.6	-10515.6
J38	VCCGT	PWR	-16002	-10515.6

Table 9-1. Ball Listing (Sheet 11 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
J39	VCCGT	PWR	-16916.4	-10515.6
J40	VCCGT	PWR	-17830.8	-10515.6
K36	VCCGT	PWR	-14173.2	-9601.2
K38	VCCGT	PWR	-16002	-9601.2
K40	VCCGT	PWR	-17830.8	-9601.2
L34	VCCGT	PWR	-12344.4	-8686.8
L35	VCCGT	PWR	-13258.8	-8686.8
L36	VCCGT	PWR	-14173.2	-8686.8
L37	VCCGT	PWR	-15087.6	-8686.8
L38	VCCGT	PWR	-16002	-8686.8
L39	VCCGT	PWR	-16916.4	-8686.8
L40	VCCGT	PWR	-17830.8	-8686.8
M33	VCCGT	PWR	-11430	-7772.4
M34	VCCGT	PWR	-12344.4	-7772.4
M36	VCCGT	PWR	-14173.2	-7772.4
M38	VCCGT	PWR	-16002	-7772.4
M40	VCCGT	PWR	-17830.8	-7772.4
N34	VCCGT	PWR	-12344.4	-6858
N35	VCCGT	PWR	-13258.8	-6858
N36	VCCGT	PWR	-14173.2	-6858
N37	VCCGT	PWR	-15087.6	-6858
N38	VCCGT	PWR	-16002	-6858
N39	VCCGT	PWR	-16916.4	-6858
N40	VCCGT	PWR	-17830.8	-6858
P33	VCCGT	PWR	-11430	-5943.6
P34	VCCGT	PWR	-12344.4	-5943.6
P36	VCCGT	PWR	-14173.2	-5943.6
P38	VCCGT	PWR	-16002	-5943.6
P40	VCCGT	PWR	-17830.8	-5943.6
R34	VCCGT	PWR	-12344.4	-5029.2
R35	VCCGT	PWR	-13258.8	-5029.2
R36	VCCGT	PWR	-14173.2	-5029.2
R37	VCCGT	PWR	-15087.6	-5029.2
R38	VCCGT	PWR	-16002	-5029.2
R39	VCCGT	PWR	-16916.4	-5029.2
R40	VCCGT	PWR	-17830.8	-5029.2
T33	VCCGT	PWR	-11430	-4114.8
T34	VCCGT	PWR	-12344.4	-4114.8
T36	VCCGT	PWR	-14173.2	-4114.8

Table 9-1. Ball Listing (Sheet 12 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
T38	VCCGT	PWR	-16002	-4114.8
T40	VCCGT	PWR	-17830.8	-4114.8
U34	VCCGT	PWR	-12344.4	-3200.4
U35	VCCGT	PWR	-13258.8	-3200.4
U36	VCCGT	PWR	-14173.2	-3200.4
U37	VCCGT	PWR	-15087.6	-3200.4
U38	VCCGT	PWR	-16002	-3200.4
U39	VCCGT	PWR	-16916.4	-3200.4
U40	VCCGT	PWR	-17830.8	-3200.4
V33	VCCGT	PWR	-11430	-2286
V34	VCCGT	PWR	-12344.4	-2286
V36	VCCGT	PWR	-14173.2	-2286
V38	VCCGT	PWR	-16002	-2286
V40	VCCGT	PWR	-17830.8	-2286
W34	VCCGT	PWR	-12344.4	-1371.6
W35	VCCGT	PWR	-13258.8	-1371.6
W36	VCCGT	PWR	-14173.2	-1371.6
W37	VCCGT	PWR	-15087.6	-1371.6
W38	VCCGT	PWR	-16002	-1371.6
Y33	VCCGT	PWR	-11430	-457.2
Y34	VCCGT	PWR	-12344.4	-457.2
Y36	VCCGT	PWR	-14173.2	-457.2
Y38	VCCGT	PWR	-16002	-457.2
F39	VCCGT_SENSE	PWR_SENSE	-16916.4	-13258.8
AJ23	VCCIO	PWR	-2286	7772.4
AK11	VCCIO	PWR	8686.8	8686.8
AK14	VCCIO	PWR	5943.6	8686.8
AK24	VCCIO	PWR	-3200.4	8686.8
M8	VCCIO	PWR	11430	-7772.4
P8	VCCIO	PWR	11430	-5943.6
T8	VCCIO	PWR	11430	-4114.8
U8	VCCIO	PWR	11430	-3200.4
W8	VCCIO	PWR	11430	-1371.6
AF4	VCCIO_SENSE	PWR_SENSE	15087.6	5029.2
AA6	VCCSA	PWR	13258.8	457.2
AA7	VCCSA	PWR	12344.4	457.2
AB6	VCCSA	PWR	13258.8	1371.6
AB7	VCCSA	PWR	12344.4	1371.6
AB8	VCCSA	PWR	11430	1371.6

Table 9-1. Ball Listing (Sheet 13 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AC7	VCCSA	PWR	12344.4	2286
AC8	VCCSA	PWR	11430	2286
N7	VCCSA	PWR	12344.4	-6858
P7	VCCSA	PWR	12344.4	-5943.6
R7	VCCSA	PWR	12344.4	-5029.2
T7	VCCSA	PWR	12344.4	-4114.8
U7	VCCSA	PWR	12344.4	-3200.4
V7	VCCSA	PWR	12344.4	-2286
W7	VCCSA	PWR	12344.4	-1371.6
Y6	VCCSA	PWR	13258.8	-457.2
Y7	VCCSA	PWR	12344.4	-457.2
Y8	VCCSA	PWR	11430	-457.2
AD5	VCCSA_SENSE	PWR_SENSE	14173.2	3200.4
V4	VCCPLL	PWR	15087.6	-2286
AJ9	VCCPLL_OC	PWR	10515.6	7772.4
V5	VCCST	PWR	14173.2	-2286
U2	VCCST_PWRGD	I	16916.4	-3200.4
E39	VIDALERT#	I	-16916.4	-14173.2
E38	VIDSCK	O	-16002	-14173.2
E40	VIDSOUT	I/O	-17830.8	-14173.2
A11	VSS	GND	8686.8	-17830.8
A13	VSS	GND	6858	-17830.8
A15	VSS	GND	5029.2	-17830.8
A17	VSS	GND	3200.4	-17830.8
A24	VSS	GND	-3200.4	-17830.8
A7	VSS	GND	12344.4	-17830.8
AA3	VSS	GND	16002	457.2
AA33	VSS	GND	-11430	457.2
AA8	VSS	GND	11430	457.2
AB39	VSS	GND	-16916.4	1371.6
AB5	VSS	GND	14173.2	1371.6
AC3	VSS	GND	16002	2286
AC33	VSS	GND	-11430	2286
AC34	VSS	GND	-12344.4	2286
AC35	VSS	GND	-13258.8	2286
AC6	VSS	GND	13258.8	2286
AD1	VSS	GND	17830.8	3200.4
AD33	VSS	GND	-11430	3200.4
AD36	VSS	GND	-14173.2	3200.4

Table 9-1. Ball Listing (Sheet 14 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AD37	VSS	GND	-15087.6	3200.4
AD38	VSS	GND	-16002	3200.4
AD39	VSS	GND	-16916.4	3200.4
AD4	VSS	GND	15087.6	3200.4
AD40	VSS	GND	-17830.8	3200.4
AD6	VSS	GND	13258.8	3200.4
AD7	VSS	GND	12344.4	3200.4
AD8	VSS	GND	11430	3200.4
AE3	VSS	GND	16002	4114.8
AE33	VSS	GND	-11430	4114.8
AE36	VSS	GND	-14173.2	4114.8
AE5	VSS	GND	14173.2	4114.8
AE8	VSS	GND	11430	4114.8
AF1	VSS	GND	17830.8	5029.2
AF33	VSS	GND	-11430	5029.2
AF36	VSS	GND	-14173.2	5029.2
AF37	VSS	GND	-15087.6	5029.2
AF40	VSS	GND	-17830.8	5029.2
AF5	VSS	GND	14173.2	5029.2
AF8	VSS	GND	11430	5029.2
AG1	VSS	GND	17830.8	5943.6
AG2	VSS	GND	16916.4	5943.6
AG3	VSS	GND	16002	5943.6
AG33	VSS	GND	-11430	5943.6
AG36	VSS	GND	-14173.2	5943.6
AG4	VSS	GND	15087.6	5943.6
AG5	VSS	GND	14173.2	5943.6
AG8	VSS	GND	11430	5943.6
AH33	VSS	GND	-11430	6858
AH36	VSS	GND	-14173.2	6858
AH37	VSS	GND	-15087.6	6858
AH38	VSS	GND	-16002	6858
AH39	VSS	GND	-16916.4	6858
AH40	VSS	GND	-17830.8	6858
AH5	VSS	GND	14173.2	6858
AH8	VSS	GND	11430	6858
AJ1	VSS	GND	17830.8	7772.4
AJ24	VSS	GND	-3200.4	7772.4
AJ30	VSS	GND	-8686.8	7772.4

Table 9-1. Ball Listing (Sheet 15 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AJ31	VSS	GND	-9601.2	7772.4
AJ32	VSS	GND	-10515.6	7772.4
AJ33	VSS	GND	-11430	7772.4
AJ34	VSS	GND	-12344.4	7772.4
AJ35	VSS	GND	-13258.8	7772.4
AJ36	VSS	GND	-14173.2	7772.4
AJ4	VSS	GND	15087.6	7772.4
AJ5	VSS	GND	14173.2	7772.4
AJ8	VSS	GND	11430	7772.4
AK10	VSS	GND	9601.2	8686.8
AK12	VSS	GND	7772.4	8686.8
AK13	VSS	GND	6858	8686.8
AK15	VSS	GND	5029.2	8686.8
AK16	VSS	GND	4114.8	8686.8
AK17	VSS	GND	3200.4	8686.8
AK18	VSS	GND	2286	8686.8
AK19	VSS	GND	1371.6	8686.8
AK20	VSS	GND	457.2	8686.8
AK22	VSS	GND	-1371.6	8686.8
AK23	VSS	GND	-2286	8686.8
AK25	VSS	GND	-4114.8	8686.8
AK26	VSS	GND	-5029.2	8686.8
AK27	VSS	GND	-5943.6	8686.8
AK28	VSS	GND	-6858	8686.8
AK29	VSS	GND	-7772.4	8686.8
AK30	VSS	GND	-8686.8	8686.8
AK36	VSS	GND	-14173.2	8686.8
AK37	VSS	GND	-15087.6	8686.8
AK40	VSS	GND	-17830.8	8686.8
AK5	VSS	GND	14173.2	8686.8
AK6	VSS	GND	13258.8	8686.8
AK7	VSS	GND	12344.4	8686.8
AK8	VSS	GND	11430	8686.8
AK9	VSS	GND	10515.6	8686.8
AL1	VSS	GND	17830.8	9601.2
AL11	VSS	GND	8686.8	9601.2
AL14	VSS	GND	5943.6	9601.2
AL2	VSS	GND	16916.4	9601.2
AL21	VSS	GND	-457.2	9601.2

Table 9-1. Ball Listing (Sheet 16 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AL24	VSS	GND	-3200.4	9601.2
AL27	VSS	GND	-5943.6	9601.2
AL3	VSS	GND	16002	9601.2
AL30	VSS	GND	-8686.8	9601.2
AL36	VSS	GND	-14173.2	9601.2
AL4	VSS	GND	15087.6	9601.2
AL5	VSS	GND	14173.2	9601.2
AM11	VSS	GND	8686.8	10515.6
AM14	VSS	GND	5943.6	10515.6
AM17	VSS	GND	3200.4	10515.6
AM19	VSS	GND	1371.6	10515.6
AM24	VSS	GND	-3200.4	10515.6
AM27	VSS	GND	-5943.6	10515.6
AM30	VSS	GND	-8686.8	10515.6
AM31	VSS	GND	-9601.2	10515.6
AM32	VSS	GND	-10515.6	10515.6
AM33	VSS	GND	-11430	10515.6
AM34	VSS	GND	-12344.4	10515.6
AM35	VSS	GND	-13258.8	10515.6
AM36	VSS	GND	-14173.2	10515.6
AM37	VSS	GND	-15087.6	10515.6
AM38	VSS	GND	-16002	10515.6
AM39	VSS	GND	-16916.4	10515.6
AM40	VSS	GND	-17830.8	10515.6
AM5	VSS	GND	14173.2	10515.6
AN1	VSS	GND	17830.8	11430
AN10	VSS	GND	9601.2	11430
AN11	VSS	GND	8686.8	11430
AN14	VSS	GND	5943.6	11430
AN16	VSS	GND	4114.8	11430
AN19	VSS	GND	1371.6	11430
AN22	VSS	GND	-1371.6	11430
AN23	VSS	GND	-2286	11430
AN24	VSS	GND	-3200.4	11430
AN27	VSS	GND	-5943.6	11430
AN30	VSS	GND	-8686.8	11430
AN36	VSS	GND	-14173.2	11430
AN4	VSS	GND	15087.6	11430
AN5	VSS	GND	14173.2	11430

Table 9-1. Ball Listing (Sheet 17 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AN6	VSS	GND	13258.8	11430
AN7	VSS	GND	12344.4	11430
AN8	VSS	GND	11430	11430
AN9	VSS	GND	10515.6	11430
AP11	VSS	GND	8686.8	12344.4
AP14	VSS	GND	5943.6	12344.4
AP24	VSS	GND	-3200.4	12344.4
AP27	VSS	GND	-5943.6	12344.4
AP30	VSS	GND	-8686.8	12344.4
AP36	VSS	GND	-14173.2	12344.4
AP37	VSS	GND	-15087.6	12344.4
AP40	VSS	GND	-17830.8	12344.4
AP5	VSS	GND	14173.2	12344.4
AR1	VSS	GND	17830.8	13258.8
AR11	VSS	GND	8686.8	13258.8
AR14	VSS	GND	5943.6	13258.8
AR16	VSS	GND	4114.8	13258.8
AR17	VSS	GND	3200.4	13258.8
AR18	VSS	GND	2286	13258.8
AR19	VSS	GND	1371.6	13258.8
AR2	VSS	GND	16916.4	13258.8
AR20	VSS	GND	457.2	13258.8
AR21	VSS	GND	-457.2	13258.8
AR22	VSS	GND	-1371.6	13258.8
AR23	VSS	GND	-2286	13258.8
AR24	VSS	GND	-3200.4	13258.8
AR27	VSS	GND	-5943.6	13258.8
AR3	VSS	GND	16002	13258.8
AR30	VSS	GND	-8686.8	13258.8
AR31	VSS	GND	-9601.2	13258.8
AR32	VSS	GND	-10515.6	13258.8
AR33	VSS	GND	-11430	13258.8
AR34	VSS	GND	-12344.4	13258.8
AR35	VSS	GND	-13258.8	13258.8
AR36	VSS	GND	-14173.2	13258.8
AR4	VSS	GND	15087.6	13258.8
AR5	VSS	GND	14173.2	13258.8
AT10	VSS	GND	9601.2	14173.2
AT11	VSS	GND	8686.8	14173.2

Table 9-1. Ball Listing (Sheet 18 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AT12	VSS	GND	7772.4	14173.2
AT13	VSS	GND	6858	14173.2
AT14	VSS	GND	5943.6	14173.2
AT15	VSS	GND	5029.2	14173.2
AT17	VSS	GND	3200.4	14173.2
AT24	VSS	GND	-3200.4	14173.2
AT25	VSS	GND	-4114.8	14173.2
AT26	VSS	GND	-5029.2	14173.2
AT27	VSS	GND	-5943.6	14173.2
AT28	VSS	GND	-6858	14173.2
AT29	VSS	GND	-7772.4	14173.2
AT30	VSS	GND	-8686.8	14173.2
AT31	VSS	GND	-9601.2	14173.2
AT32	VSS	GND	-10515.6	14173.2
AT34	VSS	GND	-12344.4	14173.2
AT36	VSS	GND	-14173.2	14173.2
AT37	VSS	GND	-15087.6	14173.2
AT38	VSS	GND	-16002	14173.2
AT39	VSS	GND	-16916.4	14173.2
AT40	VSS	GND	-17830.8	14173.2
AT5	VSS	GND	14173.2	14173.2
AT6	VSS	GND	13258.8	14173.2
AT7	VSS	GND	12344.4	14173.2
AT8	VSS	GND	11430	14173.2
AT9	VSS	GND	10515.6	14173.2
AU1	VSS	GND	17830.8	15087.6
AU25	VSS	GND	-4114.8	15087.6
AU30	VSS	GND	-8686.8	15087.6
AU34	VSS	GND	-12344.4	15087.6
AU39	VSS	GND	-16916.4	15087.6
AU4	VSS	GND	15087.6	15087.6
AU5	VSS	GND	14173.2	15087.6
AU7	VSS	GND	12344.4	15087.6
AV2	VSS	GND	16916.4	16002
AV26	VSS	GND	-5029.2	16002
AV28	VSS	GND	-6858	16002
AV30	VSS	GND	-8686.8	16002
AV34	VSS	GND	-12344.4	16002
AV38	VSS	GND	-16002	16002

Table 9-1. Ball Listing (Sheet 19 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AV5	VSS	GND	14173.2	16002
AV9	VSS	GND	10515.6	16002
AW3	VSS	GND	16002	16916.4
AW30	VSS	GND	-8686.8	16916.4
AW32	VSS	GND	-10515.6	16916.4
AW34	VSS	GND	-12344.4	16916.4
AW36	VSS	GND	-14173.2	16916.4
AW5	VSS	GND	14173.2	16916.4
AW9	VSS	GND	10515.6	16916.4
AY27	VSS	GND	-5943.6	17830.8
AY30	VSS	GND	-8686.8	17830.8
AY5	VSS	GND	14173.2	17830.8
AY7	VSS	GND	12344.4	17830.8
AY9	VSS	GND	10515.6	17830.8
B24	VSS	GND	-3200.4	-16916.4
B26	VSS	GND	-5029.2	-16916.4
B28	VSS	GND	-6858	-16916.4
B30	VSS	GND	-8686.8	-16916.4
B6	VSS	GND	13258.8	-16916.4
C10	VSS	GND	9601.2	-16002
C12	VSS	GND	7772.4	-16002
C14	VSS	GND	5943.6	-16002
C16	VSS	GND	4114.8	-16002
C18	VSS	GND	2286	-16002
C20	VSS	GND	457.2	-16002
C22	VSS	GND	-1371.6	-16002
C24	VSS	GND	-3200.4	-16002
C31	VSS	GND	-9601.2	-16002
C33	VSS	GND	-11430	-16002
C35	VSS	GND	-13258.8	-16002
C37	VSS	GND	-15087.6	-16002
C5	VSS	GND	14173.2	-16002
C8	VSS	GND	11430	-16002
D24	VSS	GND	-3200.4	-15087.6
D26	VSS	GND	-5029.2	-15087.6
D28	VSS	GND	-6858	-15087.6
D30	VSS	GND	-8686.8	-15087.6
D37	VSS	GND	-15087.6	-15087.6
D39	VSS	GND	-16916.4	-15087.6

Table 9-1. Ball Listing (Sheet 20 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
D4	VSS	GND	15087.6	-15087.6
D7	VSS	GND	12344.4	-15087.6
E11	VSS	GND	8686.8	-14173.2
E13	VSS	GND	6858	-14173.2
E15	VSS	GND	5029.2	-14173.2
E17	VSS	GND	3200.4	-14173.2
E19	VSS	GND	1371.6	-14173.2
E21	VSS	GND	-457.2	-14173.2
E23	VSS	GND	-2286	-14173.2
E3	VSS	GND	16002	-14173.2
E31	VSS	GND	-9601.2	-14173.2
E33	VSS	GND	-11430	-14173.2
E35	VSS	GND	-13258.8	-14173.2
E37	VSS	GND	-15087.6	-14173.2
E6	VSS	GND	13258.8	-14173.2
E9	VSS	GND	10515.6	-14173.2
F1	VSS	GND	17830.8	-13258.8
F10	VSS	GND	9601.2	-13258.8
F22	VSS	GND	-1371.6	-13258.8
F26	VSS	GND	-5029.2	-13258.8
F28	VSS	GND	-6858	-13258.8
F30	VSS	GND	-8686.8	-13258.8
F36	VSS	GND	-14173.2	-13258.8
F4	VSS	GND	15087.6	-13258.8
F40	VSS	GND	-17830.8	-13258.8
F7	VSS	GND	12344.4	-13258.8
G11	VSS	GND	8686.8	-12344.4
G13	VSS	GND	6858	-12344.4
G15	VSS	GND	5029.2	-12344.4
G17	VSS	GND	3200.4	-12344.4
G19	VSS	GND	1371.6	-12344.4
G22	VSS	GND	-1371.6	-12344.4
G3	VSS	GND	16002	-12344.4
G31	VSS	GND	-9601.2	-12344.4
G33	VSS	GND	-11430	-12344.4
G6	VSS	GND	13258.8	-12344.4
H1	VSS	GND	17830.8	-11430
H11	VSS	GND	8686.8	-11430
H12	VSS	GND	7772.4	-11430

Table 9-1. Ball Listing (Sheet 21 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
H21	VSS	GND	-457.2	-11430
H24	VSS	GND	-3200.4	-11430
H26	VSS	GND	-5029.2	-11430
H28	VSS	GND	-6858	-11430
H30	VSS	GND	-8686.8	-11430
H35	VSS	GND	-13258.8	-11430
H37	VSS	GND	-15087.6	-11430
H39	VSS	GND	-16916.4	-11430
H4	VSS	GND	15087.6	-11430
H7	VSS	GND	12344.4	-11430
H9	VSS	GND	10515.6	-11430
J10	VSS	GND	9601.2	-10515.6
J12	VSS	GND	7772.4	-10515.6
J16	VSS	GND	4114.8	-10515.6
J18	VSS	GND	2286	-10515.6
J20	VSS	GND	457.2	-10515.6
J3	VSS	GND	16002	-10515.6
J32	VSS	GND	-10515.6	-10515.6
J34	VSS	GND	-12344.4	-10515.6
J6	VSS	GND	13258.8	-10515.6
K1	VSS	GND	17830.8	-9601.2
K14	VSS	GND	5943.6	-9601.2
K15	VSS	GND	5029.2	-9601.2
K17	VSS	GND	3200.4	-9601.2
K19	VSS	GND	1371.6	-9601.2
K22	VSS	GND	-1371.6	-9601.2
K24	VSS	GND	-3200.4	-9601.2
K26	VSS	GND	-5029.2	-9601.2
K28	VSS	GND	-6858	-9601.2
K30	VSS	GND	-8686.8	-9601.2
K33	VSS	GND	-11430	-9601.2
K35	VSS	GND	-13258.8	-9601.2
K37	VSS	GND	-15087.6	-9601.2
K39	VSS	GND	-16916.4	-9601.2
K4	VSS	GND	15087.6	-9601.2
K7	VSS	GND	12344.4	-9601.2
L11	VSS	GND	8686.8	-8686.8
L13	VSS	GND	6858	-8686.8
L3	VSS	GND	16002	-8686.8

Table 9-1. Ball Listing (Sheet 22 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
L32	VSS	GND	-10515.6	-8686.8
L6	VSS	GND	13258.8	-8686.8
L9	VSS	GND	10515.6	-8686.8
M1	VSS	GND	17830.8	-7772.4
M10	VSS	GND	9601.2	-7772.4
M12	VSS	GND	7772.4	-7772.4
M15	VSS	GND	5029.2	-7772.4
M17	VSS	GND	3200.4	-7772.4
M19	VSS	GND	1371.6	-7772.4
M21	VSS	GND	-457.2	-7772.4
M23	VSS	GND	-2286	-7772.4
M25	VSS	GND	-4114.8	-7772.4
M27	VSS	GND	-5943.6	-7772.4
M29	VSS	GND	-7772.4	-7772.4
M35	VSS	GND	-13258.8	-7772.4
M37	VSS	GND	-15087.6	-7772.4
M39	VSS	GND	-16916.4	-7772.4
M4	VSS	GND	15087.6	-7772.4
M7	VSS	GND	12344.4	-7772.4
N3	VSS	GND	16002	-6858
N33	VSS	GND	-11430	-6858
N6	VSS	GND	13258.8	-6858
N8	VSS	GND	11430	-6858
P1	VSS	GND	17830.8	-5943.6
P35	VSS	GND	-13258.8	-5943.6
P37	VSS	GND	-15087.6	-5943.6
P39	VSS	GND	-16916.4	-5943.6
P4	VSS	GND	15087.6	-5943.6
R3	VSS	GND	16002	-5029.2
R33	VSS	GND	-11430	-5029.2
R6	VSS	GND	13258.8	-5029.2
R8	VSS	GND	11430	-5029.2
T1	VSS	GND	17830.8	-4114.8
T35	VSS	GND	-13258.8	-4114.8
T37	VSS	GND	-15087.6	-4114.8
T39	VSS	GND	-16916.4	-4114.8
T4	VSS	GND	15087.6	-4114.8
U3	VSS	GND	16002	-3200.4
U33	VSS	GND	-11430	-3200.4

Table 9-1. Ball Listing (Sheet 23 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
U6	VSS	GND	13258.8	-3200.4
V1	VSS	GND	17830.8	-2286
V35	VSS	GND	-13258.8	-2286
V37	VSS	GND	-15087.6	-2286
V39	VSS	GND	-16916.4	-2286
V8	VSS	GND	11430	-2286
W3	VSS	GND	16002	-1371.6
W33	VSS	GND	-11430	-1371.6
W6	VSS	GND	13258.8	-1371.6
Y35	VSS	GND	-13258.8	-457.2
Y37	VSS	GND	-15087.6	-457.2
Y5	VSS	GND	14173.2	-457.2
A4	VSS	GND	15087.6	-17830.8
AU40	VSS	GND	-17830.8	15087.6
AV39	VSS	GND	-16916.4	16002
AW38	VSS	GND	-16002	16916.4
B38	VSS	GND	-16002	-16916.4
C2	VSS	GND	16916.4	-16002
D40	VSS	GND	-17830.8	-15087.6
AE4	VSS_SA_SENSE	GND_SENSE	15087.6	4114.8
D38	VSS_SENSE	GND_SENSE	-16002	-15087.6
F38	VSSGT_SENSE	GND_SENSE	-16002	-13258.8
	DQ,DQS Ball Name			
	DDR4(IL) / DDR4(NIL)			
AE38	DDR0_DQ[0] / DDR0_DQ[0]	I/O	-16002	4114.8
AE37	DDR0_DQ[1] / DDR0_DQ[1]	I/O	-15087.6	4114.8
AG38	DDR0_DQ[2] / DDR0_DQ[2]	I/O	-16002	5943.6
AG37	DDR0_DQ[3] / DDR0_DQ[3]	I/O	-15087.6	5943.6
AE39	DDR0_DQ[4] / DDR0_DQ[4]	I/O	-16916.4	4114.8
AE40	DDR0_DQ[5] / DDR0_DQ[5]	I/O	-17830.8	4114.8
AG39	DDR0_DQ[6] / DDR0_DQ[6]	I/O	-16916.4	5943.6
AG40	DDR0_DQ[7] / DDR0_DQ[7]	I/O	-17830.8	5943.6
AJ38	DDR0_DQ[8] / DDR0_DQ[8]	I/O	-16002	7772.4
AJ37	DDR0_DQ[9] / DDR0_DQ[9]	I/O	-15087.6	7772.4
AL38	DDR0_DQ[10] / DDR0_DQ[10]	I/O	-16002	9601.2
AL37	DDR0_DQ[11] / DDR0_DQ[11]	I/O	-15087.6	9601.2
AJ40	DDR0_DQ[12] / DDR0_DQ[12]	I/O	-17830.8	7772.4
AJ39	DDR0_DQ[13] / DDR0_DQ[13]	I/O	-16916.4	7772.4
AL39	DDR0_DQ[14] / DDR0_DQ[14]	I/O	-16916.4	9601.2

Table 9-1. Ball Listing (Sheet 24 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AL40	DDR0_DQ[15] / DDR0_DQ[15]	I/O	-17830.8	9601.2
AN38	DDR0_DQ[16] / DDR0_DQ[32]	I/O	-16002	11430
AN40	DDR0_DQ[17] / DDR0_DQ[33]	I/O	-17830.8	11430
AR38	DDR0_DQ[18] / DDR0_DQ[34]	I/O	-16002	13258.8
AR37	DDR0_DQ[19] / DDR0_DQ[35]	I/O	-15087.6	13258.8
AN39	DDR0_DQ[20] / DDR0_DQ[36]	I/O	-16916.4	11430
AN37	DDR0_DQ[21] / DDR0_DQ[37]	I/O	-15087.6	11430
AR39	DDR0_DQ[22] / DDR0_DQ[38]	I/O	-16916.4	13258.8
AR40	DDR0_DQ[23] / DDR0_DQ[39]	I/O	-17830.8	13258.8
AW37	DDR0_DQ[24] / DDR0_DQ[40]	I/O	-15087.6	16916.4
AU38	DDR0_DQ[25] / DDR0_DQ[41]	I/O	-16002	15087.6
AV35	DDR0_DQ[26] / DDR0_DQ[42]	I/O	-13258.8	16002
AW35	DDR0_DQ[27] / DDR0_DQ[43]	I/O	-13258.8	16916.4
AU37	DDR0_DQ[28] / DDR0_DQ[44]	I/O	-15087.6	15087.6
AV37	DDR0_DQ[29] / DDR0_DQ[45]	I/O	-15087.6	16002
AT35	DDR0_DQ[30] / DDR0_DQ[46]	I/O	-13258.8	14173.2
AU35	DDR0_DQ[31] / DDR0_DQ[47]	I/O	-13258.8	15087.6
AY8	DDR0_DQ[32] / DDR1_DQ[0]	I/O	11430	17830.8
AW8	DDR0_DQ[33] / DDR1_DQ[1]	I/O	11430	16916.4
AV6	DDR0_DQ[34] / DDR1_DQ[2]	I/O	13258.8	16002
AU6	DDR0_DQ[35] / DDR1_DQ[3]	I/O	13258.8	15087.6
AU8	DDR0_DQ[36] / DDR1_DQ[4]	I/O	11430	15087.6
AV8	DDR0_DQ[37] / DDR1_DQ[5]	I/O	11430	16002
AW6	DDR0_DQ[38] / DDR1_DQ[6]	I/O	13258.8	16916.4
AY6	DDR0_DQ[39] / DDR1_DQ[7]	I/O	13258.8	17830.8
AY4	DDR0_DQ[40] / DDR1_DQ[8]	I/O	15087.6	17830.8
AV4	DDR0_DQ[41] / DDR1_DQ[9]	I/O	15087.6	16002
AT1	DDR0_DQ[42] / DDR1_DQ[10]	I/O	17830.8	14173.2
AT2	DDR0_DQ[43] / DDR1_DQ[11]	I/O	16916.4	14173.2
AV3	DDR0_DQ[44] / DDR1_DQ[12]	I/O	16002	16002
AW4	DDR0_DQ[45] / DDR1_DQ[13]	I/O	15087.6	16916.4
AT4	DDR0_DQ[46] / DDR1_DQ[14]	I/O	15087.6	14173.2
AT3	DDR0_DQ[47] / DDR1_DQ[15]	I/O	16002	14173.2
AP2	DDR0_DQ[48] / DDR1_DQ[32]	I/O	16916.4	12344.4
AM4	DDR0_DQ[49] / DDR1_DQ[33]	I/O	15087.6	10515.6
AP3	DDR0_DQ[50] / DDR1_DQ[34]	I/O	16002	12344.4
AM3	DDR0_DQ[51] / DDR1_DQ[35]	I/O	16002	10515.6
AP4	DDR0_DQ[52] / DDR1_DQ[36]	I/O	15087.6	12344.4
AM2	DDR0_DQ[53] / DDR1_DQ[37]	I/O	16916.4	10515.6

Table 9-1. Ball Listing (Sheet 25 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AP1	DDR0_DQ[54] / DDR1_DQ[38]	I/O	17830.8	12344.4
AM1	DDR0_DQ[55] / DDR1_DQ[39]	I/O	17830.8	10515.6
AK3	DDR0_DQ[56] / DDR1_DQ[40]	I/O	16002	8686.8
AH1	DDR0_DQ[57] / DDR1_DQ[41]	I/O	17830.8	6858
AK4	DDR0_DQ[58] / DDR1_DQ[42]	I/O	15087.6	8686.8
AH2	DDR0_DQ[59] / DDR1_DQ[43]	I/O	16916.4	6858
AH4	DDR0_DQ[60] / DDR1_DQ[44]	I/O	15087.6	6858
AK2	DDR0_DQ[61] / DDR1_DQ[45]	I/O	16916.4	8686.8
AH3	DDR0_DQ[62] / DDR1_DQ[46]	I/O	16002	6858
AK1	DDR0_DQ[63] / DDR1_DQ[47]	I/O	17830.8	8686.8
AD34	DDR1_DQ[0] / DDR0_DQ[16]	I/O	-12344.4	3200.4
AD35	DDR1_DQ[1] / DDR0_DQ[17]	I/O	-13258.8	3200.4
AG35	DDR1_DQ[2] / DDR0_DQ[18]	I/O	-13258.8	5943.6
AH35	DDR1_DQ[3] / DDR0_DQ[19]	I/O	-13258.8	6858
AE35	DDR1_DQ[4] / DDR0_DQ[20]	I/O	-13258.8	4114.8
AE34	DDR1_DQ[5] / DDR0_DQ[21]	I/O	-12344.4	4114.8
AG34	DDR1_DQ[6] / DDR0_DQ[22]	I/O	-12344.4	5943.6
AH34	DDR1_DQ[7] / DDR0_DQ[23]	I/O	-12344.4	6858
AK35	DDR1_DQ[8] / DDR0_DQ[24]	I/O	-13258.8	8686.8
AL35	DDR1_DQ[9] / DDR0_DQ[25]	I/O	-13258.8	9601.2
AK32	DDR1_DQ[10] / DDR0_DQ[26]	I/O	-10515.6	8686.8
AL32	DDR1_DQ[11] / DDR0_DQ[27]	I/O	-10515.6	9601.2
AK34	DDR1_DQ[12] / DDR0_DQ[28]	I/O	-12344.4	8686.8
AL34	DDR1_DQ[13] / DDR0_DQ[29]	I/O	-12344.4	9601.2
AK31	DDR1_DQ[14] / DDR0_DQ[30]	I/O	-9601.2	8686.8
AL31	DDR1_DQ[15] / DDR0_DQ[31]	I/O	-9601.2	9601.2
AP35	DDR1_DQ[16] / DDR0_DQ[48]	I/O	-13258.8	12344.4
AN35	DDR1_DQ[17] / DDR0_DQ[49]	I/O	-13258.8	11430
AN32	DDR1_DQ[18] / DDR0_DQ[50]	I/O	-10515.6	11430
AP32	DDR1_DQ[19] / DDR0_DQ[51]	I/O	-10515.6	12344.4
AN34	DDR1_DQ[20] / DDR0_DQ[52]	I/O	-12344.4	11430
AP34	DDR1_DQ[21] / DDR0_DQ[53]	I/O	-12344.4	12344.4
AN31	DDR1_DQ[22] / DDR0_DQ[54]	I/O	-9601.2	11430
AP31	DDR1_DQ[23] / DDR0_DQ[55]	I/O	-9601.2	12344.4
AL29	DDR1_DQ[24] / DDR0_DQ[56]	I/O	-7772.4	9601.2
AM29	DDR1_DQ[25] / DDR0_DQ[57]	I/O	-7772.4	10515.6
AP29	DDR1_DQ[26] / DDR0_DQ[58]	I/O	-7772.4	12344.4
AR29	DDR1_DQ[27] / DDR0_DQ[59]	I/O	-7772.4	13258.8
AM28	DDR1_DQ[28] / DDR0_DQ[60]	I/O	-6858	10515.6

Table 9-1. Ball Listing (Sheet 26 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AL28	DDR1_DQ[29] / DDR0_DQ[61]	I/O	-6858	9601.2
AR28	DDR1_DQ[30] / DDR0_DQ[62]	I/O	-6858	13258.8
AP28	DDR1_DQ[31] / DDR0_DQ[63]	I/O	-6858	12344.4
AR12	DDR1_DQ[32] / DDR1_DQ[16]	I/O	7772.4	13258.8
AP12	DDR1_DQ[33] / DDR1_DQ[17]	I/O	7772.4	12344.4
AM13	DDR1_DQ[34] / DDR1_DQ[18]	I/O	6858	10515.6
AL13	DDR1_DQ[35] / DDR1_DQ[19]	I/O	6858	9601.2
AR13	DDR1_DQ[36] / DDR1_DQ[20]	I/O	6858	13258.8
AP13	DDR1_DQ[37] / DDR1_DQ[21]	I/O	6858	12344.4
AM12	DDR1_DQ[38] / DDR1_DQ[22]	I/O	7772.4	10515.6
AL12	DDR1_DQ[39] / DDR1_DQ[23]	I/O	7772.4	9601.2
AP10	DDR1_DQ[40] / DDR1_DQ[24]	I/O	9601.2	12344.4
AR10	DDR1_DQ[41] / DDR1_DQ[25]	I/O	9601.2	13258.8
AR7	DDR1_DQ[42] / DDR1_DQ[26]	I/O	12344.4	13258.8
AP7	DDR1_DQ[43] / DDR1_DQ[27]	I/O	12344.4	12344.4
AR9	DDR1_DQ[44] / DDR1_DQ[28]	I/O	10515.6	13258.8
AP9	DDR1_DQ[45] / DDR1_DQ[29]	I/O	10515.6	12344.4
AR6	DDR1_DQ[46] / DDR1_DQ[30]	I/O	13258.8	13258.8
AP6	DDR1_DQ[47] / DDR1_DQ[31]	I/O	13258.8	12344.4
AM10	DDR1_DQ[48] / DDR1_DQ[48]	I/O	9601.2	10515.6
AL10	DDR1_DQ[49] / DDR1_DQ[49]	I/O	9601.2	9601.2
AM7	DDR1_DQ[50] / DDR1_DQ[50]	I/O	12344.4	10515.6
AL7	DDR1_DQ[51] / DDR1_DQ[51]	I/O	12344.4	9601.2
AM9	DDR1_DQ[52] / DDR1_DQ[52]	I/O	10515.6	10515.6
AL9	DDR1_DQ[53] / DDR1_DQ[53]	I/O	10515.6	9601.2
AM6	DDR1_DQ[54] / DDR1_DQ[54]	I/O	13258.8	10515.6
AL6	DDR1_DQ[55] / DDR1_DQ[55]	I/O	13258.8	9601.2
AJ6	DDR1_DQ[56] / DDR1_DQ[56]	I/O	13258.8	7772.4
AJ7	DDR1_DQ[57] / DDR1_DQ[57]	I/O	12344.4	7772.4
AE6	DDR1_DQ[58] / DDR1_DQ[58]	I/O	13258.8	4114.8
AF7	DDR1_DQ[59] / DDR1_DQ[59]	I/O	12344.4	5029.2
AH7	DDR1_DQ[60] / DDR1_DQ[60]	I/O	12344.4	6858
AH6	DDR1_DQ[61] / DDR1_DQ[61]	I/O	13258.8	6858
AE7	DDR1_DQ[62] / DDR1_DQ[62]	I/O	12344.4	4114.8
AF6	DDR1_DQ[63] / DDR1_DQ[63]	I/O	13258.8	5029.2
AF39	DDR0_DQSN[0] / DDR0_DQSN[0]	I/O	-16916.4	5029.2
AK39	DDR0_DQSN[1] / DDR0_DQSN[1]	I/O	-16916.4	8686.8

Table 9-1. Ball Listing (Sheet 27 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AP39	DDR0_DQSN[2] / DDR0_DQSN[4]	I/O	-16916.4	12344.4
AU36	DDR0_DQSN[3] / DDR0_DQSN[5]	I/O	-14173.2	15087.6
AW7	DDR0_DQSN[4] / DDR1_DQSN[0]	I/O	12344.4	16916.4
AU3	DDR0_DQSN[5] / DDR1_DQSN[1]	I/O	16002	15087.6
AN3	DDR0_DQSN[6] / DDR1_DQSN[4]	I/O	16002	11430
AJ3	DDR0_DQSN[7] / DDR1_DQSN[5]	I/O	16002	7772.4
AF34	DDR1_DQSN[0] / DDR0_DQSN[2]	I/O	-12344.4	5029.2
AK33	DDR1_DQSN[1] / DDR0_DQSN[3]	I/O	-11430	8686.8
AN33	DDR1_DQSN[2] / DDR0_DQSN[6]	I/O	-11430	11430
AN29	DDR1_DQSN[3] / DDR0_DQSN[7]	I/O	-7772.4	11430
AN13	DDR1_DQSN[4] / DDR1_DQSN[2]	I/O	6858	11430
AR8	DDR1_DQSN[5] / DDR1_DQSN[3]	I/O	11430	13258.8
AM8	DDR1_DQSN[6] / DDR1_DQSN[6]	I/O	11430	10515.6
AG6	DDR1_DQSN[7] / DDR1_DQSN[7]	I/O	13258.8	5943.6
AF38	DDR0_DQSP[0] / DDR0_DQSP[0]	I/O	-16002	5029.2
AK38	DDR0_DQSP[1] / DDR0_DQSP[1]	I/O	-16002	8686.8
AP38	DDR0_DQSP[2] / DDR0_DQSP[4]	I/O	-16002	12344.4
AV36	DDR0_DQSP[3] / DDR0_DQSP[5]	I/O	-14173.2	16002
AV7	DDR0_DQSP[4] / DDR1_DQSP[0]	I/O	12344.4	16002
AU2	DDR0_DQSP[5] / DDR1_DQSP[1]	I/O	16916.4	15087.6
AN2	DDR0_DQSP[6] / DDR1_DQSP[4]	I/O	16916.4	11430
AJ2	DDR0_DQSP[7] / DDR1_DQSP[5]	I/O	16916.4	7772.4
AF35	DDR1_DQSP[0] / DDR0_DQSP[2]	I/O	-13258.8	5029.2
AL33	DDR1_DQSP[1] / DDR0_DQSP[3]	I/O	-11430	9601.2
AP33	DDR1_DQSP[2] / DDR0_DQSP[6]	I/O	-11430	12344.4
AN28	DDR1_DQSP[3] / DDR0_DQSP[7]	I/O	-6858	11430

Table 9-1. Ball Listing (Sheet 28 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AN12	DDR1_DQSP[4] / DDR1_DQSP[2]	I/O	7772.4	11430
AP8	DDR1_DQSP[5] / DDR1_DQSP[3]	I/O	11430	12344.4
AL8	DDR1_DQSP[6] / DDR1_DQSP[6]	I/O	11430	9601.2
AG7	DDR1_DQSP[7] / DDR1_DQSP[7]	I/O	12344.4	5943.6
AU32	DDR0_DQSN[8] / DDR0_DQSN[8]	I/O	-10515.6	15087.6
AV32	DDR0_DQSP[8] / DDR0_DQSP[8]	I/O	-10515.6	16002
AN26	DDR1_DQSN[8] / DDR1_DQSN[8]	I/O	-5029.2	11430
AN25	DDR1_DQSP[8] / DDR1_DQSP[8]	I/O	-4114.8	11430
	CMD,CTRL Ball Name			
	DDR4			
AY15	DDR0_PAR	O	5029.2	17830.8
AL20	DDR1_PAR	O	457.2	9601.2
AT23	DDR0_ALERT#	I/O	-2286	14173.2
AY25	DDR1_ALERT#	I/O	-4114.8	17830.8
AV18	DDR0_CKN[0]	O	2286	16002
AW18	DDR0_CKP[0]	O	2286	16916.4
AY17	DDR0_CKN[1]	O	3200.4	17830.8
AW17	DDR0_CKP[1]	O	3200.4	16916.4
AV16	DDR0_CKN[2]	O	4114.8	16002
AW16	DDR0_CKP[2]	O	4114.8	16916.4
AU16	DDR0_CKN[3]	O	4114.8	15087.6
AT16	DDR0_CKP[3]	O	4114.8	14173.2
AM21	DDR1_CKN[0]	O	-457.2	10515.6
AM20	DDR1_CKP[0]	O	457.2	10515.6
AP21	DDR1_CKN[1]	O	-457.2	12344.4
AP22	DDR1_CKP[1]	O	-1371.6	12344.4
AN21	DDR1_CKN[2]	O	-457.2	11430
AN20	DDR1_CKP[2]	O	457.2	11430
AP20	DDR1_CKN[3]	O	457.2	12344.4
AP19	DDR1_CKP[3]	O	1371.6	12344.4
AY24	DDR0_CKE[0]	O	-3200.4	17830.8
AW24	DDR0_CKE[1]	O	-3200.4	16916.4
AV24	DDR0_CKE[2]	O	-3200.4	16002
AV25	DDR0_CKE[3]	O	-4114.8	16002
AY29	DDR1_CKE[0]	O	-7772.4	17830.8

Table 9-1. Ball Listing (Sheet 29 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AV29	DDR1_CKE[1]	O	-7772.4	16002
AW29	DDR1_CKE[2]	O	-7772.4	16916.4
AU29	DDR1_CKE[3]	O	-7772.4	15087.6
AW11	DDR0_ODT[0]	O	8686.8	16916.4
AU14	DDR0_ODT[1]	O	5943.6	15087.6
AU12	DDR0_ODT[2]	O	7772.4	15087.6
AY10	DDR0_ODT[3]	O	9601.2	17830.8
AM16	DDR1_ODT[0]	O	4114.8	10515.6
AL16	DDR1_ODT[1]	O	4114.8	9601.2
AP15	DDR1_ODT[2]	O	5029.2	12344.4
AL15	DDR1_ODT[3]	O	5029.2	9601.2
AW12	DDR0_CS#[0]	O	7772.4	16916.4
AU11	DDR0_CS#[1]	O	8686.8	15087.6
AV13	DDR0_CS#[2]	O	6858	16002
AV10	DDR0_CS#[3]	O	9601.2	16002
AP17	DDR1_CS#[0]	O	3200.4	12344.4
AN15	DDR1_CS#[1]	O	5029.2	11430
AN17	DDR1_CS#[2]	O	3200.4	11430
AM15	DDR1_CS#[3]	O	5029.2	10515.6
AW15	DDR0_MA[0]	O	5029.2	16916.4
AU18	DDR0_MA[1]	O	2286	15087.6
AU17	DDR0_MA[2]	O	3200.4	15087.6
AV19	DDR0_MA[3]	O	1371.6	16002
AT19	DDR0_MA[4]	O	1371.6	14173.2
AU20	DDR0_MA[5]	O	457.2	15087.6
AV20	DDR0_MA[6]	O	457.2	16002
AU21	DDR0_MA[7]	O	-457.2	15087.6
AT20	DDR0_MA[8]	O	457.2	14173.2
AT22	DDR0_MA[9]	O	-1371.6	14173.2
AY14	DDR0_MA[10]	O	5943.6	17830.8
AU22	DDR0_MA[11]	O	-1371.6	15087.6
AV22	DDR0_MA[12]	O	-1371.6	16002
AV12	DDR0_MA[13]	O	7772.4	16002
AU24	DDR0_ACT#	O	-3200.4	15087.6
AV14	DDR0_MA[14]	O	5943.6	16002
AY11	DDR0_MA[15]	O	8686.8	17830.8
AW13	DDR0_MA[16]	O	6858	16916.4
AY13	DDR0_BA[0]	O	6858	17830.8
AV15	DDR0_BA[1]	O	5029.2	16002

Table 9-1. Ball Listing (Sheet 30 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AW23	DDR0_BG[0]	O	-2286	16916.4
AV23	DDR0_BG[1]	O	-2286	16002
AL19	DDR1_MA[0]	O	1371.6	9601.2
AL22	DDR1_MA[1]	O	-1371.6	9601.2
AM22	DDR1_MA[2]	O	-1371.6	10515.6
AM23	DDR1_MA[3]	O	-2286	10515.6
AP23	DDR1_MA[4]	O	-2286	12344.4
AL23	DDR1_MA[5]	O	-2286	9601.2
AW26	DDR1_MA[6]	O	-5029.2	16916.4
AY26	DDR1_MA[7]	O	-5029.2	17830.8
AU26	DDR1_MA[8]	O	-5029.2	15087.6
AW27	DDR1_MA[9]	O	-5943.6	16916.4
AP18	DDR1_MA[10]	O	2286	12344.4
AU27	DDR1_MA[11]	O	-5943.6	15087.6
AV27	DDR1_MA[12]	O	-5943.6	16002
AR15	DDR1_MA[13]	O	5029.2	13258.8
AU28	DDR1_ACT#	O	-6858	15087.6
AL17	DDR1_MA[14]	O	3200.4	9601.2
AP16	DDR1_MA[15]	O	4114.8	12344.4
AN18	DDR1_MA[16]	O	2286	11430
AL18	DDR1_BA[0]	O	2286	9601.2
AM18	DDR1_BA[1]	O	2286	10515.6
AW28	DDR1_BG[0]	O	-6858	16916.4
AY28	DDR1_BG[1]	O	-6858	17830.8
AU33	DDR0_ECC[0]	I/O	-11430	15087.6
AT33	DDR0_ECC[1]	I/O	-11430	14173.2
AW33	DDR0_ECC[2]	I/O	-11430	16916.4
AV31	DDR0_ECC[3]	I/O	-9601.2	16002
AU31	DDR0_ECC[4]	I/O	-9601.2	15087.6
AV33	DDR0_ECC[5]	I/O	-11430	16002
AW31	DDR0_ECC[6]	I/O	-9601.2	16916.4
AY31	DDR0_ECC[7]	I/O	-9601.2	17830.8
AR25	DDR1_ECC[0]	I/O	-4114.8	13258.8
AR26	DDR1_ECC[1]	I/O	-5029.2	13258.8
AM26	DDR1_ECC[2]	I/O	-5029.2	10515.6
AM25	DDR1_ECC[3]	I/O	-4114.8	10515.6
AP26	DDR1_ECC[4]	I/O	-5029.2	12344.4
AP25	DDR1_ECC[5]	I/O	-4114.8	12344.4
AL25	DDR1_ECC[6]	I/O	-4114.8	9601.2

Table 9-1. Ball Listing (Sheet 31 of 31)

Ball#	Ball Name	Default	X Location (µm)	Y Location (µm)
AL26	DDR1_ECC[7]	I/O	-5029.2	9601.2
	DDR VREF			
AC40	DDR0_VREF_DQ	O	-17830.8	2286
AC39	DDR1_VREF_DQ	O	-16916.4	2286
AB40	DDR_VREF_CA	O	-17830.8	1371.6
AC36	DDR_VTT_CNTL	O	-14173.2	2286
AV1	RSVD	N/A	17830.8	16002
AW2	RSVD	N/A	16916.4	16916.4

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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