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## *Low Voltage Voice Coil Motor Driver*

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### **Discontinued Product**

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: March 4, 2013

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, contact Allegro Sales.*

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## Low Voltage Voice Coil Motor Driver

### Features and Benefits

- Fixed I<sup>2</sup>C logic thresholds
- 8-bit D-to-A converter
- 500  $\mu$ A resolution
- Low voltage I<sup>2</sup>C serial interface
- Low current-draw sleep mode
- 2.4 to 5.5 V operation
- 1.1 mm  $\times$  0.7 mm, 0.5 mm maximum overall height WLCSP

### Package: 6-ball wafer-level chip scale package (CG)



1.1 mm  $\times$  0.7 mm

Not to scale

### Description

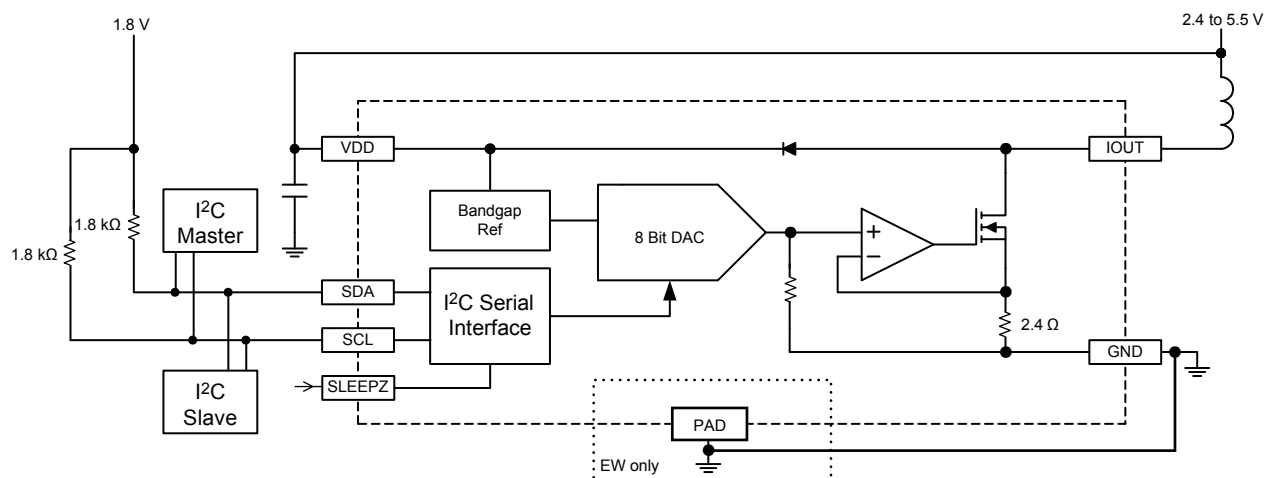
The A3904 is a voice coil motor (VCM) driver, with an I<sup>2</sup>C-compatible serial interface. Designed for camera autofocus and zoom applications, this high accuracy digital IC is provided in a WLCSP package ideal for portable devices. Its operating voltage range is 2.4 to 5.5 V, and its maximum output current is 127 mA.

Output current is programmed via the I<sup>2</sup>C interface, in 500  $\mu$ A increments, with clock rates up to 400 kHz. I<sup>2</sup>C inputs set the internal D-to-A converter output voltage that is the reference for linear current control via a MOSFET output sink transistor. To conserve battery power, a logic low signal on the SLEEPZ input disables the output MOSFET and reduces the supply current to  $<0.5 \mu$ A.

A3904 internal protection features include thermal shutdown and undervoltage lockout. Logic input levels are independent of the supply voltage. The operating temperature range is  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

The A3904 is available in a bumped wafer level chip scale package (WLCSP) (suffix CG).

### Functional Block Diagram



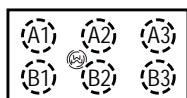
## Selection Guide

Part Number	Packing	Package	Pb-Free
A3904ECGTR	4000 pieces per reel	Bumped wafer-level chip-scale package (WLCSP)	Pb-free chip with high-temperature solder balls (RoHS compliant)

## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{DD}$		6	V
Logic Input Voltage Range	$V_{IN}$		-0.3 to $V_{DD}+0.3$	V
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

Pin-out Diagram  
CG Package



Orientation mark  
on bump side

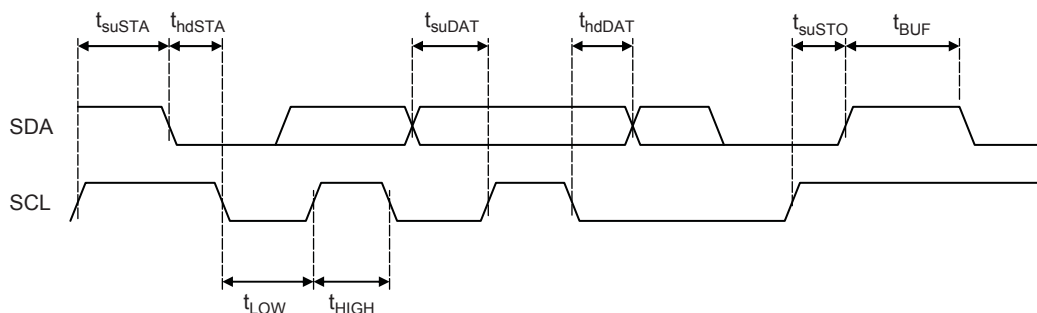
## Terminal List

Number	Name	Description
A1	SDA	I <sup>2</sup> C data input/output
A2	SCL	I <sup>2</sup> C clock
A3	VDD	Power supply
B3	GND	Ground
B2	IOUT	Sink drive output
B1	SLEEPZ	Standby mode control

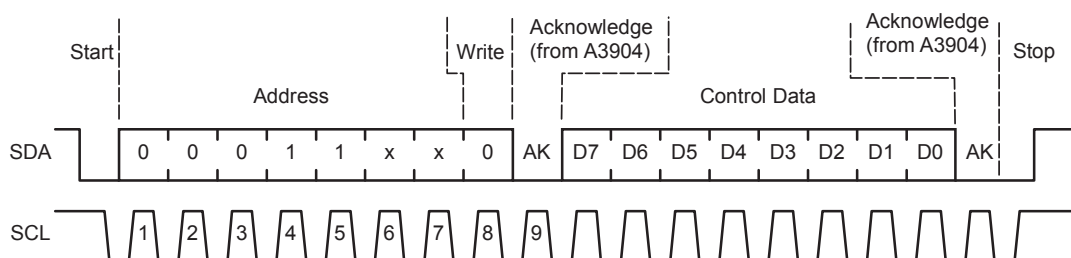
**ELECTRICAL CHARACTERISTICS** Valid at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.4$  to  $5.5\text{ V}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
General						
Supply Current	I <sub>DD</sub>		–	0.5	2	mA
		Sleep mode (SLEEPZ = Low)	–	<100	500	nA
UVLO Enable Threshold	V <sub>UV(th)</sub>	V <sub>DD</sub> rising	–	2.1	2.395	V
UVLO Hysteresis	V <sub>UV(hys)</sub>		100	–	–	mV
Thermal Shutdown Temperature	T <sub>JTSD</sub>	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT <sub>JTSD(hys)</sub>	T <sub>JTSD(hys)</sub> = T <sub>JTSD</sub> – T <sub>J(recover)</sub>	–	15	–	°C
Power-Up Delay	t <sub>d(on)</sub>		–	10	–	μs
D-to-A Converter						
Resolution	Res	Target = 500 μA / LSB	–	8	–	bit
LSB Relative Accuracy	INL	Code = 16 to 255, Endpoint method	–	±4	–	LSB
LSB Differential Nonlinearity	DNL	Guaranteed monotonic	–	–	±1	LSB
Maximum Output Current	I <sub>max</sub>	Code = 255	–	127.5	–	mA
Gain Error	err <sub>A</sub>	T <sub>J</sub> = 25°C, Code 16 to 255, V <sub>DD</sub> = 2.6 to 3.0 V	–10	<3	10	%FS
Gain Error Drift*	Δerr <sub>A</sub>	T <sub>J</sub> = –40°C to 125°C	–	0.2	–	LSB/°C
Offset Error	I <sub>errOS</sub>	Code = 1	0	1	5	mA
		Code = 16	0.5	–	–	mA
Output						
Output Voltage Range	V <sub>OUT</sub>		0.500	–	V <sub>DD</sub> –0.1	V
Output On Resistance	R <sub>DS(on)</sub>	R <sub>SENSE</sub> + R <sub>SINK</sub> , I <sub>OUT</sub> = 127.5 mA	–	3	–	Ω
I <sup>2</sup> C Interface						
Bus Free Time Between Stop and Start	t <sub>BUF</sub>		1.3	–	–	μs
Hold Time Start Condition	t <sub>hdSTA</sub>		0.6	–	–	μs
Setup Time for Repeated Start Condition	t <sub>suSTA</sub>		0.6	–	–	μs
SCL Low Time	t <sub>LOW</sub>		1.3	–	–	μs
SCL High Time	t <sub>HIGH</sub>		0.6	–	–	μs
Data Setup Time	t <sub>suDAT</sub>		100	–	–	ns
Data Hold Time	t <sub>hdDAT</sub>		0		900	ns
Setup Time for Stop Condition	t <sub>suSTO</sub>		0.6	–	–	μs
Logic Input Low Level (SDA, SCL pins)	V <sub>IL</sub>		–	–	0.84	V
Logic Input High Level (SDA, SCL pins)	V <sub>IH</sub>		1.26	–	–	V
Input Hysteresis (SDA, SCL pins)	V <sub>hys</sub>		–	100	–	mV
SLEEPZ Input Low Level	V <sub>inSLP</sub>		–	–	0.7	V
SLEEPZ Input High Level	V <sub>inSLP</sub>		1.5	–	–	V
Logic Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	–1	0	1	μA
Output Voltage (SDA pin)	V <sub>OL</sub>	I <sub>LOAD</sub> = 1.5 mA	–	–	0.36	V
Clock Frequency (SCL pin)	f <sub>CLK</sub>		–	–	400	kHz
Output Fall Time (SDA pin)	t <sub>fO</sub>	V <sub>IH</sub> to V <sub>IL</sub>	–	–	250	ns

\*Guaranteed by design and characterization, not production tested

I<sup>2</sup>C Interface Timing Diagram

## Write Register Bit Definition and Timing Diagram

I<sup>2</sup>C Control Register Bit Definition

Bit	Name	Function
0	D0	DAC LSB
1	D1	
2	D2	
3	D3	
4	D4	
5	D5	
6	D6	
7	D7	DAC MSB

## A3904 Slave Address Bit Definition

Bit							Operation
0	1	2	3	4	5	6	
0	0	0	1	1	x	X	1
							0
							Read
							Write

## Functional Description

The A3904 output current is controlled by programming the D-to-A converter value via the I<sup>2</sup>C serial port. The target output current can be calculated by:

$$I_{OUT} = DAC \times 500 \mu A ,$$

where DAC = 1 to 255. Code = 0 is a disable state for the output sink drive. The DAC will be set to code = 0 upon power-up or a fault condition on V<sub>DD</sub>.

**SLEEPZ** A logic low input disables all of the internal circuitry and prevents the IC from draining battery power.

**Output Range** The voltage on the IOUT pin should be greater than 500 mV to guarantee the accuracy and linearity of the programmed current. The output voltage is a function of the battery voltage, motor resistance, and the programmed load current.

**Clamp Diode** When the output is turned off, the load inductance causes the output voltage to rise. A clamp diode, from IOUT to VDD, is integrated in the IC to ensure that the output voltage remains at a safe level.

**I<sup>2</sup>C Interface** This is a serial interface that uses two bus lines, SCL and SDA, to access the internal Control registers. Data is exchanged between a microcontroller (master) and the A3904 (slave). The clock input to SCL is generated by the master, while the SDA line functions as either an input or an open drain output, depending on the direction of the data. The I<sup>2</sup>C input thresholds do not depend on the V<sub>DD</sub> voltage of the A3904. The levels are fixed at approximately 1 V. The fixed levels allow the SDA and SCL lines to be pulled-up to a different logic level than the V<sub>DD</sub> supply of the 3904.

**Timing Considerations** The control sequence of the communication through the I<sup>2</sup>C interface is composed of several steps

in the following sequence:

1. Start Condition. Defined by a negative edge on the SDA line, while SCL is high.
2. Address Cycle. 7 bits of address, plus 1 bit to indicate write (0) or read (1), and an acknowledge bit. The address setting is 0x18, 0x1A, 0x1C or 0x1E.
3. Data Cycles. Write 8 bits of data that address the internal Control register, followed by an acknowledge bit.
4. Stop Condition. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A3904 always responds by resetting the data transfer sequence.

The Read/Write bit is set low to indicate a write cycle. Multiple writes are allowed before issuing a Stop condition. There are no readback functions incorporated into the A3904.

The master monitors for an acknowledge pulse to determine if the slave device is responding to the address byte sent to the A3904. When the A3904 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A3904 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received.

After sending either an address byte or a data byte, the master device must release the SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

## Application Information

**Headroom** The current may not reach the programmed level if there is not adequate headroom in the output circuit. The IC output voltage must be over 500 mV to guarantee normal linear operation.  $V_{DD}$ ,  $I_{LOAD}$ , and  $R_{LOAD}$  can be adjusted to ensure that the device operates in the linear range.

If the equation shown below is not satisfied, the load current will be limited by the series impedance, and may not reach the programmed level

$$V_{DD}(\min) - R_{LOAD}(\max) \times I_{OUT}(\max) \geq 500 \text{ mV}$$

### $I_{OUT}$ Errors

**Relative accuracy (INL)** This error is calculated by measuring the worse case deviation from a straight line, defined from end points. The straight line end points are defined by the actual measured values at Code = 16 and Code = 255. See figure 1.

**Differential nonlinearity (DNL)** A measure of the monotonicity of the D-to-A converter. The slope of the line must always

be positive for each incremental step, according to the following formula:

$$DNL = (I_{OUT(n+1)} - I_{OUT(n)}) / LSB - 1 \text{ (LSB)}$$

where  $n$  is in the range 16 to 255.

**Offset error** The measured output current at input Code = 16, compared to the ideal value according to the transfer function (8 mA).

**Gain Error** The difference in the slopes of the ideal transfer function and the actual transfer function. The gain error is calculated by subtracting out the offset error, at Code = 16, from the actual transfer function. This calculated value is compared to the ideal transfer function and reported as a percentage of the ideal full scale value (127.5 mA). See figure 2.

**Gain Error Drift** The change in slope of the transfer function due to temperature, expressed as  $LSB/^{\circ}C$ .

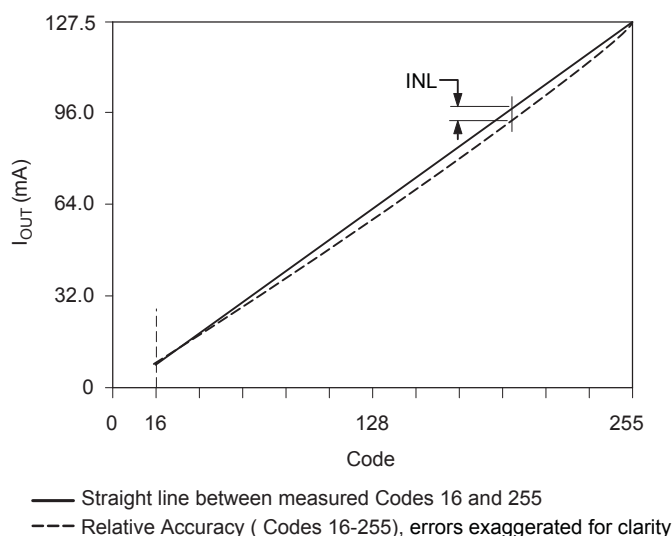


Figure 1. Relative accuracy error

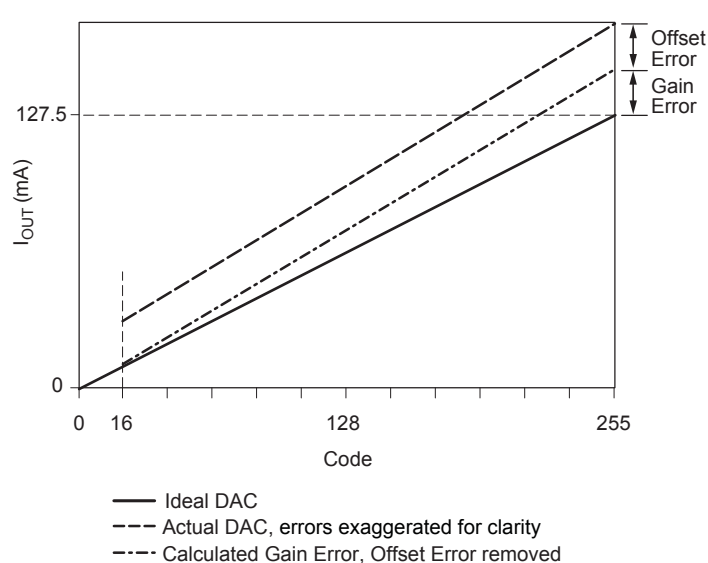
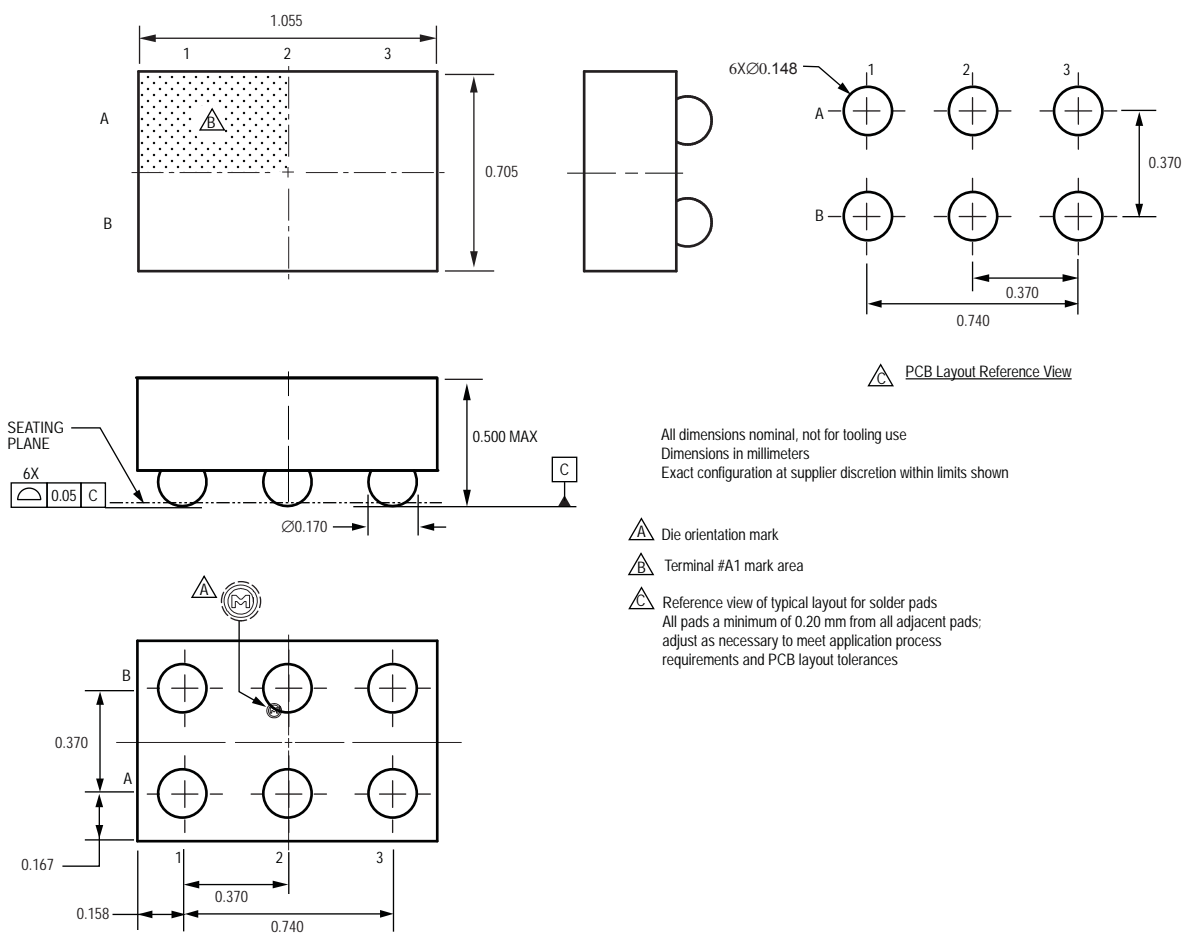


Figure 2. Gain error

## CG Package, 6-Bump WLCSP



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