# Integrated Video Decoder and HDMI Receiver

Data Sheet

# ADV7482

## FEATURES

- Analog input
  - Worldwide NTSC/PAL/SECAM color demodulation support with autodetection
  - One 10-bit ADC, 4× oversampling for CVBS, Y/C, and YPbPr
  - 8 analog video input channels with on-chip antialiasing filter
  - Fully differential, pseudo differential, and single-ended CVBS video input support
  - STB diagnostics on differential video inputs
  - CVBS (composite), Y/C (S-Video), and YPbPr (component) video input support
  - Fast switching capability between analog inputs
  - Adaptive contrast enhancement (ACE)
  - Excellent common-mode noise rejection capabilities
  - Rovi (Macrovision) copy protection detection
  - Up to 4 V common-mode input range solution
  - Vertical blanking interval (VBI) data slicer
- High-Definition Multimedia Interface (HDMI) capable receiver
  - HDCP authentication and decryption support
  - 162 MHz maximum pixel clock frequency, allowing HDTV formats up to 1080p and display resolutions up to UXGA (1600 × 1200 at 60 Hz)
  - HDCP repeater support, up to 25 KSVs supported
  - Integrated CEC controller, CEC 1.4 compatible
  - Adaptive TMDS equalizer
  - 5 V detect and Hot Plug assert
- Component video processor
  - Any-to-any 3 × 3 color space conversion (CSC) matrix
  - Contrast/brightness/hue/saturation video adjustment
  - Timing adjustments controls for horizontal sync (HS)/vertical sync (VS)/data enable (DE) timing
  - Video mute function
- Serial digital audio output interface
  - HDMI audio extraction support
  - Advanced audio muting feature
  - I²S-compatible, left justified and right justified audio output modes
  - 8-channel TDM output mode available
- 2 Mobile Industry Processor Interface (MIPI) Camera Serial Interface 2 (CSI-2) transmitters
  - 4-lane transmitter with 4 lanes, 2 lanes, and 1 lane muxing options for HDMI/SDP/digital input port sources
  - 1-lane transmitter for standard definition processor (SDP) sources
- 8-bit digital input/output port
- General
  - 2-wire serial microprocessor unit (MPU) interface (I²C compatible)
  - −40°C to +85°C temperature grade
  - 100-ball, 9 mm × 9 mm, RoHS-compliant CSP_BGA package
  - Qualified for automotive applications

## APPLICATIONS

- Portable devices
- Automotive infotainment (head unit and rear seat entertainment systems)
- HDMI repeaters and video switches

## FUNCTIONAL BLOCK DIAGRAM

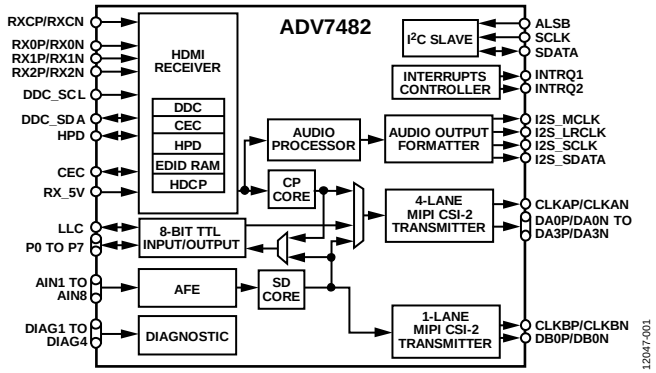



*Figure 1.*


**Rev. 0** Document Feedback



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700


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## REVISION HISTORY

**6/14—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The ADV7482 is an integrated video decoder and HDMI® receiver, targeted at connectivity enabled head units requiring a wired, uncompressed digital audio/video link from smartphones, and other consumer electronics devices to support streaming and integration of cloud-based multimedia content and applications into an automotive infotainment system.

The ADV7482 HDMI capable receiver supports a maximum pixel clock frequency of 162 MHz, allowing HDTV formats up to 1080p, and display resolutions up to UXGA (1600 × 1200 at 60 Hz). The device integrates a consumer electronics control (CEC) controller that supports the capability discovery and control (CDC) feature. The HDMI input port has dedicated 5 V detect and Hot Plug™ assert pins.

The HDMI receiver includes an adaptive transition minimized differential signaling (TMDS) equalizer that ensures robust operation of the interface with long cables.

The ADV7482 contains a component processor (CP) that processes the video signals from the HDMI receiver. It provides features such as contrast, brightness, and saturation adjustments, as well as free run and timing adjustment controls for HS/VS/DE timing.

The ADV7482 analog front end (AFE) comprises a single high speed, 10-bit analog-to-digital converter (ADC) that digitizes the analog video signal before applying it to the SDP.

The eight analog video inputs can accept single-ended, pseudo differential, and fully differential composite video signals, as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources.

Short to battery (STB) events can be detected on differential input video signals. STB protection is provided by ac coupling the input video signals. The ADV7482, in combination with an external resistor divider, provides a common-mode input range of 4 V, enabling the removal of large signal common-mode transients present on the video lines.

The automatic gain control (AGC) and clamp restore circuitry allow an input video signal up to 1.0 V p-p at the analog video input pins of the ADV7482. Alternatively, the AGC and clamp restore circuitry can be bypassed for manual settings.

The SDP of the ADV7482 is capable of decoding a large selection of analog baseband video signals in composite, S-Video, and component formats. The SDP supports worldwide NTSC, PAL, and SECAM standards.

The ADV7482 features an 8-bit digital input/output port, supporting input and output video resolutions up to 720p/1080i in both the 8-bit interleaved 4:2:2 SDR and DDR modes.

To enable glueless interfacing of these video input sources to the latest generation of infotainment system on chips (SoCs), the ADV7482 features two MIPI® CSI-2 transmitters. The four-lane transmitter provides four data lanes, two data lanes, and one data lane muxing options, and can be used to output video from the HDMI receiver, the SDP, and the digital input port. The single-lane transmitter can be used to output video from the SDP only.

The ADV7482 offers a flexible audio output port for audio data extracted from HDMI streams. The HDMI receiver has advanced audio functionality, such as a mute controller that prevents audible extraneous noise in the audio output. Additionally, the ADV7482 can be set to output time division multiplexing (TDM) serial audio, which allows the transmission of eight multiplexed serial audio channels on a single audio output interface port.

The ADV7482 is programmed via a 2-wire, serial, bidirectional port ($I^2C$ compatible).

Fabricated in an advanced CMOS process, the ADV7482 is available in a 9 mm × 9 mm, RoHS-compliant, 100-ball CSP_BGA package and is specified over the −40°C to +85°C temperature range.

The ADV7482 is offered in automotive and industrial versions.

# DETAILED FUNCTIONAL BLOCK DIAGRAM

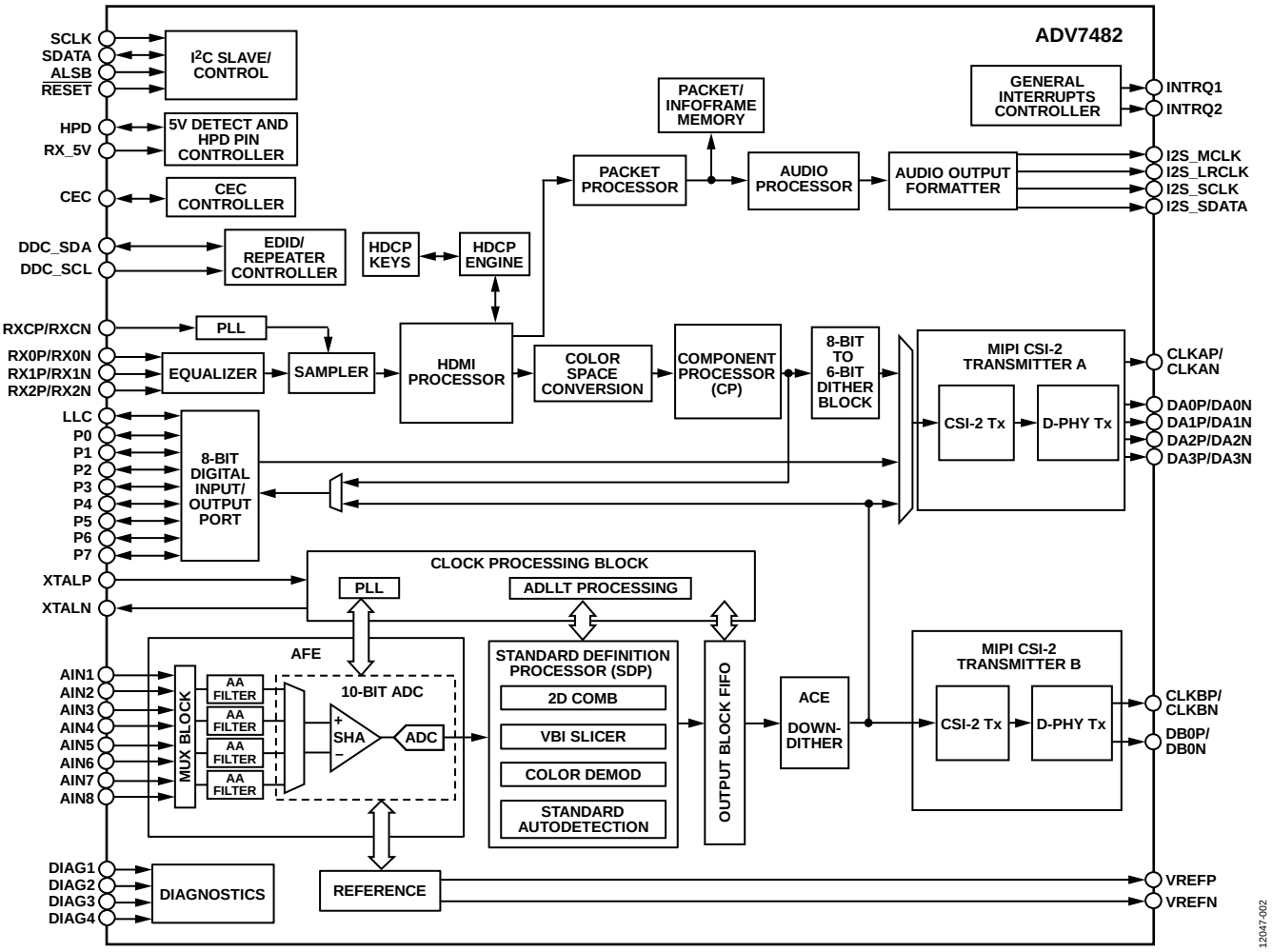



*Figure 2.*

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| STATIC PERFORMANCE | | | | | | |
| Resolution (Each ADC) | N | | | | 10 | Bits |
| Integral Nonlinearity | INL | CVBS mode | | 2 | | LSB |
| Differential Nonlinearity | DNL | CVBS mode | | ±0.6 | | LSB |
| DIGITAL INPUTS[1] | | SCLK, SDATA, $\overline{\text{RESET}}$, ALSB, LLC, and P0 to P7 | | | | |
| Input High Voltage | $V_{IH}$ | DVDDIO = 3.14 V to 3.46 V | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | DVDDIO = 3.14 V to 3.46 V | | | 0.8 | V |
| Input Leakage Current | $I_{IN}$ | | −10 | | +10 | µA |
| Input Capacitance[2] | $C_{IN}$ | | | | 10 | pF |
| CRYSTAL INPUT | | | | | | |
| Input High Voltage | $V_{IH}$ | XTALP | 1.2 | | | V |
| Input Low Voltage | $V_{IL}$ | XTALP | | | 0.4 | V |
| DIGITAL OUTPUTS[1] | | LLC, P0 to P7, I2S_MCLK, I2S_SCLK, I2S_LRCLK, I2S_SDATA, SDATA, INTRQ1 and INTRQ2 (when configured to drive when active) | | | | |
| Output High Voltage | $V_{OH}$ | DVDDIO = 3.14 V to 3.46 V and $I_{SOURCE}$ = 0.4 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | DVDDIO = 3.14 V to 3.46 V and $I_{SINK}$ = 3.2 mA | | | 0.4 | V |
| High Impedance Leakage Current | $I_{LEAK}$ | | | 10 | | µA |
| Output Capacitance[2] | $C_{OUT}$ | | | | 20 | pF |
| POWER REQUIREMENTS | | | | | | |
| Digital Power Supply | $D_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| HDMI Terminator Supply | $T_{VDD}$ | | 3.14 | 3.3 | 3.46 | V |
| HDMI Comparator Supply | $C_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| PLL Power Supply | $P_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| MIPI Transmitters Power Supply | $M_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| Digital Input/Output Power Supply[1] | $D_{VDDIO}$ | 3.3 V operation | 3.14 | 3.3 | 3.46 | V |
| Analog Power Supply | $A_{VDD}$ | | 1.71 | 1.8 | 1.89 | V |
| CURRENT CONSUMPTION[1, 2, 3, 4] | | | | | | |
| Digital Supply Current | $I_{DVDD}$ | | | | 279 | mA |
| Single-Ended CVBS Input | | | | 74.5 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 74.7 | | mA |
| Y/C Input | | | | 71.3 | | mA |
| YPbPr Input | | | | 72.8 | | mA |
| HDMI Input | | | | 68.1 | | mA |
| 8-Bit Digital Input | | | | 32.5 | | mA |
| HDMI Terminator Supply Current | $I_{TVDD}$ | | | | 40 | mA |
| Single-Ended CVBS Input | | | | 0.7 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 0.7 | | mA |
| Y/C Input | | | | 0.7 | | mA |
| YPbPr Input | | | | 0.7 | | mA |
| HDMI Input | | | | 35 | | mA |
| 8-Bit Digital Input | | | | 0.7 | | mA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| HDMI Comparator Supply Current | $I_{CVDD}$ | | | | 92 | mA |
| Single-Ended CVBS Input | | | | 0.1 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 0.1 | | mA |
| Y/C Input | | | | 0.1 | | mA |
| YPbPr Input | | | | 0.1 | | mA |
| HDMI Input | | | | 63.9 | | mA |
| 8-Bit Digital Input | | | | 0.1 | | mA |
| PLL Supply Current | $I_{PVDD}$ | | | | 52 | mA |
| Single-Ended CVBS Input | | | | 37.5 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 37.5 | | mA |
| Y/C Input | | | | 37.7 | | mA |
| YPbPr Input | | | | 37.7 | | mA |
| HDMI Input | | | | 29.2 | | mA |
| 8-Bit Digital Input | | | | 27.9 | | mA |
| MIPI Transmitters Supply Current | $I_{MVDD}$ | | | | 77 | mA |
| Single-Ended CVBS Input | | | | 23.3 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 23.3 | | mA |
| Y/C Input | | | | 23.2 | | mA |
| YPbPr Input | | | | 23.2 | | mA |
| HDMI Input | | | | 45.7 | | mA |
| 8-Bit Digital Input | | | | 38.1 | | mA |
| Digital Input/Output Supply Current | $I_{DVDDIO}$ | | | | 78 | mA |
| Single-Ended CVBS Input | | | | 0.2 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 0.2 | | mA |
| Y/C Input | | | | 0.2 | | mA |
| YPbPr Input | | | | 0.2 | | mA |
| HDMI Input | | | | 3.6 | | mA |
| 8-Bit Digital Input | | | | 0.2 | | mA |
| Analog Supply Current | $I_{AVDD}$ | | | | 93 | mA |
| Single-Ended CVBS Input | | | | 51.9 | | mA |
| Fully Differential and Pseudo Differential CVBS Input | | | | 70 | | mA |
| Y/C Input | | | | 63 | | mA |
| YPbPr Input | | | | 78.5 | | mA |
| HDMI Input | | | | 0.1 | | mA |
| 8-Bit Digital Input | | | | 0.1 | | mA |
| POWER-DOWN CURRENTS[2, 5] | | | | | | |
| Digital Supply | $I_{DVDD_PD}$ | | | 0.2 | | mA |
| HDMI Terminator Supply | $I_{TVDD_PD}$ | | | 0.4 | | mA |
| HDMI Comparator Supply | $I_{CVDD_PD}$ | | | 0.1 | | mA |
| PLL Supply | $I_{PVDD_PD}$ | | | 0.1 | | mA |
| MIPI Transmitters Supply | $I_{MVDD_PD}$ | | | 0.1 | | mA |
| Digital Input/Output Supply | $I_{DVDDIO_PD}$ | | | 0.2 | | mA |
| Analog Supply | $I_{AVDD_PD}$ | | | 0.1 | | mA |
| Total Power Dissipation in Power-Down Mode | | | | 4 | | mW |

[1] The 8-bit digital input/output port is only available when the DVDDIO supply is between 3.14 V and 3.46 V.
[2] Guaranteed by lab characterization.
[3] Typical current consumption values are recorded with nominal voltage supply levels (including DVDDIO = 3.3 V), Philips test pattern, and at room temperature.
[4] Maximum current consumption values are recorded with maximum rated voltage supply levels (including DVDDIO = 3.46 V), MoireX video pattern for analog inputs, pseudorandom test pattern for digital inputs, and at worst-case temperature.
[5] Typical power-down current consumption values are recorded with nominal voltage supply levels (including DVDDIO = 3.3 V) at room temperature.

## ANALOG VIDEO SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| NONLINEAR SPECIFICATIONS[1, 2] | | | | | | |
| Differential Phase | DP | CVBS input, modulated five-step | | 0.9 | | Degrees |
| Differential Gain | DG | CVBS input, modulated five-step | | 0.5 | | % |
| Luma Nonlinearity | LNL | CVBS input, five-step | | 2.0 | | % |
| NOISE SPECIFICATIONS | | | | | | |
| Signal-to-Noise Ratio, Unweighted[2] | SNR | Luma ramp | | 57.1 | | dB |
| | | Luma flat field | | 58 | | dB |
| Analog Front-End Crosstalk[3] | | | | 60 | | dB |
| Common-Mode Rejection Ratio[2, 4] | CMRR | | | 73 | | dB |
| LOCK TIME SPECIFICATIONS | | | | | | |
| Horizontal Lock Range[3] | | | −5 | | +5 | % |
| Vertical Lock Range[3] | | | 40 | | 70 | Hz |
| Subcarrier Lock Range[3] | $f_{SC}$ | | | ±1.3 | | kHz |
| Color Lock-In Time[3] | | | | 60 | | Lines |
| Synchronization Depth Range[3] | | | 20 | | 200 | % |
| Color Burst Range[3] | | | 5 | | 200 | % |
| Fast Switch Speed[2, 5] | | | | 100 | | ms |

[1] These specifications apply to all CVBS input types, as well as to single-ended and differential CVBS inputs.
[2] Guaranteed by lab characterization.
[3] Guaranteed by design.
[4] The CMRR of this circuit design is critically dependent on the external resistor matching its inputs. This measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.
[5] The time it takes the ADV7482 to switch from one analog input (single ended or differential) to another, for example, switching from AIN1 to AIN2.

## MIPI VIDEO OUTPUT SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

The ADV7482 MIPI CSI-2 transmitters conform to the MIPI D-PHY Version 1.00.00 specification by characterization. The clock lane of the ADV7482 remains in high speed (HS) mode even when the data lane enters low power (LP) mode. For this reason, some measurements on the clock lane that pertain to low power mode are not applicable. Unless otherwise stated, all high speed measurements were performed with the ADV7482 operating with a nominal 1 Gbps output data rate.

**Table 3**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| UNIT INTERVAL[1] | UI | 1 | | 12.5 | ns |
| DATA LANE LP Tx DC SPECIFICATIONS[2] | | | | | |
| Thevenin Output | | | | | |
| High Level | $V_{OH}$ | 1.1 | 1.2 | 1.3 | V |
| Low Level | $V_{OL}$ | −50 | 0 | +50 | mV |
| CLOCK LANE LP Tx DC SPECIFICATIONS[2] | | | | | |
| Thevenin Output | | | | | |
| High Level | $V_{OH}$ | 1.1 | 1.2 | 1.3 | V |
| Low Level | $V_{OL}$ | −50 | 0 | +50 | mV |
| DATA LANE HS Tx SIGNALING REQUIREMENTS | | | | | |
| High Speed Differential Voltage Swing | $\|V_1\|$ | 140 | 200 | 270 | mV p-p |
| Differential Voltage Mismatch | | | | 10 | mV |
| Single-Ended Output High Voltages | | | | 360 | mV |
| Static Common-Mode Voltage Level | | 150 | 200 | 250 | mV |
| CLOCK LANE HS Tx SIGNALING REQUIREMENTS | | | | | |
| High Speed Differential Voltage Swing | $\|V_2\|$ | 140 | 200 | 270 | mV p-p |
| Differential Voltage Mismatch | | | | 10 | mV |
| Single-Ended Output High Voltages | | | | 360 | mV |
| Static Common-Mode Voltage Level | | 150 | 200 | 250 | mV |
| HS Tx CLOCK TO DATA LANE TIMING REQUIREMENTS | | | | | |
| Data to Clock Skew | | 0.35 × UI | | 0.65 × UI | ns |

[1] Guaranteed by design.
[2] These measurements were performed with $C_{LOAD}$ = 50 pF.

## ANALOG SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

**Table 4.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CLAMP CIRCUITRY | | | | | |
| External Clamp Capacitor | Required by design | | 0.1 | | µF |
| Large Clamp | | | | | |
| Source Current | | | 0.32 | | mA |
| Sink Current | | | 0.32 | | mA |
| Fine Clamp | | | | | |
| Source Current | | | 7 | | µA |
| Sink Current | | | 7 | | µA |

## TIMING SPECIFICATIONS

AVDD = 1.71 V to 1.89 V, DVDD = 1.71 V to 1.89 V, PVDD = 1.71 V to 1.89 V, MVDD = 1.71 V to 1.89 V, CVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, and TVDD = 3.14 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

**Table 5.**

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| CLOCK AND CRYSTAL | | | | | | |
| Nominal Frequency[1] | | Required by design | | 28.63636 | | MHz |
| Frequency Stability[1] | | Required by design | | | ±50 | ppm |
| Input LLC Clock Frequency Range[2, 3] | | DVDDIO = 3.14 V to 3.46 V | 13.5 | | 148.5 | MHz |
| Output LLC Clock Frequency Range[2, 3] | | DVDDIO = 3.14 V to 3.46 V | 13.5 | | 148.5 | MHz |
| I2S_SCLK Frequency[3] | | | | | 12.288 | MHz |
| I2S_MCLK Frequency[3] | | | | | 24.576 | MHz |
| I²C PORT | | | | | | |
| SCLK Frequency | | | | | 400 | kHz |
| SCLK Minimum Pulse Width High | $t_1$ | | 0.6 | | | µs |
| SCLK Minimum Pulse Width Low | $t_2$ | | 1.3 | | | µs |
| Hold Time (Start Condition) | $t_3$ | | 0.6 | | | µs |
| Setup Time (Start Condition) | $t_4$ | | 0.6 | | | µs |
| SDATA Setup Time | $t_5$ | | 100 | | | ns |
| SCLK and SDATA Rise Times | $t_6$ | | | | 300 | ns |
| SCLK and SDATA Fall Times | $t_7$ | | | | 300 | ns |
| Setup Time (Stop Condition) | $t_8$ | | | 0.6 | | µs |
| $\overline{\text{RESET}}$ FEATURE | | | | | | |
| $\overline{\text{RESET}}$ Pulse Width[1] | | | 5 | | | ms |
| 8-BIT DIGITAL INPUT PORT[2] | | DVDDIO = 3.14 V to 3.46 V | | | | |
| LLC High Time[3] | $t_{21}$ | | 45 | | 55 | % duty cycle |
| LLC Low Time[3] | | | 45 | | 55 | % duty cycle |
| SDR and DDR Modes Setup Time | $t_{22}$ | Data latched on rising edge | 1 | | | ns |
| SDR and DDR Modes Hold Time | $t_{23}$ | Data latched on rising edge | 1 | | | ns |
| DDR Mode Setup Time | $t_{24}$ | Data latched on falling edge | 1 | | | ns |
| DDR Mode Hold Time | $t_{25}$ | Data latched on falling edge | 1 | | | ns |
| 8-BIT DIGITAL OUTPUT PORT[2] | | DVDDIO = 3.14 V to 3.46 V | | | | |
| LLC High Time | $t_{26}$ | | 40 | | 60 | % duty cycle |
| LLC Low Time | | | 40 | | 60 | % duty cycle |
| SDR Modes Setup Time[4, 5] | $t_{36}$ | At P0 to P7 output pin, data latched on rising edge | 1.98 | | | ns |
| SDR Modes Hold Time[4, 5] | $t_{37}$ | At P0 to P7 output pin, data latched on rising edge | 2.50 | | | ns |
| DDR Modes Setup Time[4, 5] | $t_{27}$ | At P0 to P7 output pin, data latched on rising edge | 1.66 | | | ns |
| DDR Modes Hold Time[4, 5] | $t_{28}$ | At P0 to P7 output pin, data latched on rising edge | 3.52 | | | ns |
| DDR Mode Setup TIme[4, 5] | $t_{29}$ | At P0 to P7 output pin, data latched on falling edge | 1.71 | | | ns |
| DDR Modes Hold Time[4, 5] | $t_{30}$ | At P0 to P7 output pin, data latched on falling edge | 3.17 | | | ns |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| I²S PORT, MASTER MODE | | | | | | |
| I2S_SCLK High Time | $t_{31}$ | | 45 | | 55 | % duty cycle |
| I2S_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| I2S_LRCLK Data Transition Time | $t_{32}$ | End of valid data to I2S_SCLK falling edge | | | 10 | ns |
| | $t_{33}$ | I2S_SCLK falling edge to start of valid data | | | 10 | ns |
| I2S_SDATA Data Transition Time | $t_{34}$ | End of valid data to I2S_SCLK falling edge | | | 5 | ns |
| | $t_{35}$ | I2S_SCLK falling edge to start of valid data | | | 5 | ns |

[1] Required by design.
[2] The 8-bit digital input/output port is only available when the DVDDIO supply is between 3.14 V and 3.46 V.
[3] Guaranteed by design.
[4] These specifications only apply when the LLC_DLL_PHASE[4:0] (IO Map, Register 0x0C[4:0]) is set to 00000.
[5] Guaranteed by lab characterization.

### *Timing Diagrams*

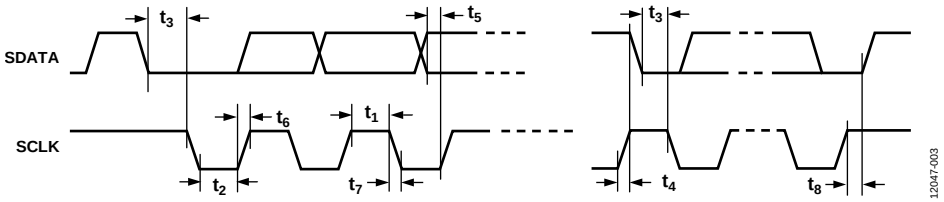



*Figure 3. I²C Timing*

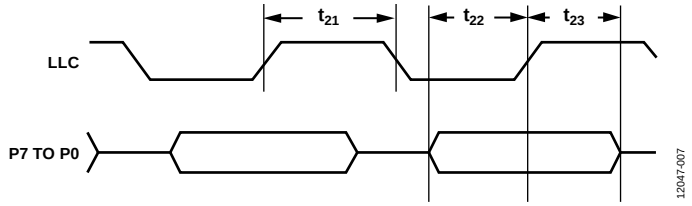



*Figure 4. 8-Bit Digital Pixel Video Input, SDR Video Data Timing*

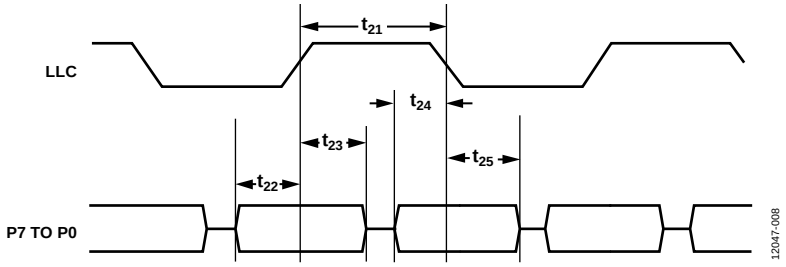



*Figure 5. 8-Bit Digital Pixel Video Input, DDR Video Data Timing*

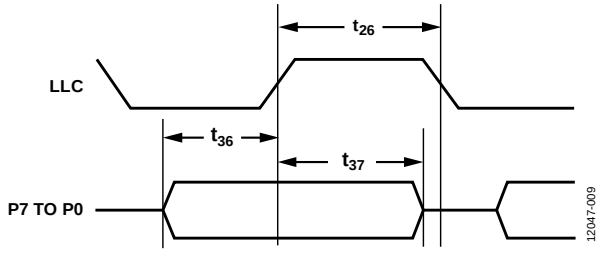



*Figure 6. 8-Bit Digital Pixel Video Output, SDR Video Data Timing*

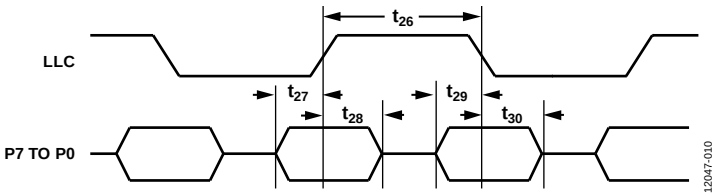



*Figure 7. 8-Bit Digital Pixel Video Output, DDR Video Data Timing*

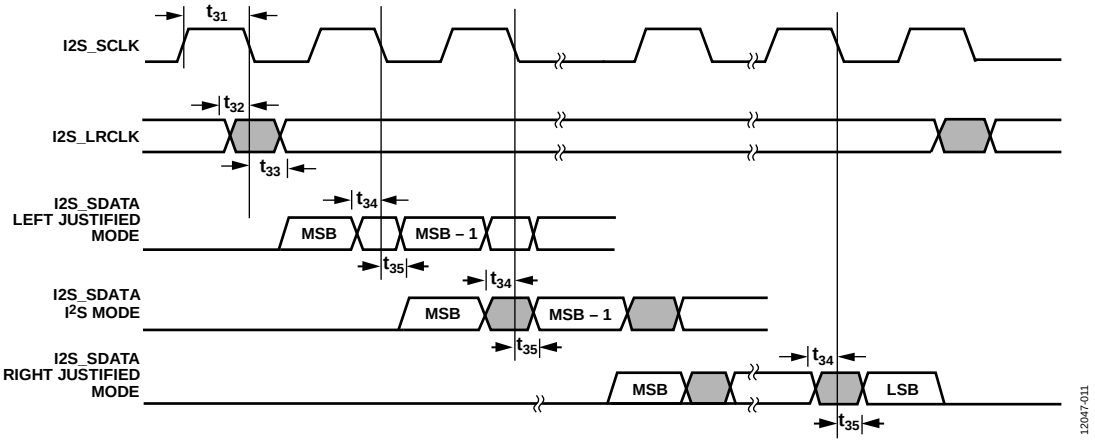



*Figure 8. I²S Timing*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| TVDD, DVDDIO to GND | 4 V |
| AVDD, PVDD, MVDD, DVDD, CVDD to GND | 2.2 V |
| CVDD to DVDD | −0.3 V to +0.3 V |
| MVDD to DVDD | −0.3 V to +0.3 V |
| PVDD to DVDD | −0.3 V to +0.3 V |
| AVDD to DVDD | −0.3 V to +0.3 V |
| Digital Inputs Voltage to GND | GND − 0.3 V to DVDDIO + 0.3 V |
| Digital Outputs Voltage to GND | GND − 0.3 V to DVDDIO + 0.3 V |
| Analog Inputs to GND | −0.3 V to AVDD + 0.3 V |
| XTALN and XTALP to GND | −0.3 V to PVDD + 0.3 V |
| HDMI Digital Inputs Voltage to GND | −0.3 V to CVDD + 0.3 V |
| 5 V Tolerant Inputs Voltage to GND[1, 2] | −0.3 V to +5.5 V |
| Maximum Junction Temperature ($T_J$ max) | 125°C |
| Storage Temperature Range | −65°C to +150°C |
| Infrared Reflow Soldering (20 sec) | 260°C |

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: DDC_SCL, DDC_SDA, HPD, RX_5V, and CEC.
[2] The following inputs are 1.8 V inputs but are 5 V tolerant: DIAG1, DIAG2, DIAG3, and DIAG4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

To reduce power consumption when using the ADV7482, turn off unused sections of the device.

Due to printed circuit board (PCB) metal variation, and, therefore, variation in PCB heat conductivity, the value of $\theta_{JA}$ may differ for various PCBs.

The most efficient measurement solution is achieved using the package surface temperature to estimate the die temperature. This eliminates the variance associated with the $\theta_{JA}$ value.

Do not exceed the maximum junction temperature ($T_J$ max) of 125°C. The following equation calculates the junction temperature ($T_J$) using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
$T_S$ is the package surface temperature (°C).
$\Psi_{JT}$ = 0.81°C/W for the 100-ball CSP_BGA (based on 2s2p test board defined by JEDEC standards.

$$W_{TOTAL} = (PVDD \times I_{PVDD}) + (TVDD \times I_{TVDD}) - P_{UpStream} + (CVDD \times I_{CVDD}) + (AVDD \times I_{AVDD}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}) + (MVDD \times I_{MVDD})$$

where $P_{UpStream}$ is the quantity of TVDD power consumed on the upstream HDMI transmitter. $P_{UpStream}$ can be estimated to be around 110 mW for a nominal HDMI transmitter.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

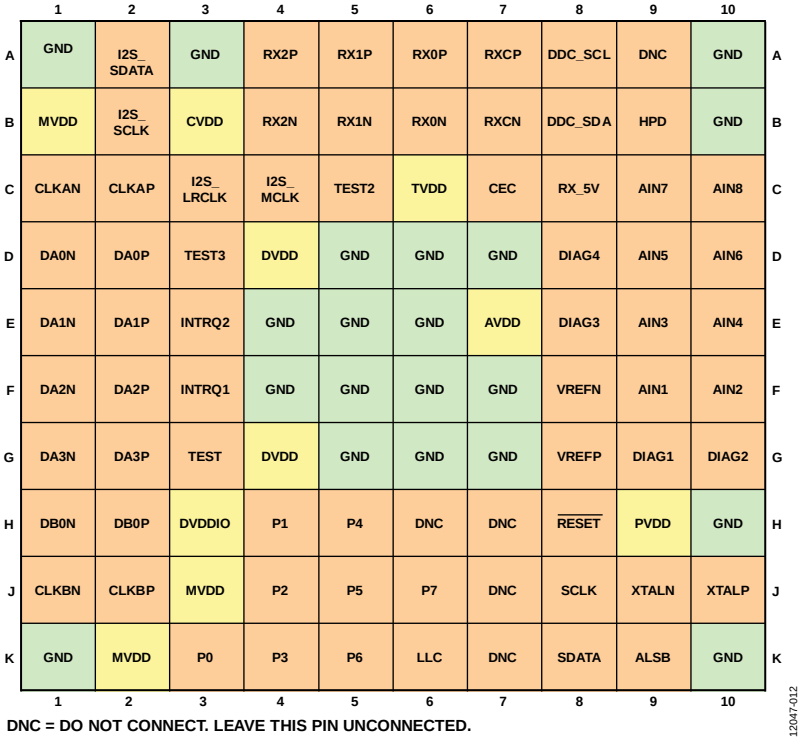



*Figure 9. Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| A1 | GND | Ground | Ground. |
| A2 | I2S_SDATA | Output | I2S Audio Output. |
| A3 | GND | Ground | Ground. |
| A4 | RX2P | HDMI | HDMI Digital Input Channel 2. |
| A5 | RX1P | HDMI | HDMI Digital Input Channel 1. |
| A6 | RX0P | HDMI | HDMI Digital Input Channel 0. |
| A7 | RXCP | HDMI | HDMI Input Clock. |
| A8 | DDC_SCL | HDMI | HDCP Slave Serial Clock. |
| A9 | DNC | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| A10 | GND | Ground | Ground. |
| B1 | MVDD | Power | MIPI Supply Voltage (1.8 V). |
| B2 | I2S_SCLK | Output | Audio Serial Clock. |
| B3 | CVDD | Power | HDMI Comparator Supply Voltage (1.8 V). This is the supply for the HDMI sensitive analog circuitry. Blocks on this supply include the TMDS PLL and the equalizers. |
| B4 | RX2N | HDMI | HDMI Digital Input Channel 2 Complement. |
| B5 | RX1N | HDMI | HDMI Digital Input Channel 1 Complement. |
| B6 | RX0N | HDMI | HDMI Digital Input Channel 0 Complement. |
| B7 | RXCN | HDMI | HDMI Input Clock Complement. |
| B8 | DDC_SDA | HDMI | HDCP Slave Serial Data. |
| B9 | HPD | HDMI | HDMI Hot Plug Assert. |
| B10 | GND | Ground | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| C1 | CLKAN | Output | MIPI Transmitter A Negative Output Clock. |
| C2 | CLKAP | Output | MIPI Transmitter A Positive Output Clock. |
| C3 | I2S_LRCLK | Output | Audio Left/Right Clock. |
| C4 | I2S_MCLK | Output | Audio Master Clock Output. |
| C5 | TEST2 | Miscellaneous | Test Pin 2. Pull down via a large pull-down resistor to ground. |
| C6 | TVDD | Power | HDMI Terminator Supply Voltage (3.3 V). |
| C7 | CEC | HDMI | CEC Channel. |
| C8 | RX_5V | HDMI | HDMI 5 V Detect. A large pull-down resistor (100 kΩ, typical) to ground must be connected to this pin. |
| C9 | AIN7 | Input | Analog Video Input Channel. |
| C10 | AIN8 | Input | Analog Video Input Channel. |
| D1 | DA0N | Output | MIPI Transmitter A Negative Data Output. |
| D2 | DA0P | Output | MIPI Transmitter A Positive Data Output. |
| D3 | TEST3 | Miscellaneous | Test Pin 3. Pull up to DVDDIO via a pull-up resistor (4.7 kΩ). |
| D4 | DVDD | Power | Digital Supply Voltage (1.8 V). |
| D5 | GND | Ground | Ground. |
| D6 | GND | Ground | Ground. |
| D7 | GND | Ground | Ground. |
| D8 | DIAG4 | Input | Analog Video Diagnostic Input. This input is 5 V tolerant. |
| D9 | AIN5 | Input | Analog Video Input Channel. |
| D10 | AIN6 | Input | Analog Video Input Channel. |
| E1 | DA1N | Output | MIPI Transmitter A Negative Data Output. |
| E2 | DA1P | Output | MIPI Transmitter A Positive Data Output. |
| E3 | INTRQ2 | Output | Interrupt Request Output. |
| E4 | GND | Ground | Ground. |
| E5 | GND | Ground | Ground. |
| E6 | GND | Ground | Ground. |
| E7 | AVDD | Power | Analog Supply Voltage (1.8 V). |
| E8 | DIAG3 | Input | Analog Video Diagnostic Input. This input is 5 V tolerant. |
| E9 | AIN3 | Input | Analog Video Input Channel. |
| E10 | AIN4 | Input | Analog Video Input Channel. |
| F1 | DA2N | Output | MIPI Transmitter A Negative Data Output. |
| F2 | DA2P | Output | MIPI Transmitter A Positive Data Output. |
| F3 | INTRQ1 | Output | Interrupt Request Output. |
| F4 | GND | Ground | Ground. |
| F5 | GND | Ground | Ground. |
| F6 | GND | Ground | Ground. |
| F7 | GND | Ground | Ground. |
| F8 | VREFN | Output | Internal Voltage Reference Output. |
| F9 | AIN1 | Input | Analog Video Input Channel. |
| F10 | AIN2 | Input | Analog Video Input Channel. |
| G1 | DA3N | Output | MIPI Transmitter A Negative Data Output. |
| G2 | DA3P | Output | MIPI Transmitter A Positive Data Output. |
| G3 | TEST | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| G4 | DVDD | Power | Digital Supply Voltage (1.8 V). |
| G5 | GND | Ground | Ground. |
| G6 | GND | Ground | Ground. |
| G7 | GND | Ground | Ground. |
| G8 | VREFP | Output | Internal Voltage Reference Output. |
| G9 | DIAG1 | Input | Analog Video Diagnostic Input. This input is 5 V tolerant. |
| G10 | DIAG2 | Input | Analog Video Diagnostic Input. This input is 5 V tolerant. |

| Pin No. | Mnemonic | Type | Description |
|---|---|---|---|
| H1 | DB0N | Output | MIPI Transmitter B Negative Data Output. |
| H2 | DB0P | Output | MIPI Transmitter B Positive Data Output. |
| H3 | DVDDIO | Power | Digital Input/Output Supply Voltage (3.3 V). |
| H4 | P1 | Input/Output | Video Pixel Input/Output Port. |
| H5 | P4 | Input/Output | Video Pixel Input/Output Port. |
| H6 | DNC | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| H7 | DNC | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| H8 | $\overline{\text{RESET}}$ | Input | System Reset Input, Active Low. A minimum low reset pulse of 5 ms is required to reset the chip. |
| H9 | PVDD | Power | PLL Supply Voltage (1.8 V). |
| H10 | GND | Ground | Ground. |
| J1 | CLKBN | Output | MIPI Transmitter B Negative Output Clock. |
| J2 | CLKBP | Output | MIPI Transmitter B Positive Output Clock. |
| J3 | MVDD | Power | MIPI Supply Voltage (1.8 V). |
| J4 | P2 | Input/Output | Video Pixel Input/Output Port. |
| J5 | P5 | Input/Output | Video Pixel Input/Output Port. |
| J6 | P7 | Input/Output | Video Pixel Input/Output Port. |
| J7 | DNC | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| J8 | SCLK | Input | $I^2C$ Port Serial Clock Input. |
| J9 | XTALN | Output | Crystal Output. This pin must be connected to the 28.63636 MHz crystal or not connected if an external 1.8 V, 28.63636 MHz clock oscillator is used. In crystal mode, the crystal must be a fundamental crystal. |
| J10 | XTALP | Input | Crystal Input or External Clock Input. This pin must be connected to the 28.63636 MHz crystal or connected to an external 1.8 V, 28.63636 MHz clock oscillator if a clock oscillator is used. In crystal mode, the crystal must be a fundamental crystal. |
| K1 | GND | Ground | Ground. |
| K2 | MVDD | Power | MIPI Supply Voltage (1.8 V). |
| K3 | P0 | Input/Output | Video Pixel Input/Output Port. |
| K4 | P3 | Input/Output | Video Pixel Input/Output Port. |
| K5 | P6 | Input/Output | Video Pixel Input/Output Port. |
| K6 | LLC | Input/Output | Line Locked Clock. Input/output clock for the pixel data. |
| K7 | DNC | Miscellaneous | Do Not Connect. Leave this pin unconnected. |
| K8 | SDATA | Input/Output | $I^2C$ Port Serial Data Input/Output. |
| K9 | ALSB | Input | Main $I^2C$ Address Selection Pin. This pin selects the main $I^2C$ address (IO Map $I^2C$ address) for the part. When ALSB is set to Logic 0, the IO Map $I^2C$ write address is 0xE0; when ALSB is set to Logic 1, the IO Map $I^2C$ write address is 0xE2. |
| K10 | GND | Ground | Ground. |

# POWER SUPPLY RECOMMENDATION

## POWER-UP SEQUENCE

Adhere to the absolute maximum ratings at all times during power-up (see Table 6). The power-up sequence for the ADV7482 is as follows:

1. Assert $\overline{\text{RESET}}$ (pull the pin low).
2. Power up the 3.3 V supplies ($D_{VDDIO}$ and $T_{VDD}$). These supplies must be powered up simultaneously.
3. Power up the 1.8 V supplies ($D_{VDD}$, $C_{VDD}$, $P_{VDD}$, $M_{VDD}$, and $A_{VDD}$). These supplies must be powered up simultaneously.
4. $\overline{\text{RESET}}$ can be deasserted (pulled high) 5 ms after all supplies are fully powered up.
5. After all power supplies and the $\overline{\text{RESET}}$ pin are powered up and stable, wait an additional 5 ms before initiating $I^2C$ communication with the ADV7482.

## POWER-DOWN SEQUENCE

The ADV7482 power supplies can be deasserted simultaneously as long as a higher rated supply (for example, $D_{VDDIO}$) does not fall to a voltage level less than a lower rated supply (for example, $D_{VDD}$), and the absolute maximum ratings specifications are followed.

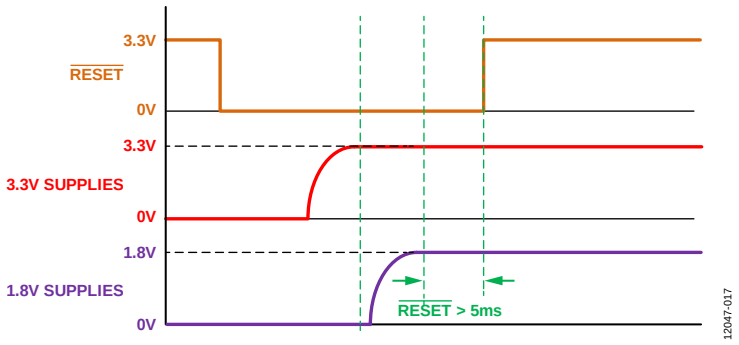



*Figure 10. Supply Power-Up Sequence*

# THOERY OF OPERATION

## HDMI RECEIVER

The HDMI receiver supports video formats ranging from 480i to 1080p, and display resolutions from VGA (640 × 480 at 60 Hz) to UXGA (1600 × 1200 at 60 Hz).

The HDMI receiver allows programmable equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. The receiver is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

The HDMI interface of the ADV7482 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol.

Dual extended display identification data (EDID) support is provided via an on-chip 512-byte EDID RAM. The EDID RAM must be programmed at power-up. It can be configured as two 256-byte EDIDs, or as a single 512-byte EDID.

The ADV7482 has a synchronization regeneration block used to regenerate the data enable (DE) signal based on the measurement of the video format being displayed and to filter the horizontal and vertical synchronization signals to prevent glitches.

The HDMI receiver also supports TMDS error reduction coding, 4-bit (TERC4) error detection, used for the detection of corrupted HDMI packets.

The main HDMI receiver features include

- 162.0 MHz (UXGA at 24 BPP) maximum TMDS clock frequency.
- Integrated fully adaptive equalizer for cable lengths up to 30 meters.
- HDCP 1.4 support.
- Internal HDCP keys.
- HDCP repeater support, up to 25 key selection vectors (KSVs) supported.
- PCM audio packet support.
- Support for 8-channel TDM output data up to 48 kHz.
- Repeater support.
- Internal EDID RAM (512-byte for single mode, and 256-byte for dual mode operation).
- Hot Plug assert output pin (HPD).
- CEC controller.

## COMPONENT PROCESSOR

The ADV7482 has one any-to-any 3 × 3 CSC matrix. The CSC block is located in the processing path before the CP section. CSC enables YCbCr-to-RGB and RGB-to-YCbCr conversions. Many other standards of color space can be implemented using the color space converter.

CP features include

- Support for all video modes supported by the HDMI receiver. These include 525i, 625i, 525p, 625p, 1080i, 1080p, and display resolutions from VGA (640 × 480 at 60 Hz) to UXGA (1600 × 1200 at 60 Hz).
- Manual adjustments including gain (contrast), offset (brightness), hue, and saturation.
- Free run output mode that provides stable timing when no video input is present.
- Timing adjustments controls for HS/VS/DE timing.

## ANALOG FRONT END

The ADV7482 AFE comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the SDP. The AFE uses differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS to be connected directly to the ADV7482.

Up to eight analog inputs can be connected to the AFE. The front end also includes an 8-channel input mux that enables different configurations of single-ended CVBS (up to eight), pseudo differential or fully differential CVBS (up to four), Y/C (up to four), and YPbPr (up to two) analog inputs.

Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter. A resistor divider network is required before each analog input channel to ensure that the input signal is within the range of the ADC. Figure 11 shows a typical voltage divider network for single-ended inputs, Figure 12 shows a typical voltage divider network for pseudo differential inputs, and Figure 13 shows a typical voltage divider network for fully differential inputs. The choice of the resistor divider shown in Figure 13 provides a common-mode range of up to 4 V in fully differential CVBS input mode. Fine clamping of the video signal is performed downstream by digital fine clamping within the ADV7482.

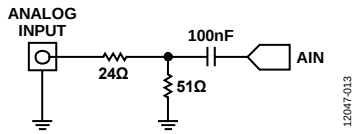



*Figure 11. Typical Single-Ended Input Voltage Divider Network*

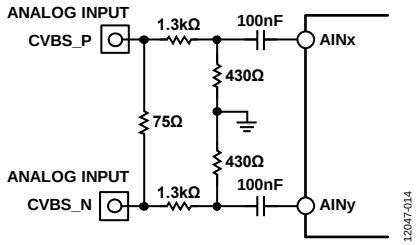



*Figure 12. Typical Pseudo Differential Input Resistor Divider Network*

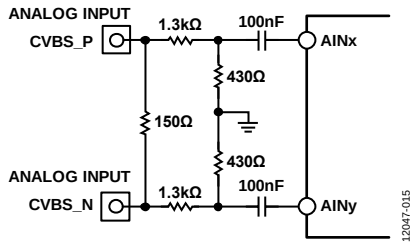



*Figure 13. Typical Fully Differential Input Resistor Divider Network*

The ADC features three clocking rates that allow 4× oversampling per channel for CVBS mode, Y/C mode, and YPbPr mode.

The fully differential AFE of the ADV7482 provides inherent small and large signal noise rejection, improved electromagnetic interference (EMI) protection, and the ability to absorb ground bounce. Support is provided for both true differential and pseudo differential signals.

The main AFE features include

- A single 172 MHz, 10-bit ADC that enables true 8-bit video decoding.
- 8-channel analog input mux that enables multiple source connections without the requirement of an external mux.
- A current clamp control loop that ensures that any dc offsets are removed from the video signal entering the SDP.
- Diagnostic capability on all differential inputs.
- Support for 4 V common-mode input range.
- Support for analog input signals up to 1 V p-p.
- Support for single-ended, pseudo differential, and fully differential inputs.

## SHORT TO BATTERY DIAGNOSTICS

In differential mode, the ADV7482 is protected against STB events by ac coupling capacitors (see Figure 12 and Figure 13). The input network resistors are sized to reduce the current flow during an STB event, thus preventing damage to the resistors. Note that the input network resistors and the ac coupling capacitors must be chosen with ratings guaranteeing they are able to withstand the high voltage of STB events.

The four diagnostic inputs of the ADV7482 provide diagnostic capability for all differential inputs. The ADV7482 can detect an STB event on either the positive or the negative composite input and trigger an interrupt. The 75 Ω (pseudo differential) or 150 Ω (fully differential) parallel termination resistor enables one DIAGx pin to sense an STB event on either input, because there is a minimal voltage drop across the resistor.

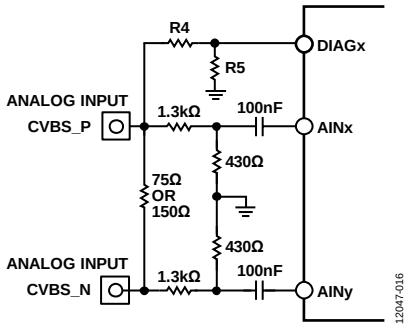



*Figure 14. Diagnostic Connection for Differential Inputs*

Resistors R4 and R5 divide down the voltage at the input connector to protect the DIAGx pin from an STB event. The DIAGx pin circuitry compares this voltage to a programmable reference voltage, known as the diagnostic slice level. When the diagnostic slice level is exceeded, an STB event has occurred.

R4 and R5 are sized to allow the use of low cost, small footprint resistors that are tolerant of STB events.

Use the following equation to find the STB voltage for a selected diagnostic slice level.

$$V_{STB_TRIGGER} = \frac{R5 + R4}{R5} \times DIAGNOSTIC_SLICE_LEVEL$$

where:
$V_{STB_TRIGGER}$ is the minimum voltage required at the input connector to trigger the STB interrupt on the ADV7482.
*DIAGNOSTIC_SLICE_LEVEL* is the programmable reference voltage.

For example, with a diagnostic slice level programmed to 1.125 V, an R4 value of 9.1 kΩ, and an R5 value of 1 kΩ, the minimum voltage required at the input connector to trigger the STB interrupt is approximately 11.4 V.

When the DIAGx pin voltage exceeds the diagnostic slice level voltage, a hardware interrupt is triggered and indicated by one of the interrupt pins. A readback register specifies the input on which the STB event occurred.

## STANDARD DEFINITION PROCESSOR

The ADV7482 is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include

- PAL B, PAL D, PAL G, PAL H, PAL I, PAL M, PAL N, PAL Nc, and PAL 60
- NTSC J, NTSC M, and NTSC 4.43
- SECAM B, SECAM D, SECAM G, SECAM K, and SECAM L

The ADV7482 can automatically detect the video standard and process it accordingly.

The ADV7482 has a five-line adaptive 2D comb filter that provides superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the

video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the ADV7482.

The ADV7482 implements the patented Adaptive Digital Line Length Tracking (ADLLT™) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7482 to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs, VCD players, and camcorders. The ADV7482 contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ACE of the ADV7482 offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. ACE allows the contrast of an image to increase depending on the content of the picture. Typically, this allows bright areas to be made brighter and dark areas to be made darker. However, the ADV7482 ACE feature also allows the contrast within dark areas to increase without significantly affecting the bright areas of the picture. This feature is particularly useful in automotive applications, where it is important to discern objects in shaded areas.

Down dithering converts the output of the ADV7482 from an 8-bit to a 6-bit output, enabling ease of design for standard LCD panels.

The SDP can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), and copy generation management system (CGMS).

The ADV7482 is fully Rovi®(Macrovision®) compliant; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

## 8-BIT DIGITAL INPUT/OUTPUT PORT

The ADV7482 features an 8-bit digital bidirectional port. The following formats are supported both as input and output ports:

- 8-bit interleaved 4:2:2 SDR input/output with embedded timing codes
- 8-bit interleaved 4:2:2 DDR input/output with embedded timing codes

The maximum input and output video resolution supported is 720p/1080i in both SDR and DDR modes.

Video received on the 8-bit digital input port can be routed to the four-lane MIPI CSI-2 transmitter. Video sent on the 8-bit digital output port can be routed from either the SD core or the CP core.

## AUDIO PROCESSING

The ADV7482 features an audio processor that handles the audio extracted from the HDMI stream by the HDMI receiver. It contains an audio mute controller that can detect a variety of conditions that may result in audible extraneous noise in the audio output. On detection of these conditions, a 2-channel linear PCM audio signal can be ramped down to a mute state to prevent audio clicks or pops.

The audio is output on a single flexible serial digital audio output port supporting $I^2S$-compatible, left justified, and right justified audio output modes in master mode only. TDM is also supported, allowing up to eight audio channels with a sample rate up to 48 kHz to be transmitted over the single serial digital audio interface.

## MIPI CSI-2 TRANSMITTERS

The ADV7482 features two MIPI CSI-2 transmitters: a four-lane transmitter (Transmitter A) and a single lane transmitter (Transmitter B).

The four-lane transmitter consists of four differential data lanes (DA0N, DA0P, DA1N, DA1P, DA2N, DA2P, DA3N and DA3P), and a differential clock lane (CLKAN and CLKAP). It supports four data lanes, two data lanes, and one data lane muxing options, and can be used to transmit video received on either the HDMI receiver (processed through the CP), the 8-bit digital input port, or the AFE (processed through the SDP).

The main features of the four-lane MIPI transmitter (Transmitter A) include

- Support for 8-bit and 10-bit YCbCr 4:2:2 video modes.
- Support for 24-bit RGB 4:4:4 (RGB888), 18-bit RGB 4:4:4 (RGB666), and 16-bit RGB 4:4:4 (RGB565) video modes.
- Support for video formats ranging from 480i to 1080p, and display resolutions from VGA to UXGA (certain restrictions apply to the muxing option, video mode, and video format that can be selected).
- Data lanes and clock lane remapping to ease PCB layout.

The single lane transmitter consists of a single differential data lane (DB0N and DB0P) and a differential clock lane (CLKBN and CLKBP). It transmits video received on the AFE (processed through the SDP).

The main features of the single lane MIPI transmitter (Transmitter B) include

- Support for 8-bit YCbCr 4:2:2 video mode.
- Support for 480i and 576i video formats.

## INTERRUPTS

The ADV7482 features two interrupt request pins. INTRQ1 and INTRQ2 can be programmed to trigger interrupts based on various selectable events related to the HDMI receiver (video and audio related), the SDP, and the CP.

# OUTLINE DIMENSIONS

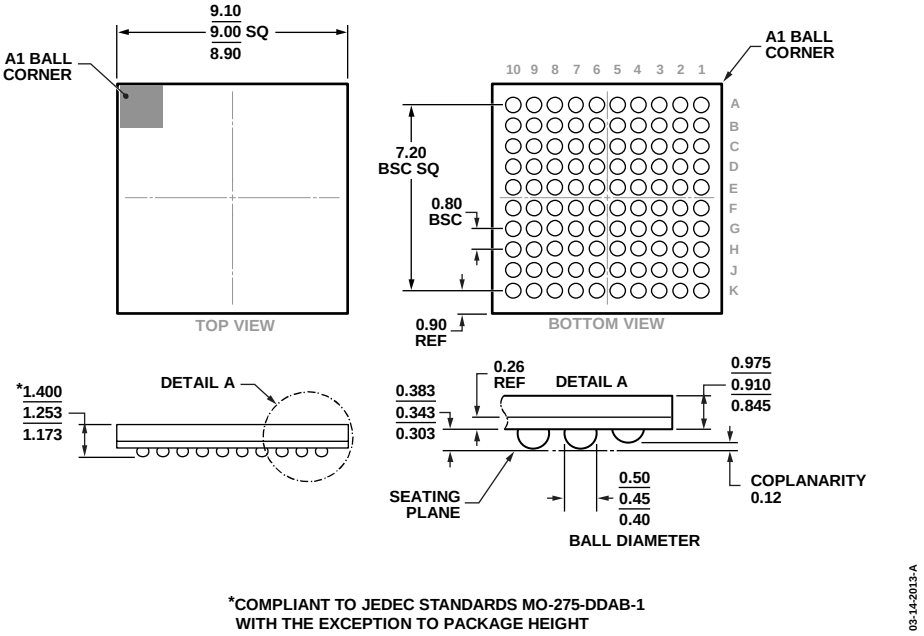



*Figure 15. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]*
*(BC-100-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2, 3] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADV7482WBBCZ | −40°C to +85°C | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4 |
| ADV7482WBBCZ-RL | −40°C to +85°C | 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-100-4 |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] This device is programmed with internal HDCP keys. Customer must have HDCP adopter status (consult Digital Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys

## AUTOMOTIVE PRODUCTS

The ADV7482W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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D12047-0-6/14(0)

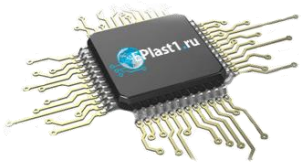
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- Техническая поддержка проекта;
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**Как с нами связаться**

**Телефон:** 8 (812) 309 58 32 (многоканальный)
**Факс:** 8 (812) 320-02-42
**Электронная почта:** org@eplast1.ru
**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.