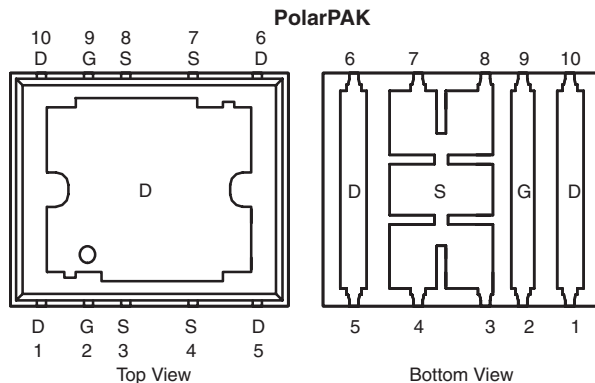




N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a		Q _g (Typ.)
		Silicon Limit	Package Limit	
20	0.00117 at V _{GS} = 10 V	258	60	45 nC
	0.0016 at V _{GS} = 4.5 V	220	60	

Package Drawing
www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10
Ordering Information: SiE874DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

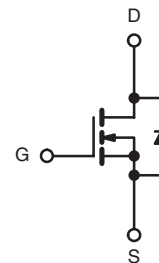
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Gen III Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size, ≤ 100 V
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- POL
- OR-ing
- DC/DC



N-Channel MOSFET

For Related Documents
www.vishay.com/ppg?65350

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	20	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	258 (Silicon Limit)	A
		T _C = 70 °C	60 ^a (Package Limit)	
		T _A = 25 °C	60 ^a	
		T _A = 70 °C	52 ^{b, c}	
Pulsed Drain Current	I _{DM}	100		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	60 ^a	
		T _A = 25 °C	4.3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	40		
Avalanche Energy	E _{AS}	80	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	125	W
		T _C = 70 °C	80	
		T _A = 25 °C	5.2 ^{b, c}	
		T _A = 70 °C	3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		260		

Notes:

- Package limit is 60 A.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	$t \leq 10$ s	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top)	Steady State	R_{thJC} (Drain)	0.8	1	
Maximum Junction-to-Case (Source) ^{a, c}		R_{thJC} (Source)	2.2	2.7	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
b. Maximum under Steady State conditions is 68 °C/W.
c. Measured at source pin (on the side of the package).

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = 250$ μ A	20			V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ μ A		20		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		- 6.5				
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ μ A	1.0	1.7	2.2	V	
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1	μ A	
		$V_{DS} = 20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	25			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 20$ A		0.00095	0.00117	Ω	
		$V_{GS} = 4.5$ V, $I_D = 20$ A		0.0013	0.0016		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15$ V, $I_D = 20$ A		110		S	
Dynamic^b							
Input Capacitance	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		6200		pF	
Output Capacitance	C_{oss}		1800				
Reverse Transfer Capacitance	C_{rss}		760				
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 10$ V, $I_D = 20$ A		95	145	nC	
Gate-Source Charge	Q_{gs}	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 20$ A		45	65		
Gate-Drain Charge	Q_{gd}		16				
Gate Resistance	R_g		13				
Turn-On Delay Time	$t_{d(on)}$	$f = 1$ MHz	0.2	1.1	2.2	Ω	
Rise Time	t_r		$V_{DD} = 10$ V, $R_L = 1$ Ω $I_D \cong 10$ A, $V_{GEN} = 4.5$ V, $R_g = 1$ Ω	45	70		ns
Turn-Off Delay Time	$t_{d(off)}$			35	55		
Fall Time	t_f			60	90		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 1$ Ω $I_D \cong 10$ A, $V_{GEN} = 10$ V, $R_g = 1$ Ω	20	30			
Rise Time	t_r		10	15			
Turn-Off Delay Time	$t_{d(off)}$		55	85			
Fall Time	t_f		10	15			
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C			60	A	
Pulse Diode Forward Current ^a	I_{SM}				100		
Body Diode Voltage	V_{SD}	$I_S = 10$ A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10$ A, $di/dt = 100$ A/ μ s, $T_J = 25$ °C		60	90	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		75	115	nC		
Reverse Recovery Fall Time	t_a		27		ns		
Reverse Recovery Rise Time	t_b		33				

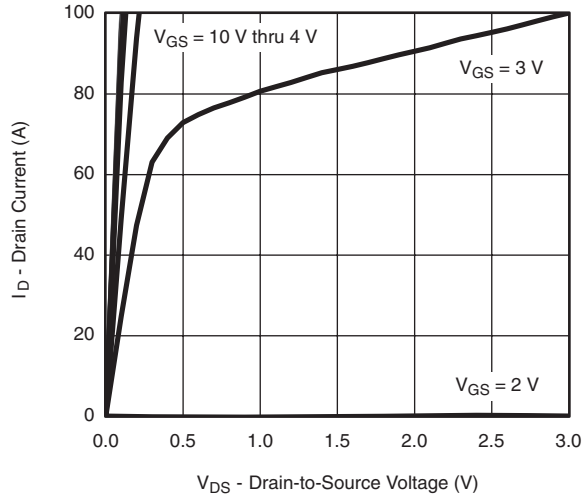
Notes:

- a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

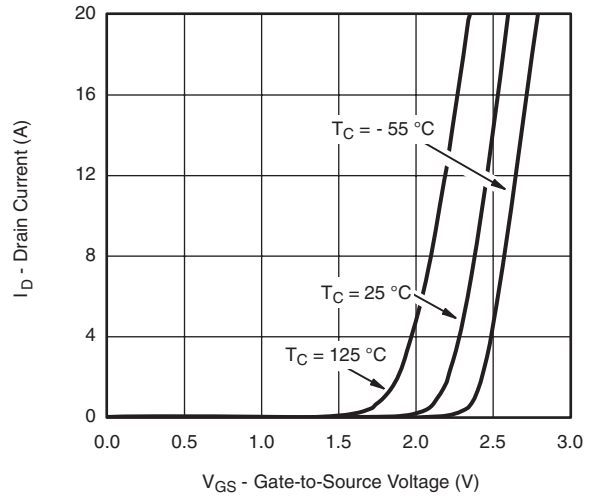
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



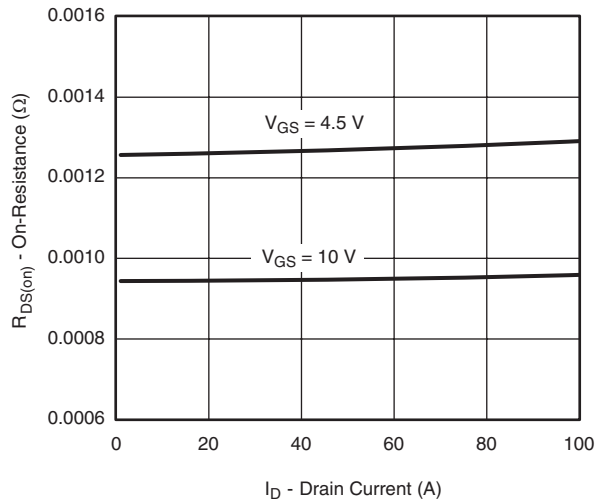
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



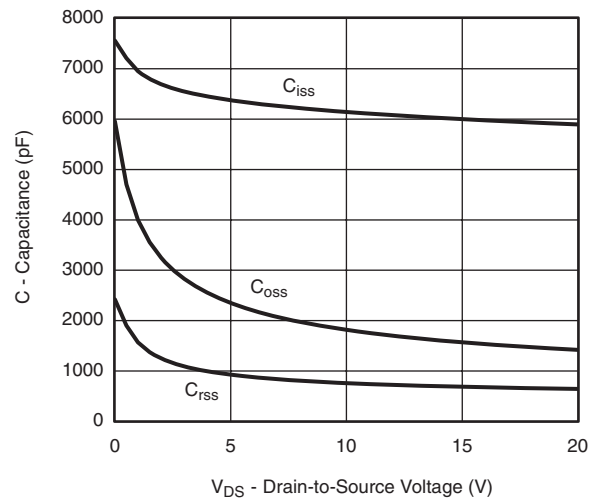
Output Characteristics



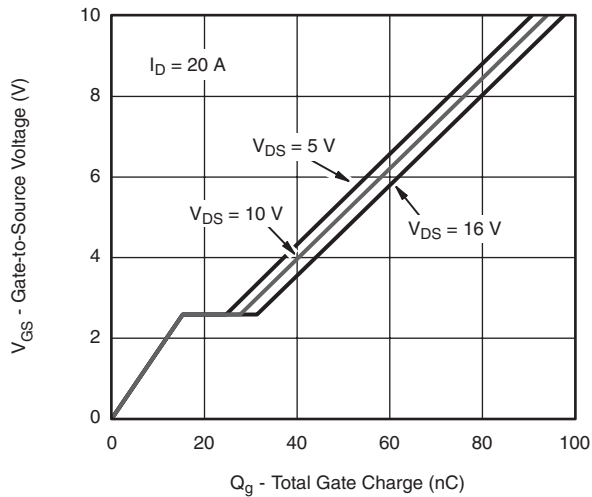
Transfer Characteristics



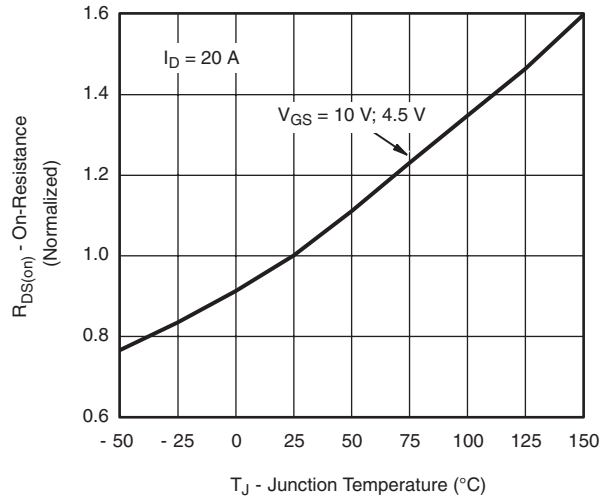
On-Resistance vs. Drain Current



Capacitance



Gate Charge



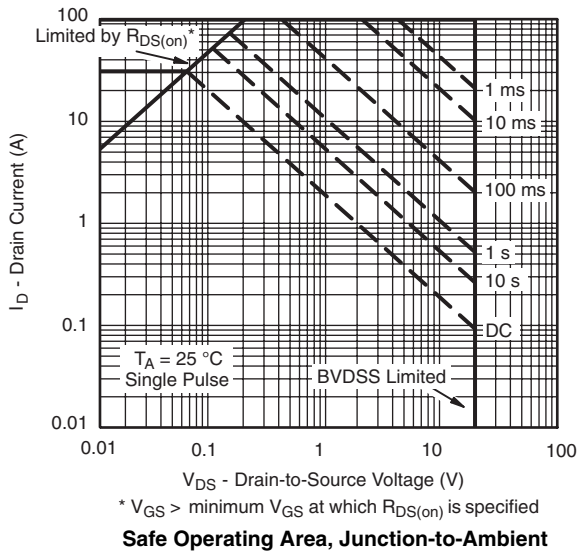
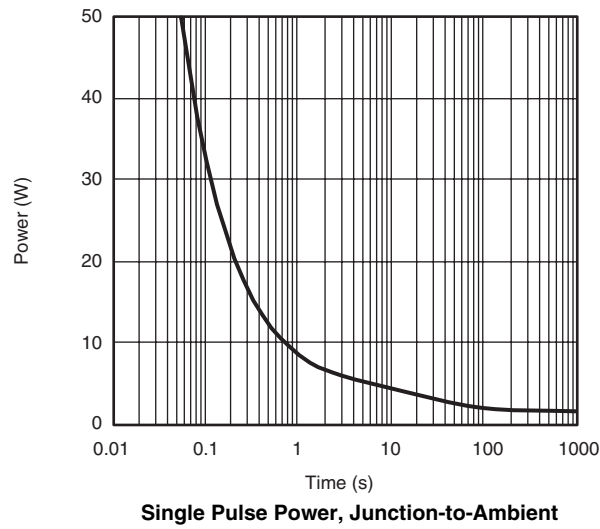
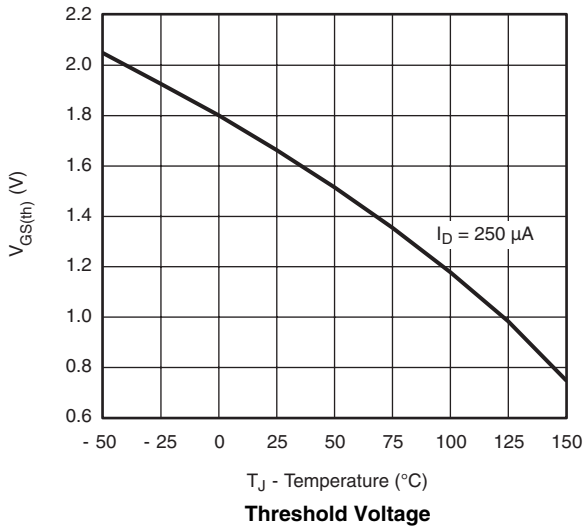
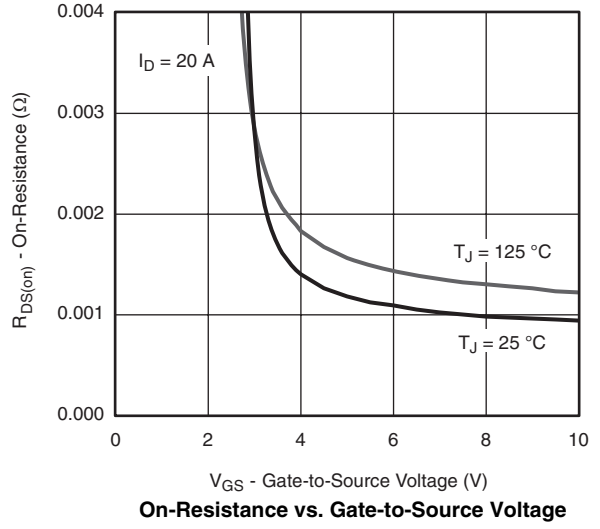
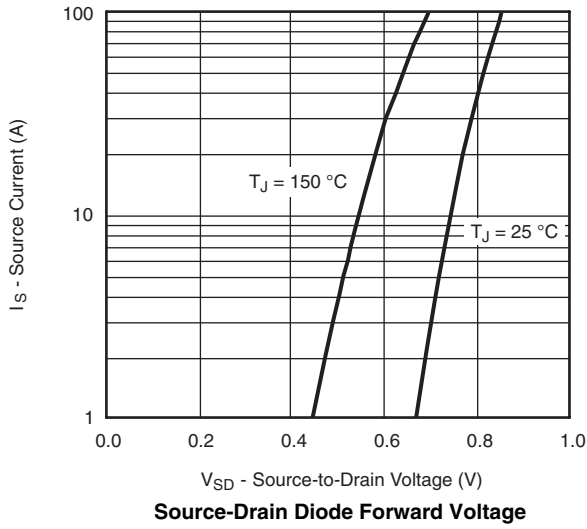
On-Resistance vs. Junction Temperature

SiE874DF

Vishay Siliconix

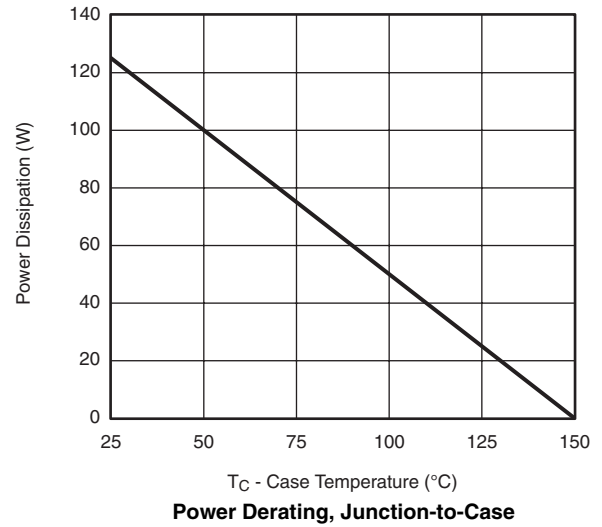
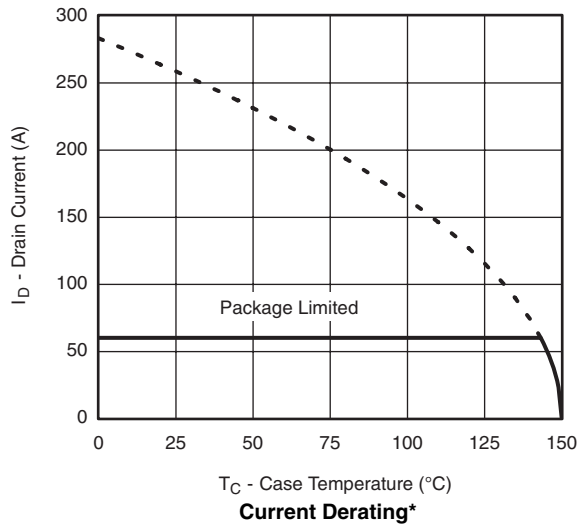


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



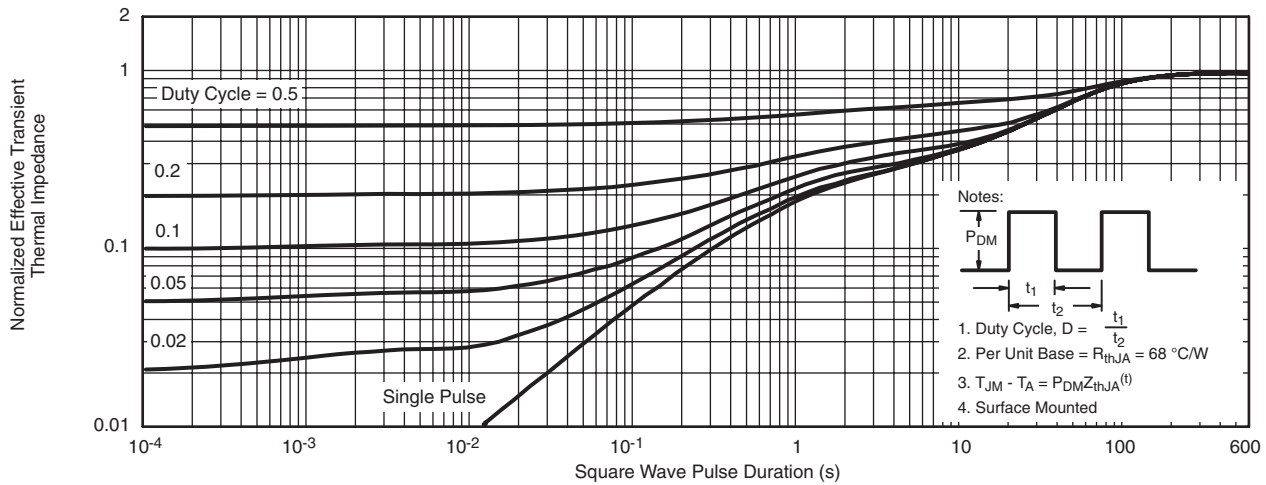


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

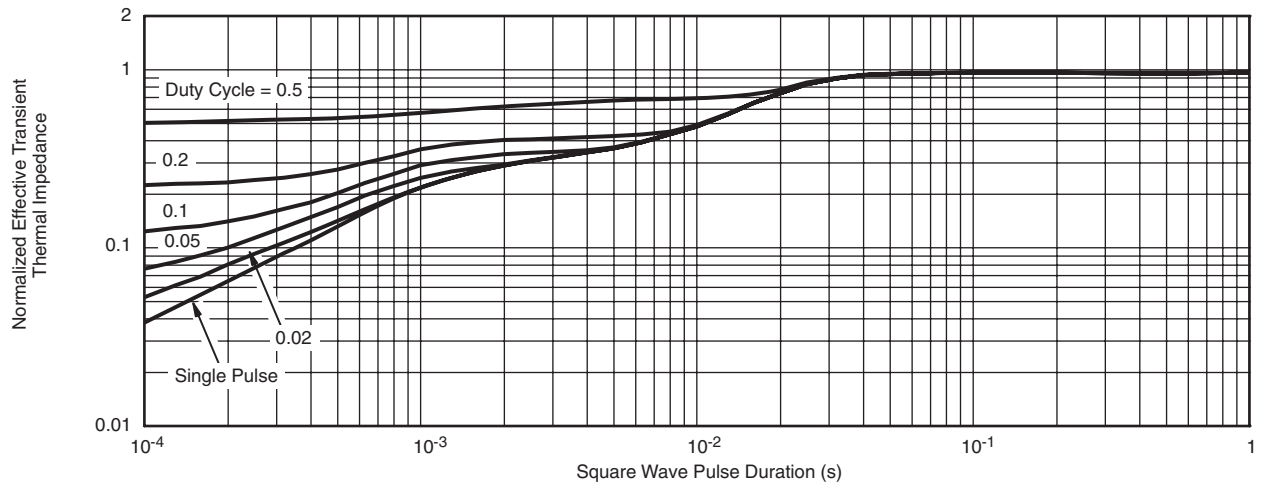


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

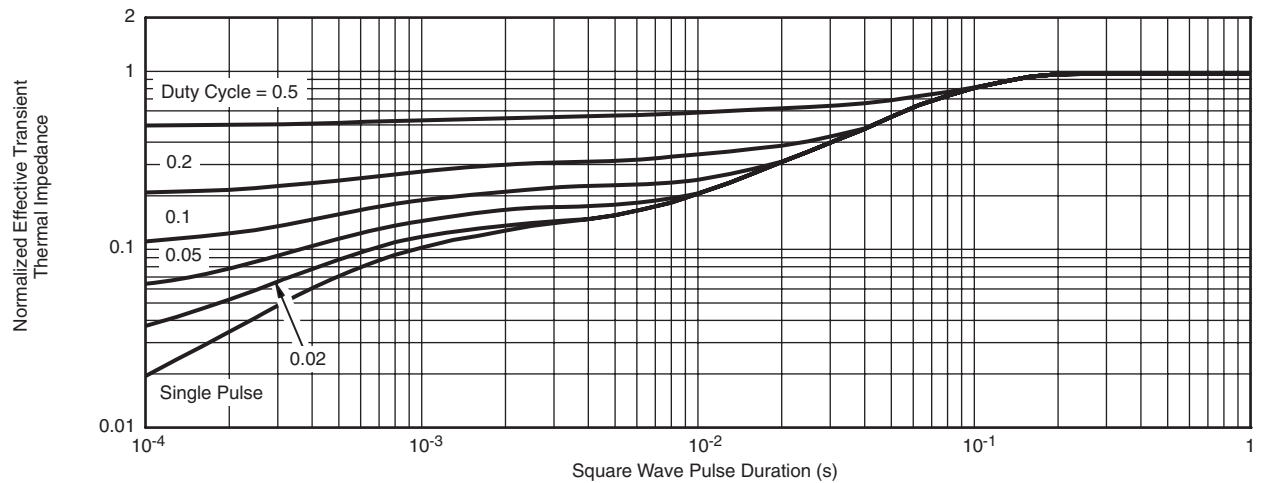
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)



Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65350.



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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