# CY25568

# Spread Spectrum Clock Generator

## Features

- 4 to 32 MHz Input frequency range
- 4 to 128 MHz Output frequency range
- accepts clock, crystal and resonator Inputs
- 1x, 2x and 4x frequency multiplication
- Non-modulated reference frequency output
- Center and down spread modulation
- Low power dissipation
  - 3.3 V = 52 mW-typ at 6 MHz
  - 3.3 V = 60 mW-typ at 12 MHz
  - 3.3 V = 72 mW-typ at 24 MHz
- Power-down mode
- Low cycle-to cycle jitter
  - 8 MHz = 195 ps-typ
  - 16 MHz = 175 ps-typ
  - 32 MHz = 100 ps-typ
- Available in 16-pin (150-mil.) SOIC package

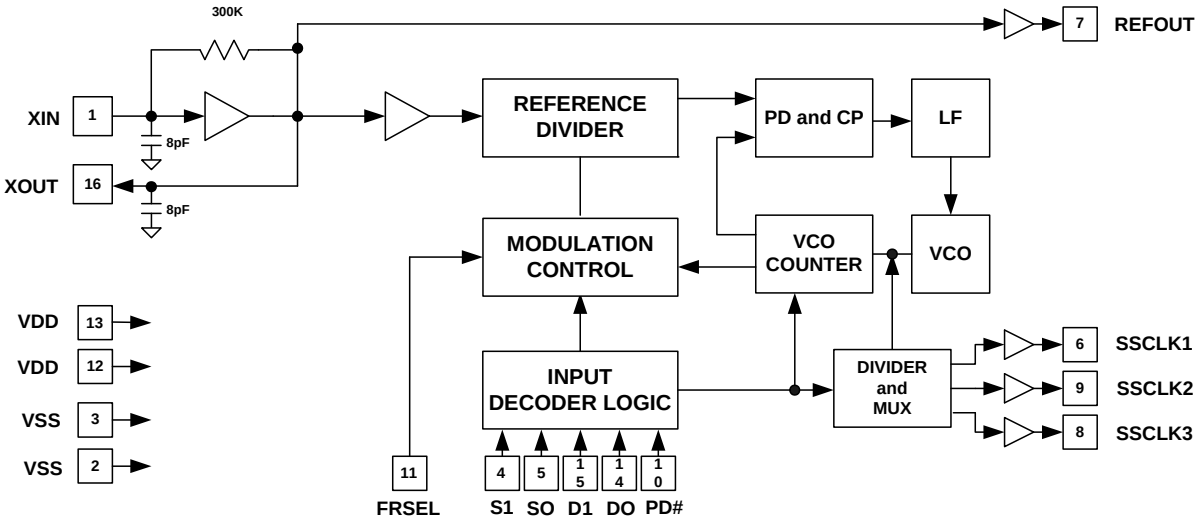
## Applications

- Printers and MFPs
- LCD panels and monitors
- Digital copiers
- PDAs
- Automotive
- CD-ROM, VCD and DVD
- Networking, LAN/WAN
- Scanners
- Modems
- Embedded digital systems

## Benefits

- Peak EMI reduction by 8 to 16dB
- Fast time to market
- Cost reduction

## Logic Block Diagram

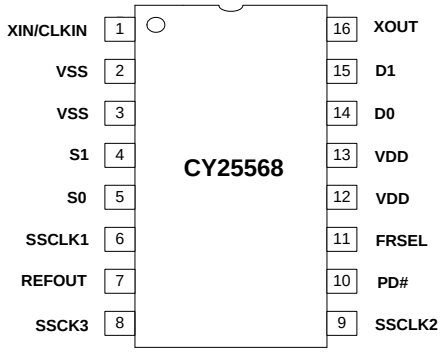


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## Pinouts

**Figure 1. CY25568 - 16 Pin SOIC**




## Pin Definitions

| Pin | Function | Description |
|---|---|---|
| 1 | Xin/CLK | Clock, crystal or ceramic resonator input pin |
| 2 | $V_{SS}$ | Power supply ground. |
| 3 | $V_{SS}$ | Power supply ground. |
| 4 | S1 | Digital Spread% control pin 3-Level input (H-M-L). Default= M. |
| 5 | S0 | Digital Spread% control pin 3-Level input (H-M-L). Default= M. |
| 6 | SSCLK1 | Output clock. Refer to Table 2 on page 5 for frequency programmability. |
| 7 | REFOUT | Reference clock output. The same frequency as Xin/CLK input. |
| 8 | SSCLK3 | Output clock. Refer to Table 2 on page 5 for frequency programmability. |
| 9 | SSCLK2 | Output clock. Refer to Table 2 on page 5 for frequency programmability. |
| 10 | PD# | Power-down control Internally pulled to $V_{DD}$, Default= High. |
| 11 | FRSEL | Input frequency range selection digital control input 3-Level input (H-M-L). Default= M. |
| 12 | $V_{DD}$ | Positive power supply. |
| 13 | $V_{DD}$ | Positive power supply. |
| 14 | D0 | 3-Level (H-M-L) Digital output clock scaling control. Refer to Table 2 on page 5. Default= M. |
| 15 | D1 | 3-Level (H-M-L) Digital output clock scaling control. Refer to Table 2 on page 5. Default= M. |
| 16 | XOUT | Crystal or ceramic resonator output pin |

## General Description

The Cypress CY25568 is a spread spectrum clock generator (SSCG) IC used for the purpose of reducing electro magnetic interference (EMI) found in today's high-speed digital electronic systems.

The CY25568 uses a Cypress proprietary phase-locked loop (PLL) and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the digital clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies is greatly reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time to market without degrading system performance.

The CY25568 input frequency range is 4 to 32 MHz and accepts clock, crystal, and ceramic resonator inputs. The output clocks can be programmed to produce 1x, 2x, and 4x multiplication of the input frequency with spread spectrum. A separate non-modulated reference clock is also provided.

The use of 2x or 4x frequency multiplication eliminates the need for higher order crystals and allows the user to generate up to 128 MHz spread spectrum clock (SSC) by using only first order crystals. This reduces the cost while improving the system clock accuracy, performance and complexity

center spread or down spread frequency modulation can be selected by the user based on 4 discrete values of Spread% for each spread mode with the option of a non-spread mode for system test and verification purposes.

The CY25568 is available in a 16 pin SOIC (150-mil.) package with a commercial operating temperature range of 0 to 70 °C. Contact Cypress for availability of –25 to +85 °C industrial temperature range operation. Refer to CY25811/12/14 products for 8-pin SOIC package versions of the CY25568.

## Absolute Maximum Ratings [1]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply voltage ($V_{DD}$): .....+5.5 V

Input voltage relative to $V_{DD}$: ..... $V_{DD}$+0.3 V

Input voltage relative to VSS: ..... $V_{SS}$–0.3 V

Operating temperature: ..... 0 to 70 ° c

storage Temperature: ..... –65 to +150 ° C

**Note**: Operation at any Absolute Maximum Rating is not implied.

## DC Electrical Characteristics

Test Conditions: $V_{DD}$=3.3 V, T=25, unless otherwise noted

| Symbol | Parameter | Min | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| VDD | Power supply range | 2.90 | 3.3 | 3.60 | V | |
| VINH | Input high voltage | 0.85 $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V | S0,S1,D0,D1 and FRSEL Inputs |
| VINM | Input middle voltage | 0.40$V_{DD}$ | 0.50$V_{DD}$ | 0.60$V_{DD}$ | V | S0,S1,D0,D1 and FRSEL Inputs |
| VINL | Input low voltage | 0.0 | 0.0 | 0.15$V_{DD}$ | V | S0,S1,D0,D1 and FRSEL Inputs |
| VINH1 | Input high voltage | 2.0 | - | - | V | PD# input only |
| VINL1 | Input low voltage | - | - | 0.8 | V | PD# input only |
| VOH1 | Output high voltage | 2.4 | - | - | V | IOH = 4 ma, all output clocks |
| VOH2 | Output high voltage | 2.0 | - | - | V | IOH = 6 ma, all output clocks |
| VOL1 | Output low voltage | - | - | 0.4 | V | IOL = 4 ma, all output clocks |
| VOL2 | Output low voltage | - | - | 1.2 | V | IOL = 10 ma, all output clocks |
| Cin1 | Input capacitance | 6.0 | 7.5 | 9.0 | pF | Xin (Pin 1) and Xout (Pin 16) |
| Cin2 | Input capacitance | 3.5 | 4.5 | 6.0 | pF | All digital inputs |
| IDD1 | Power supply current | - | 13.0 | 16.0 | mA | Fin=4 MHz, no load (refer to Figure 4 on page 8) |
| IDD2 | Power supply current | - | 28.0 | 32.0 | mA | Fin=32 MHz, no load (refer to Figure 4 on page 8) |
| IDD3 | Power supply current | - | 300 | 400 | ìA | PD#=GND |

## Timing Electrical Characteristics

Test Conditions: $V_{DD}$=3.3 V, T=25 C, CL=15pF. Rise/Fall time at 0.4 and 2.4 V, duty cycle at 1.5 V

| Symbol | Parameter | Min | Typ. | Max | Unit | Conditions |
|---|---|---|---|---|---|---|
| ICLKFR | Input frequency range | 4 | | 32 | MHz | Clock, crystal or ceramic resonator input |
| trise1 | Clock rise time | 2.4 | 3.2 | 4.0 | ns | SSCLK1,2, and 3, all cases when 1x or 2x scaling selected, when 4x if FRSEL=1 or 0 |
| tfall1 | Clock fall time | 2.4 | 3.2 | 4.0 | ns | SSCLK1,2, and 3, all cases when 1x or 2x scaling selected, when 4x if FRSEL=1 or 0 |
| trise2 | Clock rise time | 1.2 | 1.6 | 2.0 | ns | SSCLK2, and 3, only when 4x scaling is selected and FRSEL=M |
| tfall2 | Clock fall time | 1.2 | 1.6 | 2.0 | ns | SSCLK2, and 3, only when 4x scaling is selected and FRSEL=M |
| trise3 | Clock rise time | 2.4 | 3.2 | 4.0 | ns | REFOUT only |
| tfall3 | Clock fall time | 2.4 | 3.2 | 4.0 | ns | REFOUT only |
| CDCin | Input clock duty cycle | 20 | 50 | 80 | % | XIN/CLK (Pin 1) |
| CDCout | Output clock duty cycle | 45 | 50 | 55 | % | SSCLK1,2 and 3 |
| CCJ1 | Cycle-to-cycle jitter | - | 195 | 260 | ps | Fin=8 MHz (refer to Figure 4 on page 8) |
| CCJ2 | Cycle-to-cycle jitter | - | 170 | 225 | ps | Fin=16 MHz (refer to Figure 4 on page 8) |

**Notes**

1. Single Power Supply: The voltage on any input or IO pin cannot exceed the power pin during power-up.

## Timing Electrical Characteristics

Test Conditions: $V_{DD}$=3.3 V, T=25 C, CL=15pF. Rise/Fall time at 0.4 and 2.4 V, duty cycle at 1.5 V

| | | | | | | |
|---|---|---|---|---|---|---|
| CCJ3 | Cycle-to-cycle jitter | - | 100 | 150 | ps | Fin=32 MHz (refer to Figure 4A) |

## Input Frequency Range and Selection

The CY25568 input frequency range is 4 to 32 MHz. This range is divided into 3 segments and controlled by 3-Level FRSEL pin as given in Table 1.

**Table 1. Input Frequency Selection**

| FRSEL | INPUT FREQUENCY RANGE |
|---|---|
| 0 | 4.0 to 8.0 MHz |
| 1 | 8.0 to 16.0 MHz |
| M | 16.0 to 32.0 MHz |

### Output Clocks

The CY25568 provides 4 separate output clocks, REFOUT, SSCLK1, SSCLK2 and SSCLK3, for use in a wide variety of applications.Each clock output is described in detail.

### REFOUT

REFOUT is a 3.3 volt CMOS level non-modulated copy of the clock at XIN/CLKIN.

### SSCLK1, 2 and 3

SSCLK1, SSCLK2 and SSCLK3 are Spread Spectrum clock outputs used for the purpose of reducing EMI in digital systems. Each clock can drive separate nets with a capacitive load of up to 20 pF.

The frequency function of these clock outputs are selected by using 3-Level D0 and D1 digital inputs and are given in Table 2.

**Table 2. Output Clocks Function Selection**

| D0 | D1 | REFOUT | SSCLK1 | SSCLK2 | SSCLK3 |
|---|---|---|---|---|---|
| 0 | 0 | REF | REF | 1x | 1x |
| 0 | M | REF | 1x | 2x | 2x |
| 0 | 1 | REF | REF | 2x | 2x |
| M | 0 | REF | REF | 1x | 2x |
| M | M | REF | REF | REF | REF |
| M | 1 | REF | REF | 2x | 4x |
| 1 | 0 | REF | REF | 4x | 4x |
| 1 | M | REF | 1x | 2x | 4x |
| 1 | 1 | REF | 1x | 2x | 4x |

REF is the same non-modulated frequency as the input clock.

1x, 2x, or 4x are modulated and multiplied (in the case of 2x and 4x) frequency of the input clock.

## Spread % Selection

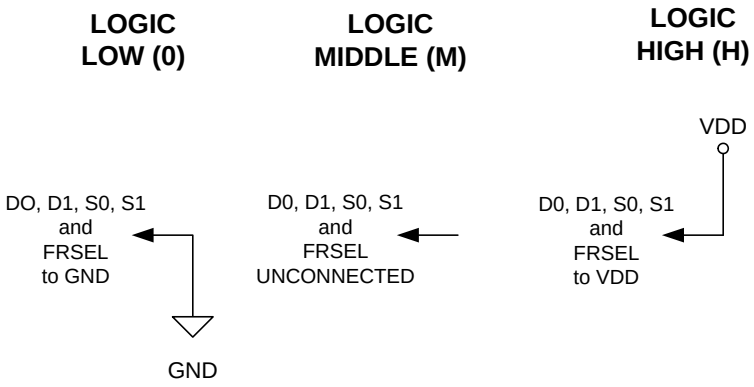
The CY25568 provides Center-Spread, Down-Spread and No-Spread functions. These functions and the amount of Spread% are selected by using 3-Level S0 and S1 digital inputs and are given in Table 3.

**Table 3. Spread% Selection**

| XIN (MHz) | FRSEL | S1=0 S0=0 | S1=0 S0=M | S1=0 S0=1 | S1=M S0=0 | S1=1 S0=1 | S1=1 S0=0 | S1=M S0=1 | S1=1 S0=M | S1=M S0=M |
|---|---|---|---|---|---|---|---|---|---|---|
| | | CENTER (%) | CENTER (%) | CENTER (%) | CENTER (%) | DOWN (%) | DOWN (%) | DOWN (%) | DOWN (%) | NO SPREAD |
| 4-5 | 0 | +/–1.4 | +/–1.2 | +/–0.6 | +/–0.5 | –3.0 | –2.2 | –1.9 | –0.7 | 0 |
| 5-6 | 0 | +/–1.3 | +/–1.1 | +/–0.5 | +/–0.4 | –2.7 | –1.9 | –.7 | –0.6 | 0 |
| 6-7 | 0 | +/–1.2 | +/–0.9 | +/–0.5 | +/–0.4 | –2.5 | –1.8 | –1.5 | –0.6 | 0 |
| 7-8 | 0 | +/–1.1 | +/–0.9 | +/–0.4 | +/–0.3 | –2.3 | –1.7 | –1.4 | –0.5 | 0 |
| 8-10 | 1 | +/–1.4 | +/–1.2 | +/–0.6 | +/–0.5 | –3.0 | –2.2 | –1.9 | –0.7 | 0 |
| 10-12 | 1 | +/–1.3 | +/–1.1 | +/–0.5 | +/–0.4 | –2.7 | –1.9 | –1.7 | –0.6 | 0 |
| 12-14 | 1 | +/–1.2 | +/–0.9 | +/–0.5 | +/–0.4 | –2.5 | –1.8 | –1.5 | –0.6 | 0 |
| 14-16 | 1 | +/–1.1 | +/–0.9 | +/–0.4 | +/–0.3 | –2.3 | –1.7 | –1.4 | –0.5 | 0 |
| 16-20 | M | +/–1.4 | +/–1.2 | +/–0.6 | +/–0.5 | –3.0 | –2.2 | –1.9 | –0.7 | 0 |
| 20-24 | M | +/–1.3 | +/–1.1 | +/–0.5 | +/–0.4 | –2.7 | –1.9 | –1.7 | –0.6 | 0 |
| 24-28 | M | +/–1.2 | +/–0.9 | +/–0.5 | +/–0.4 | –2.5 | –1.8 | –1.5 | –0.6 | 0 |
| 28-32 | M | +/–1.1 | +/–0.9 | +/–0.4 | +/–0.3 | –2.3 | –1.7 | –1.4 | –0.5 | 0 |

### 3-Level Digital Inputs

**Figure 2. 3-Level Logic**




S0, S1, D0, D1, and FRSEL digital inputs of the CY25568 are designed to sense 3 different logic levels designated as High - 1, Low- 0 and Middle- M. With this 3-Level digital input logic, the CY25568 is able to detect 9 different logic states in the case of (S0, S1) and (D0, D1) logic pairs and 3 different logic states in the case of FRSEL.

S0, S1, D0, D1, and FRSEL pins include an on chip 20K (10K /10K) resistor divider. No external application resistors are needed to implement the 3-Level logic levels as shown in the following:

Logic State 0 = 3-Level logic pin connected to GND.

Logic State M = 3-Level logic pin left floating (no connection).

Logic State 1 = 3-Level logic pin connected to VDD.

Figure 2 illustrates how to implement 3-Level Logic.

### Power-down (PD#)

CY25568 includes a Power-down (PD#, Pin 10) function. This input uses standard 2-Level CMOS logic and is internally pulled up to VDD (HIGH). Connect this pin to GND if power is to be turned off.

### Modulation Rate

Spread Spectrum Clock Generators use frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (fmax) and minimum frequency of the clock (fmin) determine this band of frequencies. The time required to transition from fmin to fmax and back to fmin is the period of the Modulation Rate, Tmod. The Modulation Rate of SSCG clocks are generally referred to in terms of frequency or fmod = 1/Tmod.

The input clock frequency, fin, and the internal divider determine the modulation rate.

In the case of CY25568, the (spread spectrum) modulation rate is given by the following formula: fmod = fin/DR

Where; fmod is the modulation rate, fin is the Input Frequency and DR is the divider ratio as given in Table 4. Notice that Input frequency range is set by FRSEL.

**Table 4. Modulation Rate**

| FRSEL | INPUT FREQUENCY RANGE (MHz) | DIVIDER RATIO (DR) |
|---|---|---|
| 0 | 4 to 8 | 128 |
| 1 | 8 to 16 | 256 |
| M | 16 to 32 | 512 |

## Characteristic Curves

The following curves demonstrate the characteristic behavior of the CY25568 when tested over a number of environmental and application specific parameters. These are typical performance curves and are not meant to replace any parameter specified in tables "DC Electrical Characteristics" on page 4 and "Timing Electrical Characteristics" on page 4.

**Figure 3. Jitter vs. Input Frequency (No Load)**

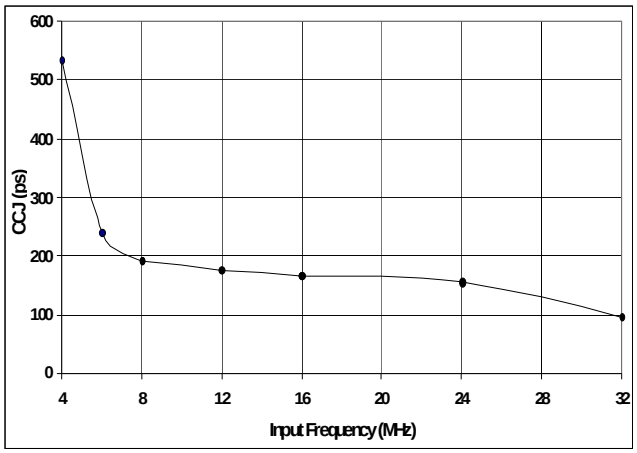



**Figure 4. Bandwidth% vs. Temperature**

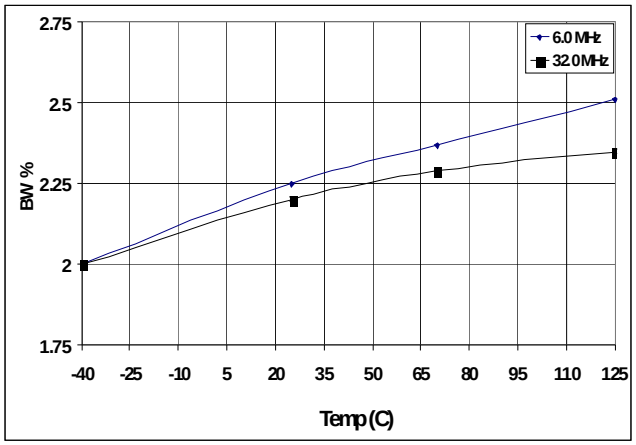



**Figure 5. IDD vs. Frequency (FRSEL = 0, 1, M)**

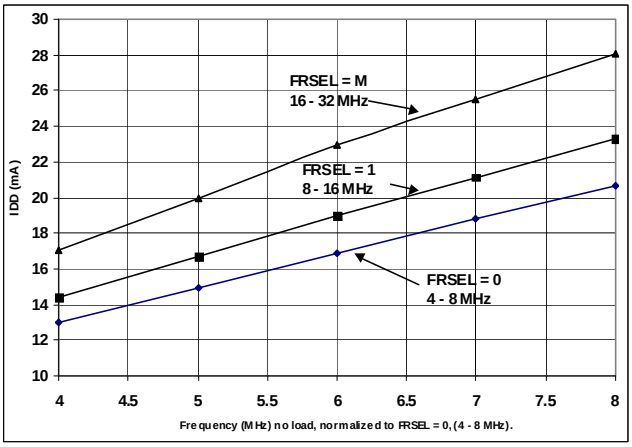
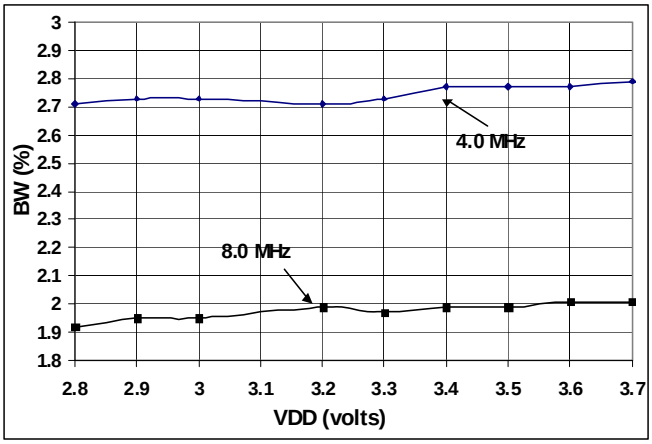


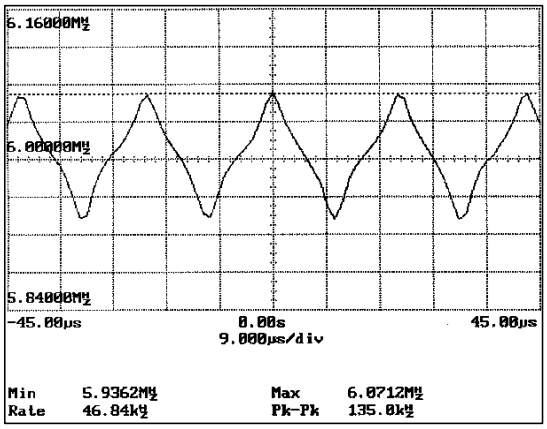

**Figure 6. Bandwidth% vs. VDD**



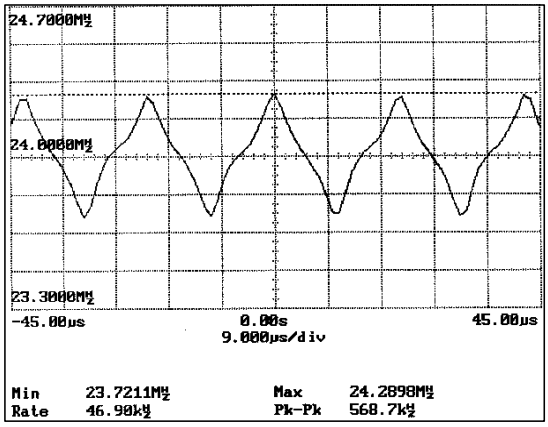
## SSCG Profiles

The CY25568 uses a non-linear frequency profile as shown in Figure 7. The use of Cypress proprietary “optimized” frequency profile maintains flat energy distribution over the fundamental and higher order harmonics. This results in additional EMI reduction in electronic systems.

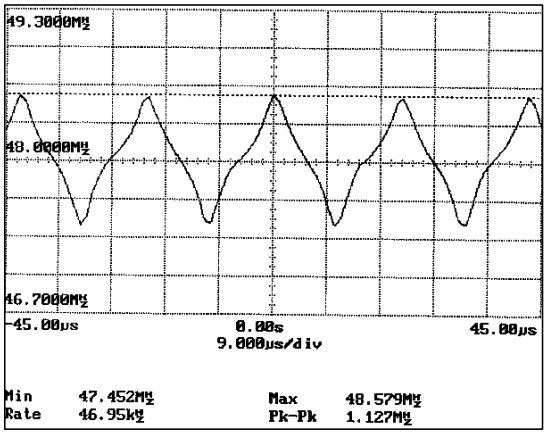
**Figure 7. Spread Spectrum Profiles (Frequency versus Time)**



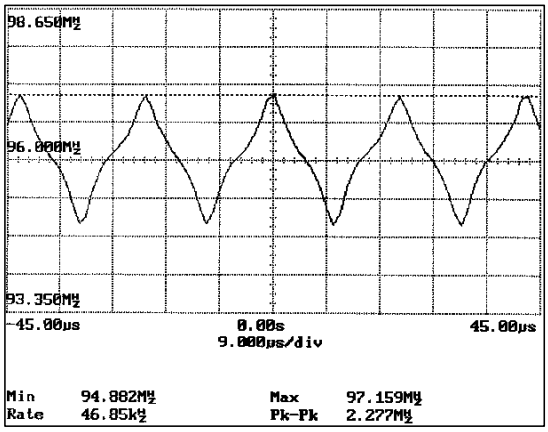

| | |
|---|---|
| Xin = 6.0 MHz | SSCLK1 = 6.0 MHz |
| S1. S0 = 0 | D1. D0 = 1 |




| | |
|---|---|
| Xin = 24.0 MHz | SSCLK1 = 24.0 MHz |
| S1, S0 = 0 | D1, D0 = 1 |



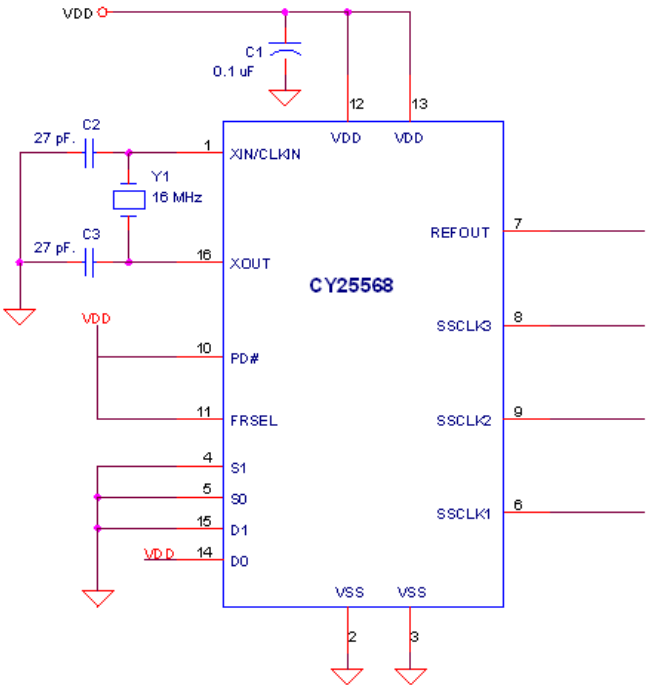

| | |
|---|---|
| Xin = 12.0 MHz | SSCLK1 = 48.0 MHz |
| S1. S0 = 0 | D1. D0 = 1 |




| | |
|---|---|
| Xin = 24.0 MHz | SSCLK1 = 96.0 MHz |
| S1. S0 = 0 | D1. D0 = 1 |

## Application Schematic

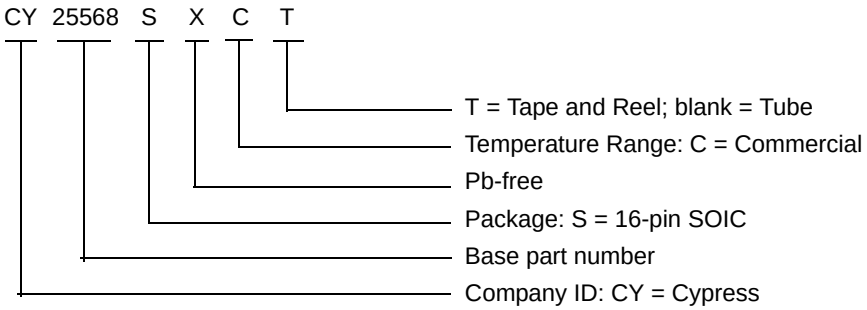
**Figure 8. Application Schematic**




## Ordering Information

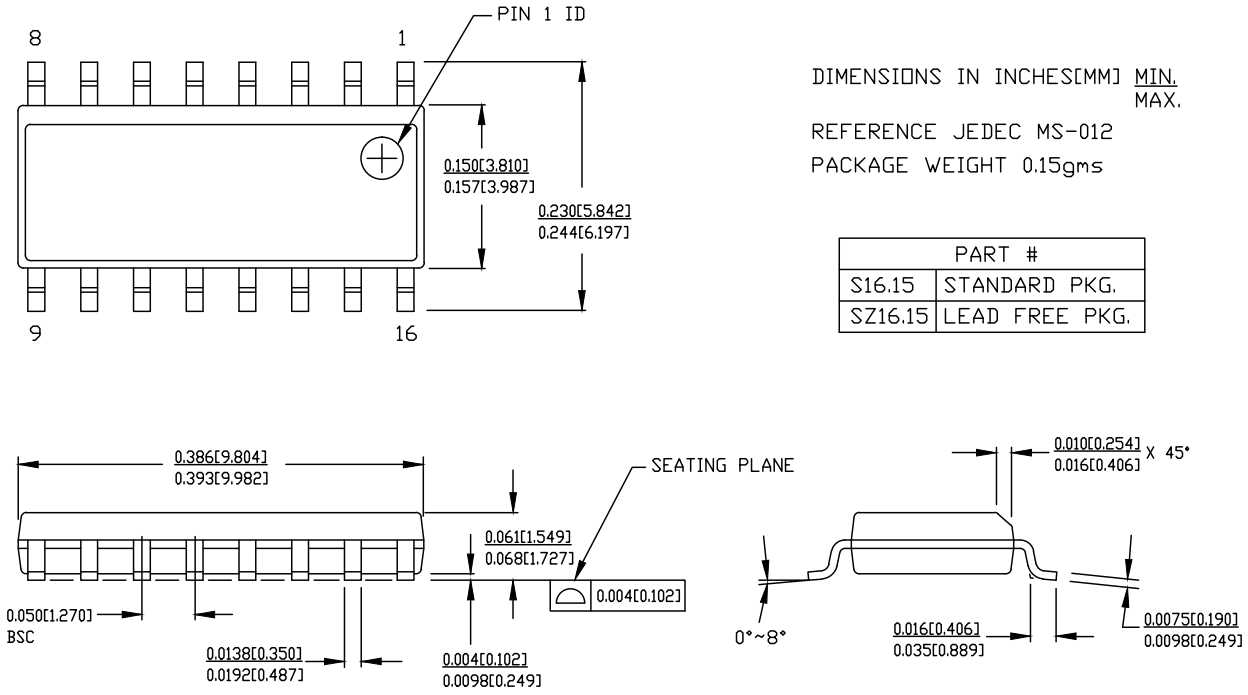
| Part No. | Package | Operating Temperature Range |
|---|---|---|
| **Pb-free** | | |
| CY25568SXC | 16 Pin SOIC | 0 to 70 °C |
| CY25568SXCT | 16 Pin SOIC – Tape and Reel | 0 to 70 °C |

### Ordering Code Definitions



## Package Diagram

**Figure 9. 16-Pin (150-Mil) SOIC**




51-85068 *C

## Acronyms

| Acronym | Description |
|---|---|
| DVD | digital versatile/video disc |
| EMI | electromagnetic interference |
| I/O | input/output |
| LAN | local area network |
| LCD | liquid crystal display |
| PLL | phase-locked loop |
| SOIC | small-outline integrated circuit |
| SSC | spread spectrum clock |
| SSCG | spread spectrum clock generator |
| VCD | video compact disc |
| WAN | wide area network |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| % | percent |
| °C | degree Celsius |
| dB | decibel |
| mA | milliamperes |
| MHz | Megahertz |
| mm | millimeter |
| ms | milliseconds |
| mW | milliwatts |
| ns | nanoseconds |
| pF | picofarad |
| ps | picoseconds |
| V | volts |
| Ω | ohms |
| W | watts |

## Document History Page

| Document Title: CY25568 Spread Spectrum Clock Generator<br>Document Number: 38-07111 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 107515 | NDP | 06/14/01 | Convert from IMI to Cypress |
| *A | 108182 | NDP | 07/03/01 | Delete “Junction Temp” in Absolute maximum Ratings (page 4) |
| *B | 122682 | RBI | 12/21/02 | Added power-up requirements to Absolute Maximum Ratings information. |
| *C | 2658020 | KVM/PYRS | 02/16/09 | Updated Ordering Information Table with Pb-free part numbers.<br>Deleted the table “16 Pin SOIC Outline Dimensions (150 mil)”<br>Updated template |
| *D | 3319217 | BASH | 07/08/18 | Update to latest template<br>Added Ordering Code Definitions<br>Updated Package Diagram<br>Added Acronyms<br>Added Units of Measure<br>Added Contents |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc<br>cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

### PSoC Solutions

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PSoC 1 | PSoC 3 | PSoC 5

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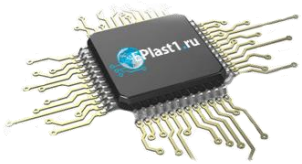
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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