

PN5180A0xx/C3

High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes

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436535

Product data sheet
COMPANY PUBLIC

1 Introduction

This document describes the functionality and electrical specification of the high-power NFC IC PN5180A0HN/C3, PN5180A0ET/C3, firmware versions equal or higher than FW3.A.

The package description of the PN5180A0ET/C3 is described in an addendum to this document.

Additional documents supporting a design-in of the PN5180 are available from NXP, this additional design-in information is not part of this document.



2 General description

PN5180, the best full NFC frontend on the market.

As a highly integrated high performance full NFC Forum-compliant frontend IC for contactless communication at 13.56 MHz, this frontend IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols.

The PN5180 ensures maximum interoperability for next generation of NFC enabled mobile phones. The PN5180 is optimized for point of sales terminal applications and implements a high-power NFC frontend functionality which allows to achieve EMV compliance on RF level without additional external active components.

The PN5180 frontend IC supports the following RF operating modes:

- Reader/Writer mode supporting ISO/IEC 14443 type A up to 848 kBit/s
- Reader/Writer communication mode for MIFARE Classic contactless IC
- Reader/Writer mode supporting ISO/IEC 14443 type B up to 848 kBit/s
- Reader/Writer mode supporting JIS X 6319-4 (comparable with FeliCa scheme)
- Supports reading of all NFC tag types (type 1, type 2, type 3, type 4A and type 4B)
- Reader/Writer mode supporting ISO/IEC 15693
- Reader/Writer mode supporting ISO/IEC 18000-3 Mode 3
- ISO/IEC 18092 (NFC-IP1)
- ISO/IEC 21481 (NFC-IP-2)
- ISO/IEC 14443 type A Card emulation up to 848 kBit/s

One host interface based on SPI is implemented:

- SPI interface with data rates up to 7 Mbit/s with MOSI, MISO, NSS and SCK signals
- Interrupt request line to inform host controller on events
- EEPROM configurable pull-up resistor on SPI MISO line
- Busy line to indicate to host availability of data for reading

The PN5180 supports highly innovative and unique features which do not require any host controller interaction. These unique features include Dynamic Power Control (DPC), Adaptive Waveform Control (AWC), Adaptive Receiver Control (ARC), and fully automatic EMD error handling. The independency of real-time host controller interactions makes this product the best choice for systems which operate a pre-emptive multitasking OS like Linux or Android.

As new power-saving feature the PN5180 allows using a general-purpose output to control an external LDO or DC-DC during Low-Power Card Detection. One general-purpose output is used to wake up an LDO or DC-DC from power-saving mode before the RF field for an LPCD polling cycle is switched on.

The PN5180 supports an external silicon system-power-on switch by using the energy of the RF field generated by an NFC phone to switch on the system, like it is generated during the NFC polling loop. This unique and new Zero-Power-Wake-up feature allows designing systems with a power consumption close to zero during standby.

3 Features and benefits

- Transmitter current up to 250 mA
- Dynamic Power Control (DPC) for optimized RF performance, even under detuned antenna conditions
- Adaptive Waveform Control (AWC) automatically adjusts the transmitter modulation for RF compliancy
- Adaptive Receiver Control (ARC) automatically adjusts the receiver parameters for always reliable communication
- Includes NXP ISO/IEC14443-A and Innovatron ISO/IEC14443-B intellectual property licensing rights
- Full compliancy with all standards relevant to NFC, contactless operation and EMVCo 3.0
- Active load modulation supports smaller antenna in Card Emulation Mode
- Automatic EMD handling performed without host interaction relaxes the timing requirements on the Host Controller
- Low-power card detection (LPCD) minimizes current consumption during polling
- Automatic support of system LDO or system DC-DC power-down mode during LPCD
- Zero-Power-Wake-up
- Small, industry-standard packages
- NFC Cockpit: PC-based support tool for fast configuration of register settings
- Development kit with 32-bit NXP LPC1769 MCU and antenna
- NFC Reader Library with source code ready for EMVCo 3.0 L1 and NFC Forum compliance

4 Applications

- Payment
- Physical-access
- eGov
- Industrial

5 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|----------------------------|--|------|-----|------|------|
| V _{DD(VBAT)} | supply voltage on pin VBAT | - | 2.7 | 3.3 | 5.5 | V |
| V _{DD(PVDD)} | supply voltage on pin PVDD | 1.8 V supply | 1.65 | 1.8 | 1.95 | V |
| | | 3.3 V supply | 2.7 | 3.3 | 3.6 | V |
| V _{DD(TVDD)} | supply voltage on pin TVDD | - | 2.7 | 5.0 | 5.5 | V |
| I _{pd} | power-down current | V _{DD(TVDD)} = V _{DD(PVDD)} =V _{DD(VDD)} 3.0 V; hard power-down; pin RESET_N set LOW, T _{amb} = 25 °C | - | 10 | - | μA |
| I _{stb} | standby current | T _{amb} = 25 °C | - | 15 | - | μA |
| I _{DD(TVDD)} | supply current on pin TVDD | - | - | 180 | 250 | mA |
| | | limiting value | - | - | 300 | mA |
| T _{amb} | ambient temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB | -30 | +25 | +85 | °C |
| T _{stg} | storage temperature | no supply voltage applied | -55 | +25 | +150 | °C |

6 Firmware Versions

Firmware versions covered by this data sheet:

Version 3.A (obsolete):

Supports EMVCo2.6 and more ARC Parameters

- By Default the EEPROM LPCD_REFERENCE_VALUE is set to 8
- By Default the EEPROM LPCD Selection is set to AUTO CALIBRATION.
Bit Field [1:0] 00 - Auto Calibration 01 - Self-Calibration 10 & 11 - RFU.
- ARC Parameters supported: MIN_LEVELP, MINLEVEL, RX_HPCF and RX_GAIN

Version 3.C:

Supports EMVCo2.6 and replaces the version 3.A.

- This version allows updating Firmware versions with lower version numbers after installing this firmware 3.C

Version 4.0:

Supports EMVCo2.6. and EMVCo 3.0 This version is available on the hardware PN5180A0HN/C3 and PN5180A0ET/C3.

- This is the firmware version available on the product PN5180A0HN/C3 (HVQFN package) and PN5180A0ET/C3 (BGA package). This version is functionally compliant to the FW3.A
- This firmware does not allow the installation of any lower firmware version than 4.x. For example, installation of FW 3.x is not possible once this firmware is installed.

Version 4.1:

Supports EMVCo2.6 and EMVCo3.0. This version is available as firmware only.

NXP recommends using this firmware version for new designs.

- This is a firmware release for software upgrade of existing PN5180 products. All hardware versions of the PN5180A0HN can be updated using this firmware version. Once installed, it is not possible to install a firmware version lower than 4.0.
- The firmware supports advanced FeliCa EMD handling using a new FELICA_EMD_CONTROL register. It is recommended to initialize this register for FeliCa reader mode with a value of 00FF0019h.
- The firmware allows circumventing communication issues with legacy Type-B cards via EEPROM configuration. It allows enabling/disabling an extra modulation pulse after every DPC gear switch from lower to higher gear number (higher to lower power level). This extra modulation pulse with the same modulation index as in the normal PCD to PICC communication can trigger and properly reset the Type B PICC UART and improve the communication for some type of cards.”

7 Ordering information

Table 2. Ordering information

| Type number | Package | | |
|-----------------|---------|---|-----------|
| | Name | Description | Version |
| PN5180A0HN/C3E | HVQFN40 | Firmware version 4.0. Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals + 1 central ground; body 6 x 6 x 1.0 mm; delivered in one tray, bakable, MSL=3. Minimum order quantity = 490 pcs | SOT618-1 |
| PN5180A0HN/C3Y | HVQFN40 | Firmware version 4.0. Plastic thermal enhanced very thin quad flat package; no leads; 40 terminals + 1 central ground; body 6 x 6 x 1.0 mm; delivered on reel 13", MSL = 3. Minimum order quantity = 4000 pcs | SOT618-1 |
| PN5180A0ET/C3QL | TFBGA64 | Firmware version 4.0. Plastic thin fine-pitch ball grid array package; 64 balls, delivered in one tray, MSL = 1. Minimum order quantity = 490 pcs | SOT1336-1 |
| PN5180A0ET/C3J | TFBGA64 | Firmware version 4.0. Plastic thin fine-pitch ball grid array package; 64 balls, delivered on reel 13", MSL = 1. Minimum order quantity = 4000 pcs | SOT1336-1 |

The PN5180 is not available with other pre-installed firmware versions than listed above.

8 Marking

Table 3. Marking code HVQFN40

| Type number | Marking code |
|---|--|
| PN5180A0HN This product is released for sale (volume production). | |
| Line A: | "PN5180A" |
| Line B1: | 6 characters: Diffusion Batch ID; example: "HHR275" |
| Line B2: | Assembly sequence ID; example: ".1 04" |
| Line C: Release for sale products does not show any X or Y, instead position 8 is left blank | 8 characters: diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: <ol style="list-style-type: none"> 1. Diffusion center code 2. Assembly center code 3. RHF-2006 indicator 4. Year code (Y) 1 5. Week code (W) 2 6. Week code (W) 2 7. Mask layout version 8. (Product life cycle status release for sale): blank example: "NSD620C " |

Note that the Firmware of the product PN5180 can be updated. Due to the update capability, the marking of the package does not allow identifying the installed version of the actual programmed firmware. The firmware version can be retrieved from address 0x12 in EEPROM.

8.1 Package marking drawing

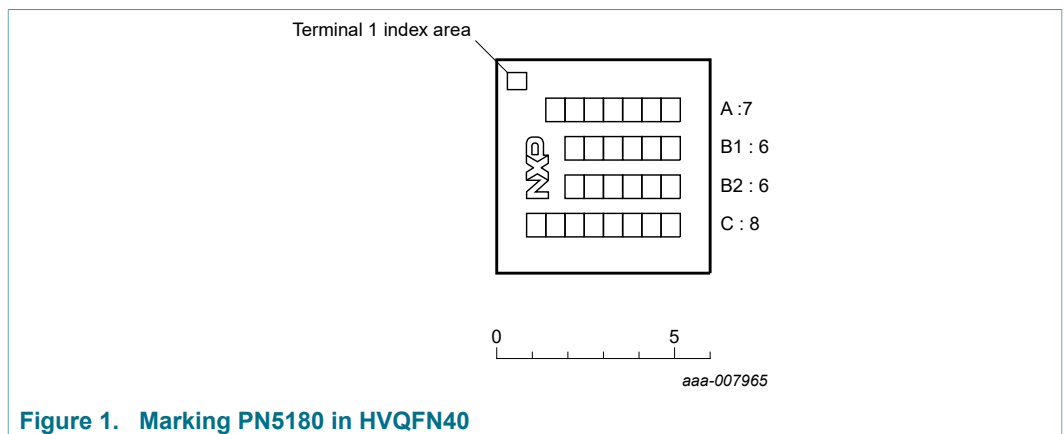


Figure 1. Marking PN5180 in HVQFN40

The Marking of the TFBGA version can be found in the data sheet addendum which is available through the NXP DocStore.

9 Block diagram

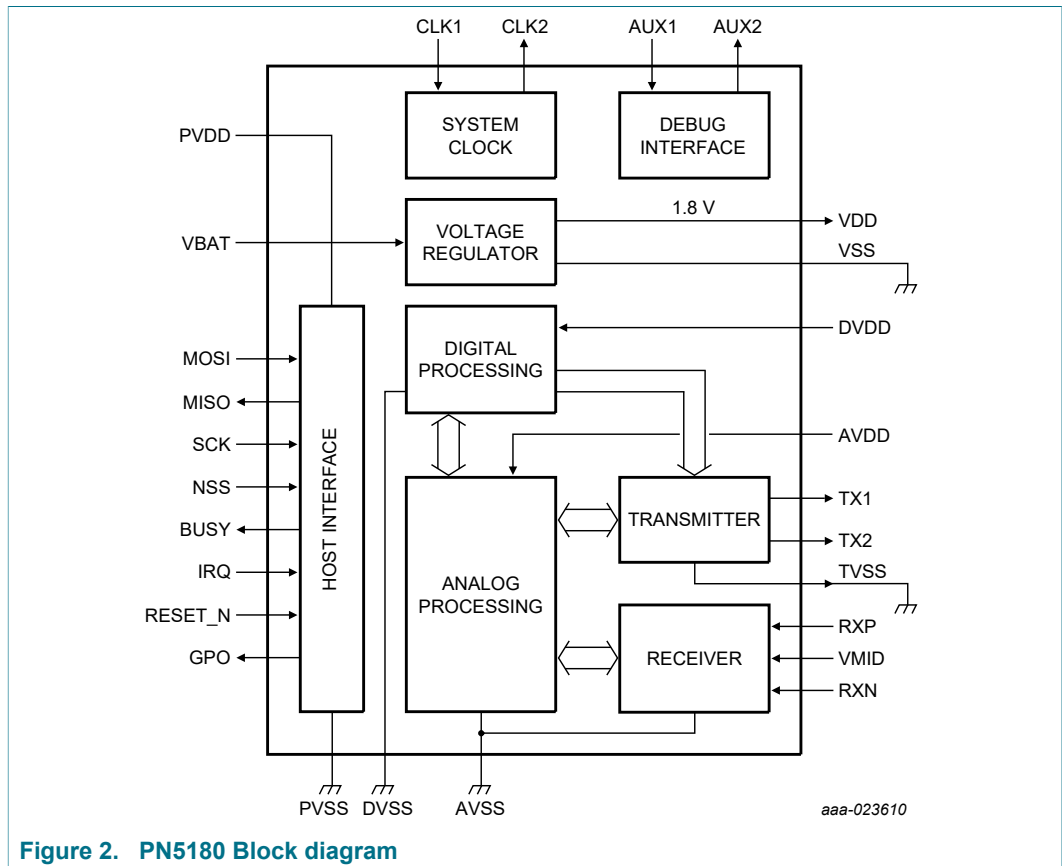


Figure 2. PN5180 Block diagram

10 Pinning information

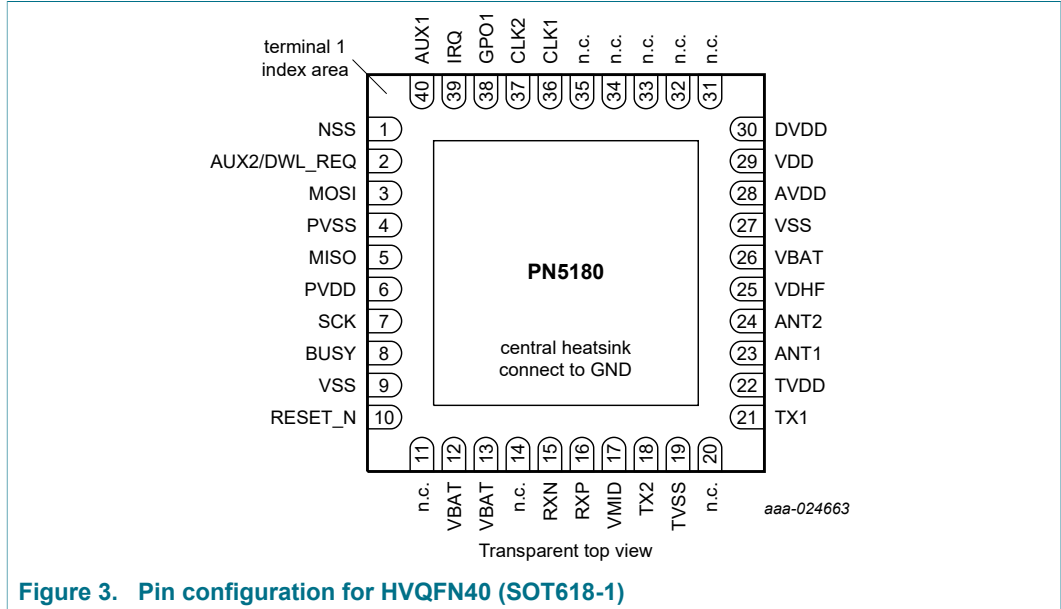


Figure 3. Pin configuration for HVQFN40 (SOT618-1)

10.1 Pin description

Table 4. Pin description HVQFN40

| Symbol | Pin | Type | Description |
|----------------|-----|--------|--|
| NSS | 1 | I | SPI NSS |
| AUX2 /DWL_ REQ | 2 | I/O | Analog test bus or Download request |
| MOSI | 3 | I | SPI MOSI |
| PVSS | 4 | supply | Pad ground |
| MISO | 5 | O | SPI MISO |
| PVDD | 6 | supply | Pad supply voltage |
| SCK | 7 | I | SPI Clock |
| BUSY | 8 | O | Busy signal |
| VSS | 9 | supply | Ground |
| RESET_N | 10 | I | RESET, Low active |
| n.c. | 11 | - | leave unconnected, do not ground |
| VBAT | 12 | supply | Supply Connection, all VBAT mandatory to be connected |
| VBAT | 13 | supply | Supply Connection, all VBAT mandatory to be connected |
| nc / LDO_OUT | 14 | O | leave unconnected, do not ground / use as 3.3 V LDO output |
| RXN | 15 | I | Receiver Input |
| RXP | 16 | I | Receiver Input |
| VMID | 17 | supply | Stabilizing capacitor connection output |
| TX2 | 18 | O | Antenna driver output 2 |

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| Symbol | Pin | Type | Description |
|--------|-----|--------|---|
| TVSS | 19 | supply | Antenna driver ground |
| n.c. | 20 | - | leave unconnected, do not ground |
| TX1 | 21 | O | Antenna driver output 1 |
| TVDD | 22 | supply | Antenna driver supply |
| ANT1 | 23 | I | Antenna connection 1 for load modulation in card emulation mode (only in case of PLM) |
| ANT2 | 24 | I | Antenna connection 2 for load modulation in card emulation mode (only in case of PLM) |
| VDHF | 25 | supply | Stabilizing capacitor connection output |
| VBAT | 26 | supply | Supply Connection, all VBAT mandatory to be connected |
| VSS | 27 | supply | Ground |
| AVDD | 28 | supply | Analog VDD supply voltage input (1.8 V), connected to VDD |
| VDD | 29 | supply | VDD output (1.8 V) |
| DVDD | 30 | supply | Digital supply voltage input (1.8 V), connected to VDD |
| n.c. | 31 | - | leave unconnected, do not ground |
| n.c. | 32 | - | leave unconnected, do not ground |
| n.c. | 33 | - | leave unconnected, do not ground |
| n.c. | 34 | - | leave unconnected, do not ground |
| n.c. | 35 | - | leave unconnected, do not ground |
| CLK1 | 36 | I | Clock input for crystal. This pin is also used as input for an external generated accurate clock (8 MHz, 12 MHz, 16 MHz, 24 MHz, other clock frequencies not supported) |
| CLK2 | 37 | O | Clock output (amplifier inverted signal output) for crystal |
| GPO1 | 38 | O | (double function pin) GPO1, Digital output 1 |
| IRQ | 39 | O | Interrupt request output, active level configurable |
| AUX1 | 40 | O | Analog/Digital Test signal |

The central heat sink of the HVQFN40 package shall be connected to GND.

The pinning of the TFBGA version can be found in the data sheet addendum which is available through the NXP DocStore.

11 Functional description

11.1 Introduction

The PN5180 is a High-Power NFC frontend. It implements the RF functionality like an antenna driving and receiver circuitry and all the low-level functionality to realize an NFC Forum-compliant reader. The PN5180 connects to a host microcontroller with a SPI interface for configuration, NFC data exchange and high-level NFC protocol implementation.

The PN5180 allows different supply voltages for NFC drivers, internal supply and host interface providing a maximum of flexibility.

The chip supply voltage and the NFC driver voltage can be chosen independently from each other.

The PN5180 uses an external 27.12 MHz crystal as clock source for generating the RF field and its internal digital logic. In addition, an internal PLL allows using an accurate external clock source of either 8, 12, 16, 24 MHz. This saves the 27.12 MHz crystal in systems which implement one of the mentioned clock frequencies (e.g. for USB or system clock).

Two types of memory are implemented in the PN5180: RAM and EEPROM.

Internal registers of the PN5180 state machine store configuration data. The internal registers are reset to initial default values. In case of a Power-On, a low level on the pin RESET_N (Hardware triggered reset), a SOFT_RESET (Software triggered reset) by writing a "1" to the SYSTEM_CONFIG register (address 0000h), bit 8 and after leaving the standby mode.

The RF configuration for dedicated RF protocols is defined by EEPROM data which is copied by a command issued from the host microcontroller - LOAD_RF_CONFIG - into the registers of the PN5180. The PN5180 is initialized with EEPROM data for the LOAD_RF_CONFIG command which has been tested to work well for one typical antenna. For customer-specific antenna sizes and dedicated antenna environment conditions like metal or ferrite, the pre-defined EEPROM settings can be modified by the user. This allows users to achieve the maximum RF performance from a given antenna design. It is mandatory to use the command LOAD_RF_CONFIG for the selection of a specific RF protocol.

The command LOAD_RF_CONFIG initializes the registers faster compared to individual register writes.

11.2 Power-up and Clock

11.2.1 Power Management Unit

11.2.1.1 Supply Connections and Power-up

The Power Management Unit of the PN5180 generates internal supplies required for operation.

The following pins are used to supply the IC:

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- PVDD - supply voltage for the SPI interface and control connections
- VBAT - Supply Voltage input
- TVDD - Transmitter supply
- AVDD - Analog supply input, connected to VDD
- DVDD - Digital supply input, connected to VDD
- VDD - 1.8 V output, to be connected to AVDD and DVDD

Decoupling capacitors shall be placed as close as possible to the pins of the package. Any additional filtering/damping of the transmitter supply, e.g. by ferrite beads, might have an impact on the analog RF signal quality and shall be monitored carefully.

Power-up sequence of the PN5180

- First ramp VBAT, PVDD can immediately follow, latest 2 ms after VBAT reaches 1.8 V.
- There is no timing dependency on TVDD, only that TVDD shall rise at the same time or later than VBAT.
- VBAT must have an equal or higher level than PVDD
- TVDD has no other relationship to VBAT or PVDD

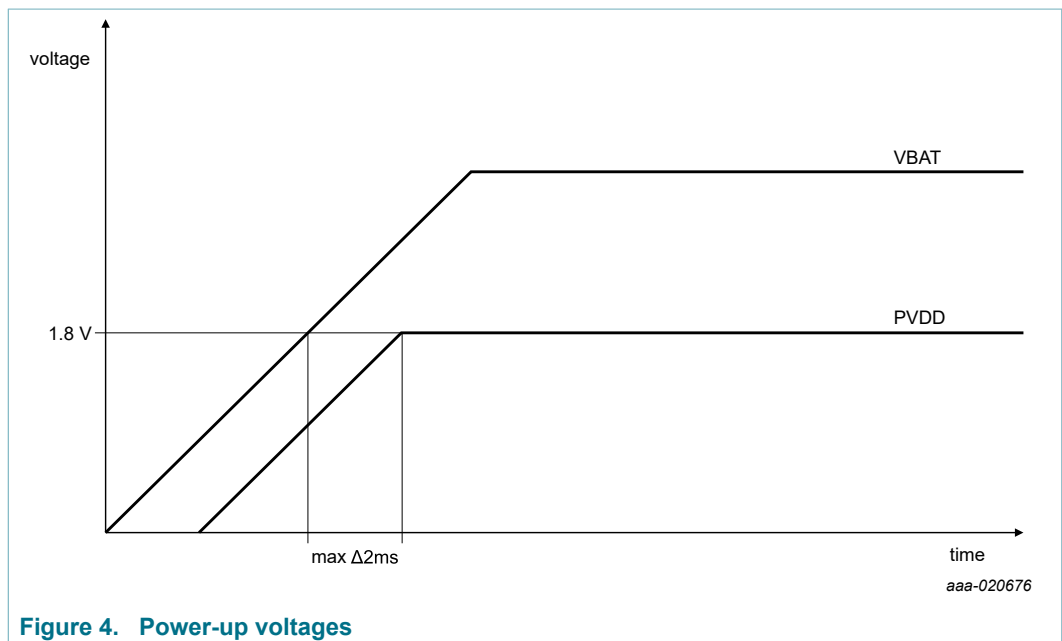


Figure 4. Power-up voltages

After power-up, the PN5180 is indicating the ability to receive command from a host microcontroller by an IDLE IRQ.

There are configurations in EEPROM, which allow to specify the behavior of the PN5180 after start-up. LPCD (Low-power card detection) and DPC (dynamic power control) are functionalities which are configurable in EEPROM.

The PN5180 supports full FNC functionality, this means Reader/Writer, Card and Peer to Peer mode. The default configuration of the PN5180 after power-up is the card mode to allow a collision avoidance with another RF field.

11.2.1.2 Power-down / Reset

A power-down is enabled by a LOW level on pin RESET_N. This low level sets the internal voltage regulators for the analog and digital core supply as well as the oscillator

in a low-power state. All digital input buffers are separated from the input pads and clamped internally (except pin RESET_N itself and the driver of the transmitter TX1, TX2). IRQ, BUSY, AUX1, AUX2 have an internal pull-down resistor which is activated on RESET_N == 0. All other output pins are switched to high impedance.

To leave the power-down mode, the level at the pin RESET_N has to be set to HIGH. This high level starts the internal start-up sequence from Power-Down.

After setting the pin RESET_N to high and starting the chip from Power-Down, all registers are set to default state (chip reset).

The Power-down does not change any data in EEPROM memory.

Setting all registers to default state can be achieved either by toggling the pin RESET_N or by writing a "1" into the SYSTEM_CONFIG register (0000h) bit8, SOFT_RESET. In contrast to a LOW level on pin RESET_N, a soft reset does not set the chip into a low-power state.

11.2.1.3 Standby

The standby mode is entered immediately after sending the instruction SWITCH_MODE with standby command. All internal current sinks are set to low-power state.

In opposition to the power-down mode, the digital input buffers are not separated by the input pads and keep their functionality. The digital output pins do not change their state.

During standby mode, all registers values, the buffer content and the configuration itself are not kept, exceptions are the registers with addresses 05h(PADCONFIG), 07h(PADOUT) 25h (TEMP_CONTROL). To leave the standby mode, various possibilities do exist. The conditions for wake-up are configured in the register STBY_CFG.

- Wake-up via Timer
- Wake-up via RF level detector
- Low Level on RESET_N
- PVDD disappears

Any host communication (data is not validated) triggers the internal start-up sequence. The reader IC is in operation mode when the internal start-up sequence is finalized, and is indicating this by an IDLE IRQ.

11.2.1.4 Temperature Sensor

The PN5180 implements a configurable temperature sensor. The temperature sensor is configurable by the TEMP_CONTROL register (25h).

The Temperature Sensor supports temperature settings for 85 °C, 115 °C, 125 °C and 135 °C.

In case the sensed device temperature is higher than configured, a TEMPSENS_ERROR IRQ is raised. In case of an TEMPSENS_ERROR, the Firmware is switching off the RF Field. Additionally host can set the device into standby as response to the raised IRQ. In case the sensed device temperature is higher than the configured, FW is automatically switching off the RF field in-order to protect the TX drivers and sets the TEMPSENS_ERROR_IRQ_STAT in the IRQ_STATUS register to 1.

The host can either poll on the TEMPSENS_ERROR_IRQ_STAT or enable the bit TEMPSENS_ERROR_IRQ_EN in IRQ_ENABLE register to get an interrupt on the IRQ pin.

In addition, the host can set the device into standby based on the TEMPSENS_ERROR_IRQ_STAT.

This feature is enabled by default. Only the interrupt can be enabled / disabled via the IRQ_ENABLE register

11.2.2 Reset and start-up time

A constant low level of at least 10 μs at the RESET_N pin starts the internal reset procedure.

When the PN5180 has finished the start_up, a IDLE_IRQ is raised and the IC is ready to receive commands on the host interface.

11.2.3 Clock concept

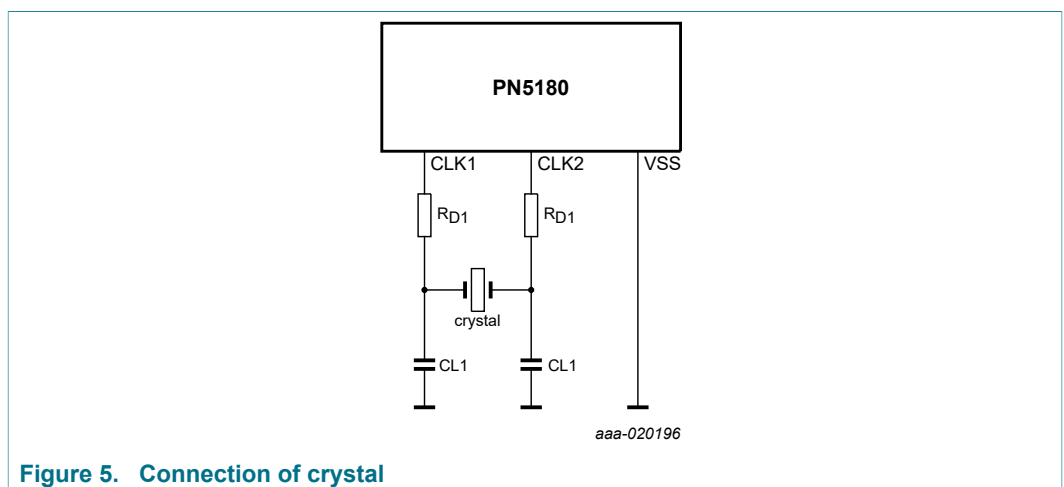
The PN5180 is supplied by an 27.12 MHz crystal for operation. In addition, the internal PLL uses an accurate external clock source of either 8, 12, 16, 24 MHz instead of the crystal.

The clock applied to the PN5180 provides a time basis for the RF encoder and decoder. The stability of the clock frequency, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. Optimum performance is best achieved using the internal oscillator buffer with the recommended circuitry.

In card emulation mode, the clock is also required.

If an external clock source of 27.12 MHz is used instead of a crystal, the clock signal must be applied to pin CLK1. In this case, special care must be taken with the clock duty cycle and clock jitter (see Table 141).

The crystal is a component which is impacting the overall performance of the system. A high-quality component is recommended here. The resistor RD1 reduces the start-up time of the crystal. A short start-up time is especially desired in case the Low-Power card detection is used. The values of these resistors depend on the crystal which is used.



11.3 Timer and Interrupt system

11.3.1 General Purpose Timer

The Timers are used to measure certain intervals between certain configurable events of the receiver, transmitter and other RF-events. The timer signals its expiration by raising a flag and the value of the timer may be accessed via the register-set.

Three general-purpose timers T0, T1, and T2 running with the PN5180 clock with several start conditions, stop conditions, time resolutions, and maximal timer periods are implemented.

For automatic timeout handling during MIFARE Classic Authentication Timer2 is blocked during this operation.

In case EMVCo EMD handling is enabled (EMD_CONTROL register (address 0028h), bit EMD_ENABLE) Timer1 is automatically restarted when an EMD event occurs.

Timers T0 to T2 has a resolution of 20 bits and may be operated at clock frequencies derived from the 13.56 MHz system clock. Several start events can be configured: start now, start on external RF-field on/off and start on Rx (receive)/Tx (transmit) started/ended. The timers allow reload of the counter value. At expiration of the timers, a flag is raised and an IRQ is triggered.

The clock may be divided by a prescaler for frequencies of:

- 6.78 MHz
- 3.39 MHz
- 1.70 MHz
- 848 kHz
- 424 kHz
- 212 kHz
- 106 kHz
- 53 kHz

11.3.2 Interrupt System

11.3.2.1 IRQ PIN

The IRQ_ENABLE configures, which of the interrupts are routed to the IRQ pin of the PN5180. All of the interrupts can be enabled and disabled independent from each other. The IRQ on the pin can either be cleared by writing to the IRQ_CLEAR register or by reading the IRQ_STATUS register (EEPROM configuration). If not all enabled IRQ's are cleared, the IRQ pin remains active.

The polarity of the external IRQ signal is configured by EEPROM in IRQ_PIN_CONFIG (01Ah).

11.3.2.2 IRQ_STATUS Register

The IRQ_STATUS register contains the status flags. The status flags cannot be disabled. Status Flag can either be cleared by writing to the IRQ_CLEAR register or when the IRQ_STATUS register is read (EEPROM configuration)

The PN5180 indicates certain events by setting bits in the register GENERAL_IRQ_STATUS and additionally, if activated, on the pin IRQ.

LPCD_IRQ, GENERAL_ERROR_IRQ and HV_ERROR_IRQ are non-maskable interrupts.

11.4 SPI Host Interface

The following description of the SPI host interface is valid for the NFC operation mode. The Secure Firmware Download mode uses a different physical host interface handling. Details are described in chapter 12.

11.4.1 Physical Host Interface

The interface of the PN5180 to a host microcontroller is based on a SPI interface, extended by signal line BUSY. The maximum SPI speed is 7 Mbit/s and fixed to CPOL = 0 and CPHA = 0. Only a half-duplex data transfer is supported. There is no chaining allowed, meaning that the whole instruction has to be sent or the whole receive buffer has to be read out. The whole transmit buffer shall be written at once as well. No NSS assertion is allowed during data transfer.

As the MISO line is per default high-ohmic in case of NSS high, an internal pull-up resistor can be enabled via EEPROM.

The BUSY signal is used to indicate that the PN5180 is not able to send or receive data over the SPI interface.

The host interface is designed to support the typical interface supply voltages of 1.8 V and 3.3 V of CPUs. A dedicated supply input which defines the host interface supply voltage independent from other supplies is available (PVDD). Only a voltage of 1.8 V or 3.3 V is supported, but no voltage in the range of 1.95 V to 2.7 V.

- Master In Slave Out (MISO)

The MISO line is configured as an output in a slave device. It is used to transfer data from the slave to the master, with the most significant bit sent first. The MISO signal is put into 3-state mode when NSS is high.

- Master Out Slave In (MOSI)

The MOSI line is configured as an input in a slave device. It is used to transfer data from the master to a slave, with the most significant bit sent first.

- Serial Clock (SCK)

The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines.

- Not Slave Select (NSS)

The slave select input (NSS) line is used to select a slave device. It shall be set to low before any data transaction starts and must stay low during the transaction.

- Busy

During frame reception, the BUSY line goes ACTIVE and goes to IDLE when PN5180 is able to receive a new frame or data is available (depending if SET or GET frame is issued). If there is a parameter error, the IRQ is set to ACTIVE and a GENERAL_ERROR_IRQ is set.

Both master and slave devices must operate with the same timing. The master device always places data on the MOSI line a half cycle before the clock edge SCK, in order for the slave device to latch the data.

The BUSY line is used to indicate that the system is processing data and cannot receive any data from a host. The system handles the busy signal different for normal mode and debug mode (test bus enabled). In the sequence below, step 3 is optional for the

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normal mode, but mandatory for debug mode enabled. Recommendation for the BUSY line handling by the host:

1. Assert NSS to Low
2. Perform Data Exchange
3. Wait until BUSY is high (optional if test bus is not enabled)
4. Deassert NSS
5. Wait until BUSY is low

In order to write data to or read data from the PN5180, "dummy reads" shall be performed. The Figure 8 and Figure 9 are illustrating the usage of this "dummy reads" on the SPI interface.

The host interface must use the following sequence as long as the test bus is enabled:

1. Assert NSS to Low
2. Perform Data Exchange
3. Wait until BUSY is high
4. Deassert NSS
5. Wait until BUSY is low

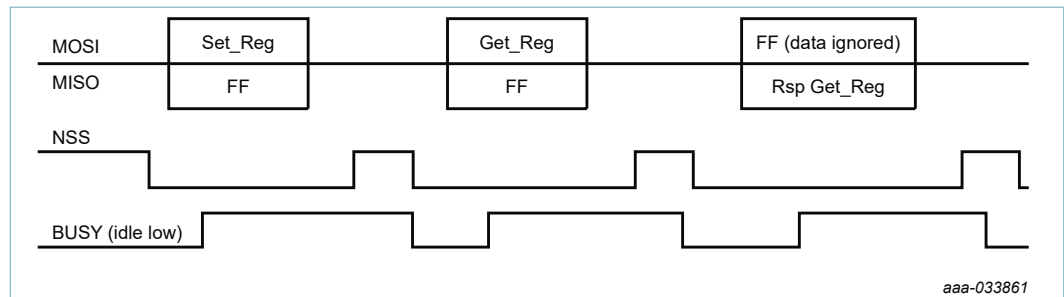


Figure 6. Read RX of SPI data using BUSY line

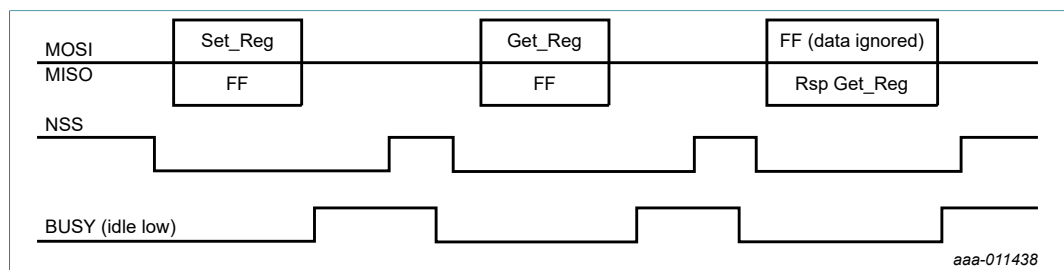


Figure 7. Read RX of SPI data using BUSY line with test bus enabled

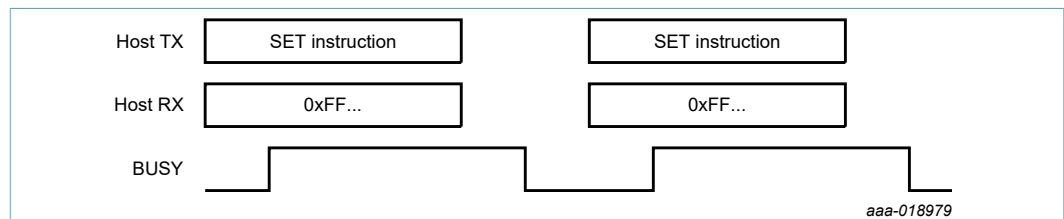


Figure 8. Writing data to the PN5180

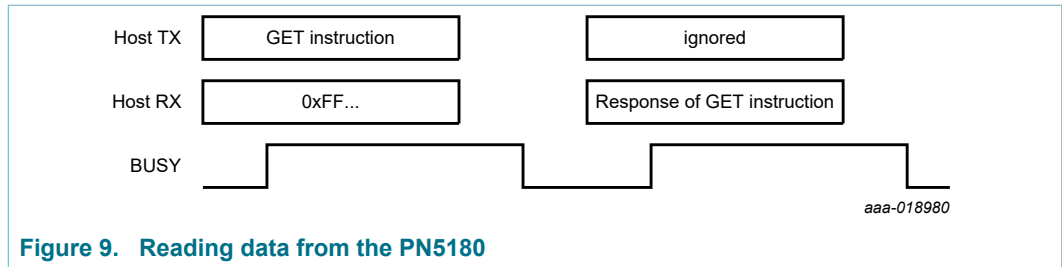


Figure 9. Reading data from the PN5180

11.4.2 Timing Specification SPI

The timing condition for SPI interface is as follows:

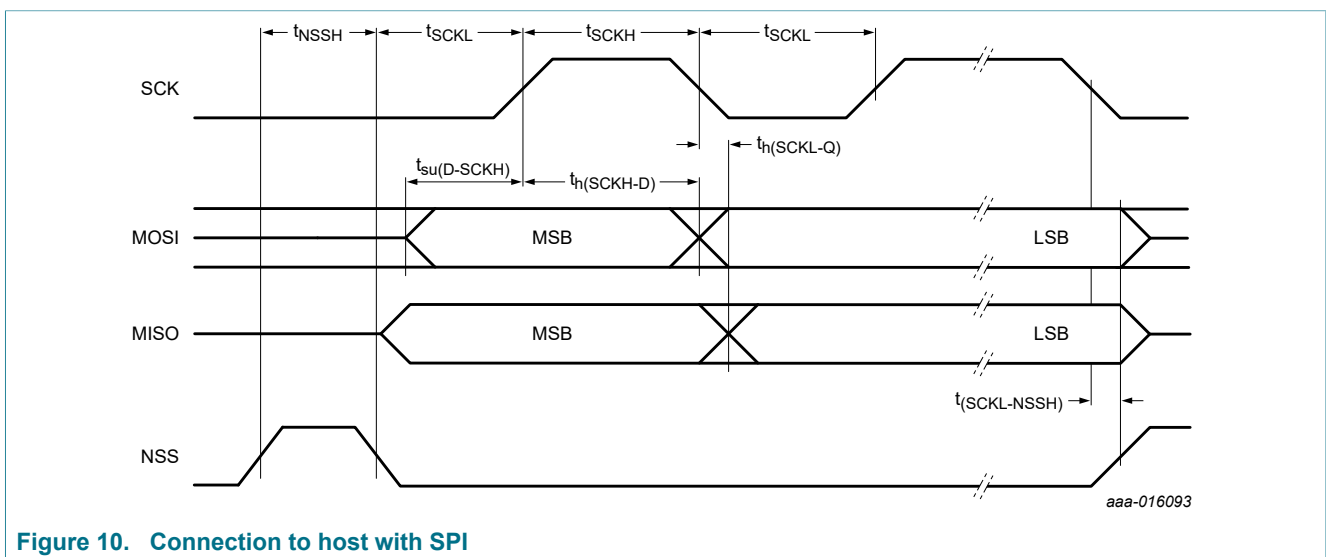


Figure 10. Connection to host with SPI

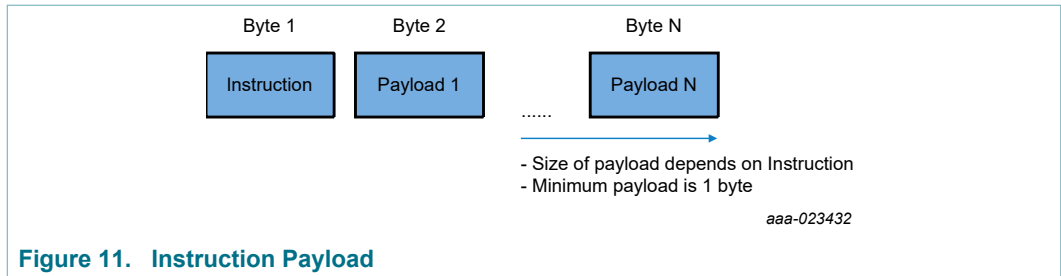
Remark: To send more bytes in one data stream, the NSS signal must be LOW during the send process. To send more than one data stream, the NSS signal must be HIGH between each data stream. Any data available to be read from the SPI interface is indicated by the BUSY signal de-asserted.

11.4.3 Logical Host Interface

11.4.3.1 Host Interface Command

A Host Interface Command consists of either 1 or 2 SPI frames depending whether the host wants to write or read data from the PN5180. An SPI Frame consists of multiple bytes.

The protocol used between the host and the PN5180 uses 1 byte indicating the instruction code and additional bytes for the payload (instruction-specific data). The actual payload size depends on the instruction used. The minimum length of the payload is 1 byte. This provides a constant offset at which message data begins.



All commands are packed into one SPI Frame. An SPI Frame consists of multiple bytes. No NSS toggles allowed during sending of an SPI frame.

For all 4 byte command parameter transfers (e.g. register values), the payload parameters passed follow the little endian approach (Least Significant Byte first).

Direct Instructions are built of a command code (1 Byte) and the instruction parameters (max. 260 bytes). The actual payload size depends on the instruction used.

Responses to direct instructions contain only a payload field (no header). All instructions are bound to conditions. If at least one of the conditions is not fulfilled, an exception is raised.



In case of an exception, the IRQ line of PN5180 is asserted and corresponding interrupt status register contain information on the exception.

11.4.3.2 Transmission Buffer

Two buffers are implemented in the PN5180. The transmission buffer has a buffer size of 260 bytes, the reception buffer has a size of 508 bytes. Both memories buffer the input and output data streams between the host and the internal state machine / contactless UART of the PN5180. Thus, it is possible to handle data streams with lengths of up to 260 bytes for transmission and up to 508 bytes for reception without taking timing constraints into account.

11.4.3.3 Host Interface Command List

Table 5. 1-Byte Direct Commands and Direct Command Codes

| Command | Command code | Description |
|-------------------------|--------------|--|
| WRITE_REGISTER | 0x00 | Write one 32bit register value |
| WRITE_REGISTER_OR_MASK | 0x01 | Sets one 32bit register value using a 32 bit OR mask |
| WRITE_REGISTER_AND_MASK | 0x02 | Sets one 32bit register value using a 32 bit AND mask |
| WRITE_REGISTER_MULTIPLE | 0x03 | Processes an array of register addresses in random order and performs the defined action on these addresses. |
| READ_REGISTER | 0x04 | Reads one 32bit register value |

| Command | Command code | Description |
|------------------------------------|--------------|--|
| READ_REGISTER_MULTIPLE | 0x05 | Reads from an array of max.18 register addresses in random order |
| WRITE_EEPROM | 0x06 | Processes an array of EEPROM addresses in random order and writes the value to these addresses |
| READ_EEPROM | 0x07 | Processes an array of EEPROM addresses from a start address and reads the values from these addresses |
| WRITE_TX_DATA | 0x08 | This instruction is used to write data into the transmission buffer |
| SEND_DATA | 0x09 | This instruction is used to write data into the transmission buffer, the START_SEND bit is automatically set. |
| READ_DATA | 0x0A | This instruction is used to read data from reception buffer, after successful reception. |
| SWITCH_MODE | 0x0B | This instruction is used to switch the mode. It is only possible to switch from NormalMode to standby, LPCD or Autocoll. |
| MIFARE_AUTHENTICATE | 0x0C | This instruction is used to perform a MIFARE Classic Authentication on an activated card. |
| EPC_INVENTORY | 0x0D | This instruction is used to perform an inventory of ISO18000-3M3 tags. |
| EPC_RESUME_INVENTORY | 0x0E | This instruction is used to resume the inventory algorithm in case it is paused. |
| EPC_RETRIEVE_INVENTORY_RESULT_SIZE | 0x0F | This instruction is used to retrieve the size of the inventory result. |
| EPC_RETRIEVE_INVENTORY_RESULT | 0x10 | This instruction is used to retrieve the result of a preceding EPC_INVENTORY or EPC_RESUME_INVENTORY instruction. |
| LOAD_RF_CONFIG | 0x11 | This instruction is used to load the RF configuration from EEPROM into the configuration registers. |
| UPDATE_RF_CONFIG | 0x12 | This instruction is used to update the RF configuration within EEPROM. |
| RETRIEVE_RF_CONFIG_SIZE | 0x13 | This instruction is used to retrieve the number of registers for a selected RF configuration |
| RETRIEVE_RF_CONFIG | 0x14 | This instruction is used to read out an RF configuration. The register address-value-pairs are available in the response |
| - | 0x15 | RFU |
| RF_ON | 0x16 | This instruction switch on the RF Field |
| RF_OFF | 0x17 | This instruction switch off the RF Field |
| CONFIGURE_TESTBUS_DIGITAL | 0x18 | Enables the Digital test bus |
| CONFIGURE_TESTBUS_ANALOG | 0x19 | Enables the Analog test bus |

The following direct instructions are supported on the Host Interface: Detail Description of the instruction.

WRITE_REGISTER - 0x00

Table 6. WRITE_REGISTER

| Payload | Length (byte) | Value/Description |
|--------------|---------------|-------------------|
| Command code | 1 | 0x00 |
| Parameter | 1 | Register address |
| | 4 | Register content |
| Response | - | - |

Description:

This command is used to write a 32-bit value (little endian) to a configuration register.

Condition:

The address of the register must exist. If the condition is not fulfilled, an exception is raised.

WRITE_REGISTER_OR_MASK - 0x01

Table 7. WRITE_REGISTER

| Payload | Length (byte) | Value/Description |
|--------------|---------------|-------------------|
| Command code | 1 | 0x01 |
| Parameter | 1 | Register address |
| | 4 | OR_MASK |
| Response | - | - |

Description:

This command modifies the content of a register using a logical OR operation. The content of the register is read and a logical OR operation is performed with the provided mask. The modified content is written back to the register.

Condition:

The address of the register must exist. If the condition is not fulfilled, an exception is raised.

WRITE_REGISTER_AND_MASK - 0x02

Table 8. WRITE_REGISTER_AND_MAKSK

| Payload | Length (byte) | Value/Description |
|--------------|---------------|-------------------|
| Command code | 1 | 0x02 |
| Parameter | 1 | Register address |
| | 4 | AND_MASK |
| Response | - | - |

Description:

This command modifies the content of a register using a logical AND operation. The content of the register is read and a logical AND operation is performed with the provided mask. The modified content is written back to the register.

Condition:

The address of the register must exist. If the condition is not fulfilled, an exception is raised.

WRITE_REGISTER_MULTIPLE - 0x03

Table 9. WRITE_REGISTER_MULTIPLE

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x03 |
| Parameter | 5...210 | Array of up to 42 elements {address, action, content} |
| | | 1 byte Register address |
| | | 1 byte Action |
| | 4 bytes | Register content |
| Response | - | - |

Description:

This instruction allows processing actions on multiple addresses with a single command. Input parameter is an array of register addresses, actions, and values (little endian). The command processes this array, register addresses are allowed to be in random order. For each address, an individual ACTION can be defined.

Parameter value is either the REGISTER_DATA, the OR_MASK or the AND_MASK.

ACTION that can be defined individually for each register address:

- 0x01 WRITE_REGISTER
- 0x02 WRITE_REGISTER_OR_MASK
- 0x03 WRITE_REGISTER_AND_MASK

Note: In case of an exception, the operation is not rolled-back, i.e. registers which have been modified until exception occurs remain in modified state. Host has to take proper actions to recover to a defined state.

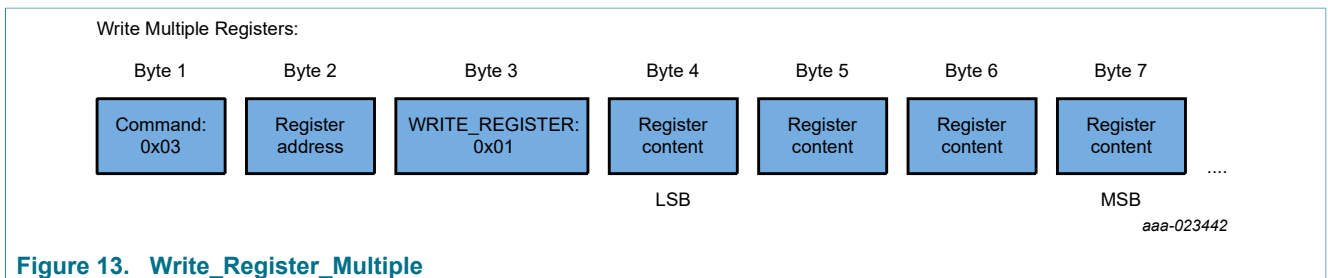
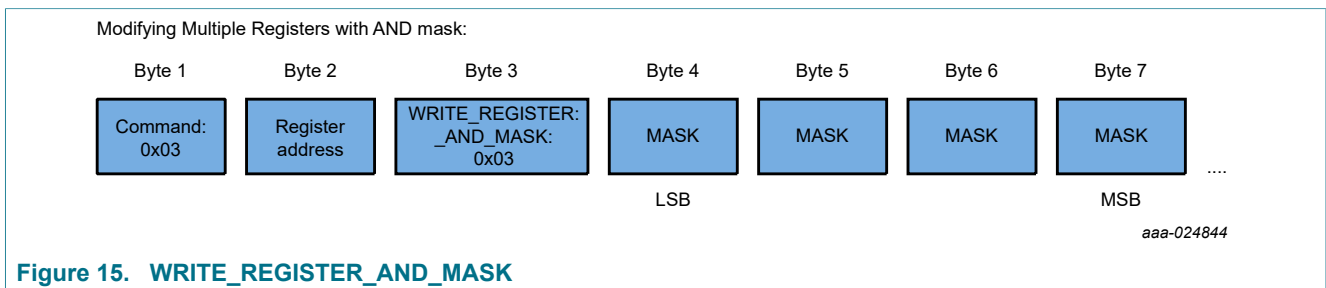
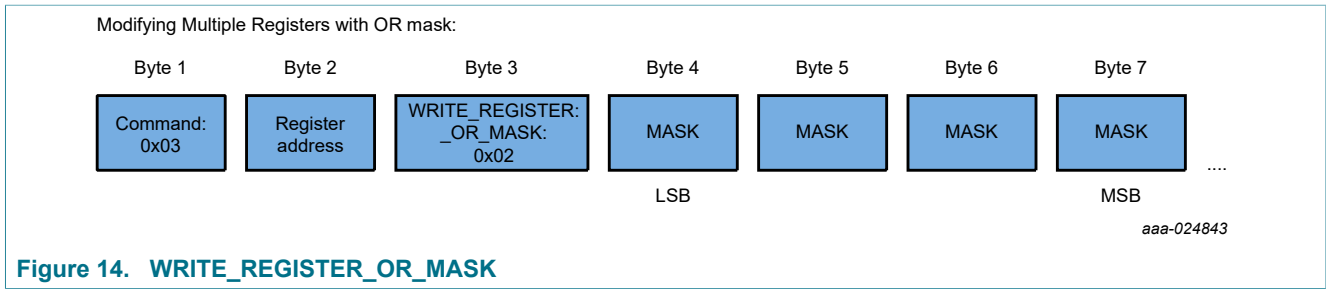


Figure 13. Write_Register_Multiple



Condition:

The address of the registers must exist. If the condition is not fulfilled, an exception is raised.

READ_REGISTER - 0x04

Table 10. READ_REGISTER

| Payload | Length (byte) | Value/Description |
|--------------|---------------|-------------------|
| Command code | 1 | 0x04 |
| Parameter | 1 | Register address |
| Response | 4 | Register content |

Description:

This command is used to read the content of a configuration register. The content of the register is returned in the 4 byte response.

Condition:

The address of the register must exist. If the condition is not fulfilled, an exception is raised.

READ_REGISTER_MULTIPLE -0x05

Table 11. READ_REGISTER_MULTIPLE

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x05 |
| Parameter | 1..18 | Array of up to 18 elements {Register address} |
| | | 1 byte Register address |

| Payload | Length (byte) | Value/Description |
|----------|---------------|--|
| Response | 4..72 | Array of up to 18 4-byte elements {Register content} |
| | 4..72 byte | Register content: n*4-Byte (32-bit) register data |

Description:

This command is used to read up to 18 configuration registers at once. The addresses are allowed to be in random order. The result (data of each register) is provided in the response to the command. Only the register values are included in the response. The order of the register contents within the response corresponds to the order of the register addresses within the command parameter.

Condition:

The address of the register must exist. The size of 'Register Address' array must be in the range from 1 – 18, inclusive. If the condition is not fulfilled, an exception is raised.

WRITE_EEPROM -0x06

Table 12. WRITE_EEPROM

| Payload | length (byte) | Value/Description |
|--------------|---------------|--|
| Command code | 1 | 0x06 |
| Parameter | 1 | Address in EEPROM from which write operation starts {EEPROM Address} |
| | 1..255 | Array of up to 255 elements {EEPROM content} |
| | 1 byte | EEPROM content |
| Response | - | - |

Description:

This command is used to write up to 255 bytes to the EEPROM. The field 'EEPROM content' contains the data to be written to EEPROM starting at the address given by byte 'EEPROM Address'. The data is written in sequential order.

Condition:

The EEPROM Address field must be in the range from 0 – 254, inclusive. The number of bytes within 'Values' field must be in the range from 1 – 255, inclusive. If the condition is not fulfilled, an exception is raised.

READ_EEPROM - 0x07

Table 13. READ_EEPROM

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x07 |
| Parameter | 1 | Address in EEPROM from which read operation starts (EEPROM Address) |
| | 1 | Number of bytes to read from EEPROM |

| Payload | Length (byte) | Value/Description |
|----------|---------------|--|
| Response | 1..255 | Array of up to 255 elements {EEPROM content} |
| | | 1 byte EEPROM content |

Description:

This command is used to read data from EEPROM memory area. The field 'Address' indicates the start address of the read operation. The field Length indicates the number of bytes to read. The response contains the data read from EEPROM (content of the EEPROM); The data is read in sequentially increasing order starting with the given address.

Condition:

EEPROM Address must be in the range from 0 to 254, inclusive. Read operation must not go beyond EEPROM address 254. If the condition is not fulfilled, an exception is raised.

WRITE_DATA - 0x08

Table 14. WRITE_DATA

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x08 |
| Parameter | 1..260 | Array of up to 260 bytes {Transmit data} |
| | | 1 byte Transmit data: Data written into the transmit buffer |
| Response | - | - |

Description:

This command is used to write data into the RF transmission buffer. The size of this buffer is 260 bytes. After this instruction has been executed, an RF transmission can be started by configuring the corresponding registers.

Condition:

The number of bytes within the 'Tx Data' field must be in the range from 1 to 260, inclusive. The command must not be called during an ongoing RF transmission. If the condition is not fulfilled, an exception is raised.

SEND_DATA - 0x09

Table 15. SEND_DATA

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x09 |
| Parameter | 1 | Number of valid bits in last Byte |
| | 1...260 | Array of up to 260 elements {Transmit data} |
| | | 1 byte Transmit data |
| Response | - | - |

Description:

This command writes data to the RF transmission buffer and starts the RF transmission. The parameter 'Number of valid bits in last Byte' indicates the exact number of bits to be transmitted for the last byte (for non-byte aligned frames).

Precondition: Host shall configure the Transceiver by setting the register SYSTEM_CONFIG.COMMAND to 0x3 before using the SEND_DATA command, as the command SEND_DATA is only writing data to the transmission buffer and starts the transmission but does not perform any configuration.

Table 16. Coding of 'valid bits in last byte'

| Number/Parameter | Functionality |
|------------------|--|
| 0 | All bits of last byte are transmitted |
| 1-7 | Number of bits within last byte to be transmitted. |

Note: When the command terminates, the transmission might still be ongoing, i.e. the command starts the transmission but does not wait for the end of transmission.

Condition:

The size of 'Tx Data' field must be in the range from 0 to 260, inclusive (the 0 byte length allows a symbol only transmission when the TX_DATA_ENABLE is cleared). 'Number of valid bits in last Byte' field must be in the range from 0 to 7. The command must not be called during an ongoing RF transmission. Transceiver must be in 'WaitTransmit' state with 'Transceive' command set. If the condition is not fulfilled, an exception is raised.

READ_DATA - 0x0A

Table 17. READ_DATA

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x0A |
| Parameter | 1 | x00 |
| Response | 1...508 | Array of up to 508 elements {Receive data} |
| | | 1 byte Receive data: data which had been received during last successful RF reception |

Description:

This command reads data from the RF reception buffer, after a successful reception. The RX_STATUS register contains the information to verify if the reception had been successful. The data is available within the response of the command. The host controls the number of bytes to be read via the SPI interface.

Condition:

The RF data had been successfully received. In case the instruction is executed without preceding an RF data reception, no exception is raised but the data read back from the reception buffer is invalid. If the condition is not fulfilled, an exception is raised.

SWITCH_MODE - 0x0B

Table 18. SWITCH_MODE

| Payload | Length (byte) | Value/Description |
|--------------|---------------|--|
| Command code | 1 | 0x0B |
| Parameter | 1 | Mode |
| | 1...n | Array of 'n' elements {Mode parameter} |
| | 1 byte | Mode parameter: Number of total bytes depends on selected mode |
| Return value | - | - |

Description:

This instruction is used to switch the mode. It is only possible to switch from normal mode to Standby, LPCD or Autocoll mode. Switching back to normal mode is not possible using this instruction. The modes Standby, LPCD and Autocoll terminate on specific conditions. Once a configured mode (Standby, LPCD, Autocoll) terminates, normal mode is entered again.

To force an exit from Standby, LPCD or Autocoll mode to normal mode, the host controller has to reset the PN5180.

Condition:

Parameter 'mode' has to be in the range from 0 to 2, inclusive. Dependent on the selected mode, different parameters have to be passed:

In case parameter 'mode' is set to 0 (Standby):

Field 'wake-up Control' must contain a bit mask indicating the enabled wake-up sources and if GPO shall be toggled. Field 'wake-up Counter Value' must contain the value used for the wake-up counter (= time PN5180 remains in standby). The value shall be in the range from 1 – 2690, inclusive.

Table 19. Standby configuration

| Parameter | Length (byte) | Value/Description |
|-----------------------|---------------|--|
| Wake-up Control | 1 | Bit mask controlling the wake-up source to be used and GPO handling. |
| Wake-up Counter Value | 2 | Used value for wake-up counter in msecs. Maximum supported value is 2690 |

Table 20. Standby wake-up counter configuration

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b1 | |
|----|----|----|----|----|----|----|----|--|
| 0 | 0 | 0 | 0 | 0 | 0 | | | RFU |
| | | | | | | X | | Wake-up on external RF field, if bit is set to 1b. |
| | | | | | | | X | Wake-up on wake-up counter expires, if bit is set to 1b. |

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The field has to be present, even if wake-up counter is not defined as wake-up source. In this case, the field ‘wake-up Counter value’ is ignored. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

In case parameter ‘mode’ is set to 1 (LPCD):

Field ‘wake-up Counter Value’ () defines the period between two LPCD attempts (=time PN5180 remains in standby) as has to be in the range from 1 to 2690, inclusive. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

Table 21. LPCD wake-up counter configuration

| Parameter | Length (bytes) | Value/Description |
|-----------------------|----------------|---|
| Wake-up Counter Value | 2 | Used value for wake-up counter in msecs. Maximum supported value is 2690. |

In case field ‘Mode’ is set to 2 (Autocoll):

Field ‘RF Technologies’ must contain a bit mask indicating the RF Technologies to support during Autocoll, according to Field ‘Autocoll Mode’ must be in the range from 0 to 2, inclusive. No instructions must be sent while being in this mode. Termination is indicated using an interrupt.

Table 22. Autocoll wake-up counter configuration

| Parameter | Length (bytes) | Value/Description |
|-----------------------|----------------|---|
| Wake-up Counter Value | 2 | Used value for wake-up counter in msecs. Maximum supported value is 2690. |

Table 23. Autocoll parameter

| Parameter | Length (bytes) | Value/Description |
|-----------------|----------------|--|
| RF Technologies | 1 | Bit mask indicating the RF technology to listen for during Autocoll |
| Autocoll Mode | 1 | 0 Autonomous mode not used, i.e. Autocoll terminates when external RF field is not present. |
| | | 1 Autonomous mode used. When no RF field is present, Autocoll automatically enters standby mode. Once RF external RF field is detected, PN5180 enters again Autocoll mode. |
| | | 2 Same as 1 but without entering standby mode. |

Table 24. Autocoll bit mask indicating the RF technologies

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b1 | |
|----|----|----|----|----|----|----|----|---|
| 0 | 0 | 0 | 0 | | | | | RFU |
| | | | | X | | | | If set, listening for NFC-F active is enabled |
| | | | | | X | | | If set, listening for NFC-A active is enabled |

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b1 | |
|----|----|----|----|----|----|----|----|--|
| | | | | | | X | | If set, listening for NFC-F is enabled |
| | | | | | | | X | If set, listening for NFC-A s enabled |

MIFARE_AUTHENTICATE - 0x0C

Table 25. MIFARE_AUTHENTICATE

| Payload | Length (bytes) | Value/Description |
|--------------|---|------------------------------------|
| Command code | 1 | 0x0C |
| Parameter | 6 | Key: Authentication key to be used |
| | 1 | Key type to be used: |
| | | 0x60 Key type A |
| | | 0x61 Key type B |
| 1 | Block address: The address of the block for which the authentication has to be performed. | |
| 4 | UID of the card | |
| Return value | 1 | Authentication Status |

Description:

This command is used to perform a MIFARE Classic Authentication on an activated card. It takes the key, card UID and the key type to authenticate at a given block address. The response contains 1 byte indicating the authentication status.

Condition:

Field 'Key' must be 6 bytes long. Field 'Key Type' must contain the value 0x60 or 0x61. Block address may contain any address from 0x0 – 0xff, inclusive. Field 'UID' must be 4 bytes long and should contain the 4 byte UID of the card. An ISO/IEC 14443-3 MIFARE Classic product-based card should be put into state ACTIVE or ACTIVE* prior to execution of this instruction.

In case of an error related to the authentication, the return value 'Authentication Status' is set accordingly (see Table 25).

Attention:

Timer2 is not available during the MIFARE Classic Authentication

If the condition is not fulfilled, an exception is raised.

Table 26. Authentication status return value

| Payload Field | Length (byte) | Value/Description |
|-----------------------|---------------|---|
| Authentication Status | 1 | 0 Authentication successful. |
| | | 1 Authentication failed (permission denied). |
| | | 2 Timeout waiting for card response (card not present). |
| | | 3..FF RFU |

EPC_INVENTORY - 0x0D

Table 27. EPC_INVENTORY PARAMETERS

| Payload | Length (byte) | Value/Description | |
|--------------|---------------|--|---|
| Command code | 1 | 0x0D | |
| Parameter | 1 | SelectCommandLength: | |
| | | 0 | No Select command is set prior to "BeginRound" command. 'Valid Bits in last Byte' field and 'Select' Command shall not be present |
| | | 1..39 | Length (n) of the 'Select' command |
| | 0, 1 | Valid Bits in last Byte | |
| | | 0 | All bits of last byte of 'Select command' field are transmitted |
| | | 1..7 | Number of bits to be transmitted in the last byte of 'Select command' field. |
| | 0..39 | Array of up to 39 elements {Select} | |
| | | 1 byte | Select: If present (dependent on the first parameter Select Command Length), this field contains the 'Select' command (according to ISO18000-3) which is sent prior to a BeginRound command. CRC-16c shall not be included. |
| | 3 | BeginRound: Contains the BeginRound command (according to ISO18000-3). CRC-5 shall not be included. | |
| | 1 | Timeslot behavior | |
| 0 | | Response contains max. Number of time slots which may fit in response buffer. | |
| 1 | | Response contains only one timeslot. | |
| | 2 | Response contains only one timeslot. If timeslot contains valid card response, also the card handle is included. | |
| Response | 0 | - | |

Description:

This instruction is used to perform an inventory of ISO18000-3M3 tags. It implements an autonomous execution of several commands according to ISO18000-3M3 in order to guarantee the timings specified by this standard.

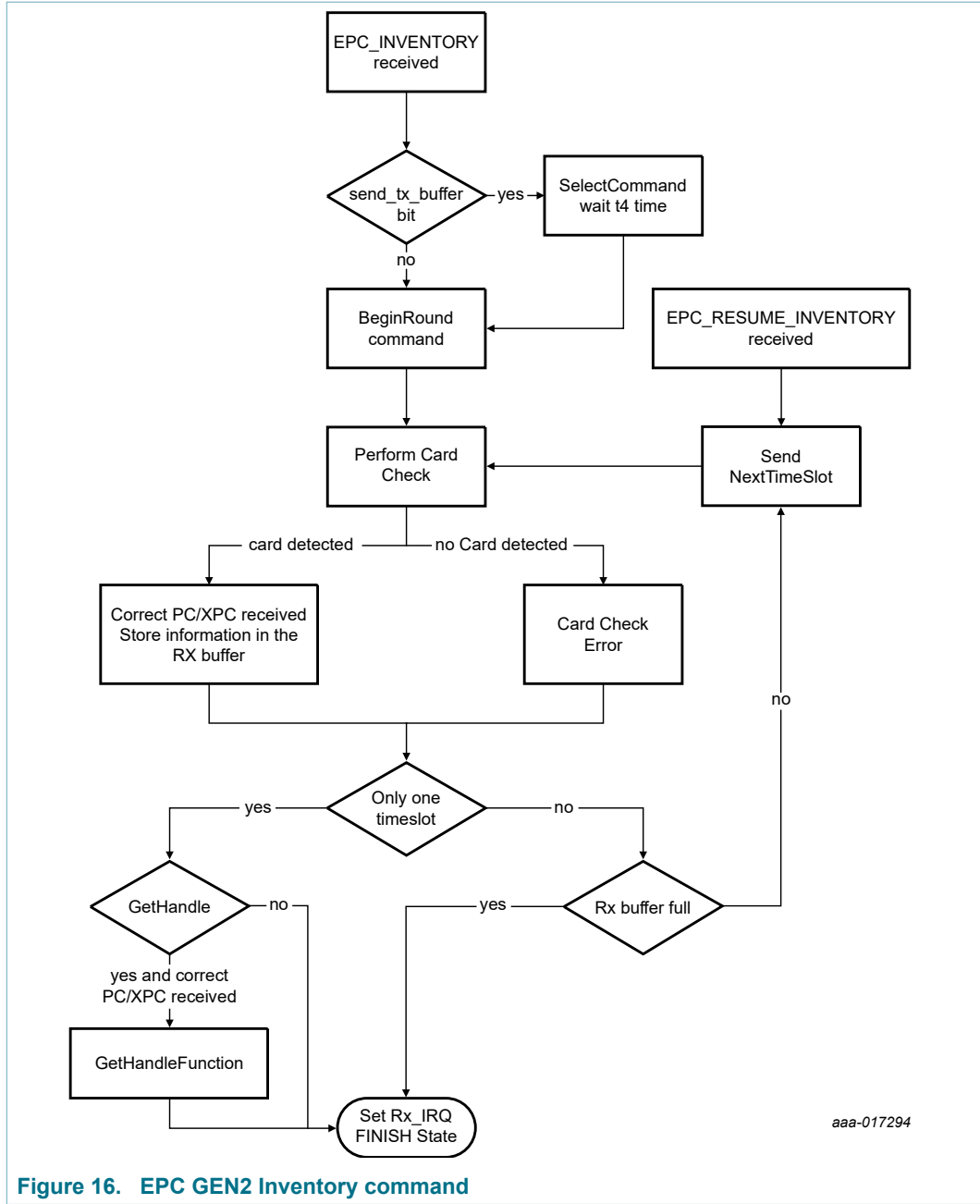


Figure 16. EPC GEN2 Inventory command

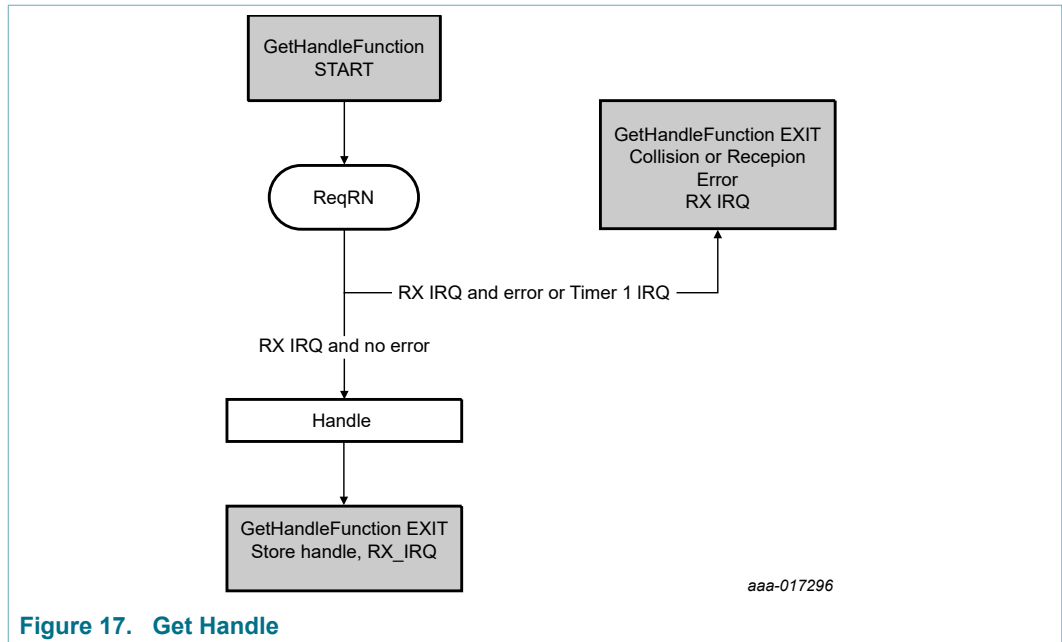


Figure 17. Get Handle

If present in the payload of the instruction, a ‘Select’ command is executed followed by a ‘BeginRound’ command. If there is a valid response in the first-time slot (no timeout, no collision), the instruction sends an ACK and saves the received PC/XPC/UII. The device performs then an action according to the definitions of the field ‘Timeslot Processed Behavior’:

- If this field is set to ‘0’, a NextSlot command is issued to handle the next time slot. This is repeated until the internal buffer is full
- If this field is set to 1 the algorithm pauses
- If this field is set to 2 a Req_Rn command is issued if, and only if, there has been a valid tag response in this timeslot

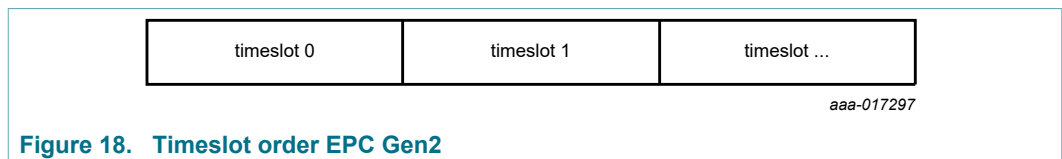


Figure 18. Timeslot order EPC Gen2

Condition:

If the condition is not fulfilled, an exception is raised.

EPC_RESUME_INVENTORY - 0x0E

Table 28. EPC_RESUME_INVENTORY PARAMETERS

| Payload | Length (byte) | Value/Description |
|--------------|---------------|-------------------|
| Command code | 1 | 0x0E |
| Parameter | 1 | 0x00 |
| Response | 0 | - |

Description:

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This instruction is used to resume the inventory algorithm for the ISO18000-3M3 Inventory in case it is paused. This instruction has to be repeatedly called, as long as 'Response Size' field in EPC_RETRIEVE_INVENTORY_RESULT_SIZE is greater than 0.

A typical sequence for a complete EPC GEN2 inventory retrieval is:

1. Execute EPC_INVENTORY to start the inventory
2. Execute EPC_RETRIEVE_INVENTORY_RESULT_SIZE
3. If size is 0, inventory has finished.
4. Otherwise, execute EPC_RETRIEVE_INVENTORY_RESULT
5. Execute EPC_RESUME_INVENTORY and proceed with step 2.

Condition:

Field 'RFU' must be present and can be set to any value. If the condition is not fulfilled, an exception is raised.

EPC_RETRIEVE_INVENTORY_RESULT_SIZE - 0x0F

Table 29. EPC_RETRIEVE_INVENTORY_RESULT_SIZE PARAMETERS

| Payload | length (byte) | Value/Description |
|--------------|---------------|--|
| Command code | 1 | 0x0F |
| Parameter | 1 | 0x00 |
| Response | 2 | Response size: If Response size == 0: Inventory has finished. If Response size == 1...512: Value indicates the length of the EPC_RETRIEVE_INVENTORY_RESULT response payload |

Description:

This instruction is used to retrieve the size of the inventory result. The size is located in the response to this instruction and reflects the payload size of the response to the next execution of EPC_RETRIEVE_INVENTORY_RESULT. If the size is 0, then no more results are available which means inventory algorithm has finished.

Condition:

Field Parameter1 must be present. If the condition is not fulfilled, an exception is raised.

EPC_RETRIEVE_INVENTORY_RESULT - 0x10

Table 30. EPC_RETRIEVE_INVENTORY_RESULT PARAMETERS

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x10 |
| Parameter | 1 | 0x00 |
| Response | 2 | Response size If Response size == 0: Inventory has finished. If Response size == 1...512: Value indicates the length of the EPC_RETRIEVE_INVENTORY_RESULT response payload |

Description:

This instruction is used to retrieve the result of a preceding or EPC_RESUME_INVENTORY instruction. The size of the payload within the response is determined by the 'Response Size' field of EPC_RETRIEVE_INVENTORY_RESULT_SIZE response. Depending on the 'Timeslot Processed Behavior' defined in that instruction, the result contains one or more time slot responses. Each timeslot response contains a status (field 'Timeslot Status') which indicates, that there has been a valid tag reply or a collision or no tag reply:

- 0 - Tag response available, XPC/PC/UII embedded in the response within 'Tag reply' field
- 1 - Tag response available and tag handle retrieved. XPC/PC/UII as well as tag handle available in the response within 'Tag reply' field and 'Tag Handle' field, respectively.
- 2 - No tag replied, empty time slot
- 3 - Collision, two or more tags replied in the same time slot

Condition:

Field 'RFU' must be present and can be set to any value. If the condition is not fulfilled, an exception is raised.

LOAD_RF_CONFIG - 0x11

Table 31. LOAD_RF_CONFIG PARAMETERS

| Payload | length (byte) | Value/Description |
|--------------|---------------|--------------------------------|
| Command code | 1 | 0x11 |
| Parameter | 1 | Transmitter configuration byte |
| | 1 | Receiver configuration byte |
| Response | 0 | - |

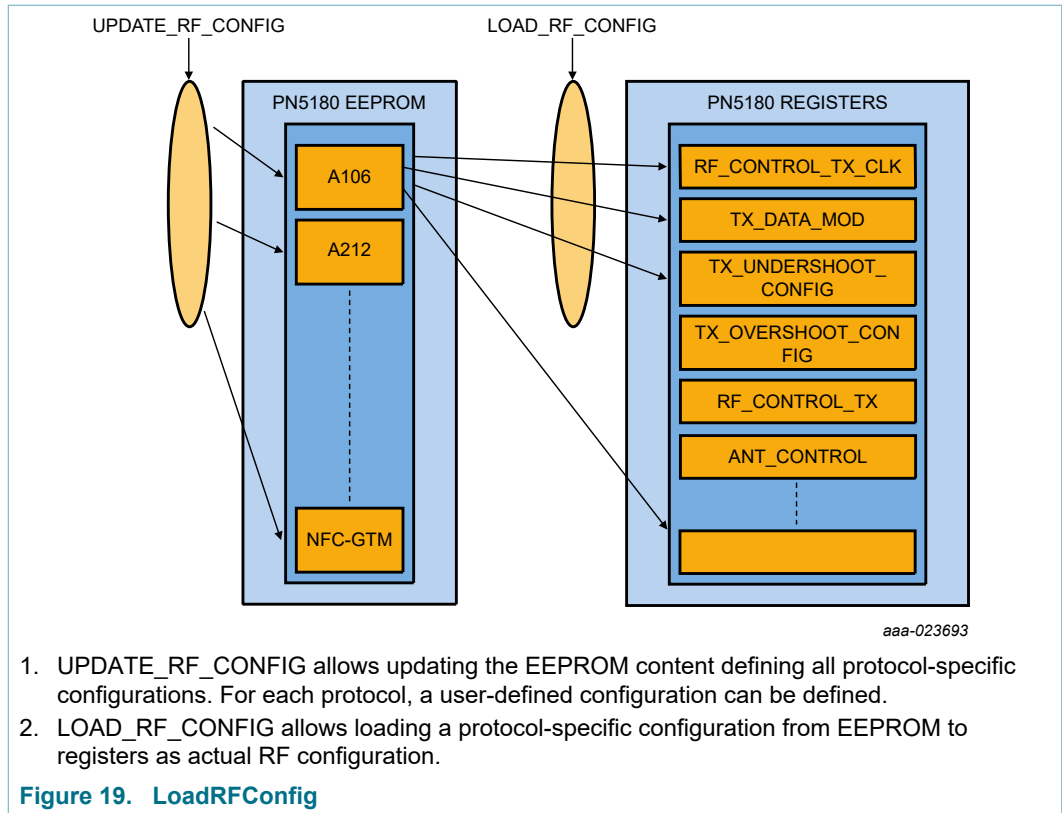
Description:

This instruction is used to load the RF configuration from EEPROM into the configuration registers. The configuration refers to a unique combination of "mode" (target/initiator) and "baud rate". The configurations can be loaded separately for the receiver (Receiver configuration) and transmitter (Transmitter configuration).

The PN5180 is pre-configured by EEPROM with settings for all supported protocols. The default EEPROM settings are considering typical antenna. It is possible for the user to modify the EEPROM content and by this adapt the default settings to individual antennas for optimum performance. The command UPDATE_RF_CONFIG is used for modification of the RF Configuration settings available in the EEPROM. There is no possibility to update the EEPROM data directly, updates have to make use of the UPDATE_RF_CONFIG command.

Note that the command LOAD_RF_CONFIG configures parameters which are not accessible by registers, and configures additional parameters depending on the protocol setting (e.g. the waveshaping AWC). It is required to execute the command LOAD_RF_CONFIG for a specific protocol first, before any register settings for this protocol are changed.

The parameter 0xFF has to be used if the corresponding configuration shall not be changed.



Condition:

Parameter 'Transmitter Configuration' must be in the range from 0x0 - 0x1C, inclusive. If the transmitter parameter is 0xFF, transmitter configuration is not changed.

Field 'Receiver Configuration' must be in the range from 0x80 - 0x9C, inclusive. If the receiver parameter is 0xFF, the receiver configuration is not changed. If the condition is not fulfilled, an exception is raised.

The transmitter and receiver configuration shall always be configured for the same transmission/reception speed. No error is returned in case this condition is not taken into account.

Table 32. LOAD_RF_CONFIG: Selection of protocol register settings

| Transmitter: RF configuration byte (hex) | Protocol | Speed (kbit/s) | Receiver: RF configuration byte (hex) | Protocol | Speed (kbit/s) |
|--|--------------------------|----------------|---------------------------------------|--------------------------|----------------|
| 00 | ISO 14443-A / NFC PI-106 | 106 | 80 | ISO 14443-A / NFC PI-106 | 106 |
| 01 | ISO 14443-A | 212 | 81 | ISO 14443-A | 212 |
| 02 | ISO 14443-A | 424 | 82 | ISO 14443-A | 424 |
| 03 | ISO 14443-A | 848 | 83 | ISO 14443-A | 848 |
| 04 | ISO 14443-B | 106 | 84 | ISO 14443-B | 106 |
| 05 | ISO 14443-B | 212 | 85 | ISO 14443-B | 212 |
| 06 | ISO 14443-B | 424 | 86 | ISO 14443-B | 424 |
| 07 | ISO 14443-B | 848 | 87 | ISO 14443-B | 848 |

High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes

| Transmitter: RF configuration byte (hex) | Protocol | Speed (kbit/s) | Receiver: RF configuration byte (hex) | Protocol | Speed (kbit/s) |
|--|-------------------------------------|----------------|---------------------------------------|--------------------------|----------------|
| 08 | FeliCa / NFC PI 212 | 212 | 88 | FeliCa / NFC PI 212 | 212 |
| 09 | FeliCa / NFC PI 424 | 424 | 89 | FeliCa / NFC PI 212 | 424 |
| 0A | NFC-Active Initiator | 106 | 8A | NFC-Active Initiator | 106 |
| 0B | NFC-Active Initiator | 212 | 8B | NFC-Active Initiator | 212 |
| 0C | NFC-Active Initiator | 424 | 8C | NFC-Active Initiator | 424 |
| 0D | ISO 15693 ASK100 | 26 | 8D | ISO 15693 | 26 |
| 0E | ISO 15693 ASK10 | 26 | 8E | ISO 15693 | 53 |
| 0F | ISO 18003M3 Manch. 424_4 Tari=18.88 | 106 | 8F | ISO 18003M3 Manch. 424_4 | 106 |
| 10 | ISO 18003M3 Manch. 424_2 Tari=9.44 | 212 | 90 | ISO 18003M3 Manch. 424_2 | 212 |
| 11 | ISO 18003M3 Manch. 848_4 Tari=18.88 | 212 | 91 | ISO 18003M3 Manch. 848_4 | 212 |
| 12 | ISO 18003M3 Manch. 848_2 Tari=9.44 | 424 | 92 | ISO 18003M3 Manch. 848_2 | 424 |
| 13 | ISO 18003M3 Manch. 424_4 | 106 | 93 | ISO 14443-A PICC | 106 |
| 14 | ISO 14443-A PICC | 212 | 94 | ISO 14443-A PICC | 212 |
| 15 | ISO 14443-A PICC | 424 | 95 | ISO 14443-A PICC | 424 |
| 16 | ISO 14443-A PICC | 848 | 96 | ISO 14443-A PICC | 848 |
| 17 | NFC Passive Target | 212 | 97 | NFC Passive Target | 212 |
| 18 | NFC Passive Target | 424 | 98 | NFC Passive Target | 424 |
| 19 | NFC Active Target 106 | 106 | 99 | ISO 14443-A | 106 |
| 1A | NFC Active Target 212 | 212 | 9A | ISO 14443-A | 212 |
| 1B | NFC Active Target 424 | 424 | 9B | ISO 14443-A | 424 |
| 1C | GTM | ALL | 9C | GTM | ALL |

UPDATE_RF_CONFIG - 0x12

Table 33. UPDATE_RF_CONFIG PARAMETERS

| Payload | length (byte) | Value/Description | |
|--------------|---------------|--|---|
| Command code | 1 | 0x12 | |
| Parameter | 6...252 | Array of up to 42 elements {RF configuration byte, Register Address, Register value} | |
| | | 1 byte | RF Configuration byte: RF configuration for which the register has to be changed. |
| | | 1 byte | Register Address: Register Address within the given RF technology. |
| | | 4 bytes | Register value: Value which has to be written into the register. |
| Response | - | - | |

Description:

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This instruction is used to update the RF configuration within the EEPROM. The command allows updating dedicated EEPROM addresses, in case the complete set does not require to be updated.

The payload parameters passed following the little endian approach (Least Significant Byte first).

Condition:

The size of the array of 'Configuration data' must be in the range from 1 – 42, inclusive. The array data elements must contain a set of 'RF Configuration byte', 'Register Address' and 'Value'. The field 'RF Configuration byte' must be in the range from 0x00 – 0x1C or 0x80-0x9C, inclusive. The address within field 'Register Address' must exist within the respective RF configuration. The 'Register Value' contains a value which will be written into the given register and must be 4 bytes long. If the condition is not fulfilled, an exception is raised.

RETRIEVE_RF_CONFIG_SIZE - 0x13

Table 34. RETRIEVE_RF_CONFIG_SIZE PARAMETERS

| Payload | length (byte) | Value/Description |
|--------------|---------------|--|
| Command code | 1 | 0x13 |
| Parameter | 1 | RF configuration ID: RF configuration for which the number of registers has to be retrieved. |
| Response | 1 | Number of registers for the selected "RF configuration ID" |

Description:

This command is used to retrieve the size (number of 32-bit registers) of a given RF configuration. The size is available in the response to this instruction.

Condition:

The field 'RF configuration ID' must be in the range from 0x00 - 0x1C or 0x80-0x9C, inclusive. If the condition is not fulfilled, an exception is raised.

RETRIEVE_RF_CONFIG - 0x14

Table 35. RETRIEVE_RF_CONFIG PARAMETERS

| Payload | length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x14 |
| Parameter | 1 | RF configuration ID: RF configuration for which the number of 32-bit registers has to be retrieved. |
| Response | 0...39 | Array of up to 39 elements {RegisterAddress, RegisterContent} |
| | 1 byte | RegisterAddress: Address of the register to read |
| | 4 bytes | RegisterContent: Data of register addressed by this element |

Description:

This command is used to read an RF configuration. The register content available in the response. In order to know how many pairs are to be expected, the command RETRIEVE_RF_CONFIGURATION_SIZE has to be executed first.

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The payload parameters passed following the little endian approach (Least Significant Byte first).

Condition:

The field 'RF configuration ID' must be in the range from 0x00-0x1C or 0x80-0x9C, inclusive. If the condition is not fulfilled, an exception is raised.

COMMAND RFU - 0x15

Table 36. RFU

| Payload | length (byte) | | Value/Description |
|--------------|---------------|------|-------------------|
| Command code | 1 | 0x15 | RFU |
| Parameter | - | | |
| Response | - | | |

Description:

This command is reserved for future use.

RF_ON - 0x16

Table 37. RF_ON

| Payload | length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x16 |
| Parameter | 1 | Bit0 == 1: disable collision avoidance according to ISO18092 Bit1 == 1: Use Active Communication mode according to ISO18092 |
| Response | - | - |

Description:

This command is used to switch on the internal RF field. If enabled the TX_RFON_IRQ is set after the field is switched on.

RF_OFF - 0x17

Table 38. RF_OFF

| Payload | length (byte) | Value/Description |
|--------------|---------------|--------------------------------|
| Command code | 1 | 0x17 |
| Parameter | 1 | dummy byte, any value accepted |
| Response | - | - |

Description:

This command is used to switch off the internal RF field. If enabled, the TX_RFOFF_IRQ is set after the field is switched off.

CONFIGURE_TESTBUS_DIGITAL - 0x18

Table 39. CONFIGURE_TESTBUS_DIGITAL

| Payload | length (byte) | Value/Description |
|--------------|---------------|--|
| Command code | 1 | 0x18 |
| Parameter | 1 | Signal Bank |
| | 1*n | TB_POS: Pad Location (bits 4:7) and digital test signal definition (bits 0:3) n can have a value between 1 and 4 |
| Response | - | - |

Description:

This command defines the type of digital test signals and their output pins on the chip.

The test bus must be enabled in the EEPROM settings (EEPROM address: 0x17, TESTBUS_ENABLE) before any signal will appear on the output pins.

There are several signal banks which can be selected, defined by the first Parameter "Signal Bank".

The second parameter, TB_POS, is defining the type of digital signal in the lower nibble (bits 0:3) of the parameter byte, and the output pin in the upper nibble (bits 4:7). All digital output pins are able to provide a digital output signal at the same time.

Sending 1- to 4-times the TB_POS configuration byte allows configuring

TB_POS byte (Pad location for signal output) has to be configured in the following way:

Table 40. TB_POS

| BitPos | Value | Description |
|--------|--------|--|
| 0_3 | 0..7h | Signal Selection of the Signal Bank |
| | 8h | 13 MHz RF clock |
| | 9h..Fh | RFU |
| 4:7 | 0h | IRQ pin (B2 on TFBGA64 -39 on HVQFN40) |
| | 1h | AUX1 pin (B1 on TFBGA64 - 40 on HVQFN40) |
| | 2h | AUX2 pin (C1 on TFBGA64 - 02 on HVQFN40) |
| | 3h | GPO1 pin (B3 on TFBGA64 - 38 on HVQFN40) |
| | 4h..Fh | RFU |

The digital debug output is configured by the command CONFIGURE_TESTBUS_DIGITAL. Two parameters are passed within this command.

The first parameter (1 byte) defines the test signal group. Out of this test signal group, one signal can be selected for output on a pin of the PN5180 (4 bits).

The signal type of the chosen test signal group is selected by the low-nibble of parameter 2. A value of 8 on this position selects the 13.56 MHz clock to be put out on the selected pin.

The high nibble of parameter 2 (1 byte) selects the output pin for the selected test signal.

The following parameter groups are possible:

Table 41. Debug Signal Group Selection

| Command parameter (hex) | Debug Signal Group |
|-------------------------|------------------------------|
| 01 | Clock signal group |
| 1B | Transmitter encoder group |
| 1D | Timer group |
| 30 | Card mode protocol group |
| 58 | Transceive group |
| 70 | Receiver data transfer group |
| 73 | Receiver error group |

The second parameter defines the pin which is used for output of the test signal in the high nibble, and the signal from one of the Debug Signal groups that are put out in the low nibble.

Table 42. Clock Signal Group

| Value low nibble (HEX) | Debug Function |
|------------------------|---|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | CLIF clock reset |
| 6 | Signal indicating the PLL is locked |
| 5 | Signal indicating an external Field is present |
| 4 | 20 MHz clock from the high frequency oscillator |
| 3 | 27.12 MHz clock from the PLL |
| 2 | 27.12 MHz clock from the RF clock recovery |
| 1 | Multiplexed 27.12 MHz clock |
| 0 | Multiplexed 13.56 MHz clock |

Table 43. Transmitter Encoder Group

| Value low nibble (HEX) | Debug Function |
|------------------------|----------------------------|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7..2 | RFU |
| 1 | Output TX envelope |
| 0 | Tx-IRQ |

Table 44. Timer Group

| Value low nibble (HEX) | Debug Function |
|------------------------|-----------------------------|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Running flag of timer T0 |
| 6 | Expiration flag of timer T0 |
| 5 | Running flag of timer T1 |
| 4 | Expiration flag of timer T1 |
| 3 | Running flag of timer T2 |
| 2 | Expiration flag of timer T2 |
| 1..0 | RFU |

Table 45. Card mode Protocol Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz Clock is put out |
| 7 | Synchronized clock-fail signal |
| 6 | Flag indicating that ISO/IEC14443-Type A (Miller) was detected |
| 5 | Flag indicating that FeliCa 212 kBd (Manchester) was detected |
| 4 | Flag indicating that FeliCa 424 kBd (Manchester) was detected |
| 3 | Flag indicating that ISO/IEC14443-Type B (NRZ) was detected |
| 2 | Flag indicating that the EOF was detected |
| 1 | CM data signal (Miller / Manchester / NRZ) |
| 0 | Signal indicating that the current data is valid |

Table 46. Transceiver Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Signal indicating that the tx prefetch was completed |
| 6 | Signal initiating a tx prefetch at the BufferManager |
| 5 | Start of transmission signal to TxEncoder |
| 4 | enable reception signal to RxDecoder |
| 3 | indicator that the waiting time was already expired |
| 2 | Transceiver state2 |

| Value low nibble (HEX) | Debug Function |
|------------------------|-------------------|
| 1 | Transceive state1 |
| 0 | Transceive state0 |

Table 47. Receiver Data Transfer Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Signal from SigPro indicating a collision |
| 6 | Signal from SigPro indicating end of data |
| 5 | Signal from SigPro indicating that data is valid |
| 4 | Signal from SigPro indicating received data |
| 3 | Status signal set by rx_start, ends when RX is completely over |
| 2 | Status signal indicating actual reception of data |
| 1 | Reset signal for receiver chain (at start of RX) |
| 0 | Internal RxDec bitclk |

Table 48. Receiver Error Group

| Value low nibble (HEX) | Debug Function |
|------------------------|---|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Combination of data/protocol error and collision |
| 6 | Set if RxMultiple is set, and the LEN byte indicates more than 28 bytes |
| 5..3 | RFU |
| 2 | Set if a collision has been detected |
| 1 | Protocol error flag |
| 0 | Data integrity error flag (Parity, CRC (Collision)) |

CONFIGURE_TESTBUS_ANALOG - 0x19

Table 49. CONFIGURE_TESTBUS_ANALOG

| Payload | Length (byte) | Value/Description |
|--------------|---------------|---|
| Command code | 1 | 0x19 |
| Parameter | 1 | Defines test signal to be provided on AUX2, the analog test signal type is defined by value (see table 49.) |

| Payload | Length (byte) | Value/Description |
|---------|---------------|---|
| | 1 | Defines test signal to be provided on AUX1, the analog test signal type is defined by value (see table 49.) |

Description:

This command enables the Analog test bus.

The command uses two parameters (each with length of 1 byte) for definition of the analog test signal type.

The test bus must be enabled in the EEPROM settings (EEPROM address: 0x17, TESTBUS_ENABLE) before any signal will appear on the output pins.

Please note "that waiting until BUSY is high" is required by the host as described in chapter 11.4.1.

Table 50. ANALOG TEST SIGNALS

| Signal Name | Parameter | Description |
|----------------|-----------|--|
| DAC_VALUE_OUT | 0h | Analog output of value defined in register DAC_VALUE |
| ADC_DATA_Q | 1h | Receiver Q-channel signal; |
| ADC_DATA_I | 2h | Receiver I-channel signal; |
| ADC_DATA_QS | 3h | Filtered Q-Channel Signal (rect-filter) |
| ADC_DATA_IS | 4h | Filtered I-Channel Signal (rect-filter) |
| AUTO_MIN_LEVEL | 5h | Defines threshold for bit detection during start bit (adjusted by minlevel register setting), after start bit detection autominlevel is 50% of the signal strength (nonlinear reduction of the correlation result) |
| CORR_FILT | 6h | Filtered correlation result; bit detected if above autominlevel |
| CORR | 7h | Correlation result, used to adjust autominlevel (start bit detection) |
| RFU | 8h | - |
| BPSK_SUM | 9h | Result of correlation for BPSK (if above threshold (adjusted by MIN_LEVELP register) a phase shift is detected) |
| DPRESENT_SUM | Ah | Correlation value for subcarrier detection (if above threshold (adjusted by minlevel register setting) subcarrier is present); only valid for if BPSK enabled; it is derived by a linear reduction of dpresent_sum_raw |

11.5 Memories

11.5.1 Overview

The PN5180 implements two different memories: EEPROM and RAM.

At start-up, all registers are initialized with default values. For the registers defining the RF functionality, the default values are not set to execute any contactless communication.

The registers defining the RF functionality are initialized by using the instruction LOAD_RF_CONFIGURATION.

Using the instruction LOAD_RF_CONFIGURATION, the initialization of the registers which define the RF behavior of the IC performs an automatic copy of a predefined EEPROM area (read/write EEPROM section1 and section2, register reset) into the registers defining the RF behavior.

11.5.2 EEPROM

The EEPROM memory maintains its content during Power-OFF, whereas the RAM (Buffers) does not keep any data stored in this volatile memory.

The EEPROM address range is from 0x00 to 0xFF.

The EEPROM contains information about Die Identifier, Firmware Version, System configuration and RF settings for fast configuration.

Table 51. EEPROM Addresses

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|----------------------|---------------------|--------|--------------|------|---|
| 0x00 | Die identifier | R | 16 | - | Each die has a unique Identifier. This entry can be treated as 16 byte unique random number. |
| 0x10 | Product Version | R | 2 | 15-0 | Product Version (Major version, minor version) - this indicates the original Firmware version as loaded into the PN5180 during production. A secure firmware update does not change the content of these EEPROM addresses. |
| 0x12 | Firmware Version | R | 2 | 15-0 | Firmware Versions (major version, minor version): FW 3.A <ul style="list-style-type: none"> EEPROM address 0x12: 0x0A EEPROM address 0x13: 0x03 FW 4.0 <ul style="list-style-type: none"> EEPROM address 0x12: 0x00 EEPROM address 0x13: 0x04 FW 4.1 <ul style="list-style-type: none"> EEPROM address 0x12: 0x01 EEPROM address 0x13: 0x04 |
| 0x14 | EEPROM Version | R | 2 | 15-0 | EEPROM Version Number (default initialization values, e.g. for Load_RF_Config, register reset values, default DPC settings) For PN5180A0HN/C1 and PN5180A0HN/C2: Version is: 00 93 |
| 0x16 | IDLE_IRQ_AFTER_BOOT | RW | 1 | 7-0 | This enables the IDLE IRQ to be set after the boot has finished |
| 0x17 | TESTBUS_ENABLE | RW | 1 | 7-0 | If bit 7 is set, the test bus functionality is enabled. |
| 0x18 | XTAL_BOOT_TIME | RW | 2 | 15-0 | XTAL boot time in us |
| 0x1A | IRQ_PIN_CONFIG | RW | 1 | 7-0 | Configures the state (active high/low) and clearing conditions for the IRQ pin |
| | | | | 0 | Cleared: IRQ active low |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|----------------------|-------------------------|--------|--------------|------|--|
| | | | | | Set: IRQ active high |
| | | | | 1 | Cleared: Use IRQ_CLEAR to clear IRQ pin Set: Auto Clear on Read of IRQ_STATUS |
| 0x1B | MISO_PULLUP_ENABLE | RW | 1 | 7-0 | Configures the pullup resistor for the SPI MISO |
| | | | | 2-0 | 000b - no pulldown 001b - no pullup 010b - pulldown 011b - pullup |
| | | | | 7-3 | 04h - FFh RFU |
| 0x1C | PLL_DEFAULT_SETTING | R/W | 8 | | PLL configuration of clock input frequency in case a 13.56 MHz Crystal is not used. The PLL setting needs to be written as two 4-byte words to the memory, little endian. This means that the e.g the value for 8 MHz (03A3531002A12210) shall be written as follows to the EPROM (ascending addresses starting at 0x1C): 10 53 A3 0310 22 A1 02 8 MHz: 03A35310 - 02A12210 12 MHz: 02A38288 - 02E10190 16 MHz: 02E2B1D8 - 02D11150 24 MHz: 02D35138 - 02E0E158 (default) |
| 0x24 | PLL_DEFAULT_SETTING_ALM | R/W | 8 | - | PLL configuration for the Active Load Modulation |
| 0x2c | PLL_LOCK_SETTING | R/W | 4 | 31-0 | Lock Settings for the PLL - do not change |
| 0x30 | CLOCK_CONFIG | RW | 1 | | Configures the source of the clock, either 27.12 MHz crystal or external clock with PLL refactoring |
| | | | | 7-3 | RFU |
| | | | | 2-0 | 000b: External clock source(8 MHz, 12 MHz, 16 MHz, 24 MHz. Default 24 MHz); 001b: RFU; 010b: RFU; 011b: XTAL; 100b-111b: RFU |
| 0x31 | RFU | RW | 1 | 7-0 | - |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|---|-------------------------|--------|--------------|------|---|
| 0x32 | MFC_AUTH_TIMEOUT | RW | 2 | 15-0 | Timeout value used for each of the Auth1 & Auth2 stages during MFC Authenticate (MIFARE Classic Authenticate). This is an unsigned 16-bit integer value in little endian order. The timebase for the timeout is 1.0 microseconds. Example: The default value of 0x0, 0x5 refers actually to 0x500 (1280 decimal) resulting in a timeout of 1.28 ms for each of the authentication stages. |
| 0x34 | LPCD_REFERENCE_VALUE | RW | 1 | 3-0 | LPCD Gear Number; defines the gear used for the LPCD in case of LPCD AUTO CALIBRATION |
| | | | | 7-4 | RFU |
| 0x35 | RFU | | 1 | 7-0 | - |
| 0x36 | LPCD_FIELD_ON_TIME | RW | 1 | 7-0 | 1 byte delay * 8 in microseconds settling time for AGC measurement |
| 0x37 | LPCD_THRESHOLD | RW | 1 | 7-0 | 1 byte AGC threshold value which is used to compare against the (Current AGC value – Reference AGC) during the Low-Power Card Detection phase |
| 0x38 | LPCD_REFVAL_GPO_CONTROL | RW | 1 | 7-0 | This byte in EEPROM is used to control the GPIO assertion during wake-up and LPCD card detect. |
| | | | | 1:0 | LPCD Mode |
| | | | | | 00b - LPCD AUTO CALIBRATION Performs one calibration with gear number as defined in EEPROM (LPCD_REFERENCE_VALUE, bit 3:0) and starts LPCD afterwards. |
| | | | | | 01b - LPCD SELF CALIBRATION LPCD is started using the gear (AGC_GEAR) and AGC reference value (AGC_REF) as available in register ACG_REF_CONFIG |
| | | | | | 10b - RFU |
| | | | | | 11b - RFU |
| | | | | 2 | GPO1 Control for external TVDD DC-DC |
| | | | | | 0b - Disable Control of external TVDD DC-DC via GPO1 1b - Enable Control of external TVDD DC-DC via GPO1 |
| | | | | 3 | GPO2 Control for external TVDD DC-DC during wake-up from standby |
| | | | | | 0b - Disable Control of external TVDD DC-DC via GPO2 on LPCD Card Detect |
| 1b - Enable Control of external TVDD DC-DC via GPO2 on LPCD Card Detect | | | | | |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|----------------------|---------------------------------|--------|--------------|------|---|
| | | | | 4 | GPO1 Control for external TVDD DC-DC during wake-up from standby 0b - Disable Control of external TVDD DC-DC via GPO1 on wake-up from standby 1b - Enable Control of external TVDD DC-DC via GPO1 on wake-up from standby |
| 0x39 | LPCD_GPO_TOGGLE_BEFORE_FIELD_ON | | 1 | 7-0 | 1 byte value defines the time between setting GPO until Field is switched on. The time can be configured in 8 bits in 5us steps |
| 0x3A | LPCD_GPO_TOGGLE_AFTER_FIELD_OFF | RW | 1 | 7-0 | 1 byte value defines the time between Field Off and clear GPO. The time can be configured in 8 bits in 5us steps |
| 0x3B | NFCLD_SENSITIVITY_VAL | RW | 1 | 7-0 | NFCLD Sensitivity value to be used during the RF On Field handling Procedure. |
| 0x3C | FIELD_ON_CP_SETTLE_TIME | RW | 1 | 7-0 | Delay in 4us steps (range: 0 - 1020us) to wait during RF on for charge pumps to be settled, to avoid initial Tx driver overcurrent |
| 0x3D | RFU | RW | 2 | 15-0 | RFU |
| 0x3F | RF_DEBOUNCE_TIMEOUT | RW | 1 | 7-0 | Defines the delay time in steps of 10 μ s between two samples of the external RF field detection. This time applies only in card mode. |
| 0x40 | SENS_RES | RW | 2 | 15-0 | Response to ReqA / ATQA in order byte 0, byte 1 |
| 0x42 | NFCID1 | RW | 3 | 23-0 | If Random UID is disabled (EEPROM address 0x51), the content of these addresses is used to generate a Fixed UID. The order is byte 0, byte 1, byte 2; the first NFCID1 byte is fixed to 08h, the check byte is calculated automatically |
| 0x45 | SEL_RES | RW | 1 | 7-0 | Response to Select |
| 0x46 | FELICA_POLLING_RESPONSE | RW | 18 | - | FeliCa Polling response (2 bytes (shall be 01h, FEh) + 6 bytes NFCID2 + 8 bytes Pad + 2 bytes system code) |
| 0x51 | RandomUID_enable | RW | 1 | 7-0 | Enables the use of a RandomUID in card modes. If enabled (EEPROM configuration, Address 0x51), a random UID is generated after each RF-off. 0: Use UID stored in EEPROM 1: Randomly generate the UID |
| 0x58 | RANDOM_UID_ENABLE | RW | 1 | 7-0 | Enables the use of a RandomUID in card modes. If enabled (EEPROM configuration, Address 0x51), a random UID is generated after each RF-off. 0: Use UID stored in EEPROM 1: Randomly generate the UID |
| 0x59 | DPC_CONTROL | RW | 1 | 7-0 | Enables DPC and configures DPC gears |
| | | | | 0 | DPC_ENABLE cleared: OFF; set: ENABLE |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|----------------------|-----------------------|--------|--------------|-------|--|
| | | | | 3-1 | GEAR_STEP_SIZE: binary definition of gear step size; position of Bit 1 is the LSB of gear step size |
| | | | | 7-4 | START_GEAR; binary definition of start gear, Position of bit 4 is the LSB of start gear number |
| 0x5A | DPC_TIME | RW | 2 | 15-0 | Sets the value for the periodic regulation. Time base is 1/20 MHz. (Example: Value of 20000 is equal to 1 ms) |
| 0x5C | DPC_XI | RW | 1 | 7-0 | Trim Value of the AGC value |
| 0x5D | AGC_CONTROL | RW | 2 | | Settings for AGC control loop |
| | | | | 9-0 | Duration |
| | | | | 10 | Duration enable |
| | | | | 12-11 | Step size |
| | | | | 13 | Step size enable |
| 15-14 | RFU | | | | |
| 0x5F | DPC_THRSH_HIGH | RW | 30 | - | Defines the AGC high threshold for each gear. DPC_AGC_GEAR_LUT_SIZE defines the number of gears. DPC_AGC_GEAR_LUT_SIZE can be 1..15. The threshold is defined by 2 bytes (bit0 located in the byte with lower address), |
| 0x7D | DPC_THRSH_LOW | RW | 2 | 15-0 | RFU |
| 0x7F | DPC_DEBUG | RW | 1 | 7-0 | Enables the debug signals |
| 0x80 | DPC_AGC_SHIFT_VALUE | RW | 1 | 7-0 | Shift Value for the AGC dynamic low adoption to prevent oscillation |
| 0x81 | DPC_AGC_GEAR_LUT_SIZE | RW | 1 | 7-0 | Defines the number of gears for the lookup table (LUT, value can be between 1...15) |
| 0x82 | DPC_AGC_GEAR_LUT | RW | 15 | - | Defines the Gear Setting for each step size starting with Gear0 at lowest address up to 15 gears. Each entry contains a definition for the DPC_CONFIG register content. Bits 8:11 are not taken into account. |
| 0x91 | DPC_GUARD_FAST_MODE | RW | 2 | 15-0 | Guard time after AGC fast mode has been triggered. This happens in the following scenarios: - End of Receive - End of Transmit - After a gear switch Time base is 1/20 MHz (Example: Value of 2000 is equal to 100 μs) |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments | |
|----------------------|------------------------|--|--------------|-------------|--|---|
| 0x93 | DPC_GUARD_SOF_DETECTED | RW | 2 | 15-0 | Guard time after SoF or SC detection. This is to avoid any DPC regulation between SoF/SC and actual begin of reception. Time base is 1/20MHz (Example: Value of 2000 is equal to 100 µs) | |
| 0x95 | DPC_GUARD_FIELD_ON | RW | 2 | 15-0 | Guard time after Gear Switch during FieldOn instruction. Time base is 1/20MHz (Example: Value of 2000 is equal to 100 µs) | |
| 0x97 | PCD_AWC_DRC_LUT_SIZE | RW | 1 | 3:0 | AWC Lookup table size in number of elements | |
| | | | | 7:4 | DRC lookup table size in number of elements | |
| 0x98 | PCD_AWC_DRC_LUT | R/W | 80 | | Adaptive Waveshaping Control (AWC) and Adaptive Receiver Control (ARC) configuration | |
| | | | | dynam ic | 3:0 | DPC Gear |
| | | | | | 7:4 | TAU_MOD_FALLING (Sign bit (MSB) + 3-bit value) |
| | | | | | 11:8 | TAU_MOD_RISING (Sign bit (MSB)+ 3-bit value) |
| | | | | | 15:12 | RESIDUAL_CARRIER (Sign bit (MSB) + 3-bit value) |
| | | | | | 28-16 | Bitmask identifying technology and baud rate: |
| | | | | | | bit 16#: 0000.0000.0000b - A106 |
| | | | | | | bit 17#: 0000.0000.0001b - A212 |
| | | | | | | bit 18#: 0000.0000.0010b - A424 |
| | | | | | | bit 19#: 0000.0000.0100b - A848 |
| | | | | | | bit 20#: 0000.0000.1000b - B106 |
| | | | | | | bit 21#: 0000.0001.0000b - B212 |
| | | | | | | bit 22#: 0000.0010.0000b - B424 |
| | | bit 23#: 0000.0100.0000b - B848 | | | | |
| | | bit 24#: 0000.1000.0000b -F212 | | | | |
| | | bit 25#: 0001.0000.0000 -F424 | | | | |
| | | bit 26#: 0010.0000.0000b - 15693 ASK 100 | | | | |
| | | bit 27#: 0100.0000.0000 - 15693 ASK 10 | | | | |
| | | bit 28#: 1000.0000.0000b - ISO18000 3M3 | | | | |
| | | | 31-29 | RFU | | |
| 0xE8 | Misc_Config | R/W | 1 | | Digital delay can be enabled in firmware by setting Bit3 of bMisc_Config byte in EEPROM. The digital delay of highest baud rate for each technology is stored in DIGITAL_CONFIG location in EEPROM. The host software now does need not calculate the additional delay required for every technology baud-rate. | |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|----------------------|-----------------------------|--------|--------------|------|---|
| | | | | 0 | DigitalDelayFWEnabled. 0: Disable digital delay in FW. 1: Enable digital delay. |
| | | | | 2-1 | Clif timer select 00b: timer0 -01b: timer1 -10b: timer2 |
| | | | | 3 | Enable/ Disable Internal regulated 3.3 V output (LDO_OUT) |
| | | | | 4 | DPC_XI_RAM_CORRECTION Enable/Disable bit: If this bit is set, the trim value for the AGC is the sum of the trim value stored in EEPROM and in the SYSTEM_CONFIG register (bits 19:12) |
| | | | | 7-5 | RFU |
| 0xE9 | DigiDelay_A_848 RW | R/W | 1 | 7-0 | Base digiDelay in used for type A: 848 base, 424 = base*2, 212 = Base*4, 106 = Base*8 |
| 0xEA | DigiDelay_B_848 RW | R/W | 1 | 7-0 | Base digiDelay in used for type B 848 base, 424 = base*2, 212 = Base*4, 106 = Base*8 |
| 0xEB | DigiDelay_F_424 RW | R/W | 1 | 7-0 | Base digiDelay in used for type F 424 base, 212 = Base*2 |
| 0xEC | DigiDelay_15693 RW_FastHigh | R/W | 1 | 7-0 | Base digiDelay in used for ISO15693 FAST_HIGH base, HIGH = base*2 |
| 0xED | DigiDelay_18000_2_848 | R/W | 1 | 7-0 | Base digiDelay in used for type 18000_2_848 |
| 0xEE | DigiDelay_18000_4_848 | R/W | 1 | 7-0 | Base digiDelay in used for type 18000_4_848 |
| 0xEF | RFU | R/W | 1 | 7-0 | - |
| 0xF0 | TestbusMode | R/W | 1 | 7-0 | 1 = TESTBUS_MODE_ANALOG. 2 = TESTBUS_MODE_DIGITAL |
| 0xF1 | TbSelect | R/W | 1 | 7-0 | NUM_VALID_DIGI_TBSELECT = {0x00,0x01,0x10,0x1B,0x1D,0x30,0x58,0x70,0x73,0xB9} NUM_VALID_ANA_DAC_SRC_CONFIG = {0x01,0x02,0x03,0x04,0x05,0x06,0x07,0x09,0x0a} |
| 0xF2 | MapTb1_to_Tb0 | R/W | 1 | 7-0 | 0: Map Tb0 to Tb1 (default) 1: Map Tb1 to Tb0 |
| 0xF3 | NumPadSignalMaps | R/W | 1 | 7-0 | Number of Pad signal maps configured. |
| 0xF4 | PadSignalMap | R/W | 4 | 7-0 | 0xXY (X: Pad Location, Y: Test bus Bit position) X = Pad location 0 - IRQ (PWR_REQ) pin 1 - AUX2 (CLK_REQ) pin 2 - DWL_REQ pin 3 - AUX1 (TB6) pin 4-15 - RFU |

| EEPROM Address (HEX) | Field / Value | Access | Size (bytes) | Bits | Comments |
|-----------------------------|--------------------------------|--------|--------------|------|---|
| | | | | | Y = bit position of the test bus to be routed to the pad 7..0 - bit7...bit0 on the test bus 8 - 13 MHz clock is available |
| 0xF5-0xF7 | RFU | - | 1 | 7-0 | RFU |
| 0xF8 | TbDac1 | R/W | 1 | 7-0 | dac1 sources are routed to IRQ |
| 0xF9 | TbDac2 | R/W | 1 | 7-0 | dac2 sources are routed to AUX2 |
| From firmware V4.1 onwards: | | | | | |
| 0xFA | Legacy_typeB_handling_enable | R/W | 1 | 1 | Enable/Disable handling of legacy Type B card: Enable: bit 0 is set, Disable: Bit 0 is cleared |
| 0xFB | Legacy_typeB_handling_interval | R/W | 1 | 1 | Length of the added extra modulation pulse in micro seconds. |
| 0xFC | DPC Config | R/W | 1 | 1 | Configuration to enable DPC based on required IRQ's |
| 0xFD-0xFE | RFU | - | 1 | 7-0 | RFU |

11.5.3 RAM

The RAM is used as Input/Output buffer, and implements independent buffers for input and output. The buffers are able to improve the performance of a system with limited interface speed.

11.5.4 Register

Registers configure the PN5180 for a specific RF protocol and other functionality. Registers can be initialized using the host interface or by copying data from EEPROM to the register as done by the command `LOAD_RF_CONFIG`.

It is mandatory to use the command `LOAD_RF_CONFIG` for selection of a specific RF protocol.

11.6 Debug Signals

11.6.1 General functionality

The debugging of the RF functionality of the PN5180 is supported by a configurable test signal output possibility. Up to 2 analog or up to 4 digital test signals can be routed to configurable output pins of the PN5180. Test signals can be either analog or digital signals. The analog test signals contain the digital data of the signal processing unit of the PN5180, converted to analog signals by two DAC's to allow the inspection of these signals in real time.

The test bus functionality as such must be enabled in the EEPROM settings (EEPROM address: 0x17, `TESTBUS_ENABLE`).

Two commands exist for configuration of the digital and analog debug signal output, CONFIGURE_TESTBUS_DIGITAL and CONFIGURE_TESTBUS_ANALOG.

11.6.2 Digital Debug Configuration

The digital debug output is configured by the command CONFIGURE_TESTBUS_DIGITAL. Two parameters are passed within this command.

The first parameter (1 byte) defines the test signal group. Out of this test signal group, one signal can be selected for output on a pin of the PN5180 (4 bits).

The signal type of the chosen test signal group is selected by the low-nibble of parameter 2. A value of 8 on this position selects the 13.56 MHz clock to be put out on the selected pin.

The high nibble of parameter 2 (1 byte) selects the output pin for the selected test signal.

The following parameter groups are possible:

Table 52. Debug Signal Group Selection

| Command parameter (hex) | Debug Signal Group |
|-------------------------|------------------------------|
| 01 | Clock signal group |
| 1B | Transmitter encoder group |
| 1D | Timer group |
| 30 | Card mode protocol group |
| 58 | Transceive group |
| 70 | Receiver data transfer group |
| 73 | Receiver error group |

The second parameter defines the pin which is used for output of the test signal in the high nibble. The signal from one of the Debug Signal groups that are put out in the low nibble.

11.6.2.1 Debug signal groups

Table 53. Clock Signal Group

| Value low nibble (HEX) | Debug Function |
|------------------------|---|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | CLIF clock reset |
| 6 | Signal indicating the PLL is locked |
| 5 | Signal indicating an external Field is present |
| 4 | 20 MHz clock from the high frequency oscillator |
| 3 | 27.12 MHz clock from the PLL |
| 2 | 27.12 MHz clock from the RF clock recovery |
| 1 | Multiplexed 27.12 MHz clock |
| 0 | Multiplexed 13.56 MHz clock |

Table 54. Transmitter Encoder Group

| Value low nibble (HEX) | Debug Function |
|------------------------|----------------------------|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7..2 | RFU |
| 1 | Output TX envelope |
| 0 | Tx-IRQ |

Table 55. Timer Group

| Value low nibble (HEX) | Debug Function |
|------------------------|-----------------------------|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Running flag of timer T0 |
| 6 | Expiration flag of timer T0 |
| 5 | Running flag of timer T1 |
| 4 | Expiration flag of timer T1 |
| 3 | Running flag of timer T2 |
| 2 | Expiration flag of timer T2 |
| 1..0 | RFU |

Table 56. Card mode Protocol Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz Clock is put out |
| 7 | Synchronized clock-fail signal |
| 6 | Flag indicating that ISO/IEC14443-Type A (Miller) was detected |
| 5 | Flag indicating that FeliCa 212 kBd (Manchester) was detected |
| 4 | Flag indicating that FeliCa 424 kBd (Manchester) was detected |
| 3 | Flag indicating that ISO/IEC14443-Type B (NRZ) was detected |
| 2 | Flag indicating that the EOF was detected |
| 1 | CM data signal (Miller / Manchester / NRZ) |
| 0 | Signal indicating that the current data is valid |

Table 57. Transceiver Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Signal indicating that the tx prefetch was completed |
| 6 | Signal initiating a tx prefetch at the BufferManager |
| 5 | Start of transmission signal to TxEncoder |
| 4 | enable reception signal to RxDecoder |
| 3 | indicator that the waiting time was already expired |
| 2 | Transceiver state2 |
| 1 | Transceiver state1 |
| 0 | Transceiver state0 |

Table 58. Receiver Data Transfer Group

| Value low nibble (HEX) | Debug Function |
|------------------------|--|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Signal from SigPro indicating a collision |
| 6 | Signal from SigPro indicating end of data |
| 5 | Signal from SigPro indicating that data is valid |
| 4 | Signal from SigPro indicating received data |
| 3 | Status signal set by rx_start, ends when RX is completely over |
| 2 | Status signal indicating actual reception of data |
| 1 | Reset signal for receiver chain (at start of RX) |
| 0 | Internal RxDec bitclk |

Table 59. Receiver Error Group

| Value low nibble (HEX) | Debug Function |
|------------------------|---|
| 9..15 | RFU |
| 8 | 13.56 MHz clock is put out |
| 7 | Combination of data/protocol error and collision |
| 6 | Set if RxMultiple is set, and the LEN byte indicates more than 28 bytes |
| 5..3 | RFU |
| 2 | Set if a collision has been detected |
| 1 | Protocol error flag |

| Value low nibble (HEX) | Debug Function |
|------------------------|---|
| 0 | Data integrity error flag (Parity, CRC (Collision)) |

11.6.2.2 Digital Debug Output Pin Configuration

Table 60. Debug Signal Output Pin Configuration

| Value high nibble (HEX) | Debug Function (PIN) |
|-------------------------|--|
| 0 | IRQ pin (B2 on TFBGA64 - 39 on HVQFN40) |
| 1 | GPO1 pin (B3 on TFBGA64 - 38 on HVQFN40) |
| 2 | AUX2 pin (C1 on TFBGA64 - 02 on HVQFN40) |
| 3 | AUX1 pin (B1 on TFBGA64 - 40 on HVQFN40) |
| all others | RFU |

The Digital Debug output pins are defined by the bits 4:7 in TB_POS

11.6.3 Analog Debug Configuration

For the output of an analog debug signal, two pins are available, AUX1 and AUX2. Internal digital signals are provided in real time on the analog output pins without the need of using a high-speed digital interface. To provide this real-time debugging functionality, two internal DAC's (Digital Analog Converter) convert internal digital signals of the PN5180 to analog signals and provide these signals on the output pins. Up to two analog output signals can be provided at the output pins AUX1, AUX2.

The analog signals provided at the output pins are defined by two parameters of the command CONFIGURE_TESTBUS_ANALOG.

11.7 AUX2 / DWL_REQ

11.7.1 Firmware update

The PN5180 offers the possibility to upgrade the internal Firmware.

The pin AUX2/DWL_REQ is a double function pin. During start-up (time from power-up of the IC until IDLE IRQ is raised), the pin is used in input mode. If the polarity on this AUX2/DWL_REQ pin during start-up is high, the PN5180 enters the download mode.

If the boot process is finished (indicated by the IDLE IRQ), the pin is switched to output mode and the pin can be used for general debug purpose.

Recommended sequence is to set the RESET_N level to 0, set AUX2 pin level to 1 and release RESET_N to 1.

Exiting the download mode is performed by setting the AUX2 pin to 0 and perform a reset of the PN5180.

11.7.2 Firmware update command set

The PN5180 uses a dedicated host interface command set for download of new firmware. The physical SPI host interface is used for download of a new firmware image.

High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes

Security features are implemented to avoid intentional or unintentional modifications of the firmware image. The access to the IC is locked based on authentication mechanism to avoid unauthorized firmware downloads. The integrity of the firmware is ensured based on a secure hash algorithm,

The Firmware image can be identified based on a version number, which contains major and minor number.

For security reasons, the download of a smaller major version number than currently installed on the PN5180 is not possible.

11.8 RF Functionality

11.8.1 Supported RF Protocols

11.8.1.1 Communication mode for ISO/IEC 14443 type A and for MIFARE Classic

The physical level of the communication is shown in Figure 19.

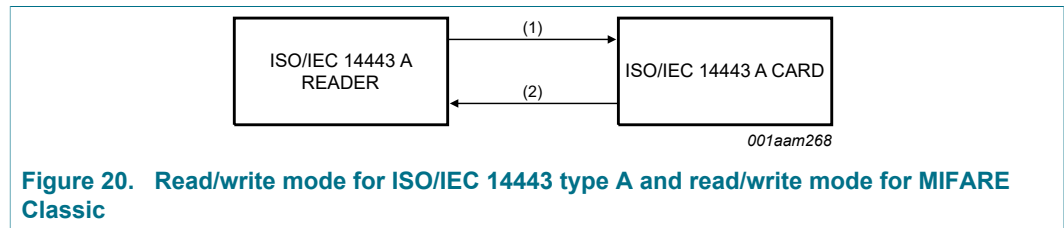


Figure 20. Read/write mode for ISO/IEC 14443 type A and read/write mode for MIFARE Classic

The physical parameters are described in Table 61.

Table 61. Communication overview for ISO/IEC 14443 type A and read/write mode for MIFARE Classic

| Communication direction | Signal type | Transfer speed | | | |
|--|------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| Reader to card (send data from the PN5180 to a card) $f_c = 13.56$ MHz | reader side modulation | 100 % ASK | 100 % ASK | 100 % ASK | 100 % ASK |
| | bit encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding | modified Miller encoding |
| | bit rate [kbit/s] | $f_c/128$ | $f_c/64$ | $f_c/32$ | $f_c/16$ |
| Card to reader (PN5180 receives data from a card) | card side modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation |
| | subcarrier frequency | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ |
| | bit encoding | Manchester encoding | BPSK | BPSK | BPSK |

The PN5180 connection to a host is required to manage the complete ISO/IEC 14443 type A and MIFARE Classic communication protocol. Figure 20 shows the data coding and framing according to communication mode for ISO/IEC 14443 type A and for MIFARE Classic.



The internal CRC coprocessor calculates the CRC value based on the selected protocol. In card mode for higher baud rates, the parity is automatically inverted as end of communication indicator. The selected protocol needs to be implemented on a host processor.

11.8.1.2 ISO/IEC14443 B functionality

The physical level of the communication is shown in Figure 21.



The physical parameters are described in Table 62.

Table 62. Communication overview for ISO/IEC 14443 B reader/writer

| Communication direction | Signal type | Transfer speed | | | |
|--|------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| Reader to card (send data from the PN5180 to a card) $f_c = 13.56$ MHz | reader side modulation | 10 % ASK | 10 % ASK | 10 % ASK | 10 % ASK |
| | bit encoding | NRZ | NRZ | NRZ | NRZ |
| | bit rate [kbit/s] | $128 / f_c$ | $64 / f_c$ | $32 / f_c$ | $16 / f_c$ |
| Card to reader (PN5180 receives data from a card) | card side modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation | subcarrier load modulation |
| | subcarrier frequency | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ |
| | bit encoding | BPSK | BPSK | BPSK | BPSK |

The PN5180 requires the host to manage the ISO/IEC 14443 B protocol.

11.8.1.3 FeliCa RF functionality

The FeliCa mode is the general reader/writer to card communication scheme according to the FeliCa specification. The communication on a physical level is shown in Figure 22.

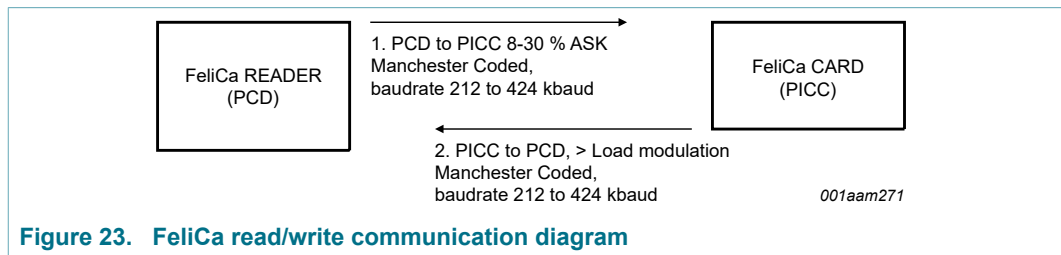


Figure 23. FeliCa read/write communication diagram

The physical parameters are described in Table 63.

Table 63. Communication for FeliCa reader/writer

| Communication direction | Signal type | Transfer speed FeliCa | FeliCa higher transfer speeds |
|--|------------------------|-----------------------|-------------------------------|
| | | 212 kbit/s | 424 kbit/s |
| Reader to card (send data from the PN5180 to a card) $f_c = 13.56$ MHz | reader side modulation | 8 % to 30 % ASK | 8 % to 30 % ASK |
| | bit encoding | Manchester encoding | Manchester encoding |
| | bit rate | $f_c/64$ | $f_c/32$ |
| Card to reader (PN5180 receives data from a card) | card side modulation | Load modulation, | Load modulation, |
| | bit encoding | Manchester encoding | Manchester encoding |

The PN5180 needs to be connected to a host which implements the FeliCa protocol.

Multiple reception cycles (RxMultiple)

For FeliCa timeslot handling in PCD mode, PN5180 implements multiple reception cycles. The feature is enabled by setting the control bit `RX_MULTIPLE_ENABLE` in the register `TRANSCEIVE_CONTROL` in combination with the transceive state machine.

Unlike for normal operation, the receiver is enabled again after a reception is finished. As there is only one receive buffer available, but several responses are expected, the buffer is split into sub buffers of 32 byte length. Hence, the maximum number of responses which can be handled is limited to 8. As the maximum length defined for a FeliCa response is 20 bytes, the buffer size defined does fulfill the requirements for that use-case. The first data frame received is copied onto buffer address 0. The subsequent frames are copied to the buffer address $32 * \text{NumberOfReceivedFrames}$. The maximum number of data bytes allowed per frame is limited to 28.

All bytes in the buffer between the payload and the status byte are uninitialized and therefore invalid. The firmware on the host shall not use these bytes. The last word of the sub buffer (position 28 to 31) contains a status word. The status word contains the number of received bytes (may vary from the FeliCa length in case of an error), the `CLError` flag indicating any error in the reception (which is a combination of 3 individual error flags `DATA_INTEGRITY_ERROR || PROTOCOL_ERROR ||`

COLLISION_DETECTED) the individual error flags and the LenError flag indicating an incorrect length byte (either length byte is greater than 28 or the number of received bytes is shorter than indicated by the length byte). All unused bits (RFU) are masked to 0.



Figure 24. RxMultiple data format

There are 4 different cases possible for a reception:

1. Correct reception - Data integrity is correct (no CRC error), and additionally the number of bytes received is equal to the length byte. Data is written to the buffer. No error set in status byte.
2. Erroneous reception - Data is incorrect (data integrity error - CRC wrong) but frame length is correct. Data is written to buffer and the bits ClError and DataError in the status byte are set.
3. Erroneous reception - the length byte received indicates a frame length greater than 28. No data is copied to buffer but status byte with LenError bit set is written.
4. Erroneous reception - the length byte is larger than the number of data bytes, which have been received. Data received is written to buffer and the ProtocolError bit in the status byte is set.

For each reception, the RX_IRQ in the IRQ_STATUS is set. The host firmware can disable the IRQ and use a timer for timeout after the last timeslot to avoid excessive interaction with the hardware. At the end of the reception, additionally the bit field RX_NUM_FRAMES_RECEIVED in the register RX_STATUS is updated to indicate the number of received frames.

After the reception of the eight frames (which is the maximum supported), a state change to next expected state is executed (WaitTransmit for transceive command). It is possible to issue the IDLE command in order to leave the RxMultiple cycle. Consequently the reception is stopped. Upon start of a new reception cycle, the flag RX_NUM_FRAMES_RECEIVED is cleared.

The duration between deactivate and reactivate is at minimum 2 RF cycles and can last typically up to 2 μs.

11.8.1.4 ISO/IEC15693 functionality

The physical parameters are described below.

Table 64. Communication for ISO/IEC 15693 reader/writer "reader to card"

| Communication direction | Signal type | Transfer speed |
|--|------------------------|------------------------------------|
| | | $f_c/512$ kbit/s |
| Reader to card (send data from the PN5180 to a card) | reader side modulation | 10 % to 30 % ASK 90 % to 100 % ASK |
| | bit encoding | 1/4 |
| | bit length | 302.08 μ s |

Table 65. Communication for ISO/IEC 15693 reader/writer "card to reader"

| Communication direction | Signal type | Transfer speed | | | |
|--|----------------------------|----------------|---------------|---------------------------------------|---------------------------------------|
| | | 6.62 kbit/s | 13.24 kbit/s | 26.48 kbit/s | 52.96 kbit/s ^[1] |
| Card to reader (PN5180 receives data from a card) $f_c = 13.56$ MHz | card side modulation | not supported | not supported | single subcarrier load modulation ASK | single subcarrier load modulation ASK |
| | bit length (μ s) | - | - | 37.76 (3.746) | 18.88 |
| | bit encoding | - | - | Manchester coding | Manchester coding |
| | subcarrier frequency [MHz] | - | - | $f_c/32$ | $f_c/32$ |

[1] Fast inventory (page) read command only (ICODE proprietary command).

11.8.1.5 ISO/IEC18000-3 Mode 3 functionality

The ISO/IEC 18000-3 mode 3 is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18000-3 standard.

The diagram below illustrates the card presence check:



Figure 25. EPC_GEN2 Card presence check

| | | | | | | | | | | | | | | | |
|---|---|----------------------------|--|------------|----------------|---------------------|----------------------------|----------------------------|-----------|---------------------------|--------|--|--------|---|---------|
| Tag response available NO TagHandle | <table border="1"> <tr> <td>status 0x00</td> <td>Tag Reply length</td> <td>Valid bits in last byte</td> <td>Tag Reply</td> </tr> <tr> <td>1 byte</td> <td>1 byte</td> <td>1 byte</td> <td>n bytes (defined in Tag Reply Length)</td> </tr> </table> | | | | status 0x00 | Tag Reply length | Valid bits in last byte | Tag Reply | 1 byte | 1 byte | 1 byte | n bytes (defined in Tag Reply Length) | | | |
| | status 0x00 | Tag Reply length | Valid bits in last byte | Tag Reply | | | | | | | | | | | |
| 1 byte | 1 byte | 1 byte | n bytes (defined in Tag Reply Length) | | | | | | | | | | | | |
| Tag response available TagHandle available | <table border="1"> <tr> <td>status 0x01</td> <td>Tag Reply length</td> <td>Valid bits in last byte</td> <td>Tag Reply</td> <td>Tag handle</td> </tr> <tr> <td>1 byte</td> <td>1 byte</td> <td>1 byte</td> <td>n bytes (defined in TagReply Length)</td> <td>2 bytes</td> </tr> </table> | | | | | status 0x01 | Tag Reply length | Valid bits in last byte | Tag Reply | Tag handle | 1 byte | 1 byte | 1 byte | n bytes (defined in TagReply Length) | 2 bytes |
| status 0x01 | Tag Reply length | Valid bits in last byte | Tag Reply | Tag handle | | | | | | | | | | | |
| 1 byte | 1 byte | 1 byte | n bytes (defined in TagReply Length) | 2 bytes | | | | | | | | | | | |
| No Tag replied | <table border="1"> <tr> <td>status 0x02</td> <td colspan="3"></td> </tr> <tr> <td>1 byte</td> <td colspan="3"></td> </tr> </table> | | | | status 0x02 | | | | 1 byte | | | | | | |
| status 0x02 | | | | | | | | | | | | | | | |
| 1 byte | | | | | | | | | | | | | | | |
| Two or more tags replied | <table border="1"> <tr> <td>status 0x03</td> <td colspan="3"></td> </tr> <tr> <td>1 byte</td> <td colspan="3">possible timeslot answers</td> </tr> </table> | | | | status 0x03 | | | | 1 byte | possible timeslot answers | | | | | |
| status 0x03 | | | | | | | | | | | | | | | |
| 1 byte | possible timeslot answers | | | | | | | | | | | | | | |

Figure 26. EPC GEN2 possible timeslot answers

11.8.1.6 NFCIP-1 modes

Overview

The NFCIP-1 communication differentiates between an Active and a Passive Communication Mode.

- Active Communication mode means both the initiator and the target are using their own RF field to transmit data.
- Passive Communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field.
- Initiator: Generates RF field at 13.56 MHz and starts the NFCIP-1 communication.
- Target: responds to initiator command either in a load modulation scheme in Passive Communication mode or using a self-generated and self-modulated RF field for Active Communication mode.

In order, to support the NFCIP-1 standard the PN5180 supports the Active and Passive Communication mode at the transfer speeds 106 kbit/s, 212 kbit/s and 424 kbit/s as defined in the NFCIP-1 standard.

Active communication mode

Active communication mode means both the initiator and the target are using their own RF field to transmit data.

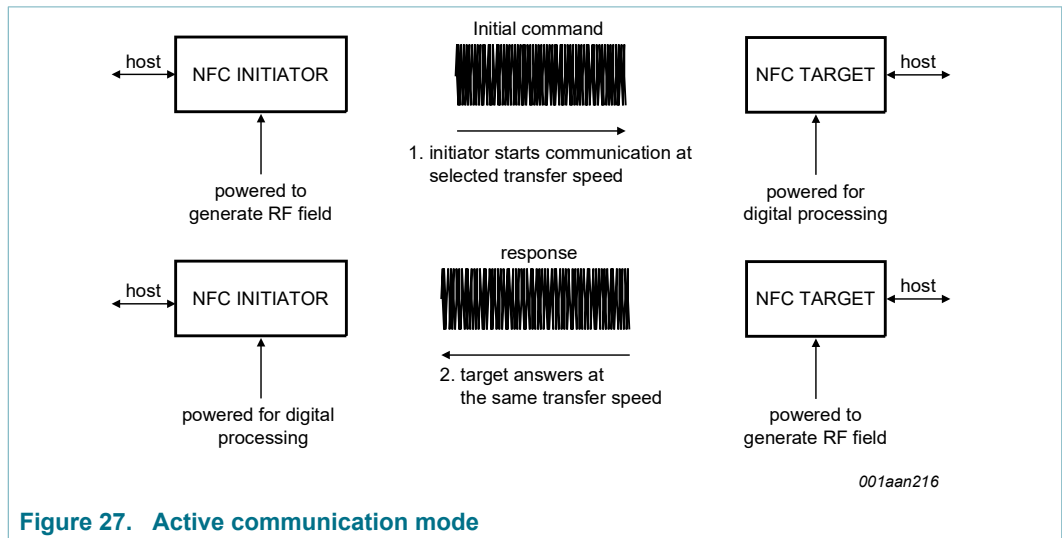


Figure 27. Active communication mode

Table 66. Communication overview for active communication mode

| Communication direction | 106 kbit/s | 212 kbit/s | 424 kbit/s |
|-------------------------|---|---|------------|
| Initiator → Target | According to ISO/IEC 14443 A 100 % ASK, modified Miller Coded | According to FeliCa, 8 % to 30 % ASK Manchester Coded | |
| Target → Initiator | | | |

A dedicated host controller firmware is required to handle the NFCIP-1 protocol. For this purpose, NXP offers an NFC Reader library (check the NXP website) which supports Reader/Writer, P2P and CardEmulation modes.

Passive communication mode

Passive communication mode means that the target answers to an initiator command in a load modulation scheme. The initiator is active (powered) to generate the RF field.

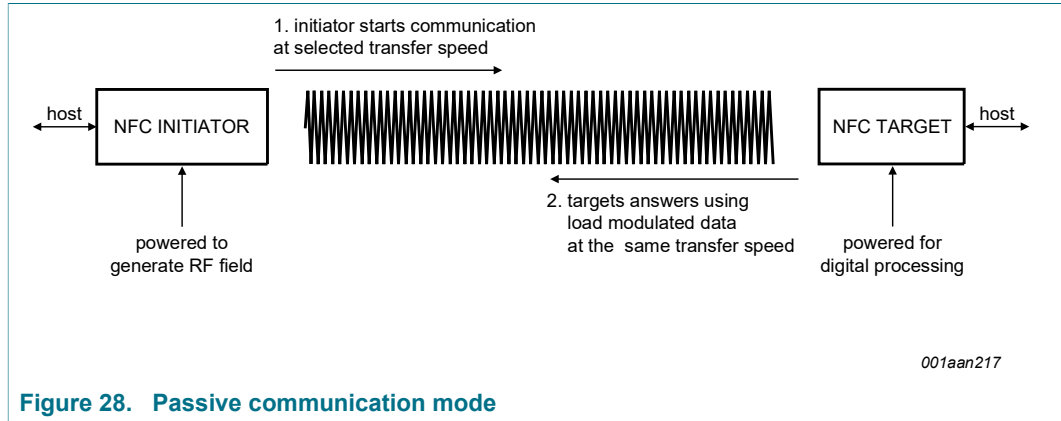


Figure 28. Passive communication mode

Table 67. Communication overview for passive communication mode

| Communication direction | 106 kbit/s | 212 kbit/s | 424 kbit/s |
|-------------------------|---|---|------------|
| Initiator → Target | According to ISO/IEC 14443 A 100 % ASK, Modified Miller Coded | According to FeliCa, 8 % to 30 % ASK Manchester Coded | |
| Target → Initiator | According to ISO/IEC 14443 A @106 kbit modified Miller Coded | According to FeliCa, > 14 % ASK Manchester Coded | |

A dedicated host controller firmware is required to handle the NFCIP-1 protocol.

Note: Transfer Speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

NFCIP-1 protocol support

The NFCIP-1 protocol is not described in this document. The PN5180 does not implement any of the high-level protocol functions. These higher-level protocol functions need to be provided by the host. For detailed explanation of the protocol, refer to the NFCIP-1 standard. However the datalink layer is according to the following policy:

- Speed shall not be changed while continuous data exchange in a transaction.
- Transaction includes initialization, anticollision methods and data exchange (in continuous way, meaning no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz, the following general rules to start an NFCIP-1 communication are defined:

1. Per default, an NFCIP-1 device is in Target mode - meaning its RF field is switched off.
2. The RF level detector is active.
3. Only if it is required by the application the NFCIP-1 device shall switch to Initiator mode.

4. An initiator shall only switch on its RF field if no external RF field is detected by the RF Level detector during a time of T_{IDT} . (Details are specified in the ISO/IEC 18092)
5. The initiator performs initialization according to the selected mode.

11.8.1.7 ISO/IEC14443 A Card operation mode

PN5180 can be configured to act as an ISO/IEC 14443 A compliant card.

In this configuration, the PN5180 can generate an answer in a load modulation scheme according to the ISO/IEC 14443 A interface description.

Note: PN5180 does not support a complete card protocol. This card protocol has to be handled by a connected host controller. Nevertheless, the layer3 type A activation is handled by the NFC frontend. The Card Activated IRQ shall be enabled and notifies if a card activation had been successfully performed.

The supports ISO/IEC14443 A card mode for data rates 106 kbit/s, 212 kbit/s, 424 kbit/s and 848 kbit/s.



11.8.1.8 NFC Configuration

The NFC protocol for the 106 kbit/s mode defines an additional Sync-Byte (0xF0 + parity) after the normal start bit had been transmitted. As this Sync-Byte includes a parity bit, it can be handled by a host firmware as a normal data byte.

11.8.1.9 Mode Detector

The Mode Detector is a functional block of the PN5180in PICC mode which senses for an RF field generated by another device. The mode detector allows distinguishing between type A and FeliCa target mode. Dependent on the recognized protocol generated by an initiator peer device the host is able to react. The PN5180 is able to emulate type A cards and peer to peer active target modes according to ISO/IEC18092.

11.8.2 RF-field handling

The NFC frontend supports generation of a RF-field dependent on external conditions like presence of another NFC device generating an RF field. A flexible mechanism to control the RF field is available.

After power-up, the RF-field is off.

The instruction RF_ON enables the generation of a RF-field. The NFC frontend can perform an initial RF collision avoidance according to ISO/IEC18092. Before enabling the RF-field, a field detection is automatically enabled for T_{IDT}. In case an external field is detected, the field is not switched on and an RF_ACTIVE_ERROR_IRQ is raised. The cause for the error can be examined in the RF_STATUS.

In order to switch off the RF-field generation, the RF_OFF instruction needs to be sent. Active Mode is supported by configuring the RF_ON instruction.

11.8.3 Transmitter TX

The transmitter is able to drive an antenna circuit connected to outputs TX1 and TX2 with a 13.56 MHz carrier signal. The signal delivered on pins TX1 and pin TX2 is the 13.56 MHz carrier modulated by an envelope signal for energy and data transmission. It can be used to drive an antenna directly, using a few passive components for matching and filtering. For a differential antenna configuration, either TX1 or TX2 can be configured to put out an inverted clock. 100 % modulation and several levels of amplitude modulation on the carrier can be performed to support 13.56 MHz carrier-based RF-reader/writer protocols as defined by standards ISO/IEC14443 A and B, FeliCa and ISO/IEC 18092.

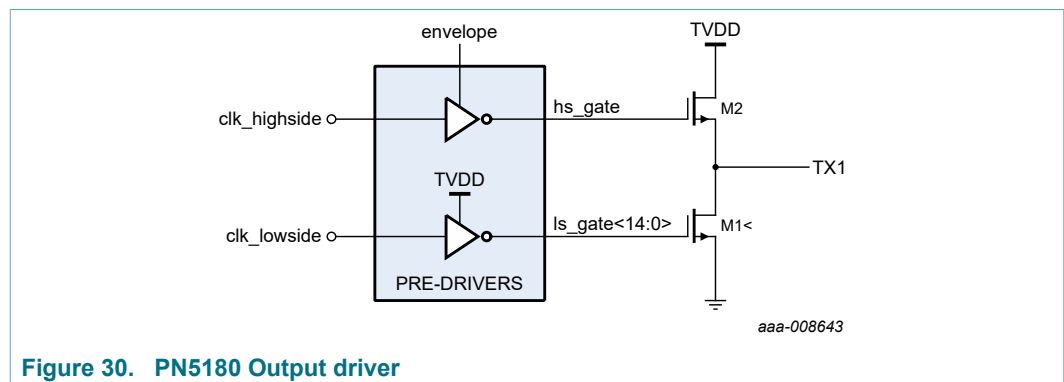


Figure 30. PN5180 Output driver

11.8.3.1 100 % Modulation

There are 5 choices for the output stage behavior during 100 % modulation, and one setting for 10 % modulation. This modulation is controlled by TX_CLK_MODE_RM in RF_CONTROL_TX_CLK:

Table 68. Settings for TX1 and TX2

| TX_CLK_MODE_RM (binary) | Tx1 and TX2 output | Remarks |
|-------------------------|--------------------|---|
| 000 | High impedance | The high impedance of the transmitters (field-off) is enabling the AGC and overwriting any AGC configuration done by the host. Before switching on the field again, the host has to take care to configure the AGC according to application requirements. |
| 001 | 0 | output pulled to 0 in any case |
| 010 | 1 | output pulled to 1 in any case |
| 110 | RF high side push | Open-drain, only high side (push) MOS supplied with clock, clock polarity defined by TX2_INV_RM; low side MOS is off |

| TX_CLK_MODE_RM (binary) | Tx1 and TX2 output | Remarks |
|-------------------------|--|--|
| 101 | RF low side pull | Open-drain, only low side (pull) MOS supplied with clock, clock polarity defined by TX1_INV_RM; high side MOS is off |
| 111 | 13.56 MHz clock derived from 27.12 MHz quartz divided by 2 | push/pull Operation, clock polarity defined by invtx; setting for 10 % modulation |

With the options "RF high side push" and "RF low side push", potentially faster fall times can be achieved for the antenna voltage amplitude at the beginning of a modulation. This basic behavior during modulation cannot be configured independently for TX1 and TX2. The clock polarity of each Transmitter driver can be configured separately with TX1_INV_RM and TX2_INV_RM if the PN5180 operating in reader mode, or TX1_INV_CM and TX2_INV_CM if the PN5180 is operating in card emulation mode.

11.8.3.2 10 % Amplitude Modulation

For a targeted ASK 10 % amplitude modulation, the bits RF_CONTROL_TX_CLK in register TX_CLK_MODE_RM need to be set to value 0b111. Then the signal envelope does not influence the clock behavior thus resulting in an ASK modulation to a modulation index as defined by RF_CONTROL_TX in the bits TX_RESIDUAL_CARRIER. The residual carrier setting is used to adjust the modulation degree at the TX output. A control loop is implemented to keep the modulation degree as constant as possible.

The settings and resulting typical residual carrier and modulation degree is given in table below:

Table 69. Modulation degree configuration

| TX_RESIDUAL_CARRIER register setting | residual carrier nominal (%) | modulation degree nominal (%) |
|--------------------------------------|------------------------------|-------------------------------|
| 00h | 100 | 0 |
| 01h | 98 | 1.01 |
| 02h | 96 | 2.04 |
| 03h | 94 | 3.09 |
| 04h | 91 | 4.71 |
| 05h | 89 | 5.82 |
| 06h | 87 | 6.95 |
| 07h | 86 | 7.53 |
| 08h | 85 | 8.11 |
| 09h | 84 | 8.7 |
| 0Ah | 83 | 9.29 |
| 0Bh | 82 | 9.89 |
| 0Ch | 81 | 10.5 |
| 0Dh | 80 | 11.11 |
| 0Eh | 79 | 11.73 |

| TX_RESIDUAL_CARRIER register setting | residual carrier nominal (%) | modulation degree nominal (%) |
|--------------------------------------|------------------------------|-------------------------------|
| 0Fh | 78 | 12.36 |
| 16 | 77 | 12.99 |
| 17 | 76 | 13.64 |
| 18 | 75 | 14.29 |
| 19 | 74 | 14.94 |
| 20 | 72 | 16.28 |
| 21 | 70 | 17.65 |
| 22 | 68 | 19.05 |
| 23 | 65 | 21.21 |
| 24 | 60 | 25 |
| 25 | 55 | 29.03 |
| 26 | 45 | 37.93 |
| 27 | 40 | 42.86 |
| 28 | 35 | 48.15 |
| 29 | 30 | 53.85 |
| 30 | 25 | 60 |
| 31 | 0 | 100 |

11.8.3.3 TX Wait

Tx_wait can be used for 2 different purposes:

On the one hand, it can be used to prevent start of transmission before a certain period has expired - even if the PN5180 has already finished data processing and set the START_SEND bit. This behavior is intended for the reader mode to guarantee the PICC to PCD frame delay time (FDT).

On the other hand, the tx_wait time can be used to start the transmission at an exactly defined time. For this purpose, data to be sent must be available and the START_SEND flag has to be set by FW before the period expires. In case the START_SEND bit is not set when tx_wait expires and MILLER_SYNC_ENABLE is set the transmission is started on the bit-grid.

The guard time tx_wait is started after the end of a reception, no matter if the frame is correct or erroneous. The tx_wait guard time counter is not started in case the reception is restarted because of an EMD-event or in case the RX_MULTIPLE_ENABLE bit is set to 1.

In case the register flag TX_WAIT_RFON_ENABLE is set to 1 the guard time counter is started when the devices own RF-Field is switched on.

To start a transmission, it is always necessary for the firmware to set the START_SEND bit in the SYSTEM_CONFIG register or sending the instruction SEND_DATA. Having said that it is possible to disable the guard time tx_wait by setting the register TX_WAIT_CONFIG to 00h.

11.8.3.4 Over- and Undershoot prevention

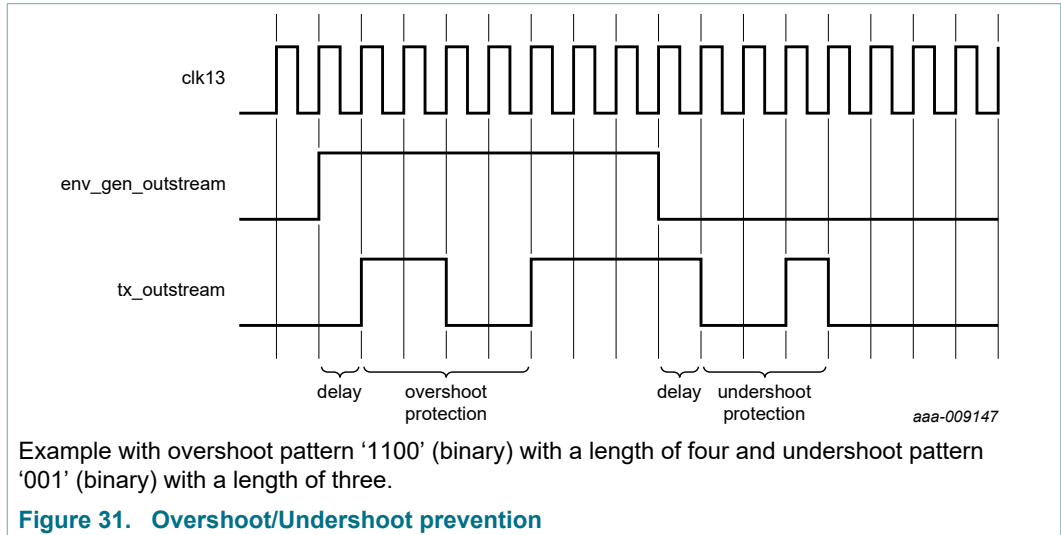


Figure 31. Overshoot/Undershoot prevention

The over- and undershoot protection allows configuring additional signals on the Transmitter output which allows to control the signal shaping of the antenna output.

The registers TX_OVERSHOOT_CONFIG and TX_UNDERSHOOT_CONFIG are used to configure the over-and undershoot protection. Additionally, in register RF_CONTROL_TX_CLK (bit TX_CLK_MODE_OVUN_PREV) it is defined which TX clock mode for the period the overshoot/undershoot prevention is active, and RF_CONTROL_TX (bit TX_RESIDUAL_CARRIER_OV_PREV) defines the value for the residual carrier for the period the overshoot prevention pattern is active.

11.8.4 Dynamic Power Control (DPC)

The Dynamic Power Control allows adjusting the Transmitter output current dependent on the loading condition of the antenna.

A lookup table is used to configure the output voltage and by this control the transmitter current. In addition to the control of the transmitter current, wave shaping settings can be controlled dependent on the selected protocol and the measured antenna load.

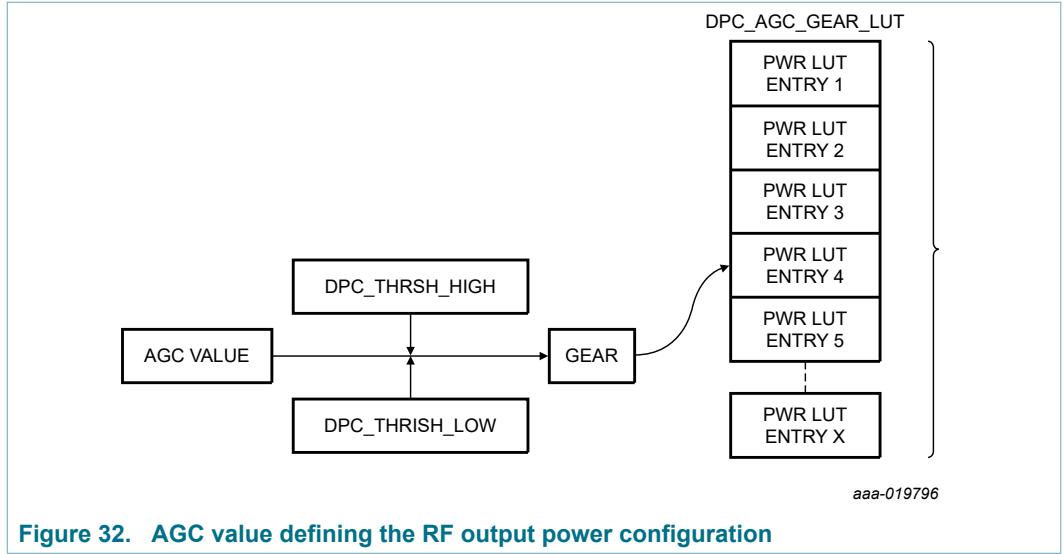


Figure 32. AGC value defining the RF output power configuration

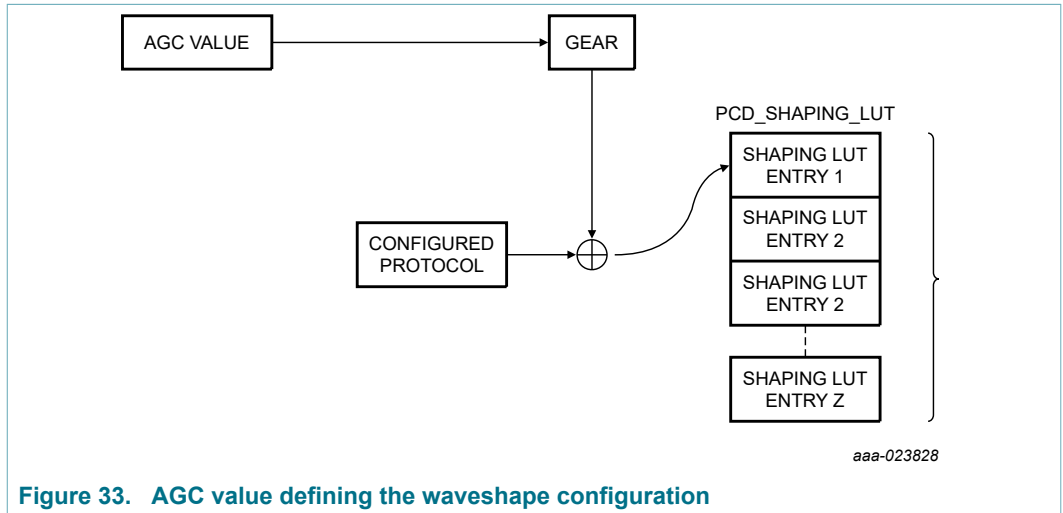


Figure 33. AGC value defining the waveshape configuration

The PN5180 allows measuring periodically the RX voltage. The RX voltage is used as indicator for the actual antenna current. The voltage measurement is done with the help of the AGC. The time interval between two measurements can be configured with the OC_TIME byte in the EEPROM.

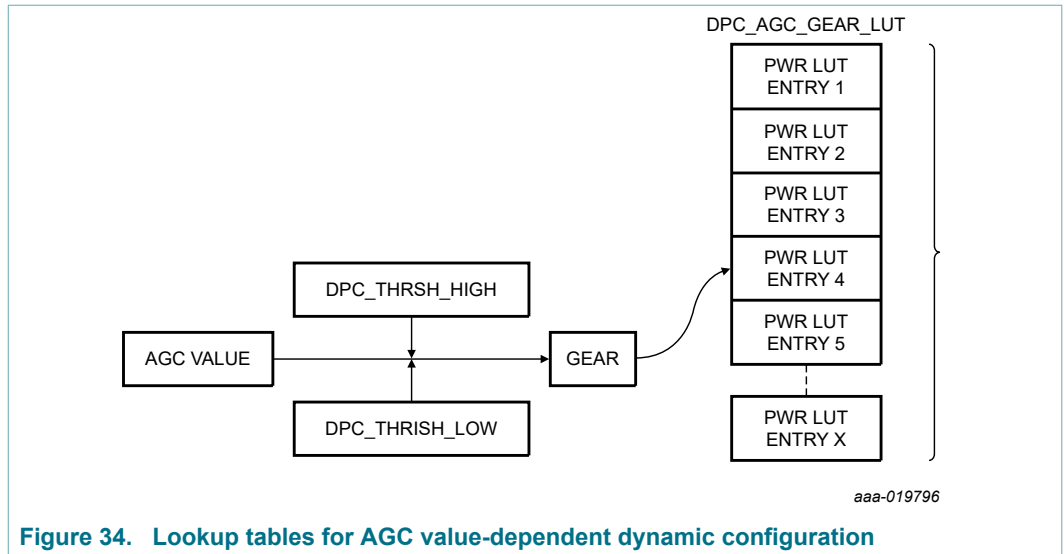


Figure 34. Lookup tables for AGC value-dependent dynamic configuration

The AGC value is compared to a maximum and minimum threshold value which is stored in EEPROM.

If the AGC value is exceeding one of the thresholds, a new gear configuring another transmitter supply driver voltage will be activated. The number of gears - and by these transmitter supply voltage configurations - can be defined by the application, up to 15 gears are available.

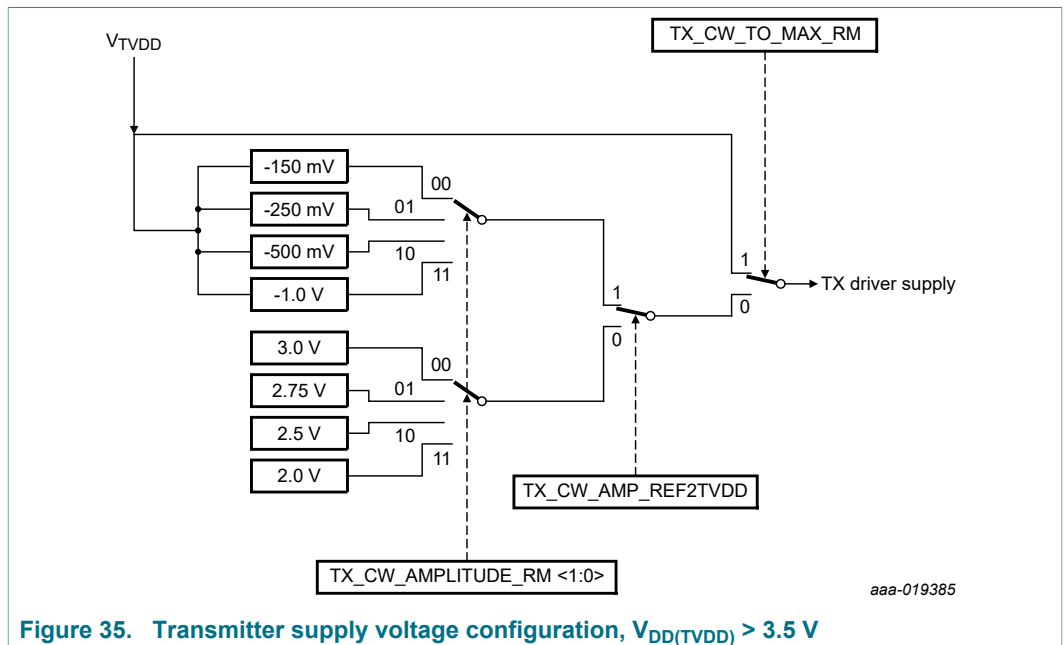


Figure 35. Transmitter supply voltage configuration, $V_{DD(TVDD)} > 3.5 V$

11.8.5 Adaptive Waveform Control (AWC)

Depending on the level of detected detuning of the antenna, RF wave shaping related register settings can be automatically updated. The shaping related register settings are stored in a lookup table located in EEPROM, and selected dependent on the actual gear. The gear numbers must be provided as part of the lookup table entries and need to be provided in ascending order in the EEPROM. Each lookup table entry allows

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configuring not only a dedicated wave shaping configuration for the corresponding gear. But in additionally it is possible to configure for this gear the wave shaping configuration dependent on the different protocols.

Each lookup table item contains a bitmask of technology and baud rate (in order to use an entry for multiple technologies and baudrates), the DPC Gear and a relative value (change compared to actual setting of register RF_CONTROL_TX) for TAU_MODE_FALLING, TAU_MODE_RISING and TX_RESIDUAL_CARRIER.

Table 70. Wave shaping lookup table

| Bit position | Function of each DWORD |
|--------------|---|
| 30:31 | RFU |
| 16:29 | From FW 3.A onwards |
| | Bitmask identifying technology and baud rate |
| | 0001h A 106 |
| | 0002h A 212 |
| | 0004h A 424 |
| | 0008h A 848 |
| | 0010h B 106 |
| | 0020h B 212 |
| | 0040h B 424 |
| | 0080h B 848 |
| | 0100h F 212 |
| | 0200h F424 |
| | 0400h ISO/IEC 15693 ASK10 |
| | 0800h ISO/IEC 15693 ASK100 |
| | 1000h ISO/IEC 18000m3_TARI_18_88 μs |
| | 2000h ISO/IEC 18000m3_TARI_9_44 μs |
| 15:12 | RESIDUAL_CARRIER (Sign bit (MSB) + 3-bit value) 0: Add value to current residual carrier configuration, 1; subtract value from current residual carrier configuration |
| 11:8 | TAU_MOD_RISING (Sign bit (MSB) + 3-bit value) 0: Add value to current TAU_MOD_RISING configuration, 1; subtract value from current TAU_MOD_RISING configuration |
| 7:4 | TAU_MOD_FALLING (Sign bit (MSB) + 3-bit value) 0: Add value to current TAU_MOD_FALLING configuration, 1; subtract value from current TAU_MOD_FALLING configuration |
| 3:0 | DPC Gear |

If there is a gear switch, a EEPROM lookup is performed if the current gear (at current protocol and baud rate) has an assigned wave shaping configuration. In case of an execution of a LoadProtocol command, this lookup will be performed (example: switching from baud rate A106 to A424) as well. The change from the wave shaping configuration as configured by LOAD_RF_CONFIG is relative, which means that bits are added or subtracted from the existing configuration. For an increasing gear value, the defined change is cumulative.



Figure 36. DPC, AGC and AWC configuration

11.8.6 Adaptive Receiver Control (ARC)

(Available from Firmware 2.6 onwards) Depending on the level of detected detuning of the antenna, receiver-related register settings can be automatically updated. The registers which allow to be dynamically controlled are RX_GAIN and RX_HPCF.

The size of the Lookup table for the ARC is done in the upper nibble of the entry PCD_SHAPING_LUT_SIZE (0x97). In case this entry is zero, the ARC is deactivated. In total 20 entries (20*1 DWORD = 80 bytes) + 1 byte for length (upper nibble for RX Gain, and lower nibble for PCD shaping) can be used for both PCD shaping (AWC) and RX Gain configuration (ARC) in the EEPROM.

The ARC lookup table (configuration data) is added at the end of the AWC (waveshaping) lookup table. This provides maximum flexibility and allows to define different lookup table sizes for both AWC and ARC. Care must be taken if the size of the AWC table is changed, this results in invalid ARC data which might have been previously configured since the ARC table offset changes as a result of the changed AWC size.

The ARC settings override the default RX_GAIN, RX_HPCF, MIN_LEVEL and MIN_LEVELP register configuration done by Load Protocol.

In case of a gear switch, an EEPROM lookup is performed. If the current gear (at current protocol and baud rate) has an assigned RX_GAIN, RX_HPCF, MIN_LEVEL and MIN_LEVELP configuration, this value is used to update the current receiver register configuration.

Table 71. Adaptive Receiver Control lookup table

| Bit position | Function of each DWORD | |
|--------------|---|--------------------------------|
| 16:31 | 0001h | A 106 |
| | 0002h | A 212 |
| | 0004h | A 424 |
| | 0008h | A 848 |
| | 0010h | B 106 |
| | 0020h | B 212 |
| | 0040h | B 424 |
| | 0080h | B 848 |
| | 0100h | F 212 |
| | 0200h | F 424 |
| | 0400h | ISO/IEC 15693 ASK10_53 |
| | 0800h | ISO/IEC 15693 ASK100_26 |
| | 1000h | ISO/IEC 18000m3_Manch424_4 |
| | 2000h | ISO/IEC 18000m3_Manch424_2_212 |
| | 4000h | ISO/IEC 18000m3_Manch848_4_212 |
| 8000h | ISO/IEC 18000m3_Manch848_2 | |
| 15:13 | MIN_LEVELP, 3 bits, relative value, defining a change of the SIGPRO_RM_CONFIG register; MIN_LEVELP value with a maximum range of +/-3. (Sign bit (MSB) + 3-bit value) | |
| 12:10 | MIN_LEVEL, 3 bits, relative value, defining a change of the SIGPRO_RM_CONFIG register; MIN_LEVEL value with a maximum range of +/-3. (Sign bit (MSB) + 3-bit value) | |
| 9:7 | RX_GAIN, 3 bits, relative value, defining a change of the RF_CONTROL_RX register; RX_GAIN value with a maximum range of +/-3. (Sign bit (MSB) + 3-bit value) | |
| 6:4 | RX_HPCF, 3 bits, relative value, defining a change of the RF_CONTROL_RX register; RX_HPCF value with a maximum range of +/-3. (Sign bit (MSB) + 3-bit value) | |
| 3:0 | DPC GEAR: the gear number, at which the related change shall apply. | |

11.8.7 Transceive state machine

The transceive command allow transmitting and the following expected receive data with a single command.

The transceive state machine is used to trigger the reception and transmission of the RF data dependent on the conditions of the interface.

The state machine for the command transceive is started when the SYSTEM_CONFIG command is set to transceive. The transceive command does not terminate automatically. In case of an error, the host can stop the transceive state machine by setting the SYSTEM_CONFIG.command to IDLE.

START_SEND can either be triggered by writing to the SYSTEM_CONFIG register start_send or by using the command SET_INSTR_SEND_DATA.



Figure 37. Transceive state machine

11.8.8 Autocoll (Card Emulation)

The Autocoll state machine performs the time critical activation for Type-A PICC and for NFC-Forum Active and Passive Target activation (Card Emulation Mode).

The PICC state machine supports three configurations:

- Autocoll mode0: Autocoll mode is left when no RF field is present
- Autocoll mode1: Autocoll mode is left when one technology is activated by an external reader. During RFOff, the chip enters standby mode automatically

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- Autocoll mode2: Autocoll mode is left when one technology is activated by an external reader. During RFOff, the chip does not enter standby mode.

At start-up, the Autocoll state machine automatically performs a LOAD_RF_CONFIG with the General Target Mode Settings. When a technology is detected during activation, the Autocoll state machine performs an additional LOAD_RF_CONFIG with the corresponding technology.

The card configuration for the activation is stored in EEPROM. If RandomUID is enabled (EEPROM configuration, Address 0x51), a random UID is generated after each RF-off.

For all active target modes, the own RF field is automatically switched on after the initiator has switched off its own field.

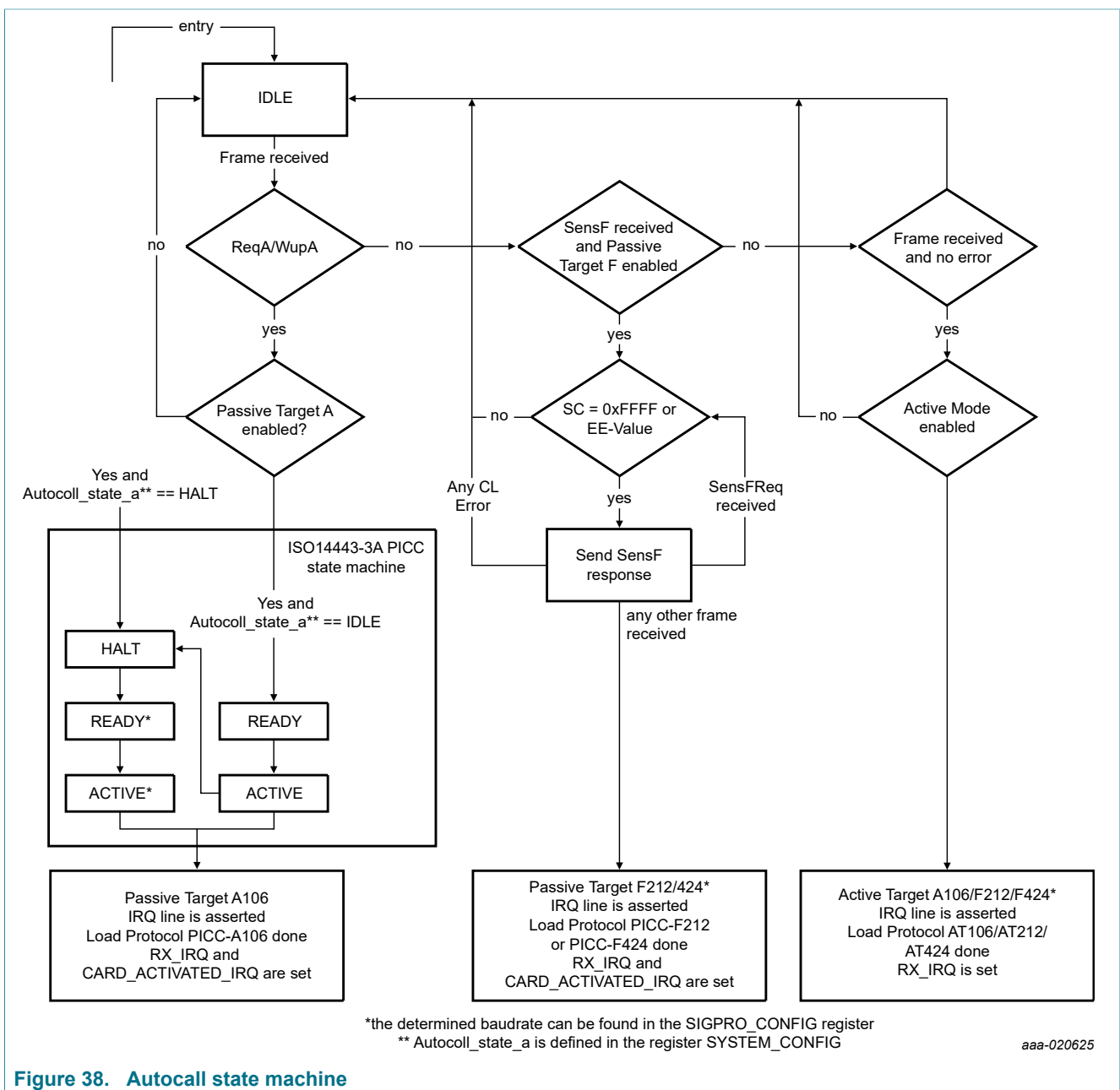


Figure 38. Autocoll state machine

11.8.9 Receiver RX

11.8.9.1 Reader Mode Receiver

In Reader Mode, the response of the PICC device is coupled from the PCB antenna to the differential input RXP/RXN. The Reader Mode Receiver extracts this signal by first removing the carrier in passive mixers (direct conversion for I and Q), then filtering and amplifying the baseband signal, and finally converting to digital values with 2 separate ADCs for I and Q channel. Both the I and Q channels have a differential structure which improves the signal quality.

The I/Q-Mixer mixes the differential input RF-signal down to the baseband. The mixer has a band with of 2 MHz.

The down mixed differential RX input signals are passed to the BBA and band-pass filtered. In order to consider all the various protocols (Type A/B, FeliCa), the high-pass cut-off frequency of BBA can be configured between 45 kHz and 250 kHz in 4 different steps. The low-pass cut-off frequency is above 2 MHz.

This band-passed signal is then further amplified with a gain factor which is configurable between 30 dB and 60 dB. The baseband amplifier (BBA)/ADC I- and Q- channel can be enabled separately. This is required for ADC-based CardMode functionality as only the I-channel is used in this case.

The gain and high pass corner frequency of the BBA are not independent from each other:

Table 72. Table 71.

| Gain setting | HPCF setting | HPCF (kHz) | LPCF (MHz) | Gain (sB20) | Band width (MHz) |
|--------------|--------------|------------|------------|-------------|------------------|
| Gain3 | 0 | 39 | 3.1 | 60 | 3.1 |
| | 1 | 78 | 3.2 | 59 | 3.1 |
| | 2 | 144 | 3.5 | 58 | 3.3 |
| | 3 | 260 | 4.1 | 56 | 3.8 |
| Gain2 | 0 | 42 | 3.1 | 51 | 3.1 |
| | 1 | 82 | 3.3 | 51 | 3.2 |
| | 2 | 150 | 3.7 | 49 | 3.5 |
| | 3 | 271 | 4.3 | 47 | 4.0 |
| Gain1 | 0 | 41 | 3.7 | 43 | 3.7 |
| | 1 | 82 | 4.0 | 42 | 3.9 |
| | 2 | 151 | 4.5 | 41 | 4.3 |
| | 3 | 276 | 5.5 | 39 | 5.2 |
| Gain0 | 0 | 42 | 3.8 | 35 | 3.8 |
| | 1 | 84 | 4.1 | 34 | 4.0 |
| | 2 | 154 | 4.7 | 33 | 4.5 |
| | 3 | 281 | 5.7 | 31 | 5.4 |

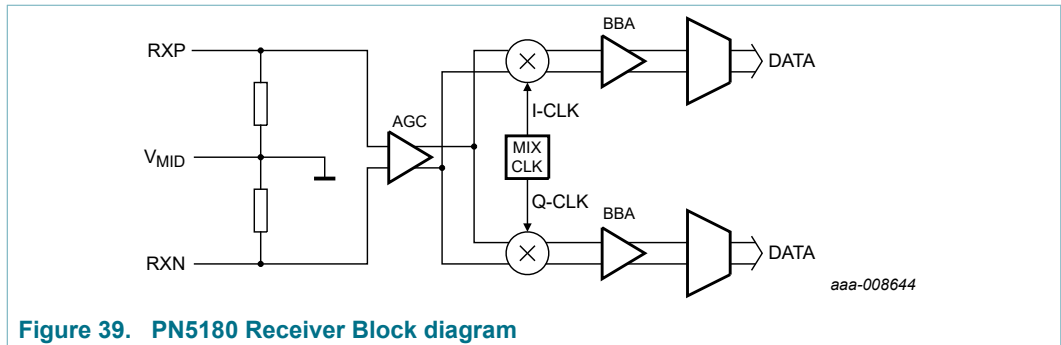


Figure 39. PN5180 Receiver Block diagram

11.8.9.2 Automatic Gain Control

The Automatic Gain Control (AGC) of the receiver is used to control the amplitude of the received 13.56 MHz input sine-wave signal from the antenna (input pins RXP and RXN).

It is desirable to achieve an input voltage in the range of 1.5 V to 1.65 V at the pins RXP, RXN. For symmetric antennas, the voltage levels are the same on the pins RXP, RXN. A voltage lower than 1.5 V lead to a reduced sensitivity of the receiver, a voltage level higher than 1.65 V could result in clipping of the received signal in the signal processing unit of the PN5180. Both conditions should be avoided for optimum performance of the IC. An antenna detuning caused by the presence of a card, or mobile phone will typically result in an RX input level which is outside the desired input voltage range. Here the AGC helps to simplify the design by keeping the RX voltage automatically within the range of 1.5 V to 1.65 V even under dynamic changing antenna detuning conditions.

Functional description:

The peak of the input signal at RXP is regulated to be equal to a reference voltage (internally generated from the supply using a resistive divider). Two external resistors are connected to the RX inputs, the specific value of these resistors in a given design depends on the selected antenna and needs to be determined during development. This external resistor, together with an on-chip variable resistor connected to VMID, forms a resistive voltage divider for the signal processor input voltage. The resolution of the variable resistor is 10 bits.

By varying the on-chip resistor, the amplitude of the input signal can be modified. The on-chip resistor value is increased or decreased depending on the output of the sampled comparator, until the peak of the input signal matches the reference voltage. The amplitude of the RX input is therefore automatically controlled by the AGC circuit.

The internal amplitude controlling resistor in the AGC has a default value of 10 kOhm typ DC coupled. (i.e. when the resistor control bits in AGC_VALUE <9:0> are all 0, the resistance is 10 k). As the control bits are increased, resistors are switched in parallel to the 10k resistor thus lowering the combined resulting resistance value down to 20 Ohm DC coupled (AGC_VALUE <9:0>, all bits set to 1).

Any RF-field-off is enabling the AGC, configuring the AGC for Card mode and is overwriting any AGC configuration done previously by the host.

11.8.9.3 RX Wait

The guard time rx_wait is started after the end of a transmission. If the register flag RX_WAIT_RFON_ENABLE is set to 1, the guard time is started when the device switches off its own RF-Field and an external RF-Field was detected.

The guard time rx_wait can be disabled by setting the register RX_WAIT_VALUE to 00h meaning the receiver is immediately enabled.

11.8.9.4 EMD Error handling

EMVCo

The PN5180 supports EMD handling according to the EMVCo standard. To support further extension the EMD block is configurable to allow adoption for further standard updates.

The PN5180 supports automatically restart of the receiver and CLIF timer1 is restarted in case of an EMD event. The CLIF timer is selectable in the EMD_CONTROL register.

An EMD event is generated:

- Independent of received number of bytes
- Any Residual bits and EMD_CONTROL.emd_transmission_error_above_noise = 0
- When the received number of bytes without CRC is <= EMD_CONTROL.emd_noise_bytes_threshold
- Independent of received number of bytes
- Any Residual bits and EMD_CONTROL.emd_transmission_error_above_noise = 0
- When the received number of bytes without CRC is <= EMD_CONTROL.emd_noise_bytes_threshold
- Missing CRC (1 byte frame) when EMD_CONTROL.emd_missing_crc_is_protocol_error_type_X = 0

11.8.10 Low-Power Card Detection (LPCD)

The low-power card detection is an energy-saving configuration option for the PN5180.

A low frequency oscillator (LFO) is implemented to drive a wake-up counter, waking-up PN5180 from standby mode. This allows implementation of low-power card detection polling loop at application level.

The SWITCH_MODE instruction allows entering the LPCD mode with a given standby duration value.

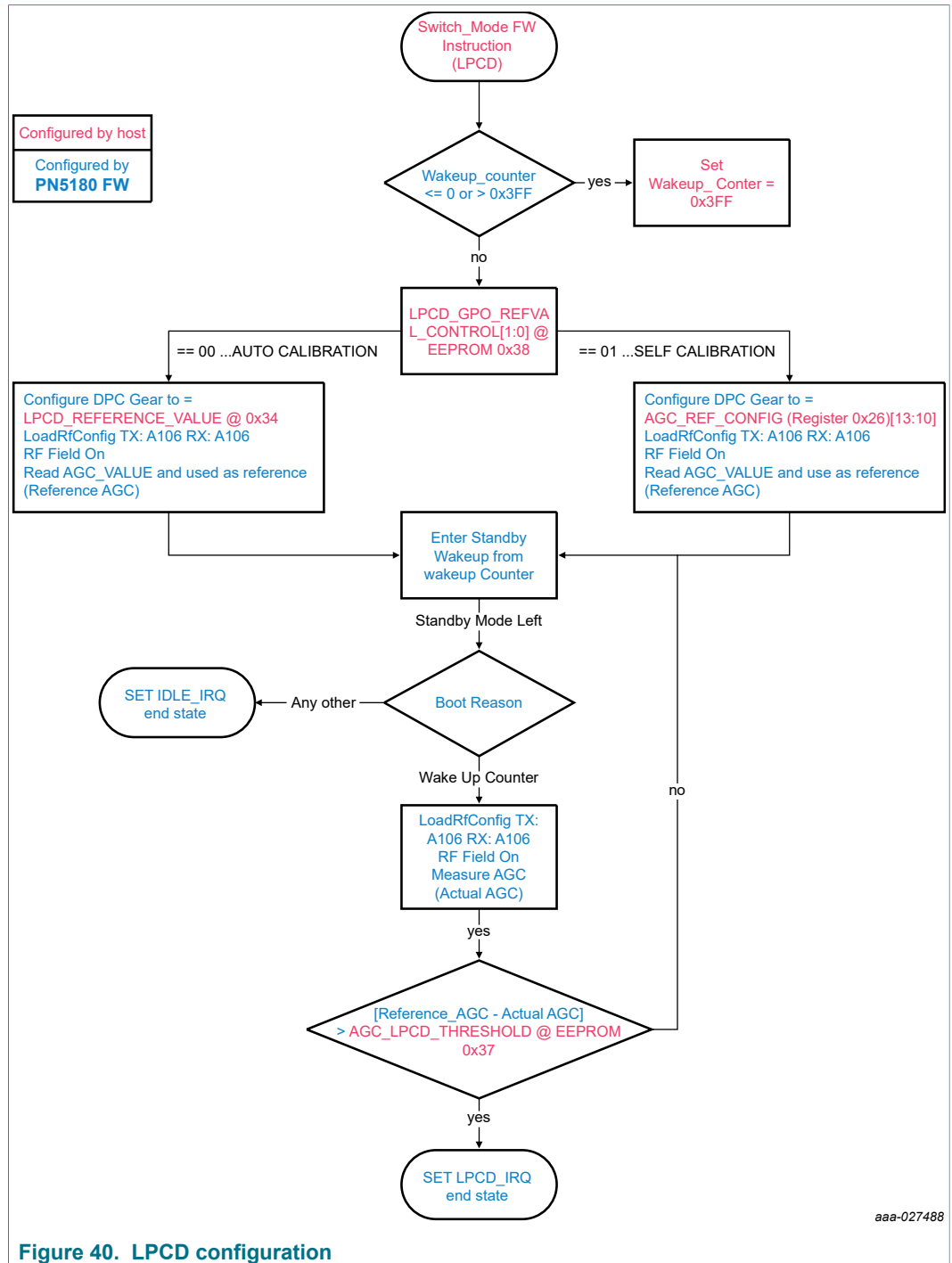


Figure 40. LPCD configuration

aaa-027488

Before entering the LPCD mode, an LPCD reference value needs to be determined. Three options do exist for generating this reference value.

The LPCD works in two phases:

First the standby phase is controlled by the wake-up counter (timing defined in the instruction), which defines the duration of the standby of the PN5180.

Second phase is the detection-phase. The RF field is switched on for a defined time (EEPROM configuration) and then the AGC value is compared to a reference value.

High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes

- If the AGC value exceeds the reference value, a LPCD_IRQ is raised to the host. The register configurations done by the host are not restored after wake-up. command. The host has to configure the NFC frontend for a dedicated protocol operation to allow a polling for a card.
- If the AGC value does not exceed the limit of the reference value, no LPC_IRQ is raised and the IC is set to the first phase (standby mode) again.

As an additional feature the GPO1 (general-purpose output) pin can be enabled to wake up an external DC-DC from power down for the TVDD supply. The GPO1 allows setting to high before the transmitter is switched on. This allows the wake-up of an external DC-DC from power down. The GPO1 can be set to low after the RF field is switched off to set an external DC-DC into power-down mode. The time of toggling the GPO in relation to the RF-on and RF-off timings can be configured in EEPROM addresses 0x39 and 0x3A.

These two phases are executed in a loop until

1. Card / metal is detected (LPCD_IRQ is raised).
2. Reset occurs, which resets all the system configurations. The LPCD is also stopped in this case.
3. NSS on Host IF
4. RF Level Detected

The behavior of the generated field is different dependent on the activation state of the DPC function:

- If the DPC feature is not active, the ISO/IEC14443 type A 106 kbit/s settings are used during the sensing time.
- If the DPC is active, the RF_ON command is executed. The RF field is switched on as soon as the timer configured by the SWITCH_MODE command elapses. The RF field is switched on for a duration as defined for an activated DPC. The timer for the LPCD_FIELD_ON_TIME starts to count as soon as the RF_ON command terminates.

Table 73. Low-Power Card Detection: EEPROM configuration

| EEPROM address | Name | Bit | value | Description |
|----------------|--|-----|-------|--|
| 0x34 | LPCD_REFERENCE_VALUE | - | - | 2 bytes: bit 15:4 RFU; bit 3:0 AGC gear |
| 0x36 | LPCD_FIELD_ON_TIME | - | - | 1 byte: Defines the RF-ON time for the AGC measurement. The minimum RF-ON time depends on the antenna configuration and the connected matching network. It needs to be chosen in such a way that a stable condition for the AGC measurement is given at the end of the time. The byte defines the delay multiplied by 8 in microseconds. |
| 0x37 | LPCD_THRESHOLD | - | - | 1 byte: Defines the AGC threshold value. This value is used to compare against the current AGC value during the low-power card detection phase. if the difference between AGC reference value and current AGC value is greater than LPCD_THRESHOLD, the IC wakes up from LPCD. |
| 0x38 | from firmware version 3.A onwards LPCD_REFVAL_GPO_CONTROL | - | - | This byte in EEPROM is used to control the GPO assertion during wake-up and LPCD card detect. |
| | | 1:0 | - | Defines the source of the LPCD reference value |
| | | 00 | | LPCD AUTO CALIBRATION Performs one calibration with gear number as defined in EEPROM (LPCD_REFERENCE_VALUE, bit 3:0) and starts LPCD afterwards. |

| EEPROM address | Name | Bit | value | Description | | |
|----------------|---------------------------------|-----|-------|---|--|--|
| | | | 01 | LPCD SELF CALIBRATION LPCD is started using the gear (AGC_GEAR) and AGC reference value (AGC_REF) as available in register ACG_REF_CONFIG | | |
| | | | 10 | RFU | | |
| | | | 11 | RFU | | |
| | | 2 | | - | | Allows enabling a GPO output level change during wake-up from standby, before the RF field is switched on. This allows waking-up an external DC-DC supplying the transmitter (pin TVDD). |
| | | | | 0 | | Disable Control for external TVDD DC-DC via GPO1 |
| | | | | 1 | | Enable Control for external TVDD DC-DC via GPO1 |
| | | 3 | | - | | GPO2 Control for external TVDD DC-DC during wake-up from standby |
| | | | | 0 | | Disable Control of external TVDD DC-DC via GPO2 on LPCD Card Detect |
| | | | | 1 | | Enable Control of external TVDD DC-DC via GPO2 on LPCD Card Detect |
| | | 4 | | - | | GPO1 Control for external TVDD DC-DC during wake-up from standby |
| | | | | 0 | | Disable Control of external TVDD DC-DC via GPO1 on wake-up from standby |
| | | | | 1 | | Enable Control of external TVDD DC-DC via GPO1 on wake-up from standby |
| 0x39 | LPCD_GPO_TOGGLE_BEFORE_FIELD_ON | - | - | 1 byte: This value defines the time between setting GPO1 until field is switched on. The byte defines the time multiplied by 5 in microseconds. | | |
| 0x3A | LPCD_GPO_TOGGLE_AFTER_FIELD_ON | - | - | 1 byte: This value defines the time between field off and clearing GPO1. The byte defines the time multiplied by 5 in microseconds. | | |

11.8.10.1 Check Card register

The Check Card register at register 0x26 performs one LPCD cycle. This means, that only the second phase - the detection phase is executed.

11.9 Register overview

11.9.1 Register overview

Table 74. Register address overview

| Address (HEX) | Address (decimal) | Name |
|---------------|-------------------|---------------|
| 0h | 0 | SYSTEM_CONFIG |
| 1h | 1 | IRQ_ENABLE |

| Address (HEX) | Address (decimal) | Name |
|---------------|-------------------|----------------------|
| 2h | 2 | IRQ_STATUS |
| 3h | 3 | IRQ_CLEAR |
| 4h | 4 | TRANSCEIVER_CONFIG |
| 5h | 5 | PADCONFIG |
| 6h | 6 | RFU |
| 7h | 7 | PADOUT |
| 8h | 8 | TIMER0_STATUS |
| 9h | 9 | TIMER1_STATUS |
| Ah | 10 | TIMER2_STATUS |
| Bh | 11 | TIMER0_RELOAD |
| Ch | 12 | TIMER1_RELOAD |
| Dh | 13 | TIMER2_RELOAD |
| Eh | 14 | TIMER0_CONFIG |
| Fh | 15 | TIMER1_CONFIG |
| 10h | 16 | TIMER2_CONFIG |
| 11h | 17 | RX_WAIT_CONFIG |
| 12h | 18 | CRC_RX_CONFIG |
| 13h | 19 | RX_STATUS |
| 14h | 20 | TX_UNDERSHOOT_CONFIG |
| 15h | 21 | TX_OVERSHOOT_CONFIG |
| 16h | 22 | TX_DATA_MOD |
| 17h | 23 | TX_WAIT_CONFIG |
| 18h | 24 | TX_CONFIG |
| 19h | 25 | CRC_TX_CONFIG |
| 1Ah | 26 | SIGPRO_CONFIG |
| 1Bh | 27 | SIGPRO_CM_CONFIG |
| 1Ch | 28 | SIGPRO_RM_CONFIG |
| 1Dh | 29 | RF_STATUS |
| 1Eh | 30 | AGC_CONFIG |
| 1Fh | 31 | AGC_VALUE |
| 20h | 32 | RF_CONTROL_TX |
| 21h | 33 | RF_CONTROL_TX_CLK |
| 22h | 34 | RF_CONTROL_RX |
| 23h | 35 | LD_CONTROL |
| 24h | 36 | SYSTEM_STATUS |
| 25h | 37 | TEMP_CONTROL |
| 26h | 38 | AGC_REF_CONFIG |

| Address (HEX) | Address (decimal) | Name |
|---------------|-------------------|--|
| 27h | 39 | DPC_CONFIG |
| 28h | 40 | EMD_CONTROL |
| 29h | 41 | ANT_CONTROL |
| 2Ah-035h | 42-53 | RFU |
| 036h | 54 | TX_CONTROL |
| 037h-038h | 55-56 | RFU |
| 39h | 57 | SIGPRO_RM_CONFIG_EXTENSION |
| 3A-42h | 58-66 | RFU |
| 43h | 67 | FELICA_EMD_CONTROL (available From firmware V4.1 onwards, otherwise RFU) |
| 44h-7Ah | 68-122 | RFU |

11.9.2 Register description

The default setting of a bit within a register is indicated by the "*". Value indicates the allowed range for the bits of a Symbol

Table 75. SYSTEM_CONFIG register (address 0000h) bit description

| Bit | Symbol | Access | Value | Description |
|---------------------|-----------------------|--------|-------|---|
| from FW 3.9 onwards | | | | |
| 31:20 | RFU | R | 0*,1 | Reserved |
| 19:12 | DPC_XI_RAM_CORRECTION | R/W | 0*,1 | Correction value for DPC_XI value stored in EEprom. Resulting AGC value will be: ActualAGCvalue + DPC_XI EEPROM + DPC_XI RAM_CORRECTION (values are ranging from -127 ...+127, sign bit is MSB) |
| 8 | SOFT_RESET | W | 0*,1 | performs a reset of the device by writing a "1" into this register. |
| 7 | RFU | R/W | 0*,1 | RFU |
| 6 | MFC_CRYPTON_ON | R/W | 0*,1 | If set to 1, the mfc-crypto is enabled for end-/de-cryption |
| 5 | PRBS_TYPE | R/W | 0*,1 | Defines the PRBS type; If set to 1, PRBS15 is selected, default value 0 selects PRBS9 |
| 4 | RFU | R/W | 0*,1 | RFU |
| 3 | START_SEND | R/W | 0*,1 | If set to 1, this triggers the data transmission according to the transceive state machine |
| 0:2 | COMMAND | R/W | 001* | These bits define the command for the transceive state machine |
| | | | 000 | IDLE/StopCom Command; stops all ongoing communication and set the CLIF to IDLE mode |
| | | | 001 | RFU |
| | | | 010 | RFU |

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|---|
| | | | 011 | Transceive command; initiates a transceive cycle. Note: Depending on the value of the Initiator bit, a transmission is started or the receiver is enabled Note: The transceive command does not finish automatically. It stays in the transceive cycle until stopped via the IDLE/StopCom command |
| | | | 100 | KeepCommand command; This command does not change the content of the command register and might be used in case other bits in the register are to be changed |
| | | | 101 | LoopBack command; This command is for test purposes only. It starts a transmission and at the same time enables the receiver. |
| | | | 110 | PRBS command, performs an endless transmission of PRBS data |
| | | | 111 | RFU |

Table 76. IRQ_ENABLE register (address 0001h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|------------------------|--------|-------|---|
| 31:17 | RFU | R | 0*, 1 | - |
| 19 | LPCD_IRQ_STAT | R | 1 | Low-Power Card Detection IRQ, fixed always to 1 |
| 18 | HV_ERROR_IRQ_STAT | R | 1 | EEPROM Failure during Programming IRQ, fixed always to 1 |
| 17 | GENERAL_ERROR_IRQ_STAT | R | 1 | General Error IRQ - fixed always to 1 |
| 16 | TEMPSENS_ERROR_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the TempSensor |
| 15 | RX_SC_DET_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RX Subcarrier Detection |
| 14 | RX_SOF_DET_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RX SOF Detection |
| 13 | TIMER2_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the Timer2 |
| 12 | TIMER1_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the Timer1 |
| 11 | TIMER0_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the Timer0 |
| 10 | RF_ACTIVE_ERROR_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RF active error |
| 9 | TX_RFON_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RF Field ON in PCD |
| 8 | TX_RFOFF_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RF Field OFF in PCD |
| 7 | RFON_DET_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RF Field ON detection |
| 6 | RFOFF_DET_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the RF Field OFF detection |

| Bit | Symbol | Access | Value | Description |
|-----|-----------------------|--------|-------|--|
| 5 | STATE_CHANGE_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the State Change in the transceive state machine |
| 4 | CARD_ACTIVATED_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin when PN5180 is activated as a Card |
| 3 | MODE_DETECTED_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin when PN5180 is detecting an external modulation scheme |
| 2 | IDLE_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for the IDLE mode |
| 1 | TX_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for End of RF transmission |
| 0 | RX_IRQ_EN | R/W | 0*, 1 | Enable IRQ propagation to the pin for End of RF reception |

Table 77. IRQ_STATUS register (address 0002h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--------------------------|--------|-------|--|
| 31:20 | RFU | R | 0*, 1 | - |
| 19 | LPCD_IRQ_STAT | R | 0*, 1 | Low-Power Card Detection IRQ |
| 18 | HV_ERROR_IRQ_STAT | R | 0*, 1 | EEPROM Failure during Programming IRQ |
| 17 | GENERAL_ERROR_IRQ_STAT | R | 0*, 1 | General Error IRQ |
| 16 | TEMPSENS_ERROR_IRQ_STAT | R | 0*, 1 | Temperature Sensor IRQ |
| 15 | RX_SC_DET_IRQ_STAT | R | 0*, 1 | RX Subcarrier Detection IRQ |
| 14 | RX_SOF_DET_IRQ_STAT | R | 0*, 1 | RX SOF Detection IRQ |
| 13 | TIMER2_IRQ_STAT | R | 0*, 1 | Timer2 IRQ |
| 12 | TIMER1_IRQ_STAT | R | 0*, 1 | Timer1 IRQ |
| 11 | TIMER0_IRQ_STAT | R | 0*, 1 | Timer0 IRQ |
| 10 | RF_ACTIVE_ERROR_IRQ_STAT | R | 0*, 1 | RF active error IRQ |
| 9 | TX_RFON_IRQ_STAT | R | 0*, 1 | RF Field ON in PCD IRQ |
| 8 | TX_RFOFF_IRQ_STAT | R | 0*, 1 | RF Field OFF in PCD IRQ |
| 7 | RFON_DET_IRQ_STAT | R | 0*, 1 | RF Field ON detection IRQ |
| 6 | RFOFF_DET_IRQ_STAT | R | 0*, 1 | RF Field OFF detection IRQ |
| 5 | STATE_CHANGE_IRQ_STAT | R | 0*, 1 | State Change in the transceive state machine IRQ |
| 4 | CARD_ACTIVATED_IRQ_STAT | R | 0*, 1 | Activated as a Card IRQ |
| 3 | MODE_DETECTED_IRQ_STAT | R | 0*, 1 | External modulation scheme detection IRQ |
| 2 | IDLE_IRQ_STAT | R | 0*, 1 | IDLE IRQ |
| 1 | TX_IRQ_STAT | R | 0*, 1 | End of RF transmission IRQ |
| 0 | RX_IRQ_STAT | R | 0*, 1 | End of RF reception IRQ |

Table 78. IRQ_CLEAR register (address 0003h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-------------------------|--------|-------|--|
| 31:20 | RFU | R | 0*, 1 | - |
| 19 | LPCD_IRQ_CLR | R/W | 0*, 1 | Clear Low-Power Card Detection IRQ |
| 18 | HV_ERROR_IRQ_CLR | R/W | 0*, 1 | Clear EEPROM Failure during Programming IRQ |
| 17 | GENERAL_ERROR_IRQ_CLR | R/W | 0*, 1 | Clear General Error IRQ |
| 16 | TEMPSENS_ERROR_IRQ_CLR | R/W | 0*, 1 | Clear Temperature Sensor IRQ |
| 15 | RX_SC_DET_IRQ_CLR | R/W | 0*, 1 | Clear RX Subcarrier Detection IRQ |
| 14 | RX_SOF_DET_IRQ_CLR | R/W | 0*, 1 | Clear RX SOF Detection IRQ |
| 13 | TIMER2_IRQ_CLR | R/W | 0*, 1 | Clear Timer2 IRQ |
| 12 | TIMER1_IRQ_CLR | R/W | 0*, 1 | Clear Timer1 IRQ |
| 11 | TIMER0_IRQ_CLR | R/W | 0*, 1 | Clear Timer0 IRQ |
| 10 | RF_ACTIVE_ERROR_IRQ_CLR | R/W | 0*, 1 | Clear RF active error IRQ |
| 9 | TX_RFON_IRQ_CLR | R/W | 0*, 1 | Clear RF Field ON in PCD IRQ |
| 8 | TX_RFOFF_IRQ_CLR | R/W | 0*, 1 | Clear RF Field OFF in PCD IRQ |
| 7 | RFON_DET_IRQ_CLR | R/W | 0*, 1 | Clear RF Field ON detection IRQ |
| 6 | RFOFF_DET_IRQ_CLR | R/W | 0*, 1 | Clear RF Field OFF detection IRQ |
| 5 | STATE_CHANGE_IRQ_CLR | R/W | 0*, 1 | Clear State Change in the transceive state machine IRQ |
| 4 | CARD_ACTIVATED_IRQ_CLR | R/W | 0*, 1 | Clear Activated as a Card IRQ |
| 3 | MODE_DETECTED_IRQ_CLR | R/W | 0*, 1 | Clear External modulation scheme detection IRQ |
| 2 | IDLE_IRQ_CLR | R/W | 0*, 1 | Clear IDLE IRQ |
| 1 | TX_IRQ_CLR | R/W | 0*, 1 | Clear End of RF transmission IRQ |
| 0 | RX_IRQ_CLR | R/W | 0*, 1 | Clear End of RF reception IRQ |

Table 79. TRANSCEIVE_CONTROL register (address 0004h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|----------------------|--------|---------|--|
| 9:4 | STATE_TRIGGER_SELECT | R/W | 000000* | Register to select the state to trigger the STATE_CHANGE_IRQ flag. Each bit of the bit field enables one state - several states are possible. Note: If all bits are 0 no IRQ is triggered. |
| | | | xxxxx1 | IDLE state enabled to trigger IRQ |
| | | | xxxx1x | WaitTransmit state enabled to trigger IRQ |
| | | | xxx1xx | Transmitting state enabled to trigger IRQ |
| | | | xx1xxx | WaitReceive state enabled to trigger IRQ |
| | | | x1xxxx | WaitForData state enabled to trigger IRQ |
| | | | 1xxxxx | Receiving state enabled to trigger IRQ |

| Bit | Symbol | Access | Value | Description |
|-----|---------------------|--------|-------|---|
| 3 | TX_SKIP_SEND_ENABLE | R/W | 0*, 1 | If set, not transmission is started after tx_wait is expired and START_SEND was set Note: The bit is cleared by HW when the WaitReceive state is entered. |
| 2 | TX_FRAMESTEP_ENABLE | R/W | 0*, 1 | If set, at every start of transmission; each byte of data is sent in a separate frame. SOF and EOF are appended to the data byte according to the framing settings. After one byte is transmitted; the TxEncoder waits for a new start trigger to continue with the next byte. |
| 1 | RX_MULTIPLE_ENABLE | R/W | 0*, 1 | If set, the receiver is reactivated after the end of a reception. A status byte is written to the RAM containing all relevant status information of the frame. Note: Data in RAM is word aligned therefore empty bytes of a data Word in RAM are padded with 0x00 bytes. SW has to calculate the correct address for the following frame. |
| 0 | INITIATOR | R/W | 0*, 1 | If set, the CLIF is configured for initiator mode. Depending on this setting, the behavior of the transceive command is different |

Table 80. PADCONFIG register (address 0005h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|----------------------|--------|-------|---|
| 7 | EN_SLEW_RATE_CONTROL | R/W | 0*, 1 | Enables slew rate control of digital pads: The Rise/Fall Time can be adjusted by the slew rate control. The slew reate value 0 is for slow slew rate with a value between 2-10ns (depending on load, cap) and the value 1 is for fast slew with a value between 1-3ns (also depending on load, cap....) |
| 6 | GPO7_DIR | R/W | 0*, 1 | Enables the output driver of GPO7. The GPO is only available for the package TFBGA64 |
| 5 | GPO6_DIR | R/W | 0*, 1 | Enables the output driver of GPO6. The GPO is only available for the package TFBGA64 |
| 4 | GPO5_DIR | R/W | 0*, 1 | Enables the output driver of GPO5. The GPO is only available for the package TFBGA64 |
| 3 | GPO4_DIR | R/W | 0*, 1 | Enables the output driver of GPO4. The GPO is only available for the package TFBGA64 |
| 2 | GPO3_DIR | R/W | 0*, 1 | Enables the output driver of GPO3. The GPO is only available for the package TFBGA64 |
| 1 | GPO2_DIR | R/W | 0*, 1 | Enables the output driver of GPO2. The GPO is only available for the package TFBGA64 |
| 0 | GPO1_DIR | R/W | 0*, 1 | Enables the output driver of GPO1. The GPO is only available for the package TFBGA64 and HVQFN40 |

Table 81. PAD_OUT register (address 0007h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|----------|--------|-------|---|
| 6 | GPO7_OUT | R/W | 0*, 1 | Output value of GPO7. The GPO is only available for the package TFBGA64 |
| 5 | GPO6_OUT | R/W | 0*, 1 | Output value of GPO6. The GPO is only available for the package TFBGA64 |
| 4 | GPO5_OUT | R/W | 0*, 1 | Output value of GPO5. The GPO is only available for the package TFBGA64 |
| 3 | GPO4_OUT | R/W | 0*, 1 | Output value of GPO4. The GPO is only available for the package TFBGA64 |
| 2 | GPO3_OUT | R/W | 0*, 1 | Output value of GPO3. The GPO is only available for the package TFBGA64 |
| 1 | GPO2_OUT | R/W | 0*, 1 | Output value of GPO2. The GPO is only available for the package TFBGA64 |
| 0 | GPO1_OUT | R/W | 0*, 1 | Output value of GPO1. The GPO is only available for the package TFBGA64 and HVQFN40 |

Table 82. TIMER0_STATUS register (address 0008h) bit description

| Bit | Symbol | Access | Value | Description |
|------|------------|--------|------------------|---|
| 20 | T0_RUNNING | R | 0*, 1 | Indicates that timer T0 is running (busy) |
| 19:0 | T0_VALUE | R | 00000h* - FFFFFh | Value of 20bit counter in timer T0 |

Table 83. TIMER1_STATUS register (address 0009h) bit description

| Bit | Symbol | Access | Value | Description |
|------|------------|--------|------------------|---|
| 20 | T1_RUNNING | R | 0*, 1 | Indicates that timer T1 is running (busy) |
| 19:0 | T1_VALUE | R | 00000h* - FFFFFh | Value of 20bit counter in timer T1 |

Table 84. TIMER2_STATUS register (address 000Ah) bit description

| Bit | Symbol | Access | Value | Description |
|------|------------|--------|------------------|---|
| 20 | T2_RUNNING | R | 0*, 1 | Indicates that timer T2 is running (busy) |
| 19:0 | T2_VALUE | R | 00000h* - FFFFFh | Value of 20bit counter in timer T2 |

Table 85. TIMER0_RELOAD register (address 000Bh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------|--------|------------------|-------------------------------|
| 32:20 | - | | | RFU |
| 19:0 | T0_RELOAD_VALUE | R/W | 00000h* - FFFFFh | Reload value of the timer T0. |

Table 86. TIMER1_RELOAD register (address 000Ch) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------|--------|------------------|-------------------------------|
| 32:20 | - | | | RFU |
| 19:0 | T1_RELOAD_VALUE | R/W | 00000h* - FFFFFh | Reload value of the timer T1. |

Table 87. TIMER2_RELOAD register (address 000Dh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------|--------|------------------|-------------------------------|
| 32:20 | - | | | RFU |
| 19:0 | T2_RELOAD_VALUE | R/W | 00000h* - FFFFFh | Reload value of the timer T2. |

Table 88. TIMER0_CONFIG register (address 000Eh) bit description

| Bit | Symbol | Access | Value | Description |
|-----|------------------------|--------|-------|---|
| 20 | T0_STOP_ON_RX_STARTED | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol-dependent and listed in the appendix. |
| 19 | T0_STOP_ON_TX_STARTED | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when a data transmission begins. |
| 18 | T0_STOP_ON_RF_ON_EXT | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when the external RF field is detected. |
| 17 | T0_STOP_ON_RF_OFF_EXT | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when the external RF field vanishes. |
| 16 | T0_STOP_ON_RF_ON_INT | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when the internal RF field is turned on. |
| 15 | T0_STOP_ON_RF_OFF_INT | R/W | 0* | T0_STOP_EVENT: If set; the timer T0 is stopped when the internal RF field is turned off. |
| 14 | T0_START_ON_RX_STARTED | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when a data reception begins (first bit is received). |
| 13 | T0_START_ON_RX_ENDED | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when a data reception ends. |
| 12 | T0_START_ON_TX_STARTED | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when a data transmission begins. |
| 11 | T0_START_ON_TX_ENDED | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when a data transmission ends. |
| 10 | T0_START_ON_RF_ON_EXT | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when the external RF field is detected. |
| 9 | T0_START_ON_RF_OFF_EXT | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when the external RF field is not detected anymore. |
| 8 | T0_START_ON_RF_ON_INT | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when an internal RF field is turned on. |
| 7 | T0_START_ON_RF_OFF_INT | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started when an internal RF field is turned off. |

| Bit | Symbol | Access | Value | Description |
|-----|------------------|--------|-------|--|
| 6 | T0_START_NOW | R/W | 0* | T0_START_EVENT: If set; the timer T0 is started immediately. |
| 5:3 | T0_PRESCALE_SEL | R/W | 000b* | Controls frequency/period of the timer T0 when the prescaler is activated in T0_MODE_SEL: |
| | | | 000b | 6.78 MHz counter |
| | | | 001b | 3.39 MHz counter |
| | | | 010b | 1.70 MHz counter |
| | | | 011b | 848 kHz counter |
| | | | 100b | 424 kHz counter |
| | | | 101b | 212 kHz counter |
| | | | 110b | 106 kHz counter |
| 2 | T0_MODE_SEL | R/W | 0* | Configuration of the timer T0 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T0_PRESCALE_SEL). |
| 1 | T0_RELOAD_ENABLE | R/W | 0* | If set to 0; the timer T0 stops on expiration. 0* After expiration the timer T0 stops counting; i.e.; remain zero; reset value. 1 After expiration the timer T0 reloads its preset value and continues counting down. |
| 0 | T0_ENABLE | R/W | 0* | Enables the timer T0 |

Table 89. TIMER1_CONFIG register (address 000Fh) bit description

| Bit | Symbol | Access | Value | Description |
|-----|------------------------|--------|-------|---|
| 20 | T1_STOP_ON_RX_STARTED | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol-dependent and listed in the appendix. |
| 19 | T1_STOP_ON_TX_STARTED | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when a data transmission begins. |
| 18 | T1_STOP_ON_RF_ON_EXT | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when the external RF field is detected. |
| 17 | T1_STOP_ON_RF_OFF_EXT | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when the external RF field vanishes. |
| 16 | T1_STOP_ON_RF_ON_INT | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when the internal RF field is turned on. |
| 15 | T1_STOP_ON_RF_OFF_INT | R/W | 0* | T1_STOP_EVENT: If set; the timer T1 is stopped when the internal RF field is turned off. |
| 14 | T1_START_ON_RX_STARTED | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when a data reception begins (first bit is received). |
| 13 | T1_START_ON_RX_ENDED | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when a data reception ends. |

| Bit | Symbol | Access | Value | Description |
|-----|------------------------|--------|-------|--|
| 12 | T1_START_ON_TX_STARTED | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when a data transmission begins. |
| 11 | T1_START_ON_TX_ENDED | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when a data transmission ends. |
| 10 | T1_START_ON_RF_ON_EXT | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when the external RF field is detected. |
| 9 | T1_START_ON_RF_OFF_EXT | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when the external RF field is not detected anymore. |
| 8 | T1_START_ON_RF_ON_INT | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when an internal RF field is turned on. |
| 7 | T1_START_ON_RF_OFF_INT | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started when an internal RF field is turned off. |
| 6 | T1_START_NOW | R/W | 0* | T1_START_EVENT: If set; the timer T1 is started immediately. |
| 5:3 | T1_PRESCALE_SEL | R/W | 000b* | Controls frequency/period of the timer T1 when the prescaler is activated in T1_MODE_SEL: |
| | | | 000b | 6.78 MHz counter |
| | | | 001b | 3.39 MHz counter |
| | | | 010b | 1.70 MHz counter |
| | | | 011b | 848 kHz counter |
| | | | 100b | 424 kHz counter |
| | | | 101b | 212 kHz counter |
| | | | 110b | 106 kHz counter |
| | | | 111b | 53 kHz counter |
| 2 | T1_MODE_SEL | R/W | 0* | Configuration of the timer T1 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T1_PRESCALE_SEL). |
| 1 | T1_RELOAD_ENABLE | R/W | 0* | If set to 0; the timer T1 stops on expiration. 0* After expiration the timer T1 stops counting; i.e.; remain zero; reset value. 1 After expiration the timer T1 reloads its preset value and continues counting down. |
| 0 | T1_ENABLE | R/W | 0* | Enables the timer T1 |

Table 90. TIMER2_CONFIG register (address 0010h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-----------------------|--------|-------|---|
| 20 | T2_STOP_ON_RX_STARTED | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when a data reception begins and the first 4 bits had been received. The additional delay of the timer is protocol-dependent and listed in the appendix. |
| 19 | T2_STOP_ON_TX_STARTED | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when a data transmission begins. |

| Bit | Symbol | Access | Value | Description |
|-----|------------------------|--------|-------|--|
| 18 | T2_STOP_ON_RF_ON_EXT | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when the external RF field is detected. |
| 17 | T2_STOP_ON_RF_OFF_EXT | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when the external RF field vanishes. |
| 16 | T2_STOP_ON_RF_ON_INT | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when the internal RF field is turned on. |
| 15 | T2_STOP_ON_RF_OFF_INT | R/W | 0* | T2_STOP_EVENT: If set; the timer T2 is stopped when the internal RF field is turned off. |
| 14 | T2_START_ON_RX_STARTED | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when a data reception begins (first bit is received). |
| 13 | T2_START_ON_RX_ENDED | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when a data reception ends. |
| 12 | T2_START_ON_TX_STARTED | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when a data transmission begins. |
| 11 | T2_START_ON_TX_ENDED | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when a data transmission ends. |
| 10 | T2_START_ON_RF_ON_EXT | R/W | 0* | T2_START_EVENT: If set; the timer T2T2 is started when the external RF field is detected. |
| 9 | T2_START_ON_RF_OFF_EXT | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when the external RF field is not detected anymore. |
| 8 | T2_START_ON_RF_ON_INT | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when an internal RF field is turned on. |
| 7 | T2_START_ON_RF_OFF_INT | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started when an internal RF field is turned off. |
| 6 | T2_START_NOW | R/W | 0* | T2_START_EVENT: If set; the timer T2 is started immediately. |
| 5:3 | T2_PRESCALE_SEL | R/W | 000b* | Controls frequency/period of the timer T2 when the prescaler is activated in T2_MODE_SEL: |
| | | | 000b | 6.78 MHz counter |
| | | | 001b | 3.39 MHz counter |
| | | | 010b | 1.70 MHz counter |
| | | | 011b | 848 kHz counter |
| | | | 100b | 424 kHz counter |
| | | | 101b | 212 kHz counter |
| | | | 110b | 106 kHz counter |
| | | | 111b | 53 kHz counter |
| 2 | T2_MODE_SEL | R/W | 0* | Configuration of the timer T2 clock. 0b* Prescaler is disabled: the timer frequency matches CLIF clock frequency (13.56 MHz). 1b Prescaler is enabled: the timer operates on the prescaler signal frequency (chosen by T2_PRESCALE_SEL). |

| Bit | Symbol | Access | Value | Description |
|-----|------------------|--------|-------|---|
| 1 | T2_RELOAD_ENABLE | R/W | 0* | If set to 0; the timer T2 stops on expiration. 0* After expiration the timer T2 stops counting; i.e.; remain zero; reset value. 1 After expiration the timer T2 reloads its preset value and continues counting down. |
| 0 | T2_ENABLE | R/W | 0* | Enables the timer T2 |

Table 91. RX_WAIT_CONFIG (address 0011h) bit description

| Bit | Symbol | Access | Value | Description |
|------|-------------------|--------|-------|---|
| 27:8 | RX_WAIT_VALUE | R/W | 0* | Defines the rx_wait timer reload value. Note: If set to 00000h, the rx_wait guard time is disabled. For I-CODE ILT-M the recommended setting at MAN2-848 (212 Kbps) is 0xA0. |
| 7:0 | RX_WAIT_PRESCALER | R/W | 0* | Defines the prescaler reload value for the rx_wait timer. For correct DPC operation, it is required to set the prescaler to 0x7F For type A communication, the prescaler has to be set to 0x7F as well. |

Table 92. CRC_RX_CONFIG (address 0012h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|------------------------|--------|----------|---|
| 31:16 | RX_CRC_PRESET_VALUE | R/W | 0*-FFFFh | Arbitrary preset value for the Rx-Encoder CRC calculation. |
| 15:12 | RFU | R | 0 | Reserved |
| 11 | RX_PARITY_TYPE | R/W | 0* | Defines which type of the parity-bit is used Note: This bit is set by the mod-detector if automatic mode detection is enabled and ISO14443A communication is detected. 0 Even parity calculation is used 1 Odd parity calculation is used |
| 10 | RX_PARITY_ENABLE | R/W | 0* | If set to 1; a parity-bit for each byte is expected; will be extracted from data stream and checked for correctness. In case the parity-bit is incorrect; the RX_DATA_INTEGRITY_ERROR flag is set. Nevertheless the reception is continued. Note: This bit is set by the mod-detector if automatic mode detection is enabled and ISO14443A communication is detected. |
| 9 | VALUES_AFTER_COLLISION | R/W | 0* | This bit defined the value of bits received after a collision occurred. 0* All received bits after a collision will be cleared. 1 All received bits after a collision keep their value. |
| 8:6 | RX_BIT_ALIGN | R/W | 0* | RxAlign defines the bit position within the byte for the first bit received. Further received bits are stored at the following bit positions. |

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|--|
| 5:3 | RX_CRC_PRESET_SEL | R/W | 000b* | Preset values of the CRC register for the Rx-Decoder. For a CRC calculation using 5bits, only the LSByte is used. |
| | | | 000b* | 0000h, reset value. This configuration is set by the Mode detector for FeliCa. |
| | | | 001b | 6363h, this configuration is set by the Mode detector for ISO14443 type A. |
| | | | 010b | A671h |
| | | | 011b | FFFFh, this configuration is set by the Mode detector for ISO14443 type B. |
| | | | 100b | 0012h |
| | | | 101b | E012h |
| | | | 111b | Use arbitrary preset value RX_CRC_PRESET_VALUE |
| 2 | RX_CRC_TYPE | R/W | 0* | Controls the type of CRC calculation for the Rx-Decoder |
| | | | 0 | 16-bit CRC calculation, reset value |
| | | | 1 | 5-bit CRC calculation |
| 1 | RX_CRC_INV | R/W | 0* | Controls the comparison of the CRC checksum for the Rx-Decoder |
| | | | 0* | Not inverted CRC value. This bit is cleared by the Mode detector for ISO14443 type A and FeliCa. |
| | | | 1 | Inverted CRC value: F0B8h, this bit is set by the Mode detector for ISO14443 type B. |
| 0 | RX_CRC_ENABLE | R/W | 0* | If set; the Rx-Decoder checks the CRC for correctness. Note: This bit is set by the Mode Detector when ISO14443 type B or FeliCa (212 kbit/s or 424 kbit/s) is detected. |

Table 93. RX_STATUS register (address 0013h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-------------|--------|-------|---|
| 31:26 | RFU | R | 0 | Reserved |
| 25:19 | RX_COLL_POS | R | 0* | <p>These bits show the bit position of the first detected collision in a received frame (only data bits are interpreted).</p> <p>Note: These bits contain information for the bit position of the first detected collision in passive communication mode at 106 kbit/s, communication mode for ISO/IEC 14443 type A and for MIFARE Classic or ISO/IEC15693 mode. Precondition: The CollPosValid bit is set.</p> <p>Note: If RX_ALIGN is set to a value different to 0, this value is included in the RX_COLL_POS.</p> |

| Bit | Symbol | Access | Value | Description |
|-------|-------------------------|--------|-------|--|
| 18 | RX_COLLISION_DETECTED | R | 0* | This flag is set to 1, when a collision has occurred. The position of the first collision is shown in the register RX_COLLPOS |
| 17 | RX_PROTOCOL_ERROR | R | 0* | This flag is set to 1, when a protocol error has occurred. A protocol error can be a wrong stop bit, a missing or wrong ISO/IEC14443 B EOF or SOF or a wrong number of received data bytes. Note: When a protocol error is detected, data reception is stopped. Note: The flag is automatically cleared at start of next reception. |
| 16 | RX_DATA_INTEGRITY_ERROR | R | 0* | This flag is set to 1, if a data integrity error has been detected. Possible caused can be a wrong parity or a wrong CRC. Note: On a data integrity error, the reception is continued Note: The flag is automatically cleared at start of next reception. Note: If a reversed parity bit is a stop criteria, the flag is not set to 1 if there is a wrong parity. |
| 15:13 | RX_NUM_LAST_BITS | R | 0* | Defines the number of valid bits of the last data byte received in bit-oriented communications. If zero the whole byte is valid. |
| 12:9 | RX_NUM_FRAMES_RECEIVED | R | 0* | Indicates the number of frames received. The value is updated when the RxIRQ is raised. Note: This bit field is only valid when the RxMultiple is active (bit RX_MULTIPLE_ENABLE set) |
| 8:0 | RX_NUM_BYTES_RECEIVED | R | 0* | Indicates the number of bytes received. The value is valid when the RxIRQ is raised until the receiver is enabled again. |

Table 94. TX_UNDERSHOOT_CONFIG register (address 0014h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|---------------------------|--------|-------|--|
| 31:16 | TX_UNDERSHOOT_PATTERN | | | Undershoot pattern which is transmitted after each falling edge. |
| 15:5 | RESERVED | | | - |
| 4:1 | TX_UNDERSHOOT_PATTERN_LEN | | | Defines length of the undershoot prevention pattern (value +1). The pattern is applied starting from the LSB of the defined pattern; all other bits are ignored. |
| 0 | TX_UNDERSHOOT_PROT_ENABLE | | | If set to 1; the undershoot protection is enabled |

Table 95. TX_OVERSHOOT_CONFIG register (address 0015h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|----------------------|--------|------------|--|
| 31:16 | TX_OVERSHOOT_PATTERN | R/W | 0* - FFFFh | Overshoot pattern which is transmitted after each rising edge. |

| Bit | Symbol | Access | Value | Description |
|------|--------------------------|--------|-------|---|
| 15:5 | RFU | R | 0 | Reserved |
| 4:1 | TX_OVERSHOOT_PATTERN_LEN | R/W | 0*-Fh | Defines length of the overshoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored. |
| 0 | TX_OVERSHOOT_PROT_ENABLE | R/W | 0*, 1 | If set to 1, the overshoot protection is enabled. |

Table 96. TX_DATA_MOD register (address 0016h) bit description

| Bit | Symbol | Access | Value | Description |
|------|-------------------|--------|----------|--|
| 15:8 | TX_DATA_MOD_WIDTH | R/W | 0*-FFh | Specifies the length of a pulse for sending data with miller pulse modulation enabled. The length is given by the number of carrier clocks + 1. |
| 7:0 | TX_BITPHASE | R/W | 0* - FFh | Defines the number of 13.56 MHz cycles used for adjustment of TX_WAIT to meet the FDT. This is done by using this value as first counter initialization value instead of TX_WAIT_PRESCALER. These bits of TX_BITPHASE, together with TX_WAIT_VALUE and TX_WAIT_PRESCALER are defining the number of carrier frequency clocks which are added to the waiting period before transmitting data in all communication modes. TX_BITPHASE is used to adjust the TX bit synchronization during passive NFCIP-1 communication mode at 106 kbit and in ISO/IEC 14443 type A. |

Table 97. TX_WAIT_CONFIG register (address 0017h) bit description

| Bit | Symbol | Access | Value | Description |
|------|---------------|--------|-------------|---|
| 27:8 | TX_WAIT_VALUE | D | 0* - FFFFFh | Defines the tx_wait timer value. The values TX_WAIT_VALUE and TX_WAIT_PRESCALER are the initial counter values of two independent counters. The counter linked to TX_WAIT_PRESCALER is decremented at every 13.56 MHz clock. As soon as the counter TX_WAIT_PRESCALER overflows (transition from 00h to FFh), the counter linked to TX_WAIT is decremented. At the same time, the counter linked to TX_WAIT_PRESCALER is reloaded with the TX_WAIT_PRESCALER value. The first initial TX_WAIT_PRESCALER counter value is always using the data defined in TX_BITPHASE (in case of PICC operation). All other subsequent counter reload values are taken from TX_WAIT_PRESCALER. Note: If set to 00000h the tx_wait guard time is disabled Note: This bit is set by HW a protocol is detected in automatic mode detector. |

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|----------|--|
| 7:0 | TX_WAIT_PRESCALER | D | 0* - FFh | Defines the prescaler reload value for the tx_wait timer. Note: This bit is set by HW a protocol is detected in automatic mode detector. For correct DPC operation, it is required to set the prescaler to 0x7F For type A communication, the prescaler has to be set to 0x7F as well. |

Table 98. TX_CONFIG register (address 0018h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|---------------------------|--------|-------|---|
| 31:14 | RFU | R | 0 | Reserved |
| 13 | TX_PARITY_LAST_INV_ENABLE | R/W | 0 | If set to 1; the parity bit of last sent data byte is inverted |
| 12 | TX_PARITY_TYPE | R/W | 0 | Defines the type of the parity bit 0 Even Parity is calculated 1 Odd parity is calculated |
| 11 | TX_PARITY_ENABLE | R/W | 0 | If set to 1; a parity bit is calculated and appended to each byte transmitted. If the Transmission Of Data Is Enabled and TX_NUM_BYTES_2_SEND is zero; then a NO_DATA_ERROR occurs. |
| 10 | TX_DATA_ENABLE | R/W | 0 | If set to 1; transmission of data is enabled otherwise only symbols are transmitted. |
| 9:8 | TX_STOP_SYMBOL | R/W | 0 | Defines which pattern symbol is sent as frame stop-symbol 00b No symbol is sent 01b Symbol1 is sent 10b Symbol2 is sent 11b Symbol3 is sent |
| 7:6 | TX_START_SYMBOL | R/W | 0 | Defines which symbol pattern is sent as frame start-symbol 00b No symbol pattern is sent 01b Symbol0 is sent 10b Symbol1 is sent 11b Symbol2 is sent. |
| 5:3 | TX_LAST_BITS | R/W | 0 | Defines how many bits of the last data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the end of the byte |
| 2:0 | TX_FIRST_BITS | R/W | 0 | Defines how many bits of the first data byte to be sent. If set to 000b all bits of the last data byte are sent. Note: Bits are skipped at the beginning of the byte |

Table 99. CRC_TX_CONFIG (address 0019h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|---------------------|--------|----------|---|
| 31:16 | TX_CRC_PRESET_VALUE | R/W | 0*-FFFFh | Arbitrary preset value for the Tx-Encoder CRC calculation. |
| 15:7 | RFU | R | 0 | Reserved |
| 6 | TX_CRC_BYTE2_ENABLE | R/W | 0 | If set; the CRC is calculated from the second byte onwards (intended for HID). This option is used in the Tx-Encoder. |

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|----------|--|
| 5:3 | TX_CRC_PRESET_SEL | R/W | 000-101b | Preset values of the CRC register for the Tx-Encoder. For a CRC calculation using 5 bits, only the LSByte is used. |
| | | | 000b* | 0000h, reset value |
| | | | 001b | 6363h |
| | | | 010b | A671h |
| | | | 011b | FFFFh |
| | | | 100b | 0012h |
| | | | 101b | E012h |
| | | | 111b | Use arbitrary preset value TX_CRC_PRESET_VALUE |
| 2 | TX_CRC_TYPE | R/W | 0, 1 | Controls the type of CRC calculation for the Tx-Encoder |
| | | | 0* | 16-bit CRC calculation, reset value |
| | | | 1 | 5-bit CRC calculation |
| 1 | TX_CRC_INV | R/W | 0, 1 | Controls the sending of an inverted CRC value by the Tx-Encoder |
| | | | 0* | Not inverted CRC checksum, reset value |
| | | | 1 | Inverted CRC checksum |
| 0 | TX_CRC_ENABLE | R/W | 0*, 1 | If set to one, the Tx-Encoder computes and transmits a CRC. |

Table 100. SIGPRO_CONFIG register (address 001Ah) bit description

| Bit | Symbol | Access | Value | Description |
|------|----------|--------|----------|---|
| 31:2 | RFU | R | 0 | Reserved |
| 2:0 | BAUDRATE | D | 000*-111 | Defines the baud rate of the receiving signal. The MSB is only relevant for reader mode. Note: These bits are set by the mode-detector if automatic mode detector is enabled and the communication mode is detected. |
| | | | 000* | Reserved |
| | | | 001 | Reserved |
| | | | 010 | Reserved |
| | | | 011 | Reserved |
| | | | 100 | 106 kBd This configuration is set by the Mode detector for ISO/IEC14443 type A and B. |
| | | | 101 | 212 kBd This configuration is set by the Mode detector for FeliCa 212 kBd. |
| | | | 110 | 424 kBd This configuration is set by the Mode detector for FeliCa 424 kBd. |

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|-------------|
| | | | 111 | 848 kBd |

Table 101. SIGPRO_CM_CONFIG register (address 001Bh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|---------------------|--------|-------|---|
| 31 | RFU | R | 0 | Reserved |
| 30:29 | RX_FRAMING | | | Defines the framing in card mode. These bits are set by the Mode detector if automatic mode detection is enabled and the communication mode is detected. 00b: ISO/IEC 14443 type A 01b: ISO/IEC 18092 (NFC - with Sync-byte 0xF0) |
| 28:26 | EDGE_DETECT_TAP_SEL | | | Selects the number of taps of the edge-detector filter. 000b: Edge detector filter with 4 taps 001b: Edge detector filter with 6 taps 010b: Edge detector filter with 8 taps 011b: Edge detector filter with 8 taps 100b: Edge detector filter with 16 taps 101b: Edge detector filter with 18 taps 110b: Edge detector filter with 24 taps 111b: Edge detector filter with 32 taps |
| 25:13 | EDGE_DETECT_TH | | | Threshold for the edge decision block of the ADCBCM. |
| 12:0 | BIT_DETECT_TH | | | Threshold for the "bit" decision block of the ADCBCM. |

Table 102. SIGPRO_RM_CONFIG register (address 001Ch) bit description

| Bit | Symbol | Access | Value | Description |
|-------|---------------|--------|----------|--|
| 31:24 | RFU | R | 0 | Reserved |
| 23:21 | BPSK_IQ_MODE | R/W | 000*-111 | Defines signal processing of I- and Q-channel |
| | | | 000* | Both channels (I and Q) are used for signal processing |
| | | | 001 | Use only I channel |
| | | | 010 | Use only Q channel |
| | | | 011 | RFU |
| | | | 100 | Use the strongest channel |
| | | | 101 | Use the first channel |
| | | | 110-111 | RFU |
| 20 | BPSK_FILT6 | R/W | 0*-1 | Reserved for test |
| 19 | RESYNC_EQ_ON | R/W | 0-1* | Resynchronization during the SOF for an equal correlation value is done (default = activated). |
| 18 | CORR_RESET_ON | R/W | 0 | The correlator is reset at a reset (default = activated). |

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| Bit | Symbol | Access | Value | Description |
|-------|-----------------|--------|--------|--|
| 17 | VALID_FILT_OFF | R/W | 0*-1 | Disables a special filter in BPSK mode. If set to 0, the correlation of 0110 is filtered with the correlation of 1110 and 0111. Otherwise the demodulation is done using the correlation with 0110 |
| 16 | DATA_BEFORE_MIN | R/W | 0 | Data is received even before the first minimum at the SOF (default: = deactivated). |
| 15:12 | MIN_LEVEL | R/W | 0*-Fh | Defines the minimum level (threshold value) for the subcarrier detector unit. Note: The MinLevel should be higher than the noise level in the system. The values in the look-up table are not absolute values. The values for MIN_LEVEL vary +/- 3 (1 sign bit and 2 bits for value) to allow an increase/decrease of the actual lookup table value. Note: Used for BPSK and Manchester with Subcarrier communication types as MinLevel |
| 11:8 | MIN_LEVELP | R/W | 0*-Fh | Defines the minimum level (threshold value) for the phase-shift detector unit. Used for BPSK communication. The values in the look-up table are not absolute values. The values in the ARC look-up table (LUT) are not absolute, but relative values. The values for MIN_LEVELP in the ARC LUT can define a change (increase or decrease) of the actual register value of up to +/- 3 digits, using 1 sign bit (MSbit) and 2 bits for value. Note: Used for BPSK with Subcarrier communication types as MinLevel |
| 7 | USE_SMALL_EVAL | R | 0 | Defines the length of the evaluation period for the correlator for Manchester subcarrier communication types. |
| 6:5 | COLL_LEVEL | R/W | 00*-11 | Defines how strong a signal must be interpreted as a collision for Manchester subcarrier communication types. |
| | | | 00* | >12.5 % |
| | | | 01 | >25 % |
| | | | 10 | >50 % |
| | | | 11 | No Collision |
| 4 | PRE_FILTER | R/W | | If set to 1 four samples are combined to one data. (average) |
| 3 | RECT_FILTER | R/W | 0 | If set to one; the ADC-values are changed to a more rectangular waveshape. |
| 2 | SYNC_HIGH | R/W | 0*-1 | Defines if the bit grid is fixed at maximum (1) or at a minimum(0) value of the correlation. |
| 1 | FSK | R | 0 | If set to 1; the demodulation scheme is FSK. |
| 0 | BPSK | R/W | 0* | If set to 1, the demodulation scheme is BPSK. |

Table 103. RF_STATUS register (address 001Dh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------------|--------|---------|--|
| 31:27 | RFU | R | 0 | - |
| 26:24 | TRANSCEIVE_STATE | R | 0* | Holds the command bits 0* IDLE state 1 WaitTransmit state 2 Transmitting state 3 WaitReceive state 4 WaitForData state 5 Receiving state 6 LoopBack state 7 reserved |
| 23:20 | DPC_CURRENT_GEAR | R | 0* | Current Gear of the DPC |
| 19 | DPLL_ENABLE | R | 0* | This bit indicates that the DPLL Controller has enabled the DPLL (RF on, RF frequency ok, PLL locked) |
| 18 | CRC_OK | R | 0 | This bit indicates the status of the actual CRC calculation. If 1 the CRC is correct; meaning the CRC register has the value 0 or the residue value if inverted CRC is used. Note: This flag should only be evaluated at the end of a communication. |
| 17 | TX_RF_STATUS | R | 0 | If set to 1 this bit indicates that the drivers are turned on; meaning an RF-Field is created by the device itself. |
| 16 | RF_DET_STATUS | R | 0 | If set to 1 this bit indicates that an external RF-Field is detected by the RF-level detectors (after digital filtering) |
| 15:13 | RF_ACTIVE_ERROR_CAUSE | R | 0 - 5 | This status flag indicates the cause of an NFC-Active error. Note: These bits are only valid when the RF_ACTIVE_ERROR_IRQ is raised and is cleared as soon as the bit TX_RF_ENABLE is set to 1. |
| | | | 0* | No Error; reset value |
| | | | 1 | External field was detected on within TIDT timing |
| | | | 2 | External field was detected on within TADT timing |
| | | | 3 | No external field was detected within TADT timings |
| | | | 4 | Peer did switch off RF-Field but no Rx event was raised (no data received) |
| 5 - 7 | Reserved | | | |
| 12 | RX_ENABLE | | | This bit indicates if the RxDecoder is enabled. If 1 the RxDecoder was enabled by the Transceiver Unit and is now ready for data reception |
| 11 | TX_ACTIVE | | | This bit indicates activity of the TxEncoder. If 1 a transmission is ongoing, otherwise the TxEncoder is in idle state. |
| 10 | RX_ACTIVE | | | This bit indicates activity of the RxDecoder. If 1 a data reception is ongoing; otherwise the RxDecoder is in idle state. |
| 9:0 | AGC_VALUE | R | 0*-3FFh | Current value of the AGC |
| | | | 0h* | Most sensitive: largest Rx-resistor, i.e., none of the switchable resistors are added in parallel |

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|---|
| | | | 3FFh | Most robust: smallest Rx-resistor, i.e., all switchable resistors are added in parallel |

Table 104. AGC_CONFIG register (address 001Eh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--------------------|--------|-------|---|
| 31:16 | RFU | R | 0* | Reserved |
| 15:14 | AGC_VREF_SEL | R/W | 0* | Select the set value for the AGC control:_ 00b: 1.15 V 01b: 1.40 V 10b: 1.50 V 11b: RFU |
| 13:4 | AGC_TIME_CONSTANT | R/W | 0* | Time constant for the AGC update. An AGC period is given by (AGC_TIME_CONSTANT+1) * 13.56 MHz. The minimum allowed value for the AGC_TIME_CONSTANT is 4. |
| 3 | AGC_INPUT_SEL | R/W | 0* | Selects the AGC value to be loaded into the AGC and the data source for fix-mode operation: 0b: AGC_VALUE.AGC_CM_VALUE 1b: AGC_VALUE.AGC.RM_VALUE |
| 2 | AGC_LOAD | W | 0* | If set, the RX divider setting is loaded from AGC_VALUE. AGC_INPUT_SEL defines the source of the data. This bit is automatically cleared. |
| 1 | AGC_MODE_SEL | R/W | 0* | Selects the fix AGC value: 0b: Rx-divider is set according to AGC_VALUE dependent on bit AGC_INPUT_SEL 1b: The last RX divider setting before AGC control operation had been deactivated is used (AGC_ENABLE_CONTROL=0, last RX divider setting is frozen). This bit is not causing any loading of new Rx-divider data. Set the bit AGC_LOAD for updating the RX divider with a new value. |
| 0 | AGC_ENABLE_CONTROL | R/W | 0* | 0b: Fix mode operation. The RX divider is fixed to one value. The value is defined by AGC_MODE_SEL 1b: AGC control operation enabled |

Table 105. AGC_VALUE register (address 001Fh) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--------------|--------|-------|---------------------------------------|
| 31:20 | RFU | R | 0 | Reserved |
| 19:10 | AGC_RM_VALUE | R/W | 0 | Static AGC value used for reader mode |
| 0:9 | AGC_CM_VALUE | R/W | 0 | Static AGC value used for card mode |

Table 106. RF_CONTROL_TX register (address 0020h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------------------|--------|-------|---|
| 31:27 | RFU | R | 0 | Reserved |
| 26 | TX_ALM_TYPE_SELECT | R/W | 0* | 0 ... Both drivers used for ALM 1 ... Single driver used for ALM |
| 25:24 | TX_CW_AMPLITUDE_ALM_CM | R/W | 0* | set amplitude of unmodulated carrier at card mode |
| 23:19 | TX_RESIDUAL_CARRIER_OV_PREV | R/W | 0* | Defines the value for the residual carrier for the period the overshoot prevention pattern is active. |
| 18 | TX_CW_TO_MAX_ALM_CM | R/W | 0* | TX HI output is the maximum voltage obtainable from charge pump (CM setting); if set to 1 -> TX_CW_AMPLITUDE_CM is overruled. |
| 17:13 | TX_RESIDUAL_CARRIER | R/W | 0* | set residual carrier (0=100 %, 1F = 0 %) |
| 12 | TX_BYPASS_SC_SHAPING | R/W | 0* | Bypasses switched capacitor TX shaping of the Transmitter Signal and disables the shaping control for the rising edge. So this bit must be 0, if the TAU_MOD_RISING settings shall apply. The rising edge provides the fastest rise time, if TX_SET_BYPASS_SC_SHAPING = 1 (TAU_MOD_RISING does not matter). |
| 11:8 | TX_SLEW_SHUNTREG | R/W | 0* | Set slew rate for shunt regulator. Set slew rate for Tx Shaping shunt regulator (0= slowest slew rate, 0xF = fastest slew rate) for both the falling and rising edge. |
| 7:4 | TX_TAU_MOD_FALLING | R/W | 0* | Transmitter TAU setting for falling edge of modulation shape. In AnalogControl module, the output signal is switched with the tx_envelope. Only valid is TX_SINGLE_CP_MODE is set |
| 3:0 | TX_TAU_MOD_RISING | R/W | 0* | Transmitter TAU setting for rising edge of modulation shape. In Analog Control module, the output signal is switched with the tx_envelope. Only valid is TX_SINGLE_CP_MODE is set |

Table 107. RF_CONTROL_TX_CLK register (address 0021h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------------------|--------|-------|--|
| 31:19 | RFU | R | 0* | Reserved |
| 18 | TX_ALM_ENABLE | R/W | 0* | If set to 1 ALM (active load modulation) is used for transmission in card mode |
| 17:14 | RFU | R | | RFU |
| 13:11 | DPLL_CLOCK_CONFIG_ALM | R/W | 0* | Configures the phase difference in integer multiples of 45° steps between the recovered and the transmitted RF clock |
| 10:8 | TX_CLK_MODE_OVUN_PREV | R/W | 0* | Defines the TX clock mode for the period the overshoot/undershoot prevention is active |
| 7 | TX2_INV_RM | R/W | 0* | If 1 -> TX2 output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used, this setting is active in reader mode only |

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|--|
| 6 | TX2_INV_CM | R/W | 0* | If 1 -> TX2 output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used, this setting is active in card emulation mode only |
| 5 | TX1_INV_RM | R/W | 0* | If 1 -> TX1 output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used, this setting is active in reader mode only |
| 4 | TX1_INV_CM | R/W | 0* | If 1 -> TX1 output is inverted (clk_13m56_n is used); 0 -> clk_13m56 is used, this setting is active in card emulation mode only |
| 3:1 | TX_CLK_MODE_RM | R/W | 0* | TX clock mode: Allows to configure the transmitter for 1. High impedance (RF-OFF) 2. RF high side push 3. RF low side pull 4. 13.56 MHz clock derived from 27.12 MHz quartz divided by 2. See table 68: Settings for TX1 and TX2 |
| 0 | CLOCK_ENABLE_DPLL | R/W | 0* | Enables the DPLL |

Table 108. RF_CONTROL_RX register (address 0022h) bit description

| Bit | Symbol | Access | Value | Description |
|------|------------------|--------|--------|--|
| 31:8 | RFU | R | 0* | Reserved |
| 7:6 | CM_MILLER_SENS | R/W | | Configuration bits for reference level of Miller demodulator |
| 5:4 | RX_MIXER_CONTROL | R/W | | Mixer Control Enable 00, 11 ... power down both mixer 01... reader mode mixer 10... card mode mixer, |
| 3:2 | RX_HPCF | R/W | | High Pass Corner Frequency: 00->45 kHz, 01-> 85 kHz, 10->150 kHz, 11->250 kHz |
| 1:0 | RX_GAIN | R/W | 0h*-3h | Gain Adjustment BBA: 00->33 dB, 01->40 dB, 10-> 50 dB, 11->57 dB |

Table 109. LD_CONTROL register (address 0023h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|------------------|--------|-------|---|
| 31:15 | RFU | R | 0* | Reserved |
| 14 | CM_PD_NFC_DET | R/W | 0* | Power Down NFC level detector |
| 13:12 | RFDET_SOURCE_SEL | R/W | 0* | Selects the source for RF-Field detection; 0* -> NFC-Level detector indication signal is used; 1 -> RF-Level detector indication signal is used 2; -> NFC- and RF-Level detector indication signal is used 3; -> Override - RF-Field detected is emulated |
| 11:8 | CM_RFL_NFC | R/W | 0* | Programming of detection level |
| 7:4 | RFLD_REF_LO | R/W | 0* | Higher Reference Value for RF Level Detector |
| 3:0 | RFLD_REF_HI | R/W | 0* | Lower Reference Value for RF Level Detector |

Table 110. SYSTEM_STATUS register (address 0024h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-------------------|--------|-------|---|
| 31:10 | RFU | R | 0 | Reserved |
| 9 | LDO_TVDD_OK | R | 0* | If set, bit indicates that LDO voltage is available on output pin LDO_OUT |
| 8 | PARAMETER_ERROR | R | 0* | Parameter Error on Host Communication |
| 7 | SYNTAX_ERROR | R | 0* | Syntax Error on Host Communication |
| 6 | SEMANTIC_ERROR | R | 0* | Semantic Error on Host Communication |
| 5 | STBY_PREVENT_RFLD | R | 0* | Entry of STBY mode prevented due to existing RFLD |
| 4 | BOOT_TEMP | R | 0* | Boot Reason Temp Sensor |
| 3 | BOOT_SOFT_RESET | R | 0* | Boot Reason due to SOFT RESET |
| 2 | BOOT_WUC | R | 0* | Boot Reason wake-up Counter |
| 1 | BOOT_RFLD | R | 0* | Boot Reason RF Level Detector |
| 0 | BOOT_POR | R | 0* | Boot Reason "Power on" or pin RESET_N set to HIGH |

Table 111. TEMP_CONTROL register (address 0025h) bit description

| Bit | Symbol | Access | Value | Description |
|------|------------------|--------|-------|--|
| 31:4 | RFU | R | 0 | Reserved |
| 3 | TEMP_ENABLE_HYST | R/W | 0* | Enable hystereses of Temperature Sensor |
| 2 | TEMP_ENABLE | R/W | 0* | Enable Temp Sensor |
| 0:1 | TEMP_DELTA | R/W | 0* | selects temperature value: <ul style="list-style-type: none"> • 00b: 85 deg • 01b: 115 deg • 10b: 125 deg • 11b: 135 deg |

Table 112. AGC_REF_CONFIG register (address 0026h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|-----------|--------|-------|--|
| 31:14 | RFU | R | 0 | RFU |
| 13:10 | AGC_GEAR | R/W | 0 | Gear number used during LPCD Self-Calibration. Either written by the use or derived from an automatic DPC cycle during reading of this register |
| 9:0 | AGC_VALUE | R/W | 0 | AGC reference value used during the LPCD self-calibration. This value is derived automatically when reading or writing this register. Writing data to these bits has no functional effect. |

Reading from this register:

Reading from this register - without prior writing - starts an LPCD calibration. The calibration is executed using the gear which is resulting from the actual DPC setting

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under the actual antenna detuning condition. AGC_GEAR is used in the LPCD self-calibration.

Reading from this register - without prior writing - delivers in addition to the AGC_GEAR value the AGC_VALUE. The AGC_VALUE is used in the LPCD self-calibration.

Writing to this register:

Writing data to this register defines the values for AGC_GEAR without taking the actual detuning condition into account. The value of AGC_GEAR to perform an LPCD calibration which derives the AGC_VALUE. This AGC_VALUE and the AGC_GEAR are used in the LPCD self-calibration.

Table 113. DPC_CONFIG register (address 0027h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--------------------|--------|-------|--|
| 31:20 | | RFU | R | 0 |
| 19:16 | TX_GSN_CW_CM | R/W | 0 | GSN value for continuous wave in Card Mode |
| 15:12 | TX_GSN_MOD_CM | R/W | 0 | GSN value for modulation in Card Mode |
| 11:8 | TX_GSN_MOD_RM | R/W | 0 | GSN value for modulation in Reader Mode |
| 7:4 | TX_GSN_CW_RM | R/W | 0 | GSN value for continuous wave in Reader Mode |
| 3 | TX_CW_TO_MAX_RM | R/W | 0 | Maximum output voltage on TX driver |
| 2:1 | TX_CW_AMPLITUDE_RM | R/W | 0 | set amplitude of unmodulated carrier at reader mode |
| 0 | TX_CW_AMP_REF2TVDD | RW | 0 | If set to 1 the reference of the unmodulated carrier is defined relative to TVDD |

Table 114. EMD_CONTROL register (address 0028h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--|--------|-------|--|
| 31:10 | RFU | R | 0 | Reserved |
| 9:8 | EMD_TRANSMISSION_TIMER_USED | R/W | 0 | Timer used for RF communication. 00 Timer0, 01 Timer1, 10 Timer 2, 11 RFU |
| 7 | EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_B | R/W | 0 | RFU |
| 6 | EMD_MISSING_CRC_IS_PROTOCOL_ERROR_TYPE_A | R/W | 0 | RFU |
| 5:2 | EMD_NOISE_BYTES_THRESHOLD | R/W | 0 | Defines the threshold under which transmission errors are treated as noise. Note: CRC bytes are NOT included/counted! |
| 1 | EMD_TRANSMISSION_ERROR_ABOVE_NOISE_THRESHOLD_IS_NO_EMD | R/W | 0 | Transmission errors with received byte length >= EMD_NOISE_BYTES_THRESHOLD is never treated as EMD (EMVCo 2.5 standard). All transmission with number of received bytes < 4 bytes are treated as EMD noise (ignored). For transmission errors >= 4 bytes the host is notified. |
| 0 | EMD_ENABLE | R/W | 0 | Enable EMD handling |

Recommended EMD_CONTROL register value for EMVCo 2.6 compliancy; 0x187

Recommended timer for all EMVCo compliant EMD error handlings: Timer 1

Table 115. ANT_CONTROL register (address 0029h) bit description

| Bit | Symbol | Access | Value | Description |
|------|----------------------------|--------|-------|--|
| 31:8 | RFU | R | 0 | Reserved |
| 7 | ANT_INVERT_ON_TXACTIVE | R/W | 0 | If set to 1, the ANT short interface in card mode is inverted when tx_active is asserted (i.e. while transmission). Note: this bit is only valid in card mode. Note: if it ANT_ALM_AUTO_SWITCH_ENABLE is set this setting is ignored |
| 6 | ANT_ALM_AUTO_SWITCH_ENABLE | R/W | 0 | If set to 1, the ANT setting for ALM is switched automatically by HW. By default for ALM the ANT_short and ANT_mod uses the same settings as for PLM. |
| 5 | ANT_ALM_FW_RESET | R/W | 0 | If set to 1 the ANT setting for ALM is reset to its initial receive configuration |
| 4 | ANT_SHORT_SELECT_RM | R/W | 0 | Selects the control of the ANT modulation interface in reader mode |
| 3:2 | ANT_SHORT_SELECT | R/W | 0 | Selects the control of the ANT short interface in card mode for PLM; in reader mode and ALM the analog control signals are switched by digital logic. 00b Constant 0 (ANT open) 01b Constant 1 (ANT short) 10b TxEnvelope used (idle = 1, modulation = 0) 11b Inverted TxEnvelope used (idle = 0, modulation = 1) |
| 1:0 | ANT_MOD_SELECT | R/W | 0 | Selects the control of the ANT modulation interface in card mode for PLM; in reader mode and ALM the analog control signals are switched by digital logic. 00b Constant 0 (No modulation on ANT mod) 01b Constant 1 (modulation on ANT mod) 10b TxEnvelope used (idle = 1, modulation = 0) 11b Inverted TxEnvelope used (idle = 0, modulation = 1) |

Table 116. TX_CONTROL register (address 0036h) bit description

| Bit | Symbol | Access | Value | Description |
|------|--------------------|--------|-------|---|
| 31:2 | RFU | RW | 0 | - |
| 1 | TX_CM_GSN_TXACTIVE | RW | 0 | If set, CM GSN value is switched with tx_active instead of envelope |
| 0 | TX_INVERT | RW | 0 | If this bit is set, the resulting signal is inverted |

Table 117. SIGPRO_RM_CONFIG_EXTENSION register (address 0039h) bit description

| Bit | Symbol | Access | Value | Description |
|-------|--------------|--------|-------|--|
| 31:16 | SYNC_VAL | R/W | 0* | Defines the Sync Pattern; which is expected to be sent as preamble before the actual data. |
| 15:12 | SYNC_LEN | R/W | 0* | Defines how many Bits of Sync_Val are valid. Example: 0 configures 1 Bit to be valid. |
| 11 | SYNC_NEGEDGE | R/W | 0* | Defines a SOF with no min or max in correlation. The bit grid will be defined by the negative edge (EPC; UID). |

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|-------|--|
| 10 | LAST_SYNC_HALF | R/W | 0* | The last Bit of the Sync code has only half of the length compared to all other bits (EPC V2). |
| 9:8 | SYNC_TYPE | R/W | 0* | Set to 0 all 16 bits of SyncVal are interpreted as bits. Set to 1 a nippel of bits is interpreted as one bit in following way:{data; coll} data=zero or one; coll=1 means a collision on this bit. Note: if Coll=1 the vale of data is ignored. Set to 2 the synchronization is done at every start bit of each byte (TypeB) |
| 7:0 | RFU | R/W | 0* | - |

Sync pattern is fixed to B24D and it is configurable via the SIGPRO_RM_CONFIG_EXTENSION, bits 16:31 (16 bits).

At LoadRfConfig for FeliCa Reader (212 / 424 kbit/s), the value SYNC_VAL is set to 0xB24D. This value can be modified by writing to the bit field Sync_Val (16:31). This is required after each LoadRfConfig command. SYNC_LEN = 0xF (1111b).

Table 118. FELICA_EMD_CONTROL register (address 0043h) bit description (only available from firmware V4.1 onwards)

| Bit | Symbol | Access | Value | Description |
|-------|---------------------------------------|--------|--------|--|
| 31:24 | FELICA_EMD_RC_BYTE_VALUE | R/W | 00*-FF | Response Code (RC) byte definition of the FeliCa response frame. All received data, which does not start with the RC, is treated as EMD, if the FELICA_EMD_RC_CHECK_ENABLE is set. |
| 23:16 | FELICA_EMD_LENGTH_BYTE_MAX | R/W | 00*-FF | Maximum allowed length of FeliCa response. The received length byte of the FeliCa response must indicate a length (length byte info) which is less or equal to FELICA_EMD_LENGTH_BYTE_MAX. Otherwise the received data is treated as EMD, if the FELICA_EMD_LEN_CHECK_ENABLE is set. |
| 15:8 | FELICA_EMD_LENGTH_BYTE_MIN | R/W | 00*-FF | Minimum allowed length of FeliCa response. The received length byte of the FeliCa response must indicate a length (length byte info) which is greater or equal to FELICA_EMD_LENGTHBYTE_MIN. Otherwise the received data is treated as EMD, if the FELICA_EMD_LEN_CHECK_ENABLE is set. |
| 7:5 | RFU | R/W | 000* | RFU, must be 000b |
| 4 | FELICA_EMD_INTEGRITY_ERR_CHECK_ENABLE | R/W | 0*,1 | Enable FeliCa EMD integrity error check. If set, a response with integrity error is treated as EMD. |
| 3 | FELICA_EMD_PROTOCOL_ERR_CHECK_ENABLE | R/W | 0*,1 | Enable FeliCa EMD protocol error check. If set, a response with protocol error is treated as EMD. |
| 2 | FELICA_EMD_RC_CHECK_ENABLE | R/W | 0*,1 | Enable RC check. If set, the Response Code (RC) of the received data is checked. If not set, any RC is accepted. This bit has only an effect, if FELICA_EMD_ENABLE is set. |

| Bit | Symbol | Access | Value | Description |
|-----|-----------------------------|--------|-------|---|
| 1 | FELICA_EMD_LEN_CHECK_ENABLE | R/W | 0*, 1 | Enable length check. If set, the length byte of the received data is checked. If not set, any length is accepted. This bit has only an effect, if FELICA_EMD_ENABLE is set. |
| 0 | FELICA_EMD_ENABLE | R/W | 0*, 1 | Enable FeliCa EMD handling. If not set, all other settings in the FELICA_EMD_CONTROL register are ignored. |

Reset value of the FELICA_EMD_CONTROL register is 00000000h. For best FeliCa performance, it is recommended to initialize this register in FeliCa reader mode with a value of 00FF0019h.

12 Secure Firmware Update

12.1 General functionality

The PN5180 supports a secure update of the implemented firmware. The secure firmware download mode is using a dedicated command set and framing which is different from the standard host interface commands used for NFC operation of the device.

In Secure Firmware update mode, the PN5180 requires a dedicated physical handling of the SPI interface lines and the BUSY line.

The secure firmware download mode is entered by setting the DWL_REQ pin to high during startup of the device. This pin can be used for any other functionality after startup, the level of this pin has no impact on the download functionality after startup during standard NFC operation.

The firmware binary file which is used to update the PN5180 is protected with a signature. This prevents a download of any other software which is not signed by NXP.

An anti-tearing function is implemented in order to detect supply voltage removal or memory fault.

During the secure firmware download, the normal mode NFC operation is not available and only the command set defined for the secure firmware download is valid.

In case of any failure or exception during the download, the PN5180 remains in the secure firmware download mode until a full firmware update sequence has been performed successfully.

Updating the firmware of the PN5180 programs the memories for user EEPROM and RF configuration with default values. Any previous user configuration will be overwritten. The user has to take care to restore the data of these memories after a secure firmware update.

The PN5180 can be used for firmware update as follows:

1. Set DWL_REQ pin to high
2. Reset
3. The PN1580 boots in download mode
4. Download new firmware version
5. Execute the check integrity command to verify the successful update (The CheckIntegrity command cannot be called while a download session is open)
6. Reset the PN5180
7. The device starts in NFC operation mode

12.1.1 Physical Host Interface during Secure Firmware Download

In Secure Firmware update mode, the PN5180 is using a different physical host interface signaling than in NFC operation mode.

The BUSY line is used in a different way than for NFC operation mode, and the data is packed in frames protected by a CRC16 checksum.

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In Secure Firmware Download mode, the single frame read as well as the split frame read (split read can be multiple SPI frames - meaning multiple NSS assertions & deassertions) is supported.

SPI write is always a single frame as the length is composed by the host and known to the host.

SPI read can be single frame or multiple (split) frames:

- single frame read, if the length is already known to the host
- split frame read, if the length is not known to the host.

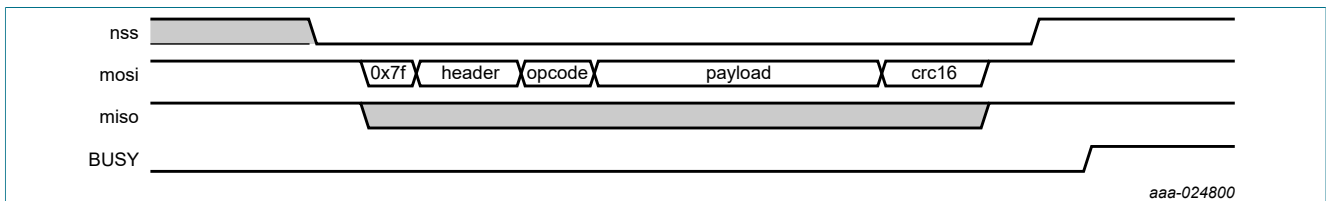


Figure 41. Example SPI WRITE data send in single frame (single NSS assertion/deassertion)

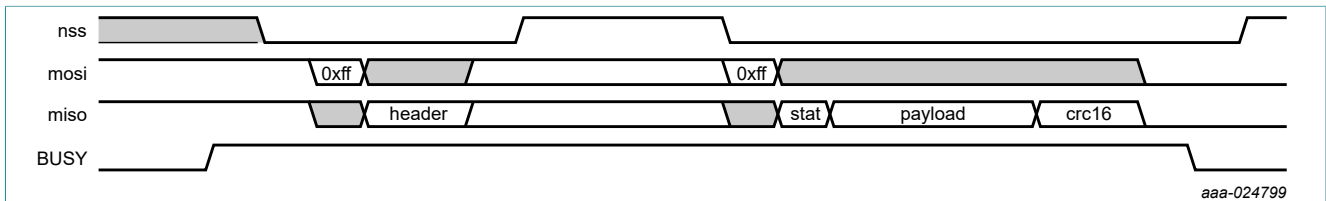


Figure 42. Example SPI READ data retrieved in two frames (two NSS assertion/deassertions)

A complete frame transmitted in Secure Firmware Update mode consists of

For the WRITE:

1. 1 byte direction (0x7F)
2. 2 byte header (chunk bit + length of (Payload + command))
3. 1 byte command
4. (LENGTH-1) byte payload (the LENGTH in the header includes the 1 byte command, therefore the length of the payload needs to be reduced by 1)
5. 2 byte CRC16 (is not included in the header length number)

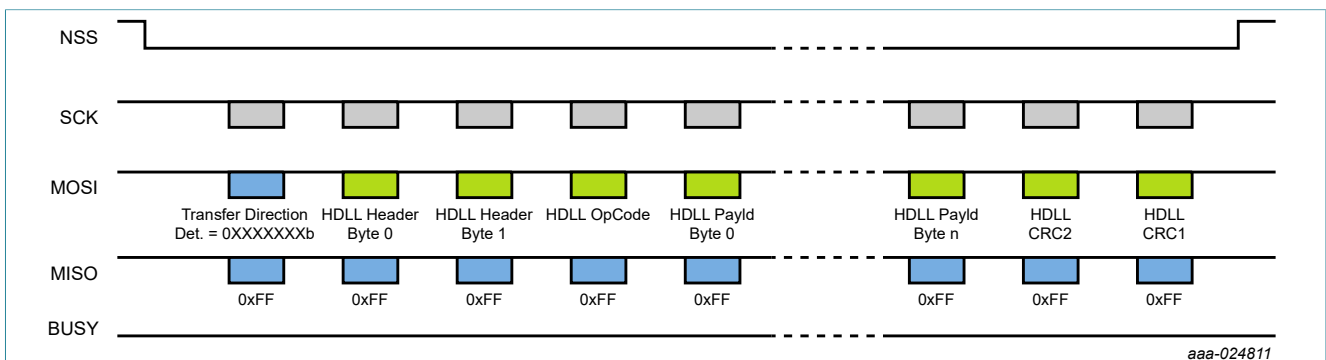


Figure 43. Secure Firmware Download: SPI Write (byte level information)

For the READ:

1. 1 byte direction (0xFF)
2. 2 byte header (chunk bit + length of (Payload + status))
3. 1 byte status
4. (LENGTH-1) byte payload (the LENGTH in the header includes the 1 byte status, therefore the length of the payload needs to be reduced by 1)
5. 2 byte CRC16 (is not included in the header length number)

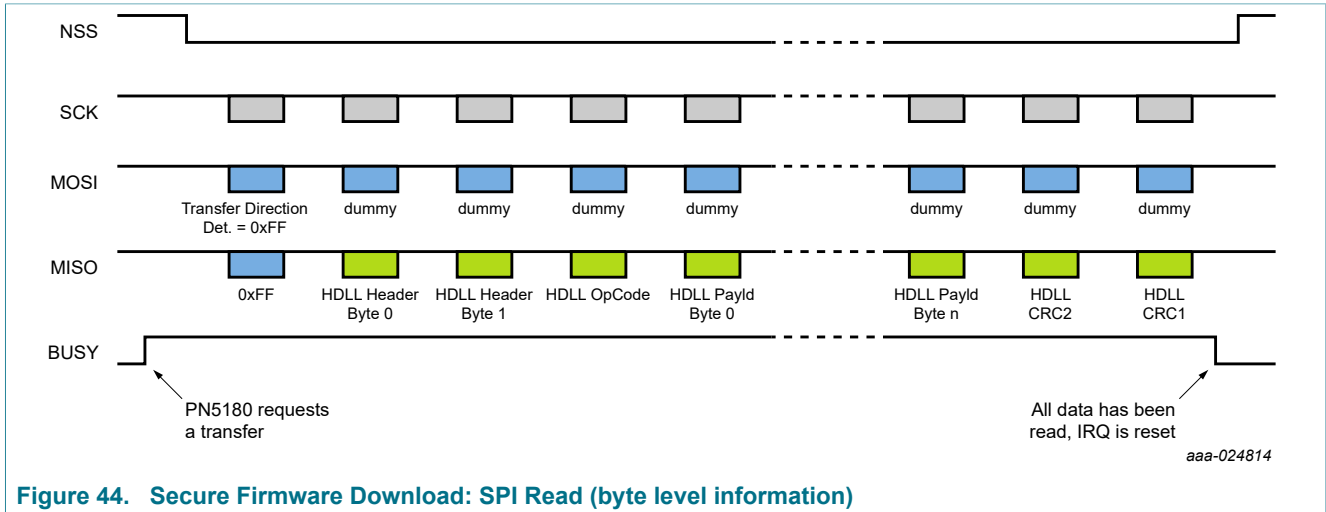


Figure 44. Secure Firmware Download: SPI Read (byte level information)

12.2 Download Protection

Data of the PN5180 like firmware version numbers, are protected against any tearing attempt.

The PN5180 uses a chained hash approach having the first command hash protected with an RSA signature. The chained hash sequence binds each frame with the next one comparable to an S/KEY mechanism. Hence authenticity of the downloaded code can be ensured due to secrecy of the RSA private key. Any firmware which is not issued and signed by NXP, is rejected by the security system of the PN5180 and cannot be loaded into the memory of the device.

The security system of the PN5180 assures that no firmware data can be overwritten without verifying the authenticity and integrity of the new data beforehand.

During the secure firmware download, a new firmware version number is sent. The firmware version number is composed of a major and a minor number:

1. Major number: 8 bit (MSB)
2. Minor number: 8 bit (LSB)

The PN5180 checks if the new major version number is equal or higher than the current one. In case the current major version number is larger than the already installed version number of the firmware, the secure firmware update is rejected. Downgrading major firmware versions is therefore not possible.

An integrity check command is available which can be executed by the host immediately after a firmware update to check if the update had been successful.

The major and minor firmware version numbers can be read out at any time using the host interface and commands in NFC mode to identify exactly which firmware is installed

on a dedicated hardware. It is not required to enter the secure firmware download mode to retrieve this firmware version information.

An already started firmware download may be interrupted for any of the following reasons:

- Reset (hard or soft)
- Failure of the Signature verification of the first secure write command
- Hash chain is broken during the download between two consecutive secure write commands
- Protocol error in framing
- Address mismatch
- critical memory failure

The PN5180 provides comprehensive mechanisms to recover from all these conditions.

12.3 Commands

12.3.1 Frame format

All messages transmitted between the host and the PN5180 always have the following frame format: Header - Frame - CRC

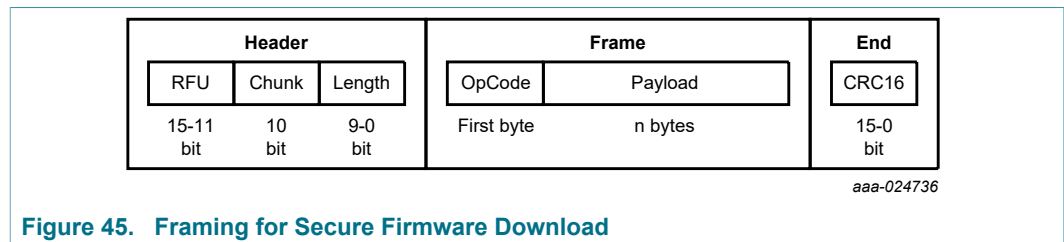


Figure 45. Framing for Secure Firmware Download

Header (2 bytes)

- RFU (bit 11..15)
- Chunk flag used for fragmentation (bit 10)
- length of the frame (bit 0..9 bit)

Frame ((n+1) byte)

- Command (1 byte)
- Payload of the command: (n-byte)

CRC (2 bytes)

- The CRC16 is compliant to X.25 (CRC-CCITT, ISO/IEC13239) standard with polynomial $x^{16} + x^{12} + x^5 + 1$ and preload value 0xFFFF.

The payload of one command consists of

- Memory block address: 3 bytes Memory block size: 2 bytes
- Memory data block: 512 bytes maximum
- Hash of the next frame: 32 bytes

The first write command used for a secure firmware download includes the version number, and a hash value over the following command and the RSA signature. Every

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following command includes the actual data block to be updated and the hash value over the following command and data. The last command does not contain any hash value.

The Payload including command can be split into chunks which allows the transfer of large payloads.



Figure 46. Splitting commands by chunks

12.3.2 Command Code Overview

The following commands are supported in Secure Firmware Download Mode

Table 119. Secure Firmware Download Commands

| Command | Command code (hex) | Description |
|--------------|--------------------|---|
| RESET | F0 | This command resets the IC |
| GET_VERSION | F1 | This command provides the IC version and firmware version |
| SECURE_WRITE | C0 | Writes chunks of data to the IC |
| GET_DIE_ID | F4 | The command returns the die Identifier |
| - | all other | RFU |

The Firmware Download Mode uses a data structure which consists of header (indicating the packet length), frame (opcode/command-code and payload) and end (CRC16). Refer to the related application note for a description how the firmware update files for new firmware versions (*.SFwu binary files) are internally organized and how to use the secure firmware download commands for downloading of the *.SFwu data to the PN5180.

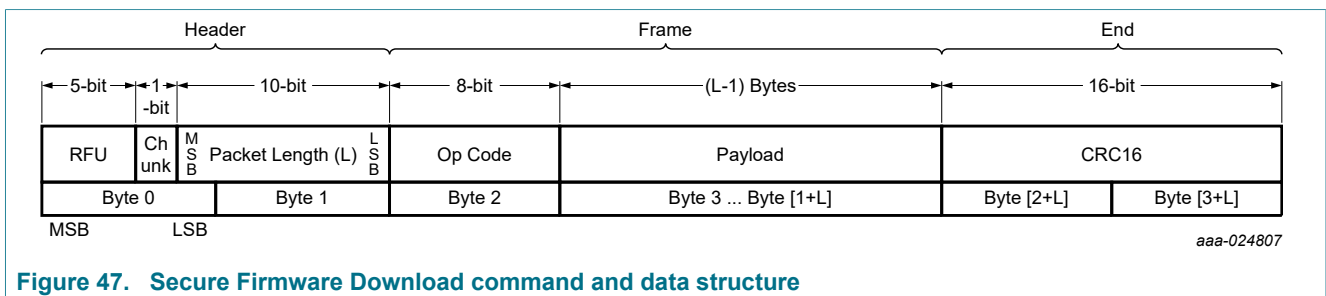


Figure 47. Secure Firmware Download command and data structure

12.3.3 Command Code Response

A response message is always a multiple of 4 bytes. The first byte of the response is used to indicate the status of the last executed command.

Table 120. Secure Firmware Command Status Return Codes

| Command | Command code (hex) | Description |
|---------|--------------------|---|
| OK | 00 | command processed properly |
| ERROR | 01-FF | any response different from 0x00 indicates an error |

12.3.4 Command Code Description

12.3.4.1 RESET

Command code: 0xF0

Frame format exchange:

Host -> PN5180 [0x00 0x04 0xF0 0x00 0x00 0x00 0x18 0x5B]

Host <- PN5180 [0x00 0x04 STAT 0x00 0x00 0x00 CRC16]

The reset prevents the PN5180 from sending the OK return code. Only error codes are sent. STAT is the status return code.

12.3.4.2 GET_VERSION

Command code: 0xF1

Frame format exchange:

Host -> PN5180 [0x00 0x04 0xF1 0x00 0x00 0x00 0x6E 0xEF]

Host <- PN5180 [0x00 0x0A STAT MD FM1V FM2V CRC16]

The payload of the GetVersion command response is:

Table 121. Secure Firmware update: GetVersion command response

| Field | size (Byte) | Description |
|-------|-------------|------------------------|
| STAT | 1 | Status return code |
| MD | 6 | Manufacturer Data |
| FM1V | 1 | Firmware major version |
| FM2V | 1 | Firmware minor version |

12.3.4.3 SECURE_WRITE

Command code: 0xC0

The secure write function differs between first, middle and last write frames.

To ease the usage of the download, the Firmware binaries provided by NXP are already prepared in such a way that only the CRC16 needs to be added. All other data can be packed in the Frames without further need of, e.g., HASH calculations. The provided binaries include the command code as well. The first 3 bytes of each data block to be

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transferred always contain the 2-byte length information and the one-byte command code 0xC0

Host -> PN5180 [Data **CRC16**]

Host <- PN5180 [0x00 0x04 STAT 0x00 0x00 0x00 CRC16]

Table 122. Secure Firmware update: First Secure Write Command response

| Field | size (Byte) | Description |
|-------|-------------|--------------------|
| STAT | 1 | Status return code |

12.3.4.4 GET_DIE_ID

Command code: 0xF4

This command returns the die Identifier (Unique chip serial number):

Host -> PN5180 [0x00 0x04 0xF4 0x00 0x00 0x00 0xD2 0xAA]

Host <- PN5180 [0x00 0x14 STAT 0x00 0x00 0x00 ID0 ID2 ID3 ID4 ID5 ID6 ID7 ID8 ID9 ID10 ID11 ID12 ID13 ID14 ID15 ID16 CRC16]

12.3.5 Error handling

If the last firmware download was not completed without error, the PN5180 responds to all commands with an answer 0x2A. No additional parameters are transmitted. In this error case, a new firmware download is required.

13 Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device.

Table 123. Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|---------------------------------|---|-----|------|--------------------|
| $V_{DD(PVDD)}$ | supply voltage on pin PVDD | - | - | 3.6 | V |
| $V_{DD(TVDD)}$ | supply voltage on pin TVDD | - | - | 5.5 | V |
| V_{ESD} | electrostatic discharge voltage | Human Body Model (HBM); 1500 Ω , 100 pF; ANSI/ESDA/ JEDEC JS-001 | - | 1500 | V |
| T_{stg} | storage temperature | no supply voltage applied | -55 | +150 | $^{\circ}\text{C}$ |
| P_{tot} | total power dissipation | in still air with exposed pins soldered on a 4 layer JEDEC PCB | - | 1125 | mW |
| $I_{DD(TVDD)}$ | supply current on pin TVDD | | - | 300 | mA |
| $I_{OUT(LDO_OUT)}$ | output current of pin LDO_OUT | $V_{(OUT)LDO_OUT}=3.3\text{ V}$, $I_{DD(TVDD)}$ = 250 mA | 0.0 | 100 | mA |
| T_j | junction temperature | - | - | 150 | $^{\circ}\text{C}$ |

14 Recommended operating conditions

Exposure of the device to other conditions than specified in the recommended operating conditions section for extended periods may affect device reliability.

Electrical parameters (minimum, typical and maximum) of the device are guaranteed only when it is used within the recommended operating conditions.

Table 124. Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------|--|------|-----|------|------|
| $V_{DD(VBAT)}$ | supply voltage on pin VBAT | - | 2.7 | 3.3 | 5.5 | V |
| $V_{DD(PVDD)}$ | supply voltage on pin PVDD | 1.8 V supply | 1.65 | 1.8 | 1.95 | V |
| | | 3.3 V supply | 2.7 | 3.3 | 3.6 | V |
| $V_{DD(TVDD)}$ | supply voltage on pin TVDD | - | 2.7 | 5.0 | 5.5 | V |
| $I_{DD(TVDD)}$ | supply current on pin TVDD | in still air with exposed pins soldered on a 4 layer JEDEC PCB | - | 180 | 250 | mA |
| $V_{OUT(LDO_OUT)}$ | output voltage of pin LDO_OUT | $I_{(OUT)LDO_OUT} = 0...100mA$ | 3.2 | 3.3 | 3.6 | V |
| T_{amb} | ambient temperature | in still air with exposed pins soldered on a 4 layer JEDEC PCB | -30 | +25 | +85 | °C |

The system design shall consider that maximum supply voltages are not exceeded during power-on of the system.

15 Thermal characteristics

Table 125. Thermal characteristics HVQFN40 package

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|---|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air with exposed pad soldered on a 4 layer JEDEC PCB, package HVQFN40 | 40 | K/W |

Table 126. Thermal characteristics TFBGA64 package

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|---|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air with exposed pad soldered on a 4 layer JEDEC PCB, package HVQFN40 | 66 | K/W |

Table 127. Junction Temperature

| Symbol | Parameter | Conditions | Max | Unit |
|--------|----------------------|------------|-----|------|
| T_j | junction temperature | - | 125 | °C |

16 Characteristics

Table 128. Current consumption

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|----------------------------|---|-----|-----|-----|---------------|
| $I_{DD(PVDD)}$ | supply current on pin PVDD | $V_{DD(PVDD)} = 3.3\text{ V}$ | - | 20 | - | mA |
| $I_{DD(VBAT)}$ | supply current on pin VBAT | $V_{DD(VBAT)} = 3.3\text{ V}$ max current includes current of all GPO's | - | - | 20 | mA |
| I_{pd} | power-down current | $V_{DD(TVDD)} = V_{DD(PVDD)} = V_{DD(VDD)} = 3.0\text{ V}$; hard power-down; pin RESET_N set LOW, $T_{amb} = 25\text{ °C}$ | - | 10 | - | μA |
| I_{stb} | standby current | $T_{amb} = 25\text{ °C}$ | - | 15 | - | μA |

Table 129. Reset pin RESET_N

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|--------------------------|----------------------------------|-----|-----|----------------|---------------|
| $t_{(reset)}$ | reset time | | 10 | - | - | μs |
| V_{IH} | HIGH-level input voltage | $V_{DD(PVDD)} \leq V_{DD(VBAT)}$ | 1.1 | - | $V_{DD(PVDD)}$ | V |
| V_{IL} | LOW-level input voltage | | 0 | - | 0.4 | V |
| I_{IH} | HIGH-level input current | $V_I = V_{DD(VBAT)}$ | - | - | 1 | mA |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$ | -1 | - | - | mA |
| C_i | input capacitance | | - | 5 | - | pF |

Table 130. Input Pin (AUX2) / DWL_REQ

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|----------------------------------|-----------------------|-----|----------------|---------------|
| V_{IH} | HIGH-level input voltage | $V_{DD(PVDD)} \leq V_{DD(VBAT)}$ | $0.65 \times P_{VDD}$ | - | $V_{DD(PVDD)}$ | V |
| V_{IL} | LOW-level input voltage | | 0 | - | 0.4 | V |
| I_{IH} | HIGH-level input current | $V_I = V_{DD(VBAT)}$ | - | - | 1 | mA |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$ | -1 | - | - | mA |
| C_i | load capacitance | | - | 5 | - | pF |
| $t_{(RESET_N-AUX2/DWL_REQ)}$ | time from RESET_N high to AUX2 /DWL_REQ high | | 0 | - | 50 | μs |

Table 131. output Pin AUX2 / (DWL_REQ)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|-------------------------------|-----------------------|-----|----------------|------|
| V_{OH} | HIGH-level output voltage | $V_{DD(PVDD)} = 1.8\text{ V}$ | $0.65 \times P_{VDD}$ | - | $V_{DD(PVDD)}$ | V |
| | | $V_{DD(PVDD)} = 3.0\text{ V}$ | 2.0 | - | $V_{DD(PVDD)}$ | V |
| V_{OL} | LOW-level output voltage | $V_{DD(PVDD)} = 1.8\text{ V}$ | 0 | - | 0.4 | V |
| | | $V_{DD(PVDD)} = 3.0\text{ V}$ | 0 | - | 0.8 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|----------------------|-----|-----|-----|------|
| I_{OH} | HIGH-level output current | $V_I = V_{DD(VBAT)}$ | - | - | 3 | mA |
| C_i | load capacitance | - | - | 5 | - | pF |

Table 132. GPO pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|----------------------------|-------------------------------|-----|-----|----------------|------|
| $V_{i(p-p)}$ | peak-to-peak input voltage | - | - | - | $V_{DD(PVDD)}$ | V |
| I_{OH} | HIGH-level output current | $V_{DD(PVDD)} = 3.3\text{ V}$ | - | - | 3 | mA |
| I_{IL} | LOW-level input current | $V_{DD(PVDD)} = 3.3\text{ V}$ | - | - | 3 | mA |

Table 133. CLK1, CLK2 pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|-------------------------------|--|-----|-----|------|---------------|
| $V_{i(p-p)}$ | peak-to-peak input voltage | - | 0.2 | - | 1.65 | V |
| I_{IH} | HIGH-level input current | $V_I = 1.65\text{ V}$ | - | - | 1 | μA |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$ | 1 | - | - | μA |
| δ | duty cycle | - | 35 | - | 65 | % |
| $C_{i(CLK1)}$ | input capacitance on pin CLK1 | $V_{DD} = 1.8\text{ V}$, $V_{DC} = 0.65\text{ V}$, $V_{AC} = 0.9\text{ V (p-p)}$ | - | 2 | - | pF |
| $C_{i(CLK2)}$ | input capacitance on pin CLK2 | $V_{DD} = 1.8\text{ V}$, $V_{DC} = 0.65\text{ V}$, $V_{AC} = 0.9\text{ V (p-p)}$ | - | 2 | - | pF |

Table 134. Output pin characteristics IRQ

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|--------------------------|----------------------|-----|----------------|------------------|
| V_{OH} | HIGH-level output voltage | $I_{OH} < 3\text{ mA}$ | $V_{DD(PVDD)} - 0.4$ | - | $V_{DD(PVDD)}$ | V |
| V_{OL} | LOW-level output voltage | $I_{OL} < 3\text{ mA}$ | 0 | - | 0.4 | V |
| C_L | load capacitance | | - | - | 20 | pF |
| t_f | fall time | $C_L = 12\text{ pF max}$ | 1 | - | 3 | ns |
| t_r | rise time | $C_L = 12\text{ pF max}$ | 1 | - | 3 | ns |
| R_{pd} | pull-down resistance | | 0.4 | - | 0.7 | $\text{M}\Omega$ |

Table 135. Input pins SCLK, MOSI, NSS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|------------|----------------------------|-----|----------------|------|
| V_{IH} | HIGH-level input voltage | | $0.65 \times V_{DD(PVDD)}$ | - | $V_{DD(PVDD)}$ | V |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|--------------------|-----|-----|----------------------------|------|
| V_{IL} | LOW-level input voltage | | 0 | - | $0.35 \times V_{DD(PVDD)}$ | V |
| C_i | input capacitance | | - | 5 | - | pF |
| I_{IH} | HIGH-level input current | $V_I = P_{VDD}$ | - | - | 1 | mA |
| I_{IL} | LOW-level input current | $V_I = 0\text{ V}$ | - | - | 1 | mA |

Table 136. Output pin MISO

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|--------------------------|----------------------|-----|----------------|------|
| V_{OH} | HIGH-level output voltage | $I_{OH} < 3\text{ mA}$ | $V_{DD(PVDD)} - 0.4$ | - | $V_{DD(PVDD)}$ | V |
| V_{OL} | LOW-level output voltage | $I_{OL} < 3\text{ mA}$ | 0 | - | 0.4 | V |
| C_L | load capacitance | | - | - | 20 | pF |
| t_f | fall time | $C_L = 12\text{ pF max}$ | 1 | - | 3 | ns |
| t_r | rise time | $C_L = 12\text{ pF max}$ | 1 | - | 3 | ns |

Table 137. Timing conditions SPI

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|------------------------------------|-----|-----|-----|------|
| t_{SCKL} | SCK LOW time | 72 | - | - | ns |
| t_{SCKH} | SCK HIGH time | 72 | - | - | ns |
| $t_{h(SCKH-D)}$ | SCK HIGH to data input hold time | 25 | - | - | ns |
| $t_{su(D-SCKH)}$ | data input to SCK HIGH set-up time | 25 | - | - | ns |
| $t_{h(SCKL-Q)}$ | SCK LOW to data output hold time | - | - | 25 | ns |
| $t_{(SCKL-NSSH)}$ | SCK LOW to NSS HIGH time | 0 | - | - | ns |
| t_{NSSH} | NSS HIGH time | 72 | - | - | ns |

Table 138. Output pins ANT1 and ANT2

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|-----------------------------|-----|-----|-----|----------|
| $Z_{i(\text{diff})}$ | differential impedance from ANT1 to ANT2 | Low impedance configuration | - | 10 | 17 | Ω |
| $V_{i(\text{start})(\text{lim})(\text{ANT1})}$ | limiter start input voltage on ANT1 | $I=10\text{ mA}$ | - | 3.3 | - | V |
| $V_{i(\text{start})(\text{lim})(\text{ANT2})}$ | limiter start input voltage on ANT2 | $I=10\text{ mA}$ | - | 3.3 | - | V |

Table 139. Input pins RXp and RXn

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-----------------------|------------|-----|-----|-----|------|
| $V_{i(\text{dyn})}$ | dynamic input voltage | | - | - | 1.8 | V |

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|--|----------------------------|-----|-----|-----|------------|
| C_i | input capacitance | | - | 12 | - | pF |
| Z_i | input impedance from RXN, RXP pins to VMID | Reader, Card and P2P modes | 0 | - | 15 | k Ω |

Table 140. Output pins TX1 and TX2

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|---------------------------|-----|------------------------------|----------------|------|
| V_{OH} | HIGH-level output voltage | $V_{DD(TVDD)}=5\text{ V}$ | - | $V_{DD(TVDD)}-150\text{ mV}$ | $V_{DD(TVDD)}$ | V |
| V_{OL} | LOW-level output voltage | $V_{DD(TVDD)}=5\text{ V}$ | 0 | 200 | - | mV |

Table 141. Start-up time

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------------------|----------------|-----|-----|--|------|
| t_{boot} | start-up time ^[1] | RESET_N = High | 2.3 | 2.5 | dependent on configuration of XTAL_BOOT_TIME in EEPROM | ms |

[1] (PN5180 ready to receive commands on the host interface). The PN5180 indicates the ability to receive commands from a host by raising an IDLE IRQ.

Table 142. Crystal requirements for ISO/IEC14443 compliant operation

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------------------|------------|------|-----|------|---------------|
| f_{xtal} | crystal frequency | - | -100 | - | +100 | ppm |
| ESR | equivalent series resistance | - | - | 50 | 100 | Ω |
| C_L | load capacitance | - | - | 10 | - | pF |
| P_{xtal} | crystal power dissipation | - | - | - | 100 | μW |

Table 143. Reference input frequency requirements for 8 MHz, 12 MHz, 16 MHz and 24 MHz

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------------------|------------------------------------|------|-----|------|--------|
| Φ_n | phase noise | Input noise floor at 50 kHz offset | - | - | -140 | dBc/Hz |
| $V_{i(p-p)}$ | peak-to-peak input voltage | sinus signal | 0.2 | - | 1.8 | V |
| $V_{i(p-p)}$ | peak-to-peak input voltage | square signal | 0 | 1.8 | 1.98 | V |
| $f_{i(ref)acc}$ | reference input frequency accuracy | - | -100 | - | +100 | ppm |

17 Application information

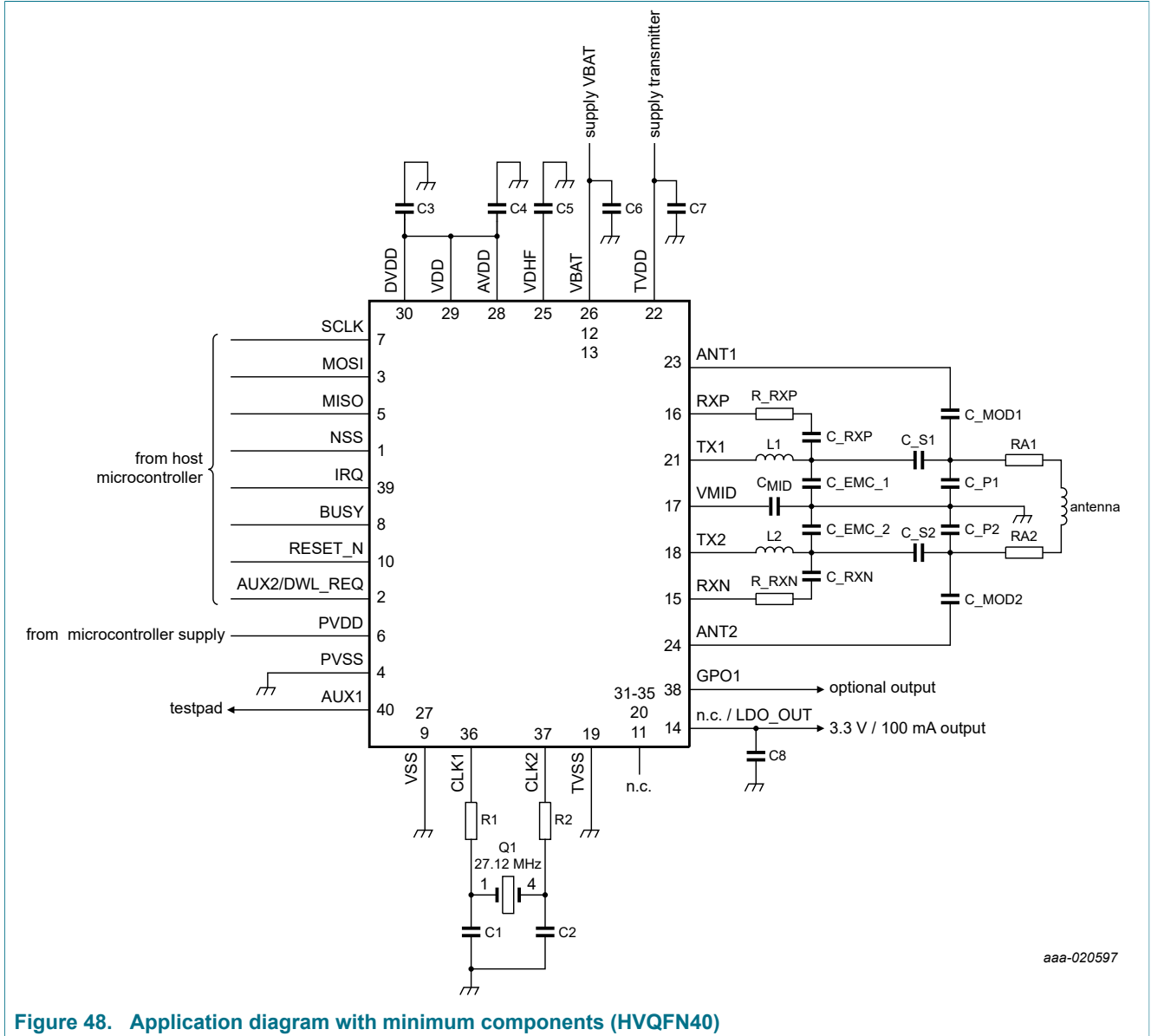


Figure 48. Application diagram with minimum components (HVQFN40)

17.1 Typical component values

The following component values are typical values for a design. Refer to the Application note "PN5180 Antenna Design Guide" how to determine the values listed to be dependent on antenna design.

Table 144. Table 140.

| Component | Value |
|------------------------|---|
| C1, C2 | 15 pF |
| C3 | 1 nF |
| C4 | 2.2 μ F |
| C5 | 470 nF |
| C6 | 100 nF |
| C7 | 6.8 μ F, additional blocking capacitors 100 nF might be required dependent on PCB layout and supply characteristics |
| C8 | 10 μ F (only required in case 3.3 V regulated output is used) |
| L1, L2 | 470 nH |
| C_EMC_1, C_EMC_2 | 220 pF |
| C_RCXP, C_RXN | 1 nF |
| R_RXP, R_RXN | Dependent on antenna design |
| C_MOD | 82 pF |
| C_S1, C_S2, C_P1, C_P2 | Dependent on antenna design |

17.2 Power supply of a microcontroller by the PN5180 / LDO_OUT

The PN5180 is able to provide a regulated 3.3 V voltage with currents of up to 100 mA. This regulated voltage is available on pin LDO_OUT.

The PN5180 needs to be configured properly to enable the output of the regulated 3.3 V Voltage output.

The output of the 3.3 V can be enabled either by a register configuration after boot or by EEPROM configuration at startup:

Register: SYSTEM_CONFIG.LDO_ENABLE (bit 11)

EEPROM Address 0xE8, Misc_Config (bit 3) - if set the 3.3 V output is enabled.

The supply voltage will be available during Idle mode.

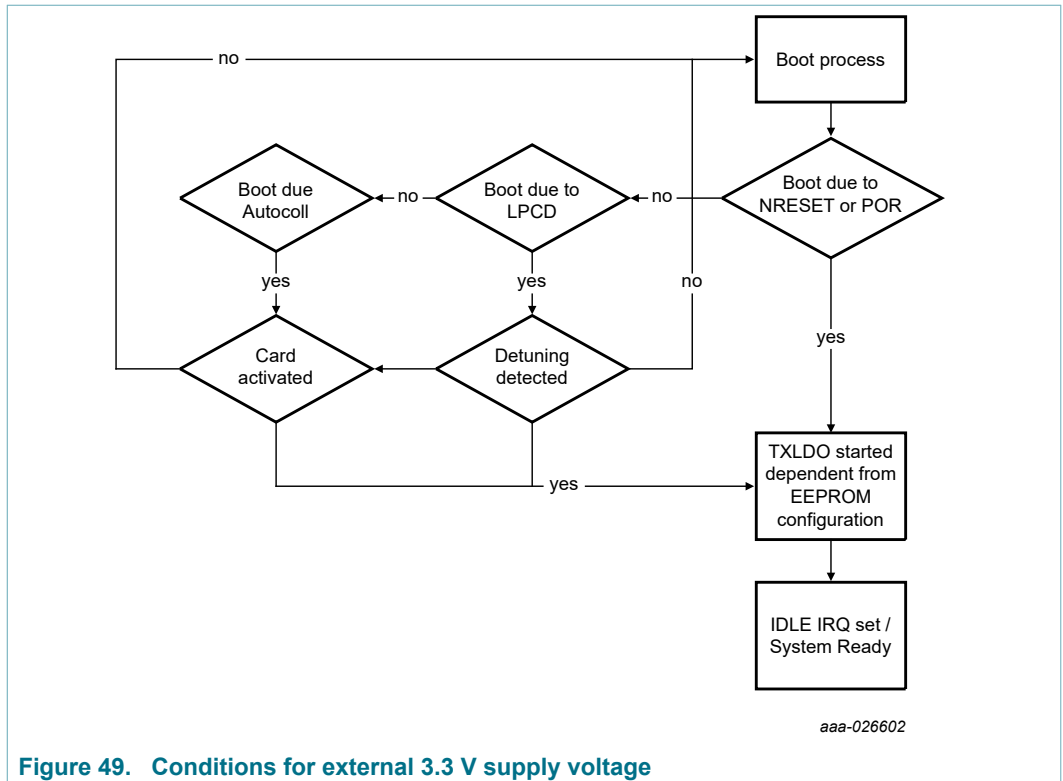


Figure 49. Conditions for external 3.3 V supply voltage

17.3 Zero Power wake-up

The PN5180 allows using the energy of an external reader RF field to provide an output voltage on the pin VDHF, even if the chip is not otherwise supplied with power. This voltage generated from the external RF field allows triggering a silicon main switch to supply the chip. Any NFC mobile phone polling for cards is generating periodically such an RF field which can be used to toggle this silicon main switch.

No configuration of registers is required to use this functionality.

This feature allows developing systems with a power consumption close to zero during power-off.

17.4 LPCD while using an external DC-DC

As power-saving feature the PN5180 allows using a general-purpose output to control an external DC-DC during Low-Power Card Detection.

A system might use a DC-DC for supply of the transmitters from a battery is in low-power card detection mode. Typically, the DC-DC will be permanently active resulting in a high average current consumption. There is no way to use a power-saving feature of a DC-DC, because the time of RF-on of a low-power card detection cycle is not known to the DC-DC.

The solution is now to use a GPO to wake up the DC-DC from power down before the RF of a low-power card detection cycle is switched on. The DC-DC needs to be woken up sufficiently early to allow a settling of the supplied output.

The sequence will be as follows:

1. The GPO wakes up the DC-DC

2. The PN5180 switches on the RF (low-power card detection cycle)
3. If no card had been detected, the RF is switched off
4. The GPO sets the DC-DC in power-saving mode

The GPO function as such can be enabled by the EEPROM register:
LPCD_REFVAL_GPO_CONTROL.

- The time between trigger of the DC-DC and RF-OFF is configured by the EEPROM register: LPCD_GPO_TOGGLE_AFTER_FIELD_OFF
- The time between trigger of the DC-DC and RF-ON is configured by the EEPROM register: LPCD_GPO_TOGGLE_BEFORE_FIELD_ON

This functionality allows implementing power efficient LPCD function even in case of a required DC-DC.

18 Packaging information

Moisture Sensitivity Level (MSL) evaluation has been performed according to SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C).

MSL for the HVQFN40 package is level 3 which means 260 °C convection reflow temperature.

- 1-week out-of-pack floor life at maximum ambient temperature 30°C/ 60 % RH (Relative Humidity) to limit possible moisture intrusion.
- When used in production, stored under nitrogen conditions for not more than 8 days

MSL for the TFBGA64 package is level 1:

- No dry pack is required.
- No out-of-pack floor live spec. required.

19 Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

20 Package outline

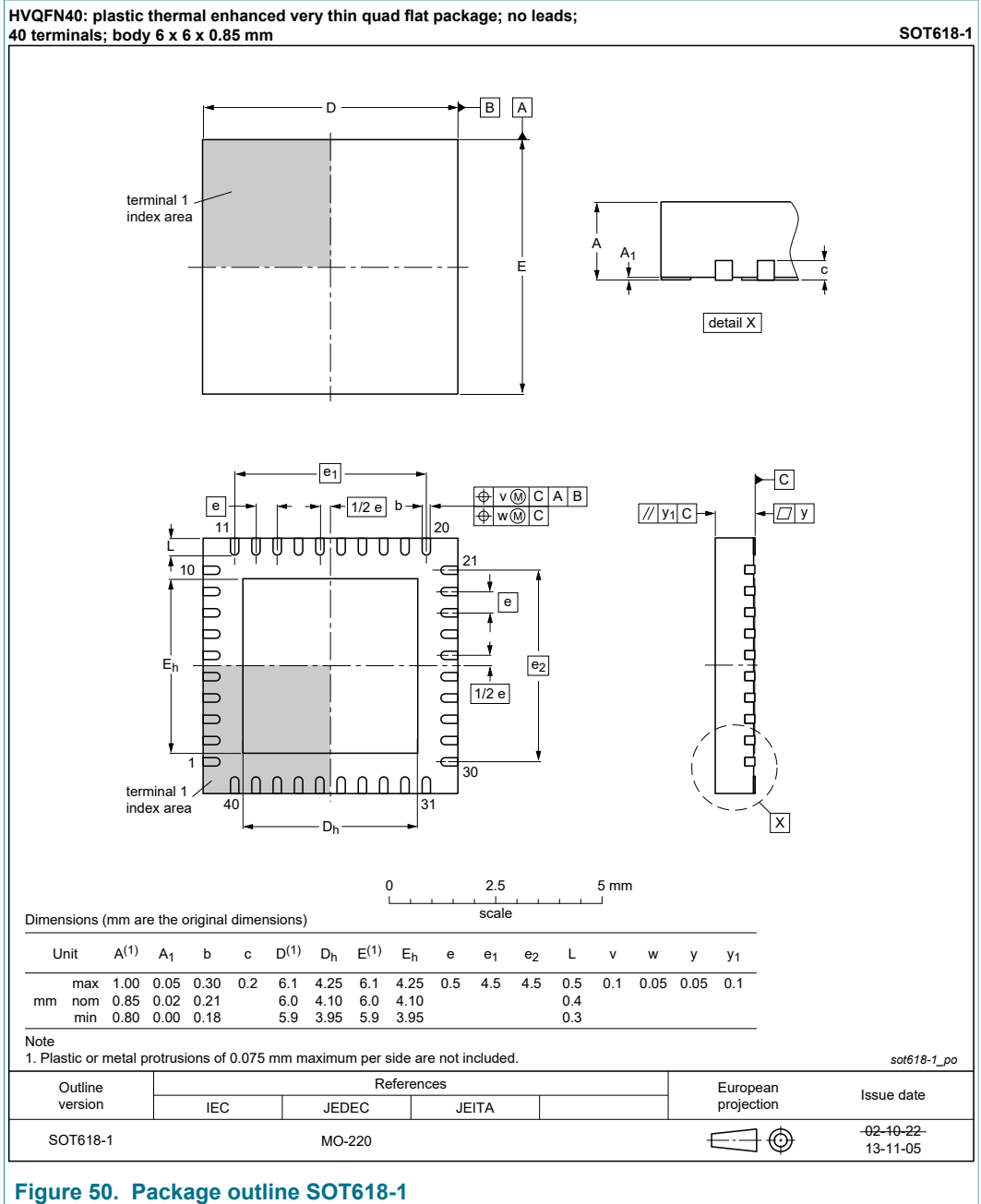


Figure 50. Package outline SOT618-1

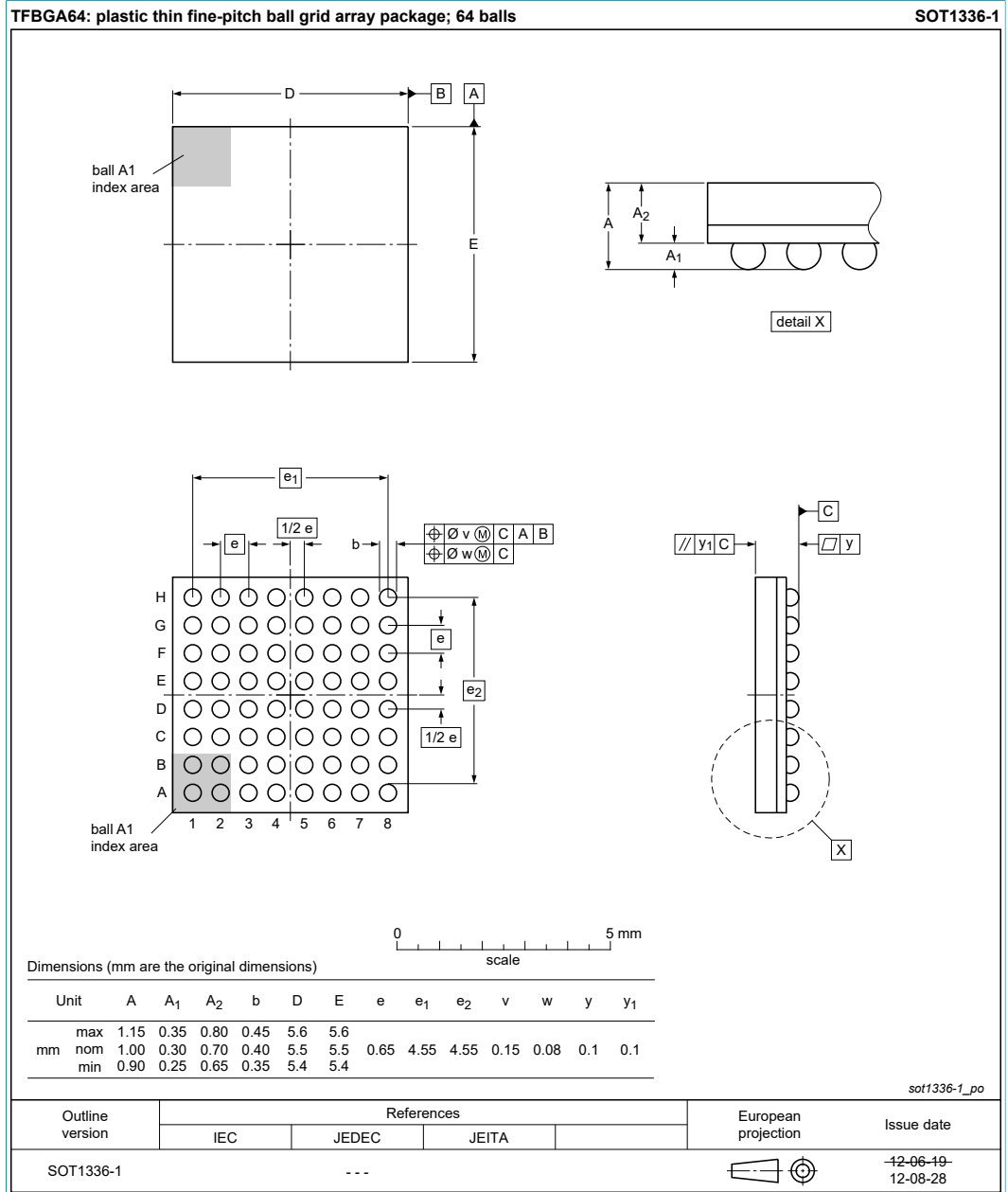


Figure 51. Package outline SOT1336-1

21 Appendix

21.1 Timer Delay for start of reception measurement

These timer values are automatically set by Firmware. No special timer setting is required by the user.

21.2 Default protocol settings for LOAD_RF_CONFIG, Transmitter

21.2.1 ISO/IEC 14443 A-106

Table 145. ISO/IEC 14443 A-106

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x74 |
| TX_DATA_MOD | 0x2350 |
| TX_UNDERSHOOT_CONFIG | 0x17 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBCF43 |
| ANT_CONTROL | 0x10 |

21.2.2 ISO/IEC 14443 A-212

Table 146. ISO/IEC 14443 A-212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x82 |
| TX_DATA_MOD | 0x2350 |
| TX_UNDERSHOOT_CONFIG | 0x17 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBCF043 |
| ANT_CONTROL | 0x10 |

21.2.3 ISO/IEC 14443 A-424

Table 147. ISO/IEC 14443 A-424

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x82 |
| TX_DATA_MOD | 0x650 |
| TX_UNDERSHOOT_CONFIG | 0x5 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBCF43 |
| ANT_CONTROL | 0x10 |

21.2.4 ISO/IEC 14443 A-848

Table 148. ISO/IEC 14443 A-848

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x82 |
| TX_DATA_MOD | 0x150 |
| TX_UNDERSHOOT_CONFIG | 0x1 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xF9EF45 |
| ANT_CONTROL | 0x10 |

21.2.5 ISO/IEC 14443 B-106

Table 149. ISO/IEC 14443 B-106

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x3A4756 |
| ANT_CONTROL | 0x10 |

21.2.6 ISO/IEC 14443 B-212

Table 150. ISO/IEC 14443 B-212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39C746 |
| ANT_CONTROL | 0x10 |

21.2.7 ISO/IEC 14443 B-424

Table 151. ISO/IEC 14443 B-424

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x78E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x1FE0013 |
| RF_CONTROL_TX | 0x71CF54 |

| Register name | Initialization value |
|---------------|----------------------|
| ANT_CONTROL | 0x10 |

21.2.8 ISO/IEC 14443 B-848

Table 152. ISO/IEC 14443 B-848

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x78E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x7E000D |
| RF_CONTROL_TX | 0x69AF32 |
| ANT_CONTROL | 0x10 |

21.2.9 FeliCa-212

Table 153. FeliCa-212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39E744 |
| ANT_CONTROL | 0x10 |

21.2.10 FeliCa-424

Table 154. FeliCa-424

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39EF33 |
| ANT_CONTROL | 0x10 |

21.2.11 NFC active initiator A-106

Table 155. NFC active initiator A-106

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8782 |
| TX_DATA_MOD | 0x2350 |

| Register name | Initialization value |
|----------------------|----------------------|
| TX_UNDERSHOOT_CONFIG | 0x17 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBC43 |
| ANT_CONTROL | 0x10 |

21.2.12 NFC active initiator A-212

Table 156. NFC active initiator A-212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x808E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39E744 |
| ANT_CONTROL | 0x10 |

21.2.13 NFC active initiator A-424

Table 157. NFC active initiator A-424

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x808E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39EF33 |
| ANT_CONTROL | 0x10 |

21.2.14 ISO/IEC15693-26

Table 158. ISO/IEC15693-26

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x782 |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0xF00001F |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBC745 |
| ANT_CONTROL | 0x10 |

21.2.15 ISO/IEC15693-53**Table 159. ISO/IEC15693-53**

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0xFF000F |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x3A4F44 |
| ANT_CONTROL | 0x10 |

21.2.16 ISO/IEC18003M3 - TARI=18.88 μ s**Table 160. ISO/IEC18003M3 - TARI=18.88us**

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0xFF000F |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x3A2734 |
| ANT_CONTROL | 0x10 |

21.2.17 ISO/IEC18003M3 - TARI=9.44 μ s**Table 161. ISO/IEC18003M3 - TARI=9.44 μ s**

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0xFF000F |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x3A4734 |
| ANT_CONTROL | 0x10 |

21.2.18 PICC ISO/IEC14443-A 106**Table 162. PICC ISO/IEC14443-A 106**

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x72 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.19 PICC ISO/IEC14443-A 212

Table 163. PICC ISO/IEC14443-A 212

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x72 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.20 PICC ISO/IEC14443-A 424

Table 164. PICC ISO/IEC14443-A 424

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x72 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.21 PICC ISO/IEC14443-A 848

Table 165. PICC ISO/IEC14443-A 848

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x72 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.22 NFC passive target 212

Table 166. NFC passive target 212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.23 NFC passive target 424

Table 167. NFC passive target 424

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |

| Register name | Initialization value |
|----------------------|----------------------|
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x0 |
| ANT_CONTROL | 0xC |

21.2.24 NFC active target 106

Table 168. NFC active target 106

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8782 |
| TX_DATA_MOD | 0x2350 |
| TX_UNDERSHOOT_CONFIG | 0x17 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0xDBCF43 |
| ANT_CONTROL | 0x10 |

21.2.25 NFC active target 212

Table 169. NFC active target 212

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x0808E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39E744 |
| ANT_CONTROL | 0x10 |

21.2.26 NFC active target 424

Table 170. NFC active target 424

| Register name | Initialization value |
|----------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x808E |
| TX_DATA_MOD | 0x0 |
| TX_UNDERSHOOT_CONFIG | 0x0 |
| TX_OVERSHOOT_CONFIG | 0x0 |
| RF_CONTROL_TX | 0x39EF33 |
| ANT_CONTROL | 0x10 |

21.2.27 NFC general target mode - all data rates

Table 171. NFC general target mode - all data rates

| Register name | Initialization value |
|-------------------|----------------------|
| RF_CONTROL_TX_CLK | 0x8000 |
| TX_DATA_MOD | 0x72 |

21.3 Default protocol settings for LOAD_RF_CONFIG, Receiver

21.3.1 ISO/IEC 14443 A-106

Table 172. ISO/IEC 14443 A-106

| Register name | Initialization value |
|--------------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x804B |
| ANA_RX_POWER_CONTROL_RFU | 0x200 |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x430DC |
| RF_CONTROL_RX | 0x1E |

21.3.2 ISO/IEC 14443 A-212

Table 173. ISO/IEC 14443 A-212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x0x801F0801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x430DC |
| RF_CONTROL_RX | 0x1E |

21.3.3 ISO/IEC 14443 A-424

Table 174. ISO/IEC 14443 A-424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x192905 |
| RF_CONTROL_RX | 0x16 |

21.3.4 ISO/IEC 14443 A-848

Table 175. ISO/IEC 14443 A-848

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xF2505 |
| RF_CONTROL_RX | 0x11 |

21.3.5 ISO/IEC 14443 B-106

Table 176. ISO/IEC 14443 B-106

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x1F2415 |
| RF_CONTROL_RX | 0x16 |

21.3.6 ISO/IEC 14443 B-212

Table 177. ISO/IEC 14443 B-212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x192805 |
| RF_CONTROL_RX | 0x16 |

21.3.7 ISO/IEC 14443 B-424

Table 178. ISO/IEC 14443 B-424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x192A05 |
| RF_CONTROL_RX | 0x16 |

21.3.8 ISO/IEC 14443 B-848

Table 179. ISO/IEC 14443 B-848

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xF2505 |
| RF_CONTROL_RX | 0x1A |

21.3.9 FeliCa 212

Table 180. FeliCa 212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xF2605 |
| RF_CONTROL_RX | 0x11 |

21.3.10 FeliCa 424

Table 181. FeliCa 424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x2605 |
| RF_CONTROL_RX | 0x15 |

21.3.11 NFC Active Initiator 106

Table 182. NFC Active Initiator 106

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| RX_RFU | 0x1 |
| SIGPRO_CM_CONFIG | 0x0 |
| RF_CONTROL_RX | 0x23 |

21.3.12 NFC Active Initiator 212

Table 183. NFC Active Initiator 212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.13 NFC Active Initiator 424

Table 184. NFC Active Initiator 424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.14 ISO/IEC 15693-26

Table 185. ISO/IEC 15693-26

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x804B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0x4010 |
| RF_CONTROL_RX | 0x1A |

21.3.15 ISO/IEC 15693-53

Table 186. ISO/IEC 15693-53

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x804B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xC4010 |
| RF_CONTROL_RX | 0x1A |

21.3.16 ISO 18003M3- Tari 18.88

Table 187. ISO 18003M3- Tari 18.88

| Register name | Initialization value |
|---------------|----------------------|
| AGC_VALUE | 0x801F0 |

| Register name | Initialization value |
|----------------------|----------------------|
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_CM_CONFIG_RFU | 0x0 |
| SIGPRO_RM_CONFIG | 0x8014 |
| RF_CONTROL_RX | 0x1A |

21.3.17 ISO 18003M3- Tari 9.44 848_2

Table 188. ISO 18003M3- Tari 9.44 848_2

| Register name | Initialization value |
|-----------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xC6014 |
| SIGPRO_CM_CONFIG2_RFU | 0x1 |

21.3.18 ISO 18003M3- Tari 9.44 -848_4

Table 189. ISO18003M3- Tari 9.44 -848_4

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0x801F0 |
| AGC_CONFIG | 0x860B |
| SIGPRO_CM_CONFIG | 0x0 |
| SIGPRO_RM_CONFIG | 0xC8094 |
| RF_CONTROL_RX | 0x1F |

21.3.19 ISO 14443A-PICC 106

Table 190. ISO 14443A-PICC 106

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| RX_RFU | 0x1 |
| SIGPRO_CM_CONFIG | 0x1000801C |
| RF_CONTROL_RX | 0x23 |

21.3.20 ISO 14443A-PICC 212

Table 191. ISO 14443A-PICC 212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x1C0600E0 |

High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes

| Register name | Initialization value |
|---------------|----------------------|
| RF_CONTROL_RX | 0xE3 |

21.3.21 ISO 14443A-PICC 424

Table 192. ISO 14443A-PICC 424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x14040040 |
| RF_CONTROL_RX | 0x23 |

21.3.22 ISO 14443A-PICC 848

Table 193. ISO 14443A-PICC 848

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x8030040 |
| RF_CONTROL_RX | 0x2F |

21.3.23 NFC-Passive target -212

Table 194. NFC-Passive target -212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.24 NFC-Passive target -424

Table 195. NFC-Passive target -424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.25 NFC-active target - 106

Table 196. NFC-active target - 106

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| SIGPRO_CM_CONFIG | 0x0 |
| RF_CONTROL_RX | 0x23 |

21.3.26 NFC-active target - 212

Table 197. NFC-active target - 212

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.27 NFC-active target - 424

Table 198. NFC-active target - 424

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA00B |
| SIGPRO_CM_CONFIG | 0x50010060 |
| RF_CONTROL_RX | 0x23 |

21.3.28 NFC-General target mode - all data rates

Table 199. NFC-General target mode - all data rates

| Register name | Initialization value |
|------------------|----------------------|
| AGC_VALUE | 0xC0150 |
| AGC_CONFIG | 0xA003 |
| SIGPRO_CM_CONFIG | 0x10010060 |
| RF_CONTROL_RX | 0x23 |

22 Abbreviations

Table 200. Abbreviations

| Acronym | Description |
|---------|--|
| ADC | Analog-to-Digital Converter |
| ALM | Active Load modulation: modulation type in card emulation mode, allows achieving a larger communication distance between reader-card than PLM - passive modulation |
| AWC | Adaptive Waveform Control |
| BPSK | Binary Phase Shift Keying |
| BBA | Base Band Amplifier |
| CRC | Cyclic Redundancy Check |
| DPC | Dynamic Power Control |
| EGT | Extra Guard Time |
| EMC | ElectroMagnetic Compatibility |
| EMD | ElectroMagnetic Disturbance |
| EOF | End Of Frame |
| ETU | Elementary Time Unit |
| HBM | Human Body Model |
| LFO | Low Frequency Oscillator |
| LPCD | Low-Power Card Detection |
| LSB | Least Significant Bit |
| MISO | Master In Slave Out |
| MOSI | Master Out Slave In |
| MSB | Most Significant Bit |
| NRZ | Not Return to Zero |
| NSS | Not Slave Select |
| PCD | Proximity Coupling Device |
| PLL | Phase-Locked Loop |
| PLM | Passive Load Modulation: modulation type in card emulation mode, resistive load modulation as used by contactless smartcards which are powered by the energy of the RF-field |
| RZ | Return To Zero |
| RX | Receiver |
| SOF | Start Of Frame |
| SPI | Serial Peripheral Interface |
| SW | Software |
| TX | Transmitter |
| UART | Universal Asynchronous Receiver Transmitter |
| UID | Unique Identification |

23 References

1. **ISO/IEC 14443** - parts 2: 2001 COR 1 2007 (01/11/2007), part 3: 2001 COR 1 2006 (01/09/2006) and part 4: 2nd edition 2008 (15/07/2008)

24 Revision history

Table 201. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|---|--------------------|---------------|----------------------|
| PN5180A0xx/C3 v. 3.5 | 20191211 | Product data sheet | - | PN5180A0xx/C3 v. 3.4 |
| Modifications: | <ul style="list-style-type: none"> • Section Firmware Version: overview description for version 4.1 added • Table 50 "ANALOG TEST SIGNALS" updated: removed SIGPRO_IN_SEL in ADC_DATA_Q/I descriptions (not available) • EEPROM address 7Dh is now RFU • Section 11.9.2 "Register description": Table register FELICA_EMD_CONTROL register (address 0043h) added • Memories: Table 51 "EEPROM Addresses": EEPROM address of TbDac1 and TbDac2 corrected | | | |
| PN5180A0xx/C3 v. 3.4 | 20180507 | Product data sheet | - | PN5180A0xx/C3 v. 3.2 |
| Modifications: | <ul style="list-style-type: none"> • Improved description of EEPROM configuration RF_DEBOUNCE_TIMEOUT in Section 11.5.2 | | | |
| PN5180A0xx/C3 v. 3.3 | 20180419 | Product data sheet | - | PN5180A0xx/C3 v. 3.2 |
| Modifications: | <ul style="list-style-type: none"> • Editorial updates | | | |
| PN5180A0xx/C3 v. 3.2 | 20171220 | Product data sheet | - | PN5180A0xx/C3 v. 3.1 |
| Modifications: | <ul style="list-style-type: none"> • Descriptive title updated • EEPROM clock configuration updated • ANALOG TEST SIGNAL addresses updated • Name of CECK_CARD_RESULT register changed to AGC_REF_CONFIG • Description in SIGPRO_RM_CONFIG register for MinLevel and MinLeveP updated • Description in Table 71 "Adaptive Receiver Control lookup table "updated • Figure 48: updated • Command UPDATE_RF_CONFIG - 0x12: "length byte" info corrected from 42 to 42 x 6 bytes • Condition for VBAT deleted in Section 16 "Characteristics" | | | |
| PN5180A0xx/C3 v. 3.1 | 20170731 | Product data sheet | - | PN5180A0xx/C3 v. 3.0 |
| Modifications: | <ul style="list-style-type: none"> • Figure 2 and Figure 3 updated | | | |
| PN5180A0xx/C3 v. 3.0 | 20170718 | Product data sheet | - | - |
| Modifications: | Initial version of the data sheet | | | |

25 Legal information

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|-----------------------------------|-------------------------------|---|
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Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



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