

NTMFS4H01NF

Power MOSFET

25 V, 334 A, Single N-Channel, SO-8FL

Features

- Integrated Schottky Diode
- Optimized Design to Minimize Conduction and Switching Losses
- Optimized Package to Minimize Parasitic Inductances
- Optimized material for improved thermal performance
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Performance DC-DC Converters
- System Voltage Rails
- Netcom, Telecom
- Servers & Point of Load

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V_{DS}	25	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ ($T_A = 25^\circ\text{C}$, Note 1)	I_D	54	A
Power Dissipation $R_{\theta JA}$ ($T_A = 25^\circ\text{C}$, Note 1)	P_D	3.2	W
Continuous Drain Current $R_{\theta JC}$ ($T_C = 25^\circ\text{C}$, Note 1)	I_D	334	A
Power Dissipation $R_{\theta JC}$ ($T_C = 25^\circ\text{C}$, Note 1)	P_D	125	W
Pulsed Drain Current ($t_p = 10 \mu\text{s}$)	I_{DM}	568	A
Single Pulse Drain-to-Source Avalanche Energy (Note 1) ($I_L = 57 \text{ A}_{pk}$, $L = 0.3 \text{ mH}$)	E_{AS}	487	mJ
Drain to Source dV/dt	dV/dt	7	V/ns
Maximum Junction Temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 2)	T_{SLD}	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Values based on copper area of 645 mm^2 (or 1 in^2) of 2 oz copper thickness and FR4 PCB substrate.
2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
3. This is the absolute maximum rating. Parts are 100% UIS tested at $T_J = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $I_L = 37 \text{ A}$, $E_{AS} = 205 \text{ mJ}$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Thermal Resistance, Junction-to-Ambient (Note 1 and 4) Junction-to-Case (Note 1 and 4)	$R_{\theta JA}$ $R_{\theta JC}$	38.9 1.0	$^\circ\text{C/W}$

4. Thermal Resistance $R_{\theta JA}$ and $R_{\theta JC}$ as defined in JESD51-3.



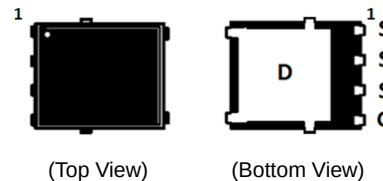
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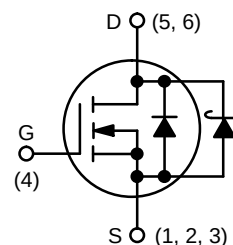
V_{GS}	MAX $R_{DS(on)}$	TYP Q_{GTOT}
4.5 V	1.0 m Ω	37.8 nC
10 V	0.7 m Ω	82 nC

PIN CONNECTIONS

SO8-FL (5 x 6 mm)



N-CHANNEL MOSFET



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 10\text{ mA}$ reference to 25°C		16		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			500	μA
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}$			+100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 10\text{ mA}$ reference to 25°C		3.7		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		0.56	0.7	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		0.79	1	
Forward Transconductance	g_{FS}	$V_{DS} = 12\text{ V}, I_D = 20\text{ A}$		101		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		5538		pF
Output Capacitance	C_{OSS}			3416		
Reverse Transfer Capacitance	C_{RSS}			175.3		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		37.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.3		
Gate-to-Source Charge	Q_{GS}			11.8		
Gate-to-Drain Charge	Q_{GD}			8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		82		nC
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.3	2	Ω

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		16.9		ns
Rise Time	t_r			42.3		
Turn-Off Delay Time	$t_{d(OFF)}$			46.3		
Fall Time	t_f			30.9		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		10.9		ns
Rise Time	t_r			33.2		
Turn-Off Delay Time	$t_{d(OFF)}$			58.3		
Fall Time	t_f			23.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 2.0 A	T _J = 25°C		0.35	0.6	V
			T _J = 125°C		0.27		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 30 A			66.7		ns
Charge Time	t _a				33.1		
Discharge Time	t _b				33.6		
Reverse Recovery Charge	Q _{RR}					90	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

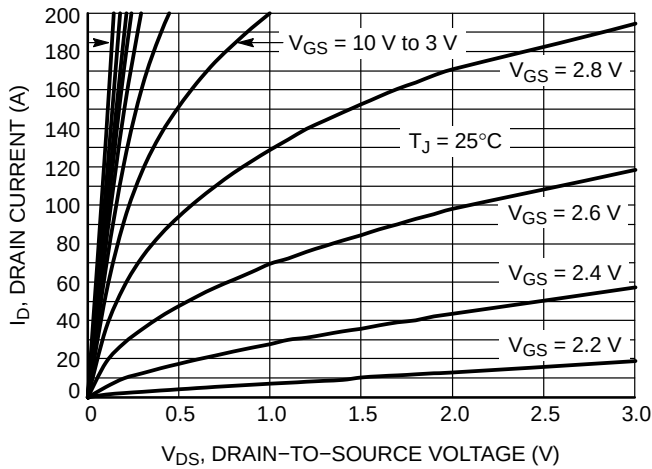


Figure 1. On-Region Characteristics

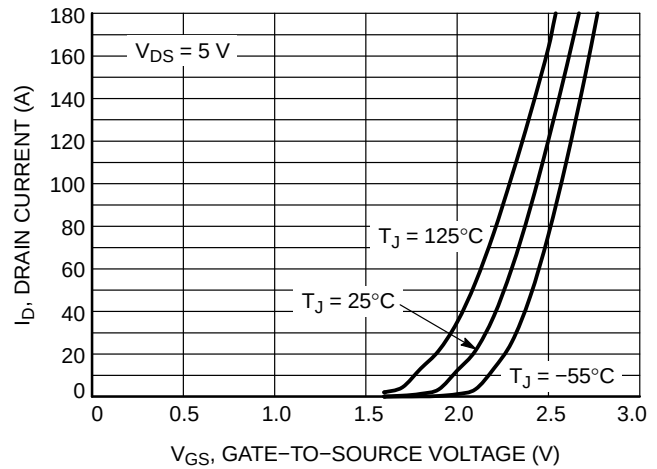


Figure 2. Transfer Characteristics

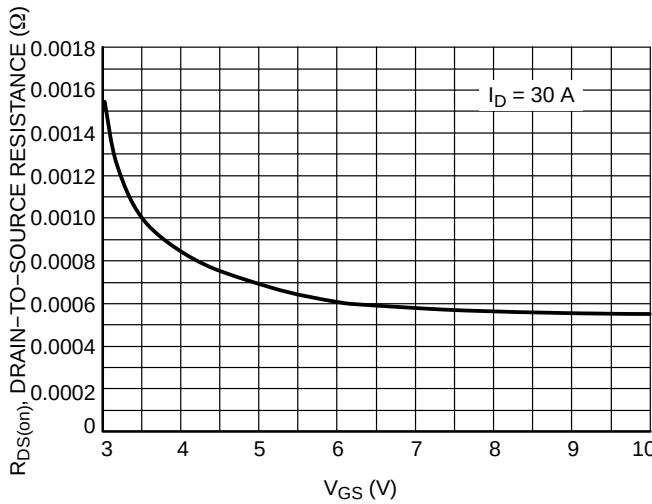


Figure 3. On-Resistance vs. V_{GS}

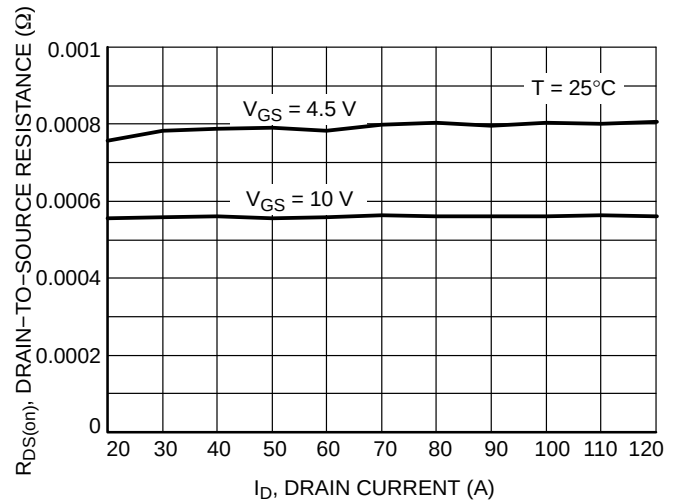


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

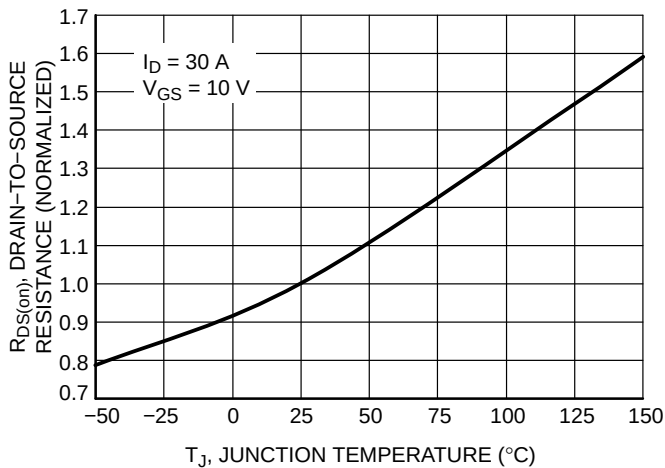


Figure 5. On-Resistance Variation with Temperature

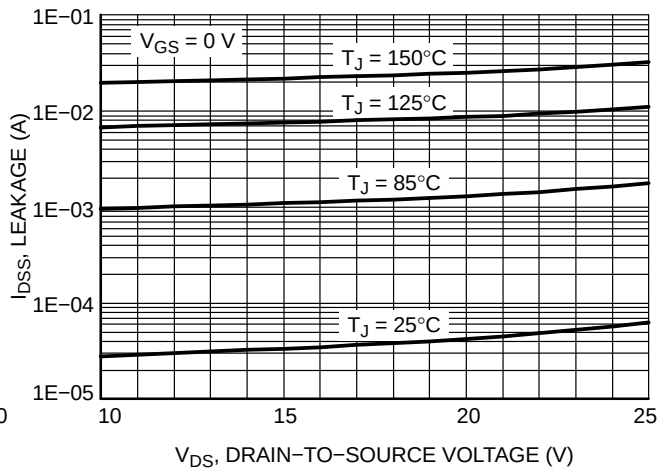


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

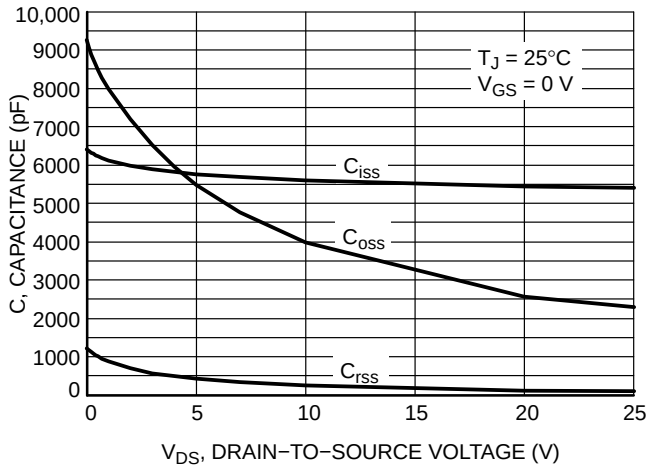


Figure 7. Capacitance Variation

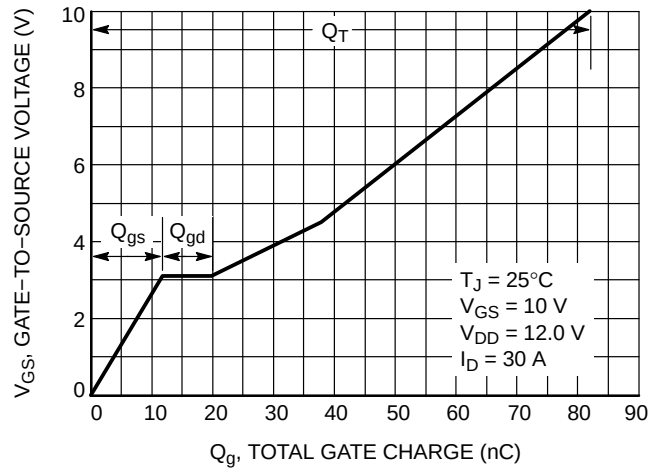


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

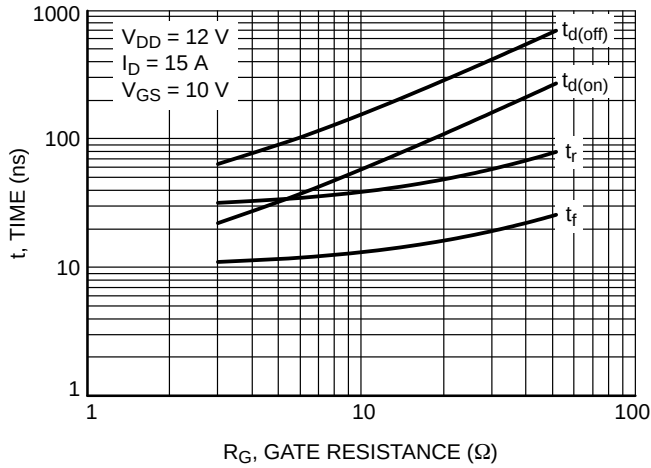


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

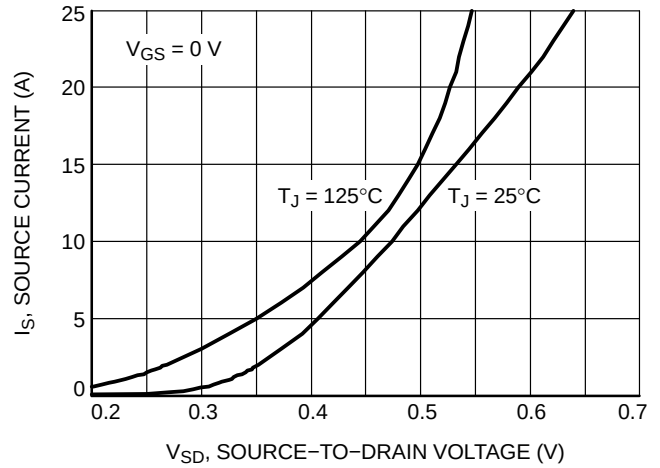


Figure 10. Diode Forward Voltage vs. Current

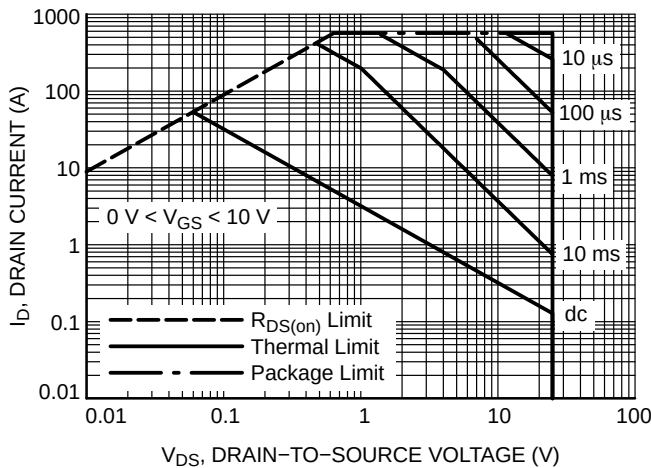


Figure 11. Maximum Rated Forward Biased Safe Operating Area

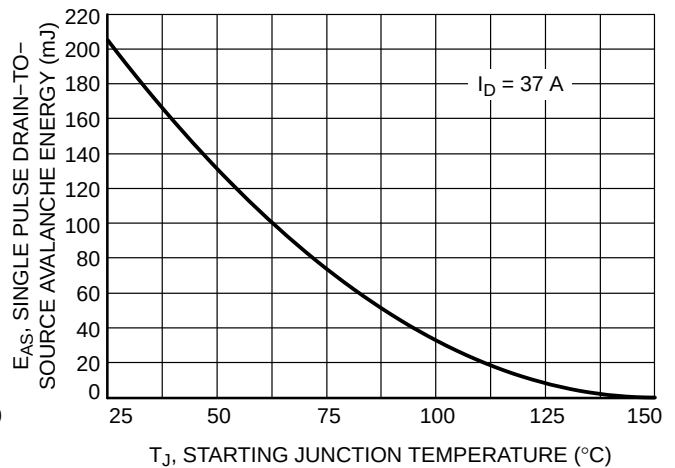


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL CHARACTERISTICS

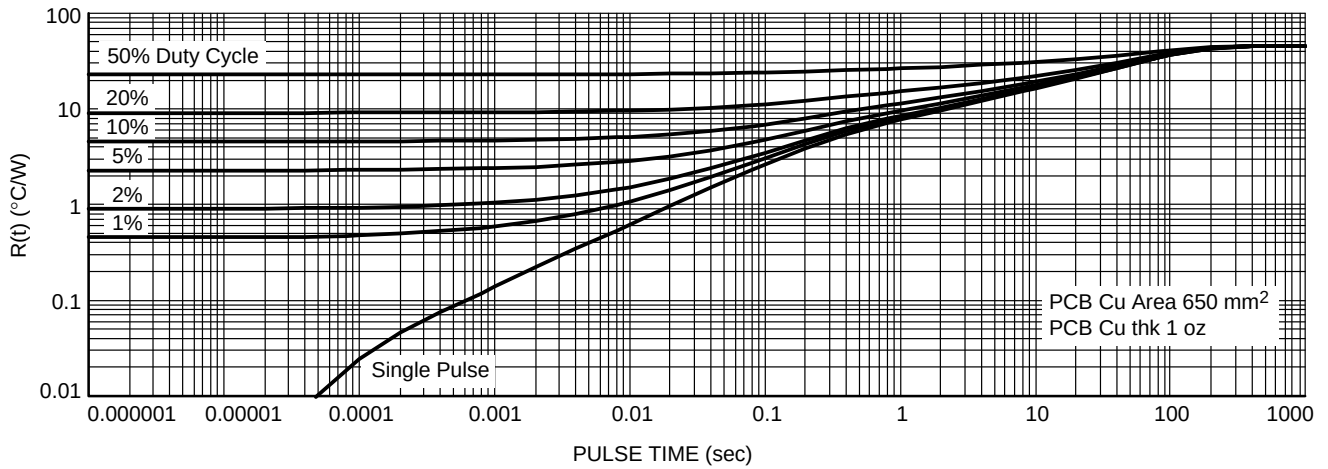


Figure 13. Thermal Characteristics

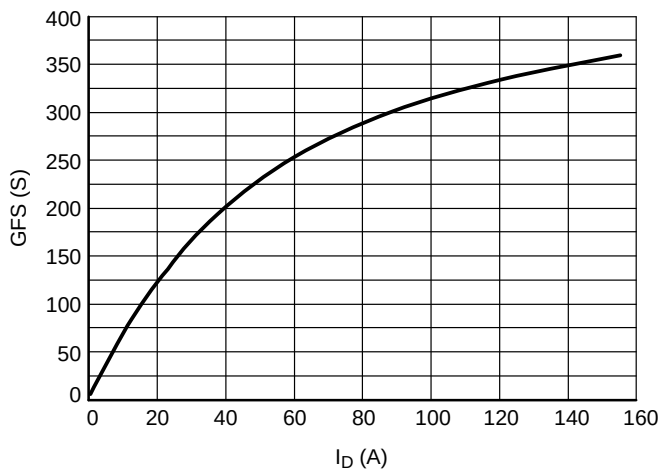


Figure 14. GFS vs. I_D

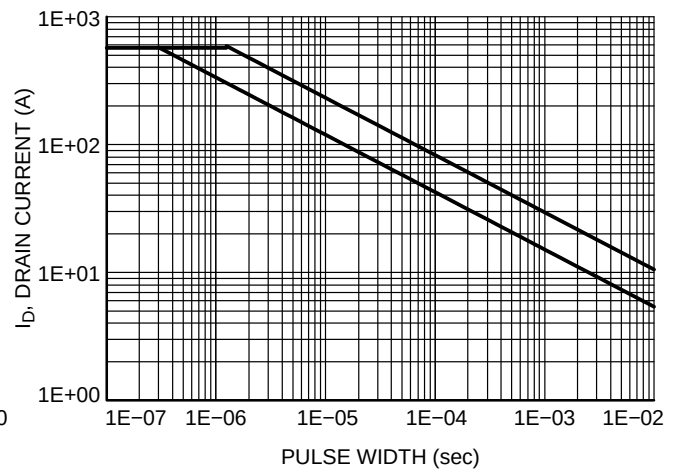


Figure 15. Avalanche Characteristics

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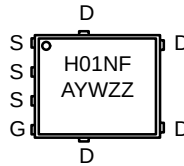
ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4H01NFT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel
NTMFS4H01NFT3G	SO8-FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



MARKING DIAGRAM

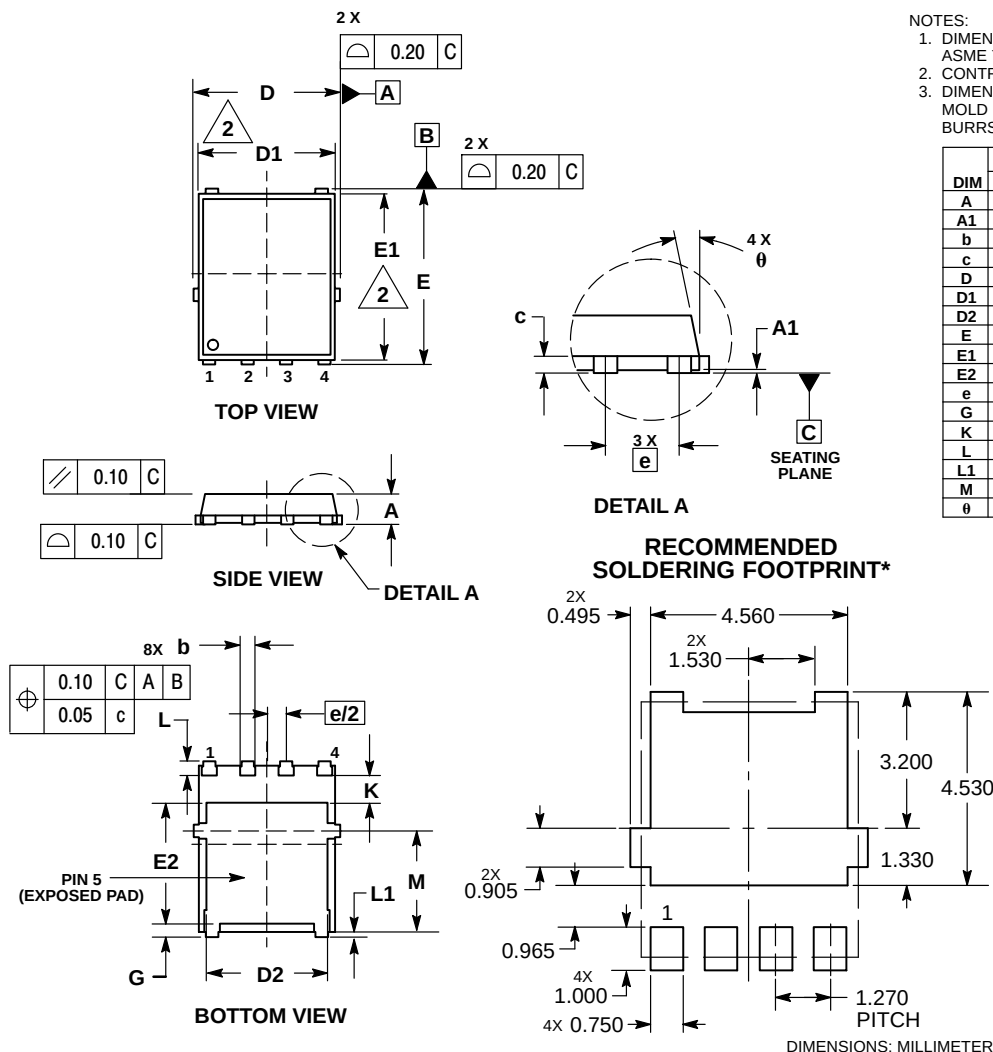


A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

NTMFS4H01NF

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE L



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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