



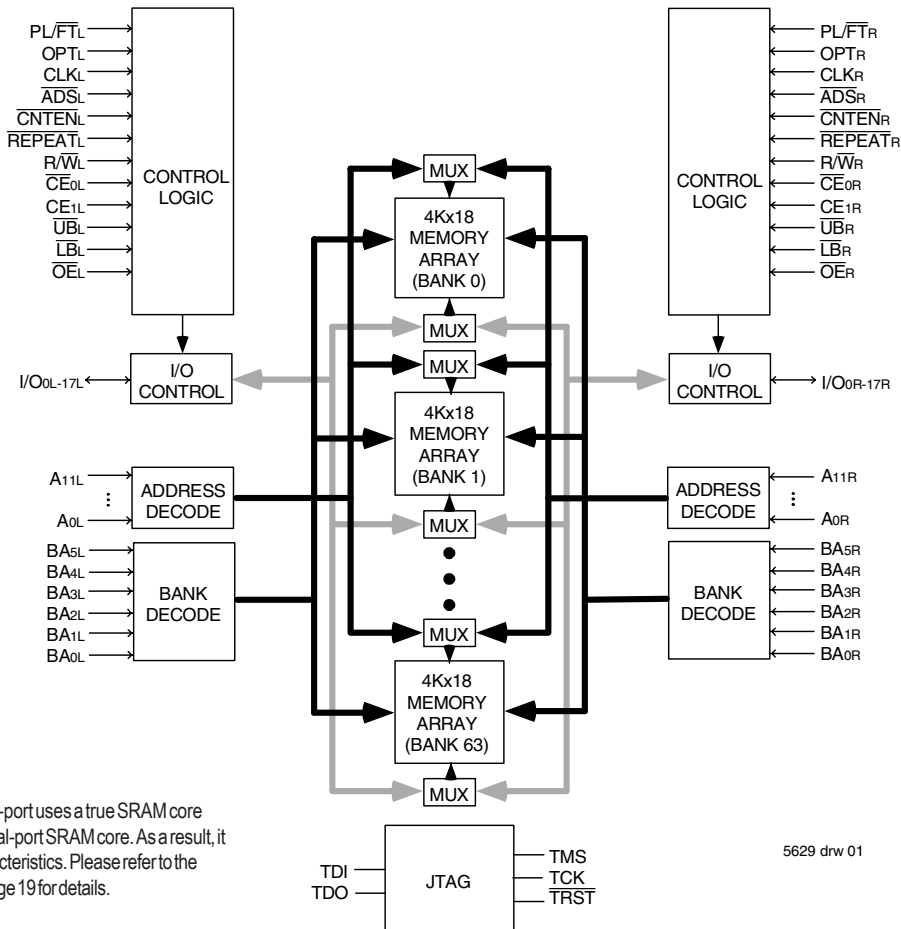
# HIGH-SPEED 3.3V 256K x 18 SYNCHRONOUS BANK-SWITCHABLE DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

IDT70V7319S

## Features:

- ◆ 256K x 18 Synchronous Bank-Switchable Dual-ported SRAM Architecture
  - 64 independent 4K x 18 banks
  - 4 megabits of memory on chip
- ◆ Bank access controlled via bank address pins
- ◆ High-speed data access
  - Commercial: 3.4ns (200MHz)/3.6ns (166MHz)/4.2ns (133MHz) (max.)
  - Industrial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
  - Fast 3.4ns clock to data out
- 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, 3.3V (±150mV) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to +85°C) is available at 166MHz and 133MHz
- ◆ Available in a 208-pin fine pitch Ball Grid Array (fpBGA) and 256-pin Ball Grid Array (BGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1
- ◆ Green parts available, see ordering information

## Functional Block Diagram



### NOTE:

1. The Bank-Switchable dual-port uses a true SRAM core instead of the traditional dual-port SRAM core. As a result, it has unique operating characteristics. Please refer to the functional description on page 19 for details.

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JUNE 2015

**Description:**

The IDT70V7319 is a high-speed 256Kx18 (4Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx18 banks. The device has two independent ports with separate control, address, and I/O pins for each port, allowing each port to access any 4Kx18 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via the bank address pins under the user's direct control.

Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data

register, the IDT70V7319 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. The dual chip enables also facilitate depth expansion.

The 70V7319 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V. Please refer also to the functional description on page 18.

**Pin Configuration<sup>(1,2,3,4)</sup>**

A1 IO9L	A2 NC	A3 VSS	A4 TDO	A5 NC	A6 BA4L	A7 BA0L	A8 A8L	A9 NC	A10 VDD	A11 CLKL	A12 CNTENL	A13 A4L	A14 A0L	A15 OPTL	A16 NC	A17 VSS									
B1 NC	B2 VSS	B3 NC	B4 TDI	B5 BA5L	B6 BA1L	B7 A9L	B8 NC	B9 CE0L	B10 VSS	B11 ADSL	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 I/O8L	B17 NC									
C1 VDDQL	C2 I/O9R	C3 VDDQR	C4 PL/FTL	C5 NC	C6 BA2L	C7 A10L	C8 UBL	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 I/O8R	C16 NC	C17 VSS									
D1 NC	D2 VSS	D3 I/O10L	D4 NC	D5 BA3L	D6 A11L	D7 A7L	D8 LBL	D9 VDD	D10 OEL	D11 REPEATL	D12 A3L	D13 VDD	D14 NC	D15 VDDQL	D16 I/O7L	D17 I/O7R									
E1 I/O11L	E2 NC	E3 VDDQR	E4 I/O10R	<p>70V7319BF BF-208<sup>(5)</sup></p> <p>208-Pin fpBGA Top View<sup>(6)</sup></p>									E14 I/O6L	E15 NC	E16 VSS	E17 NC									
F1 VDDQL	F2 I/O11R	F3 NC	F4 VSS										F14 VSS	F15 I/O6R	F16 NC	F17 VDDQR									
G1 NC	G2 VSS	G3 I/O12L	G4 NC										G14 NC	G15 VDDQL	G16 I/O5L	G17 NC									
H1 VDD	H2 NC	H3 VDDQR	H4 I/O12R										H14 VDD	H15 NC	H16 VSS	H17 I/O5R									
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS										J14 VSS	J15 VDD	J16 VSS	J17 VDDQR									
K1 I/O14R	K2 VSS	K3 I/O13R	K4 VSS										K14 I/O3R	K15 VDDQL	K16 I/O4R	K17 VSS									
L1 NC	L2 I/O14L	L3 VDDQR	L4 I/O13L										L14 NC	L15 I/O3L	L16 VSS	L17 I/O4L									
M1 VDDQL	M2 NC	M3 I/O15R	M4 VSS										M14 VSS	M15 NC	M16 I/O2R	M17 VDDQR									
N1 NC	N2 VSS	N3 NC	N4 I/O15L										N14 I/O1R	N15 VDDQL	N16 NC	N17 I/O2L									
P1 I/O16R	P2 I/O16L	P3 VDDQR	P4 NC										P5 TRST	P6 BA4R	P7 BA0R	P8 A8R	P9 NC	P10 VDD	P11 CLKR	P12 CNTENR	P13 A4R	P14 NC	P15 I/O1L	P16 VSS	P17 NC
R1 VSS	R2 NC	R3 I/O17R	R4 TCK										R5 BA5R	R6 BA1R	R7 A9R	R8 NC	R9 CE0R	R10 VSS	R11 ADSR	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 I/O0R	R17 VDDQR
T1 NC	T2 I/O17L	T3 VDDQL	T4 TMS										T5 NC	T6 BA2R	T7 A10R	T8 UBR	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 NC	T16 VSS	T17 NC
U1 VSS	U2 NC	U3 PL/FTL	U4 NC	U5 BA3R	U6 A11R	U7 A7R	U8 LBR	U9 VDD	U10 OER	U11 REPEATR	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 NC	U17 I/O0L									

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**NOTES:**

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Configuration<sup>(1,2,3,4)</sup> (con't.)70V7319BC  
BC-256<sup>(5)</sup>256-Pin BGA  
Top View<sup>(6)</sup>

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	TDI	NC	BA5L	BA2L	A11L	A8L	NC	CE1L	OE <sub>L</sub>	CNTEN <sub>L</sub>	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
NC	NC	TDO	NC	BA3L	BA0L	A9L	UB <sub>L</sub>	CE0L	R/W <sub>L</sub>	REPEAT <sub>L</sub>	A4L	A1L	VDD	NC	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
NC	I/O9L	VSS	BA4L	BA1L	A10L	A7L	NC	LB <sub>L</sub>	CLKL	ADSL	A6L	A3L	OPT <sub>L</sub>	NC	I/O8L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
NC	I/O9R	NC	PL/F <sub>T</sub> <sub>L</sub>	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	NC	NC	I/O8R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O10R	I/O10L	NC	VDDQL	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQR	NC	I/O7L	I/O7R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O11L	NC	I/O11R	VDDQL	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O6R	NC	I/O6L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
NC	NC	I/O12L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O5L	NC	NC
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
NC	I/O12R	NC	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	NC	NC	I/O5R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O13L	I/O14R	I/O13R	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O4R	I/O3R	I/O4L
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
NC	NC	I/O14L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	NC	NC	I/O3L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O15L	NC	I/O15R	VDDQR	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O2L	NC	I/O2R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O16R	I/O16L	NC	VDDQR	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O1R	I/O1L	NC
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
NC	I/O17R	NC	PL/F <sub>T</sub> <sub>R</sub>	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	NC	I/O0R	NC
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
NC	I/O17L	TMS	BA4R	BA1R	A10R	A7R	NC	LB <sub>R</sub>	CLKR	ADSR	A6R	A3R	NC	NC	I/O0L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
NC	NC	TRST	NC	BA3R	BA0R	A9R	UB <sub>R</sub>	CE0R	R/W <sub>R</sub>	REPEAT <sub>R</sub>	A4R	A1R	OPT <sub>R</sub>	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	TCK	NC	BA5R	BA2R	A11R	A8R	NC	CE1R	OE <sub>R</sub>	CNTEN <sub>R</sub>	A5R	A2R	A0R	NC	NC

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## NOTES:

- All VDD pins must be connected to 3.3V power supply.
- All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
- All VSS pins must be connected to ground supply.
- Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
- This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}, CE_{1L}$	$\overline{CE}_{0R}, CE_{1R}$	Chip Enables
$R/\overline{WL}$	$R/\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$BA_{0L} - BA_{5L}$	$BA_{0R} - BA_{5R}$	Bank Address <sup>(4)</sup>
$A_{0L} - A_{11L}$	$A_{0R} - A_{11R}$	Address
$I/O_{0L} - I/O_{17L}$	$I/O_{0R} - I/O_{17R}$	Data Input/Output
$CLK_L$	$CLK_R$	Clock
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat <sup>(3)</sup>
$\overline{LB}_L, \overline{UB}_L$	$\overline{LB}_R, \overline{UB}_R$	Byte Enables (9-bit bytes)
$V_{DDQL}$	$V_{DDQR}$	Power (I/O Bus) (3.3V or 2.5V) <sup>(1)</sup>
$OPT_L$	$OPT_R$	Option for selecting $V_{DDQX}$ <sup>(1,2)</sup>
$V_{DD}$		Power (3.3V) <sup>(1)</sup>
$V_{SS}$		Ground (0V)
$TDI$		Test Data Input
$TDO$		Test Data Output
$TCK$		Test Logic Clock (10MHz)
$TMS$		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

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### NOTES:

- $V_{DD}$ ,  $OPT_X$ , and  $V_{DDQX}$  must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- $OPT_X$  selects the operating voltage levels for the I/Os and controls on that port. If  $OPT_X$  is set to  $V_{IH}$  (3.3V), then that port's I/Os and controls will operate at 3.3V levels and  $V_{DDQX}$  must be supplied at 3.3V. If  $OPT_X$  is set to  $V_{IL}$  (0V), then that port's I/Os and address controls will operate at 2.5V levels and  $V_{DDQX}$  must be supplied at 2.5V. The  $OPT$  pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
- When  $\overline{REPEAT}_X$  is asserted, the counter will reset to the last valid address loaded via  $\overline{ADS}_X$ .
- Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e.,  $BA_{0L} - BA_{5L} \neq BA_{0R} - BA_{5R}$ ). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

**Truth Table I—Read/Write and Enable Control<sup>(1,2,3,4)</sup>**

$\overline{OE}^3$	CLK	$\overline{CE}_0$	$CE_1$	$\overline{UB}$	$\overline{LB}$	R/ $\overline{W}$	Upper Byte I/O <sub>9-17</sub>	Lower Byte I/O <sub>0-8</sub>	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D <sub>IN</sub>	Write to Lower Byte Only
X	↑	L	H	L	H	L	D <sub>IN</sub>	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D <sub>IN</sub>	D <sub>IN</sub>	Write to both Bytes
L	↑	L	H	H	L	H	High-Z	D <sub>OUT</sub>	Read Lower Byte Only
L	↑	L	H	L	H	H	D <sub>OUT</sub>	High-Z	Read UpperByte Only
L	↑	L	H	L	L	H	D <sub>OUT</sub>	D <sub>OUT</sub>	Read both Bytes
H	X	X	X	X	X	X	High-Z	High-Z	Outputs Disabled

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**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{REPEAT}$  are set as appropriate for address access. Refer to Truth Table II for details.
- $\overline{OE}$  is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

**Truth Table II—Address and Address Counter Control<sup>(1,2,7)</sup>**

Address	Previous Address	Addr Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{REPEAT}^{(6)}$	I/O <sup>(8)</sup>	MODE
A <sub>n</sub>	X	A <sub>n</sub>	↑	L <sup>(4)</sup>	X	H	D <sub>I/O</sub> (n)	External Address Used
X	A <sub>n</sub>	A <sub>n</sub> + 1	↑	H	L <sup>(5)</sup>	H	D <sub>I/O</sub> (n+1)	Counter Enabled—Internal Address generation
X	A <sub>n</sub> + 1	A <sub>n</sub> + 1	↑	H	H	H	D <sub>I/O</sub> (n+1)	External Address Blocked—Counter disabled (A <sub>n</sub> + 1 reused)
X	X	A <sub>n</sub>	↑	X	X	L <sup>(4)</sup>	D <sub>I/O</sub> (0)	Counter Set to last valid $\overline{ADS}$ load

5629 tbl 03

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/ $\overline{W}$ ,  $\overline{CE}_0$ ,  $CE_1$ ,  $\overline{UB}/\overline{LB}$  and  $\overline{OE}$ .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- $\overline{ADS}$  and  $\overline{REPEAT}$  are independent of all other memory control signals including  $\overline{CE}_0$ ,  $CE_1$  and  $\overline{UB}/\overline{LB}$ .
- The address counter advances if  $\overline{CNTEN} = V_{IL}$  on the rising edge of CLK, regardless of all other memory control signals including  $\overline{CE}_0$ ,  $CE_1$ ,  $\overline{UB}/\overline{LB}$ .
- When  $\overline{REPEAT}$  is asserted, the counter will reset to the last valid address loaded via  $\overline{ADS}$ . This value is not set at power-up: a known location should be loaded via  $\overline{ADS}$  during initialization if desired. Any subsequent  $\overline{ADS}$  access during operations will update the  $\overline{REPEAT}$  address location.
- The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0. Refer to Timing Waveform of Counter Repeat, page 17. Care should be taken during operation to avoid having both counters point to the same bank (i.e., ensure BA<sub>0L</sub> - BA<sub>5L</sub> ≠ BA<sub>0R</sub> - BA<sub>5R</sub>), as this condition will invalidate the access for both ports. Please refer to the functional description on page 18 for details.

## Recommended Operating Temperature and Supply Voltage<sup>(1)</sup>

Grade	Ambient Temperature	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	3.3V ± 150mV
Industrial	-40°C to +85°C	0V	3.3V ± 150mV

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## NOTE:

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

## Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

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## NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 150mV.

## Recommended DC Operating Conditions with V<sub>DDQ</sub> at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	2.4	2.5	2.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs)	1.7	—	V <sub>DDQ</sub> + 100mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	1.7	—	V <sub>DDQ</sub> + 100mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

5629 tbl 05a

## NOTES:

- Undershoot of V<sub>IL</sub> ≥ -1.5V for pulse width less than 10ns is allowed.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 100mV.
- To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IL</sub> (0V), and V<sub>DDQx</sub> for that port must be supplied as indicated above.

## Recommended DC Operating Conditions with V<sub>DDQ</sub> at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage	3.15	3.3	3.45	V
V <sub>DDQ</sub>	I/O Supply Voltage <sup>(3)</sup>	3.15	3.3	3.45	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage (Address & Control Inputs) <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IH</sub>	Input High Voltage - I/O <sup>(3)</sup>	2.0	—	V <sub>DDQ</sub> + 150mV <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.8	V

5629 tbl 05b

## NOTES:

- Undershoot of V<sub>IL</sub> ≥ -1.5V for pulse width less than 10ns is allowed.
- V<sub>TERM</sub> must not exceed V<sub>DDQ</sub> + 150mV.
- To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V<sub>IH</sub> (3.3V), and V<sub>DDQx</sub> for that port must be supplied as indicated above.

**Capacitance<sup>(1)</sup>****(TA = +25°C, F = 1.0MHz) PQFP ONLY**

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	8	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10.5	pF

5629 tbl 07

**NOTES:**

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C<sub>OUT</sub> also references C<sub>I/O</sub>.

**DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V<sub>DD</sub> = 3.3V ± 150mV)**

Symbol	Parameter	Test Conditions	70V7319S		Unit
			Min.	Max.	
I <sub>L</sub>	Input Leakage Current <sup>(1)</sup>	V <sub>DDQ</sub> = Max., V <sub>IN</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
I <sub>LO</sub>	Output Leakage Current <sup>(1)</sup>	$\overline{CE_0} = V_{IH}$ or $CE_1 = V_{IL}$ , V <sub>OUT</sub> = 0V to V <sub>DDQ</sub>	—	10	μA
V <sub>OL</sub> (3.3V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +4mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (3.3V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -4mA, V <sub>DDQ</sub> = Min.	2.4	—	V
V <sub>OL</sub> (2.5V)	Output Low Voltage <sup>(2)</sup>	I <sub>OL</sub> = +2mA, V <sub>DDQ</sub> = Min.	—	0.4	V
V <sub>OH</sub> (2.5V)	Output High Voltage <sup>(2)</sup>	I <sub>OH</sub> = -2mA, V <sub>DDQ</sub> = Min.	2.0	—	V

5629 tbl 08

**NOTES:**

- At V<sub>DD</sub> ≤ 2.0V leakages are undefined.
- V<sub>DDQ</sub> is selectable (3.3V/2.5V) via OPT pins. Refer to page 4 for details.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range<sup>(5)</sup> ( $V_{DD} = 3.3V \pm 150mV$ )

Symbol	Parameter	Test Condition	Version	70V7319S200 <sup>(7)</sup> Com'l Only		70V7319S166 <sup>(6)</sup> Com'l & Ind		70V7319S133 Com'l & Ind		Unit	
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	815	950	675	790	550	645	mA
			IND	S	—	—	675	830	550	675	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	340	410	275	340	250	295	mA
			IND	S	—	—	275	355	250	310	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ} - 0.2V$ , $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , $f = 0^{(2)}$	COM'L	S	10	30	10	30	10	30	mA
			IND	S	—	—	10	40	10	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	

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## NOTES:

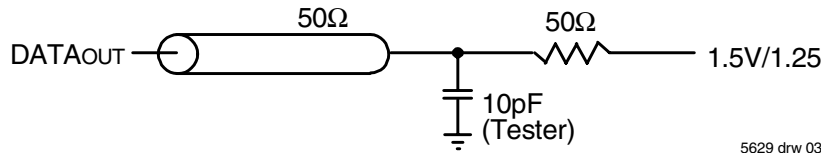
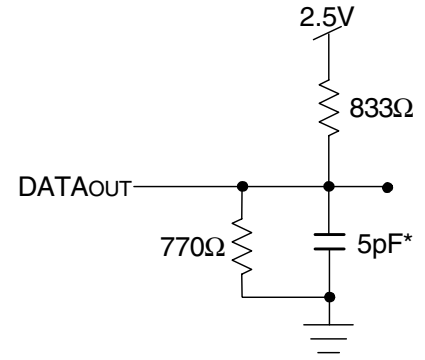
- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of  $1/t_{CYC}$ , using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$  for Typ, and are not production tested.  $I_{DDDC}(f=0) = 120mA$  (Typ).
- $\overline{CE}_X = V_{IL}$  means  $\overline{CE}_{0X} = V_{IL}$  and  $CE_{1X} = V_{IH}$   
 $\overline{CE}_X = V_{IH}$  means  $\overline{CE}_{0X} = V_{IH}$  or  $CE_{1X} = V_{IL}$   
 $\overline{CE}_X \leq 0.2V$  means  $\overline{CE}_{0X} \leq 0.2V$  and  $CE_{1X} \geq V_{DDQ} - 0.2V$   
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$  means  $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$  or  $CE_{1X} \leq 0.2V$   
"X" represents "L" for left port or "R" for right port.
- 166MHz Industrial Temperature not available in BF-208 package.
- This speed grade available when  $V_{DDQ} = 3.3V$  for a specific port (i.e.,  $OPTx = V_{IH}$ ). This speed grade available in BC-256 package only.



**AC Test Conditions (V<sub>DDQ</sub> - 3.3V/2.5V)**

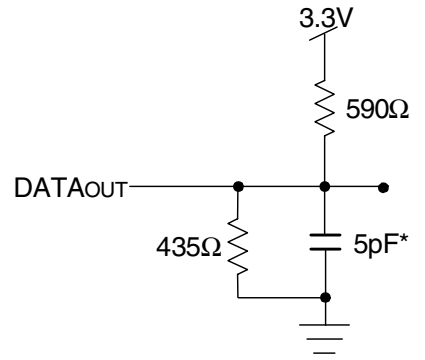
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5629 tbl 10



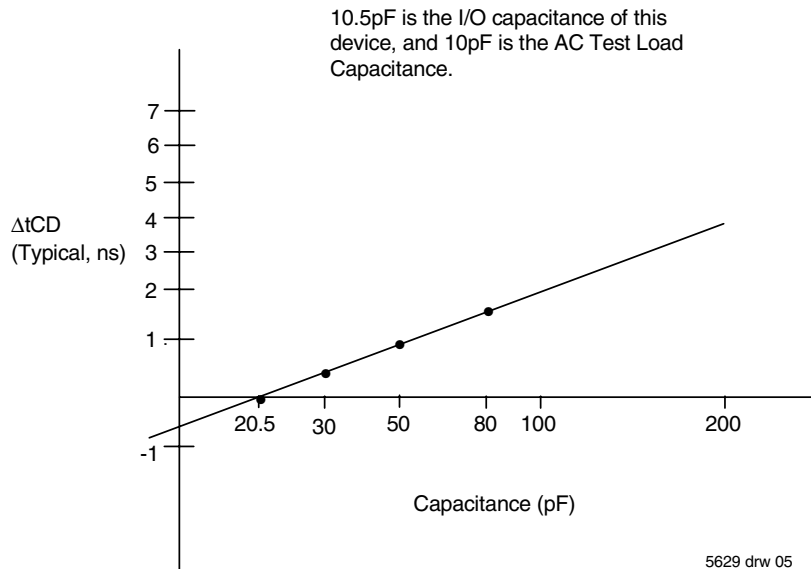
5629 drw 03

Figure 1. AC Output Test load.



5629 drw 04

Figure 2. Output Test Load  
(For t<sub>CKLZ</sub>, t<sub>CKHZ</sub>, t<sub>OLZ</sub>, and t<sub>OHZ</sub>).  
\*Including scope and jig.



5629 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(2,3)</sup> ( $V_{DD} = 3.3V \pm 150mV$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

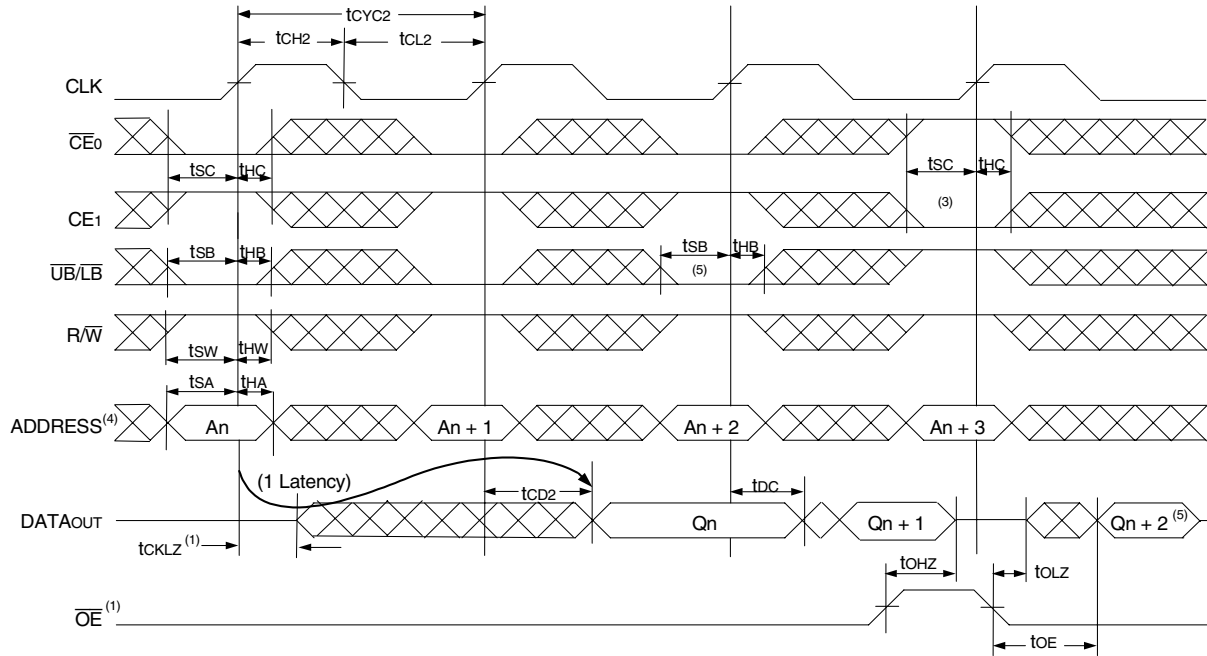
Symbol	Parameter	70V7319S200 <sup>(5)</sup> Com'1 Only		70V7319S166 <sup>(3,4)</sup> Com'1 & Ind		70V7319S133 <sup>(3)</sup> Com'1 & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC1</sub>	Clock Cycle Time (Flow-Through) <sup>(1)</sup>	15	—	20	—	25	—	ns
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined) <sup>(1)</sup>	5	—	6	—	7.5	—	ns
t <sub>CH1</sub>	Clock High Time (Flow-Through) <sup>(1)</sup>	5	—	6	—	7	—	ns
t <sub>CL1</sub>	Clock Low Time (Flow-Through) <sup>(1)</sup>	5	—	6	—	7	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined) <sup>(2)</sup>	2.0	—	2.1	—	2.6	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined) <sup>(1)</sup>	2.0	—	2.1	—	2.6	—	ns
t <sub>r</sub>	Clock Rise Time	—	1.5	—	1.5	—	1.5	ns
t <sub>f</sub>	Clock Fall Time	—	1.5	—	1.5	—	1.5	ns
t <sub>SA</sub>	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HA</sub>	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SW</sub>	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HW</sub>	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SD</sub>	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HD</sub>	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SAD</sub>	$\overline{ADS}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HAD</sub>	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>SRPT</sub>	$\overline{REPEAT}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t <sub>HRPT</sub>	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t <sub>OE</sub>	Output Enable to Data Valid	—	4.0	—	4.0	—	4.2	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t <sub>CD1</sub>	Clock to Data Valid (Flow-Through) <sup>(1)</sup>	—	10	—	12	—	15	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined) <sup>(1)</sup>	—	3.4	—	3.6	—	4.2	ns
t <sub>DC</sub>	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
<b>Port-to-Port Delay</b>								
t <sub>CO</sub>	Clock-to-Clock Offset	5.0	—	6.0	—	7.5	—	ns

5629 tbl 11

**NOTES:**

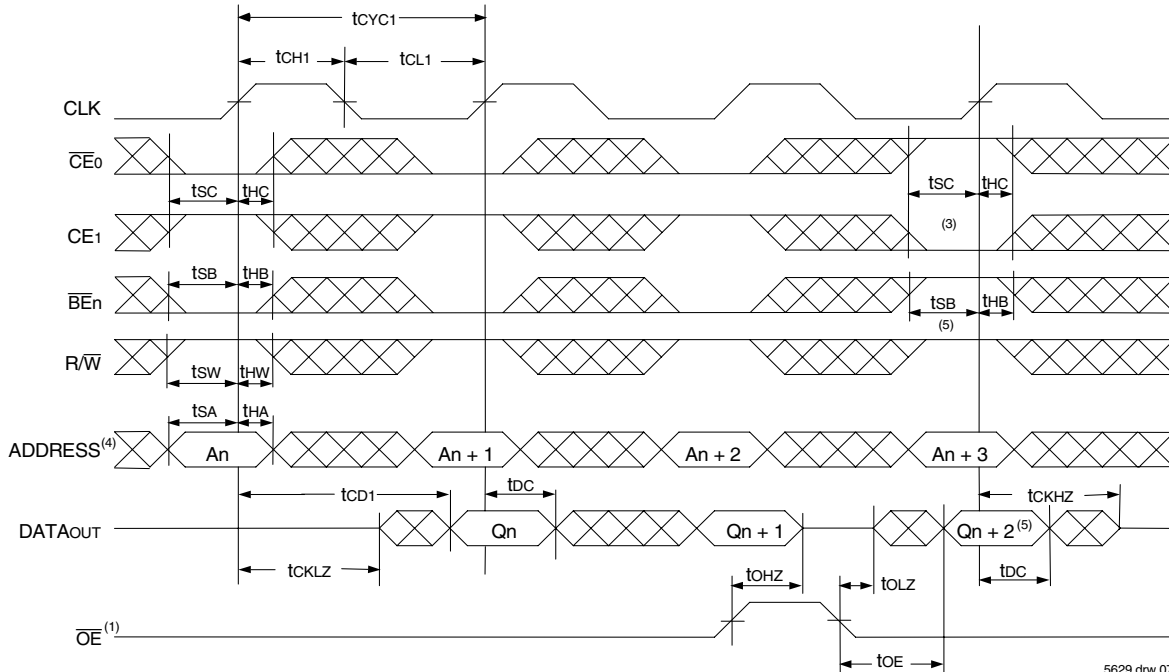
- The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both left and right ports when  $\overline{FT}/PIPEX = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPEX = V_{IL}$  for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ) and  $\overline{FT}/PIPEX$ .  $\overline{FT}/PIPEX$  should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of  $V_{DDQ}$  (3.3V/2.5V). See page 4 for details on selecting the desired operating voltage levels for each port.
- 166MHz Industrial Temperature not available in BF-208 package.
- This speed grade available when  $V_{DDQ} = 3.3V$  for a specific port (i.e.,  $OPTx = V_{IH}$ ). This speed grade available in BC-256 package only.

### Timing Waveform of Read Cycle for Pipelined Operation (ADS Operation) ( $PL/\overline{FT} \cdot x = V_{IH}$ )<sup>(2)</sup>



5629 drw 06

### Timing Waveform of Read Cycle for Flow-through Output ( $PL/\overline{FT} \cdot x = V_{IL}$ )<sup>(2,6)</sup>

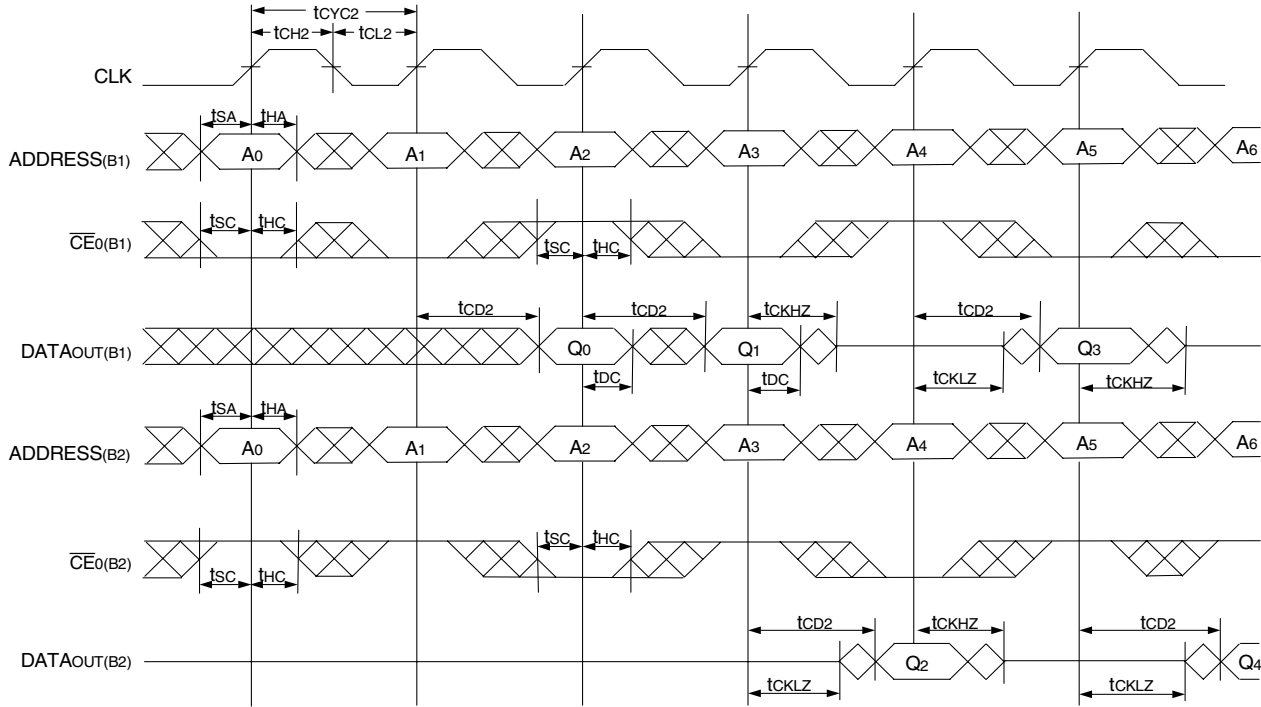


5629 drw 07

**NOTES:**

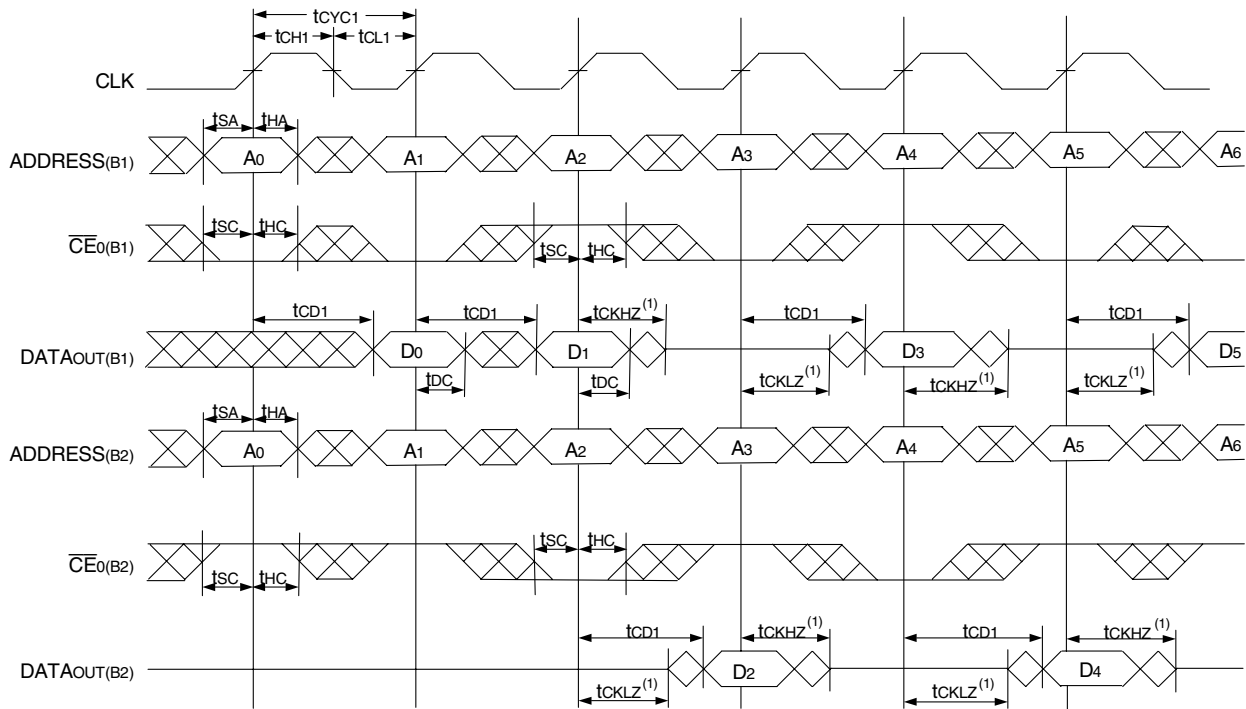
1.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2.  $ADS = V_{IL}$ ,  $CNTEN$  and  $REPEAT = V_{IH}$ .
3. The output is disabled (High-Impedance state) by  $\overline{CE0} = V_{IH}$ ,  $CE1 = V_{IL}$ ,  $\overline{UB/LB} = V_{IH}$  following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If  $\overline{UB/LB}$  was HIGH, then the appropriate Byte of DATAOUT for  $Qn + 2$  would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

### Timing Waveform of a Multi-Device Pipelined Read<sup>(1,2)</sup>



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### Timing Waveform of a Multi-Device Flow-Through Read<sup>(1,2)</sup>

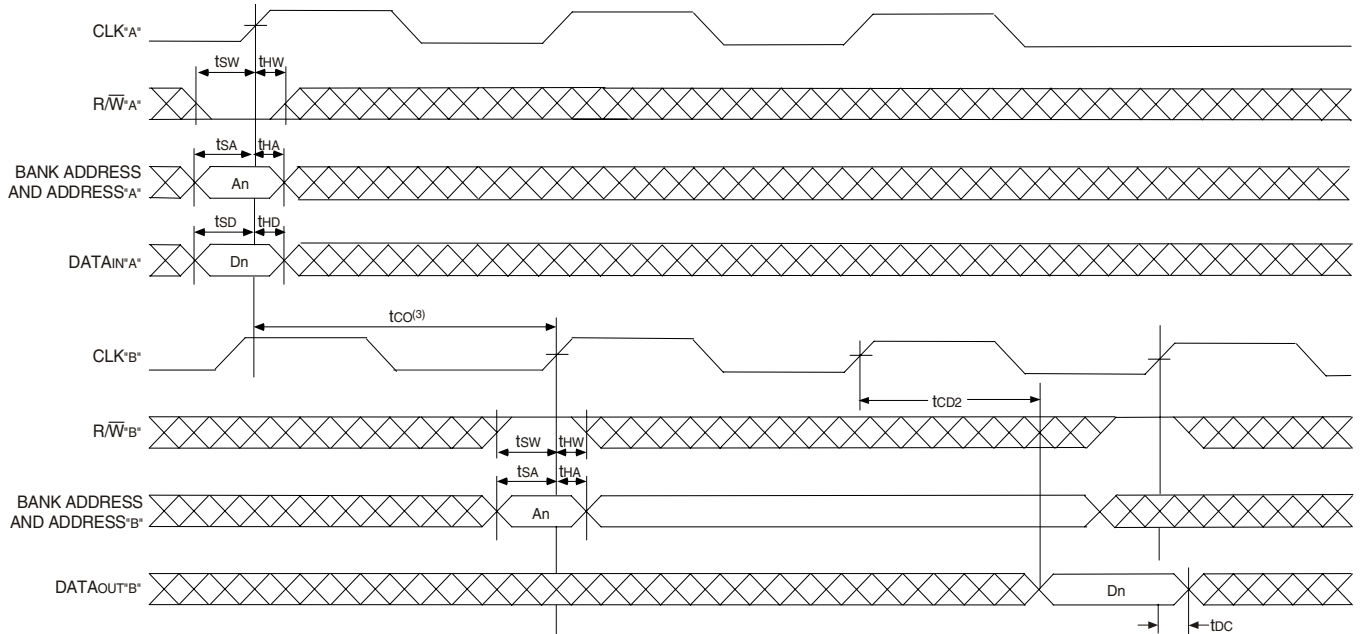


5629 drw 09

**NOTES:**

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V7319 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. UB/LB, OE, and ADS = VIL; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = VIH.

### Timing Waveform of Port A Write to Pipelined Port B Read(1,2,4)

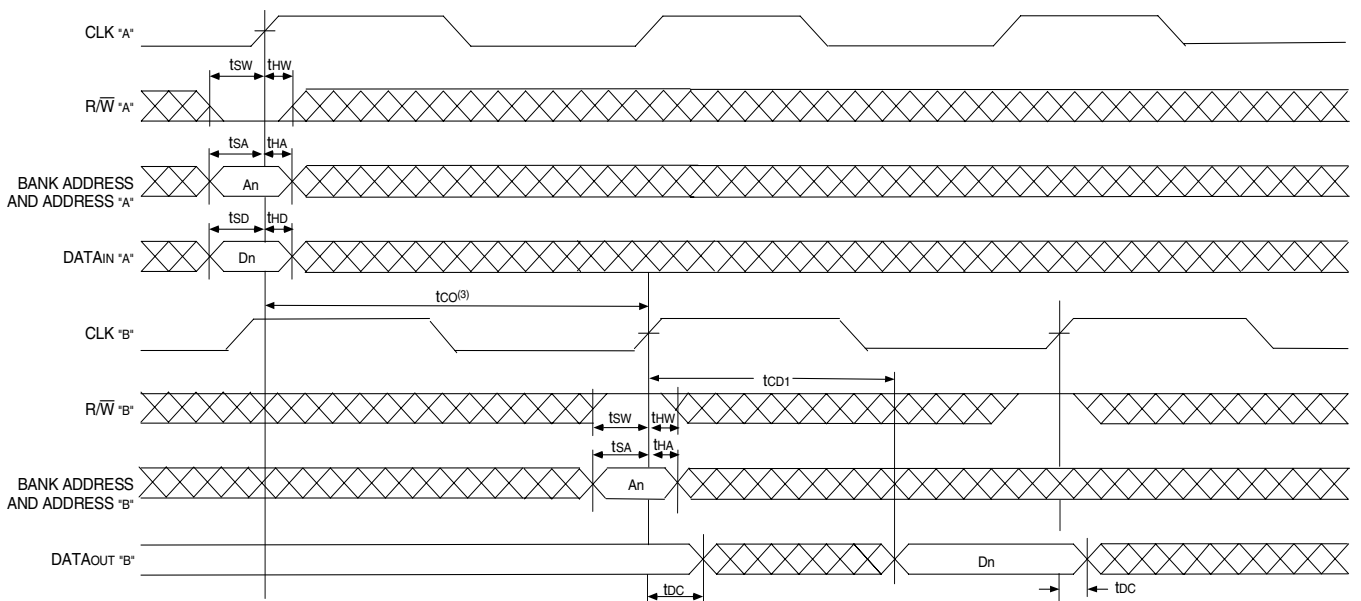


5629 drw 10

**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BEN}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} <$  minimum specified, then operations from both ports are INVALID. If  $t_{CO} \geq$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be  $t_{CO} + t_{CYC2} + t_{CD2}$ ).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

### Timing Waveform with Port-to-Port Flow-Through Read(1,2,4)

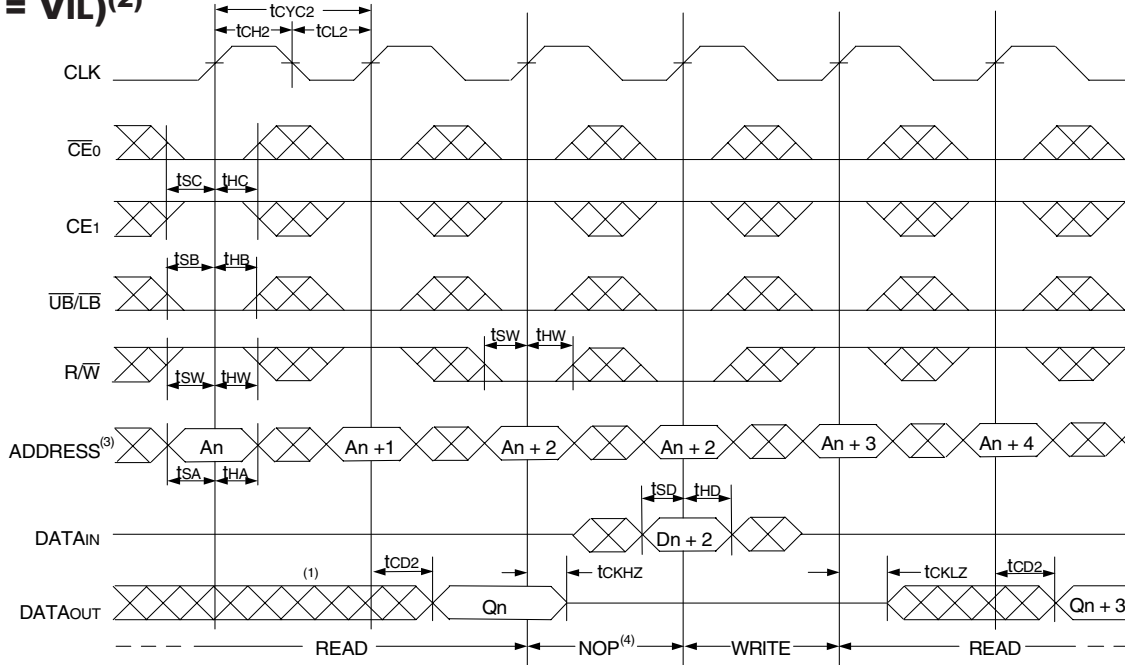


5622 drw 11

**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{BEN}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE}_1$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
3. If  $t_{CO} <$  minimum specified, then operations from both ports are INVALID. If  $t_{CO} \geq$  minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be  $t_{CO} + t_{CD1}$ ).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>

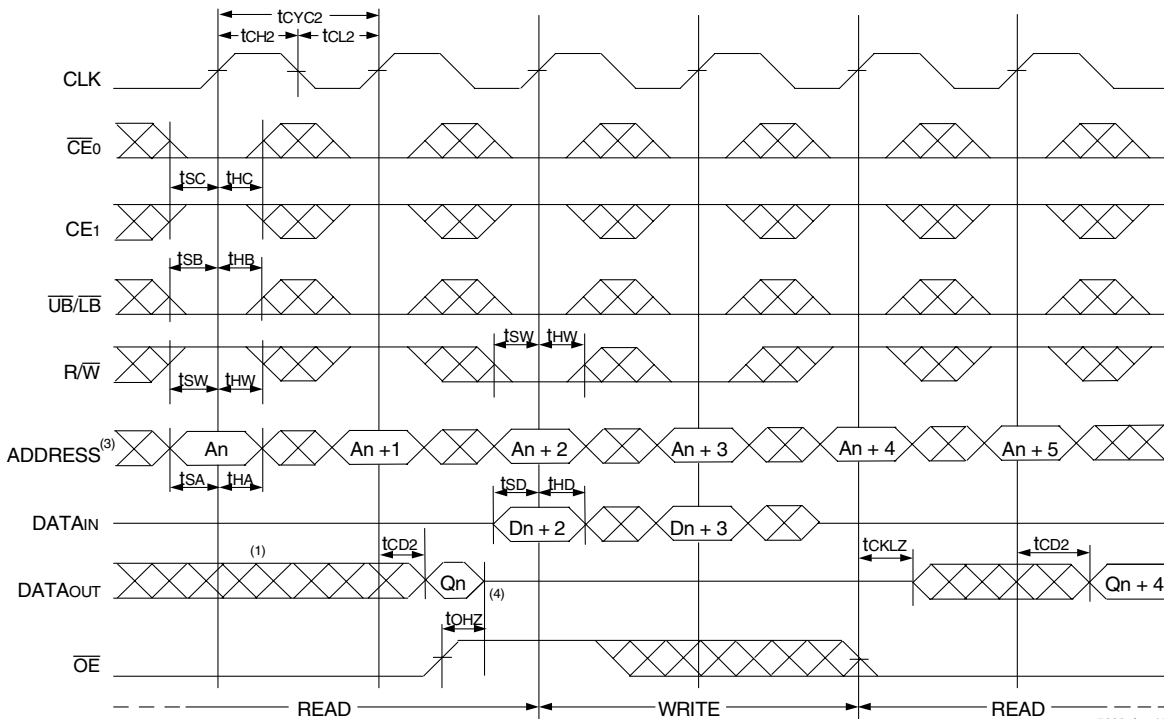


**NOTES:**

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{UB/LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ . "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>

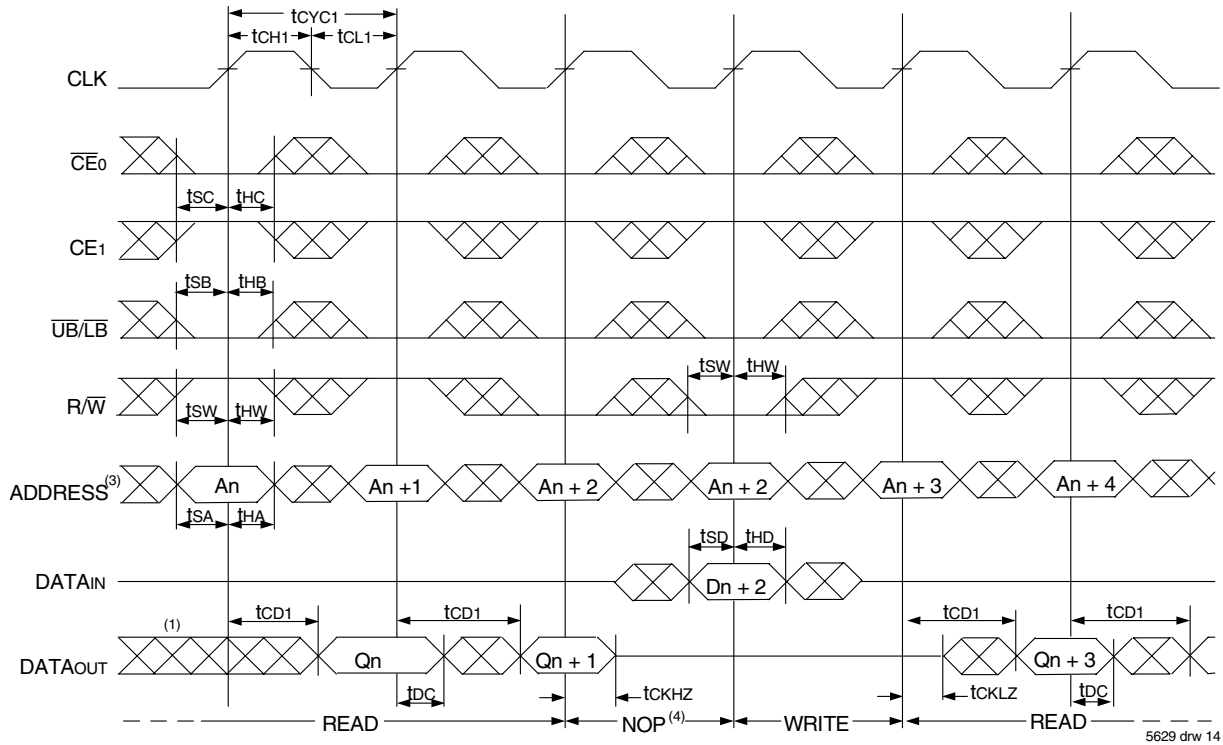


**NOTES:**

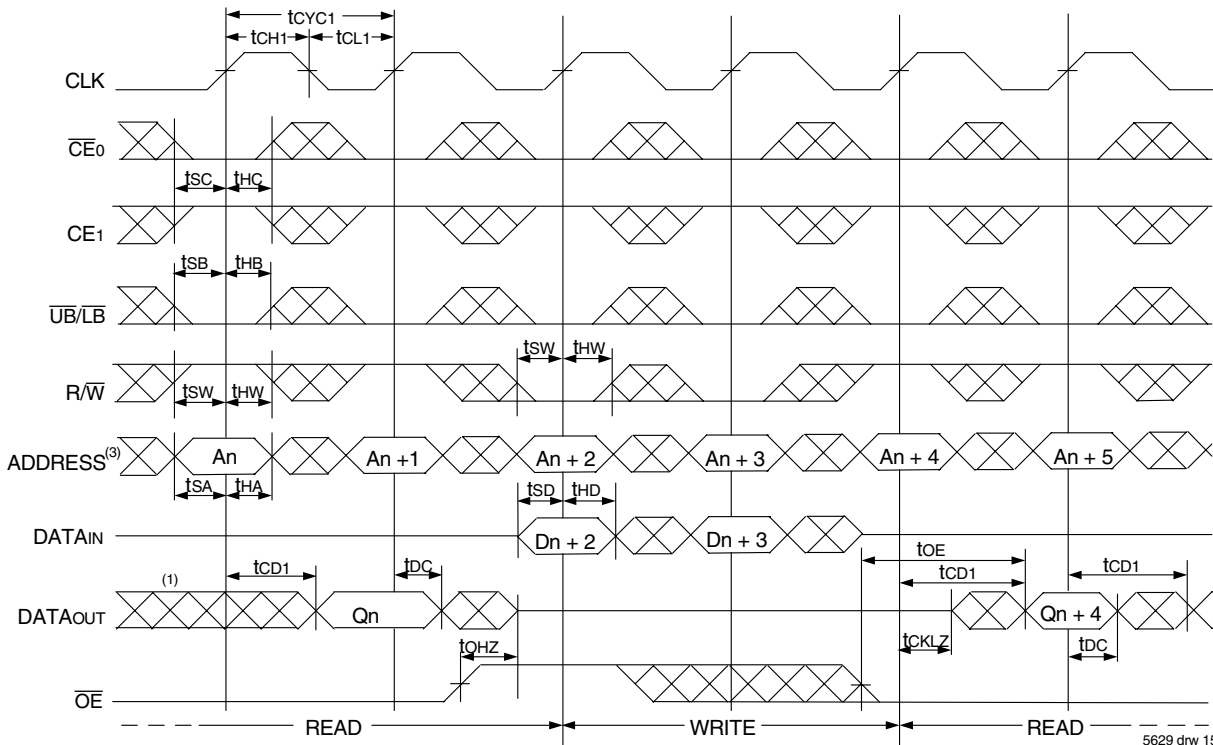
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE}_0$ ,  $\overline{UB/LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $CNTEN$ , and  $REPEAT = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(2)</sup>



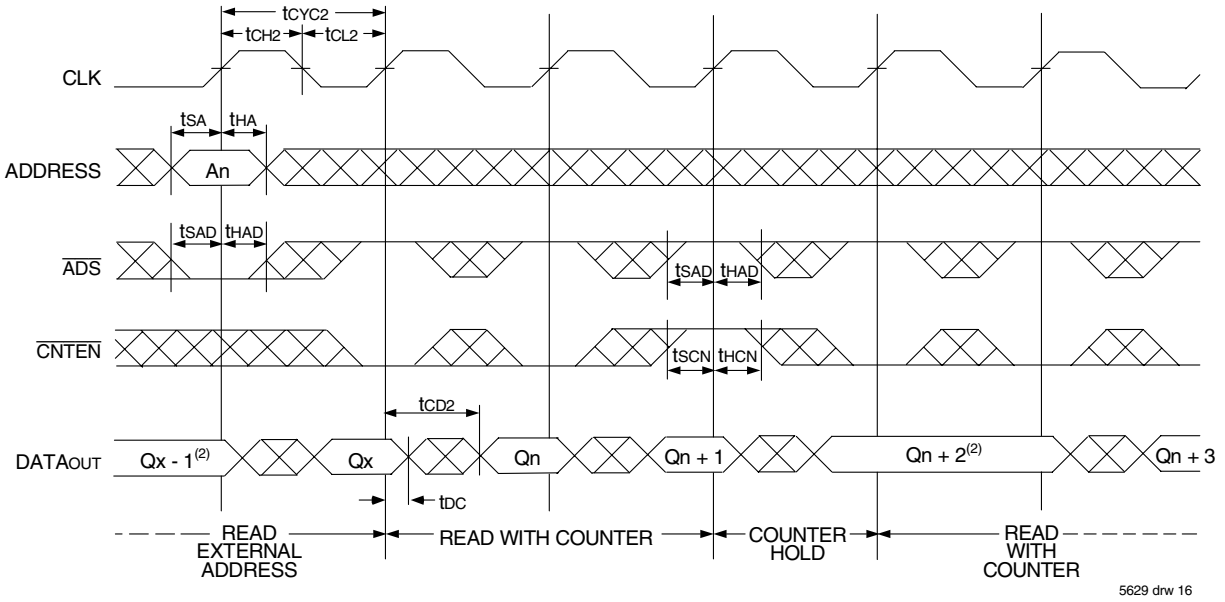
### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(2)</sup>



**NOTES:**

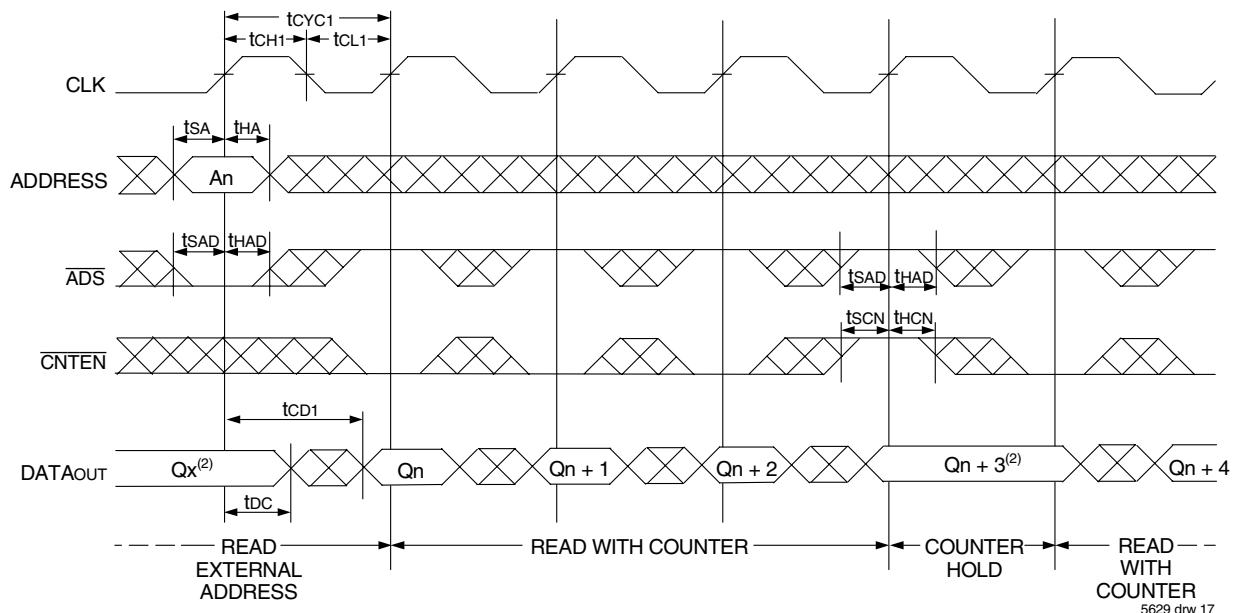
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2.  $\overline{CE0}$ ,  $\overline{UB/LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE1}$ ,  $\overline{CNTEN}$ , and  $\overline{REPEAT} = V_{IH}$ .
3. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

### Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



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### Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>



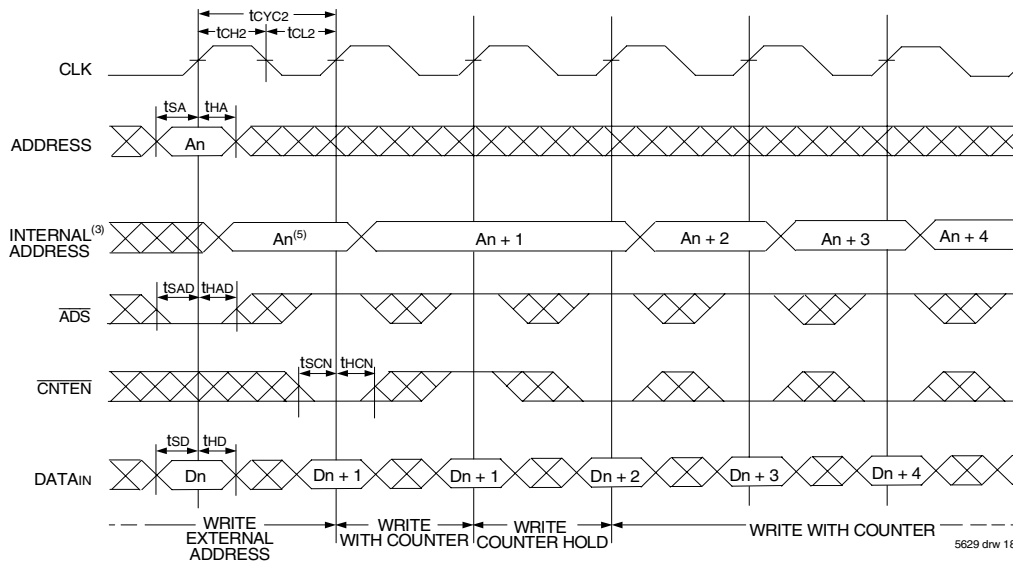
5629 drw 17

**NOTES:**

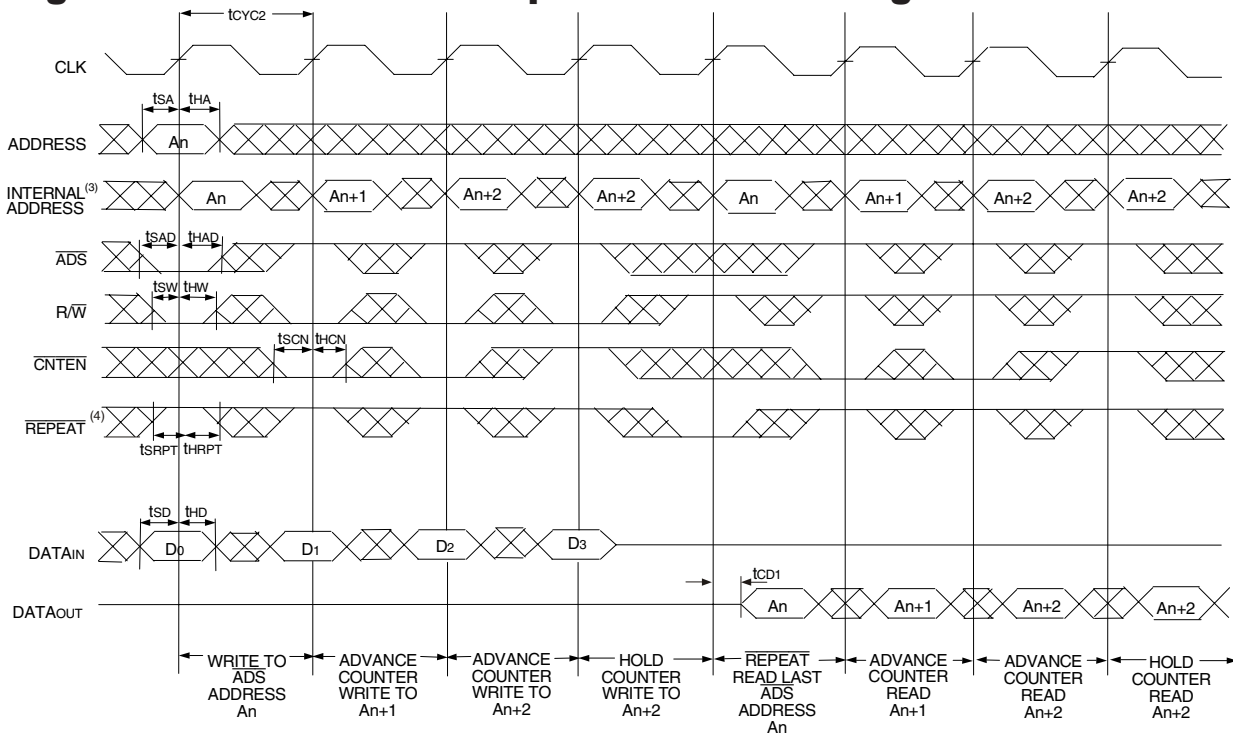
1.  $\overline{CE_0}, \overline{OE}, \overline{UB/LB} = V_{IL}; CE_1, R/\overline{W}, \text{ and } \overline{REPEAT} = V_{IH}.$
2. If there is no address change via  $\overline{ADS} = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.



## Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)<sup>(1,6)</sup>



## Timing Waveform of Counter Repeat for Flow Through Mode<sup>(2,6,7)</sup>



**NOTES:**

1.  $\overline{CE}_0, \overline{UB}/\overline{LB}$ , and  $R/\overline{W} = V_{IL}$ ;  $CE_1$  and  $\overline{REPEAT} = V_{IH}$ .
2.  $\overline{CE}_0, \overline{UB}/\overline{LB} = V_{IL}$ ;  $CE_1 = V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. No dead cycle exists during REPEAT operation. A READ or WRITE cycle may be coincidental with the counter REPEAT cycle: Address loaded by last valid  $\overline{ADS}$  load will be accessed. For more information on REPEAT function refer to Truth Table II.
5.  $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.
6. The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0.
7. For Pipelined Mode users should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

## Functional Description

The IDT70V7319 is a high-speed 256Kx18 (4 Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 4Kx18 banks. Based on a standard SRAM core instead of a traditional true dual-port memory core, this bank-switchable device offers the benefits of increased density and lower cost-per-bit while retaining many of the features of true dual-ports. These features include simultaneous, random access to the shared array, separate clocks per port, 166 MHz operating speed, full-boundary counters, and pinouts compatible with the IDT70V3319 (256Kx18) dual-port family.

The two ports are permitted independent, simultaneous access into separate banks within the shared array. Access by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., BA0L - BA5L ≠ BA0R - BA5R). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

The IDT70V7319 provides a true synchronous Dual-Port Static RAM

interface. Registered inputs provide minimal setup and hold times on address, data and all critical control inputs.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on  $\overline{CE_0}$  or a LOW on  $CE_1$  for one clock cycle will power down the internal circuitry on each port (individually controlled) to reduce static power consumption. Dual chip enables allow easier banking of multiple IDT70V7319s for depth expansion configurations. Two cycles are required with  $\overline{CE_0}$  LOW and  $CE_1$  HIGH to read valid data on the outputs.

## Depth and Width Expansion

The IDT70V7319 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V7319 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

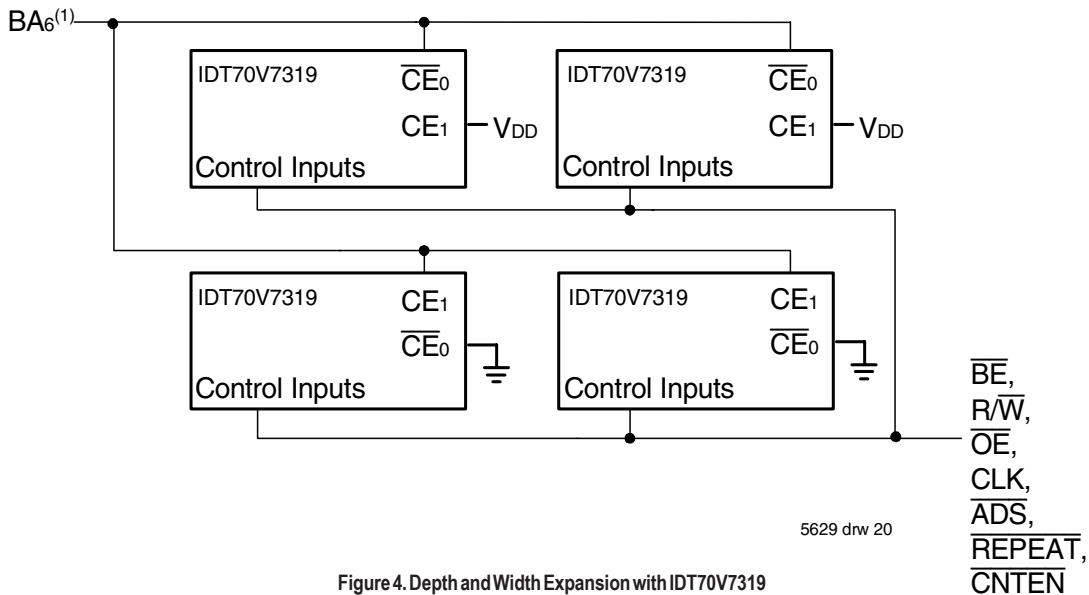


Figure 4. Depth and Width Expansion with IDT70V7319

**NOTE:**

1. In the case of depth expansion, the additional address pin logically serves as an extension of the bank address. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory within the shared array that is not currently being accessed by the opposite port (i.e., BA0L - BA6L ≠ BA0R - BA6R). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the parts within that bank may be corrupted (in the case that either or both parts are writing) or may result in invalid output (in the case that both ports are trying to read).

## JTAG Timing Specifications

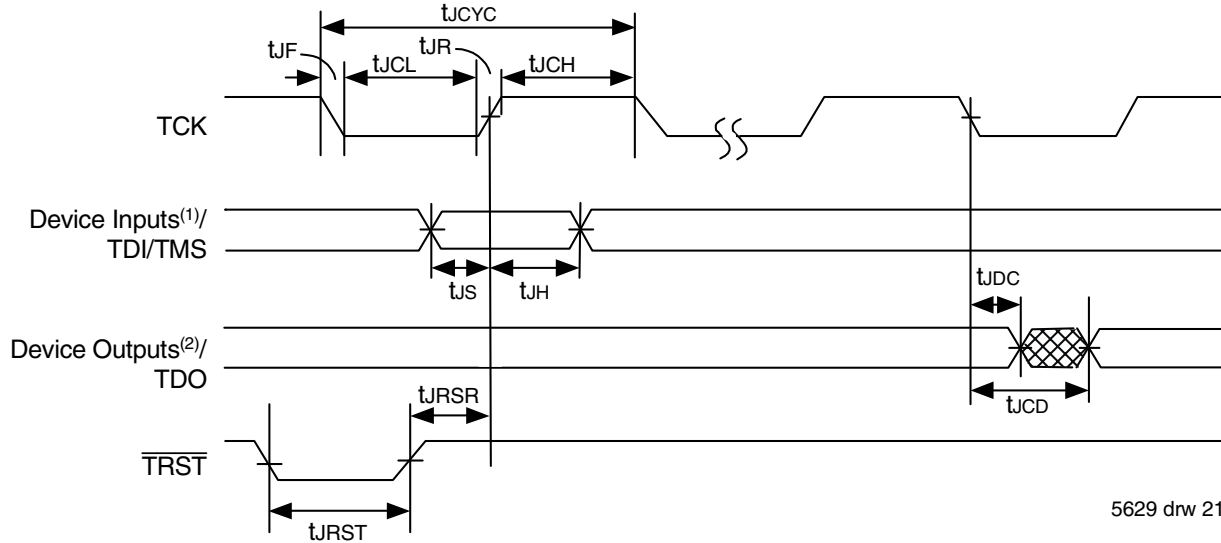


Figure 5. Standard JTAG Timing

**NOTES:**

1. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
2. Device outputs = All device outputs except TDO.

## JTAG AC Electrical Characteristics<sup>(1,2,3,4)</sup>

Symbol	Parameter	70V7319		
		Min.	Max.	Units
t <sub>JCYC</sub>	JTAG Clock Input Period	100	—	ns
t <sub>JCH</sub>	JTAG Clock HIGH	40	—	ns
t <sub>JCL</sub>	JTAG Clock Low	40	—	ns
t <sub>JR</sub>	JTAG Clock Rise Time	—	3 <sup>(1)</sup>	ns
t <sub>JF</sub>	JTAG Clock Fall Time	—	3 <sup>(1)</sup>	ns
t <sub>JRST</sub>	JTAG Reset	50	—	ns
t <sub>JRSR</sub>	JTAG Reset Recovery	50	—	ns
t <sub>JCD</sub>	JTAG Data Output	—	25	ns
t <sub>JDC</sub>	JTAG Data Output Hold	0	—	ns
t <sub>JS</sub>	JTAG Setup	15	—	ns
t <sub>JH</sub>	JTAG Hold	15	—	ns

5629 tbl 12

**NOTES:**

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

## Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x309	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5629 tbl 13

## Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5629 tbl 14

## System Interface Parameters

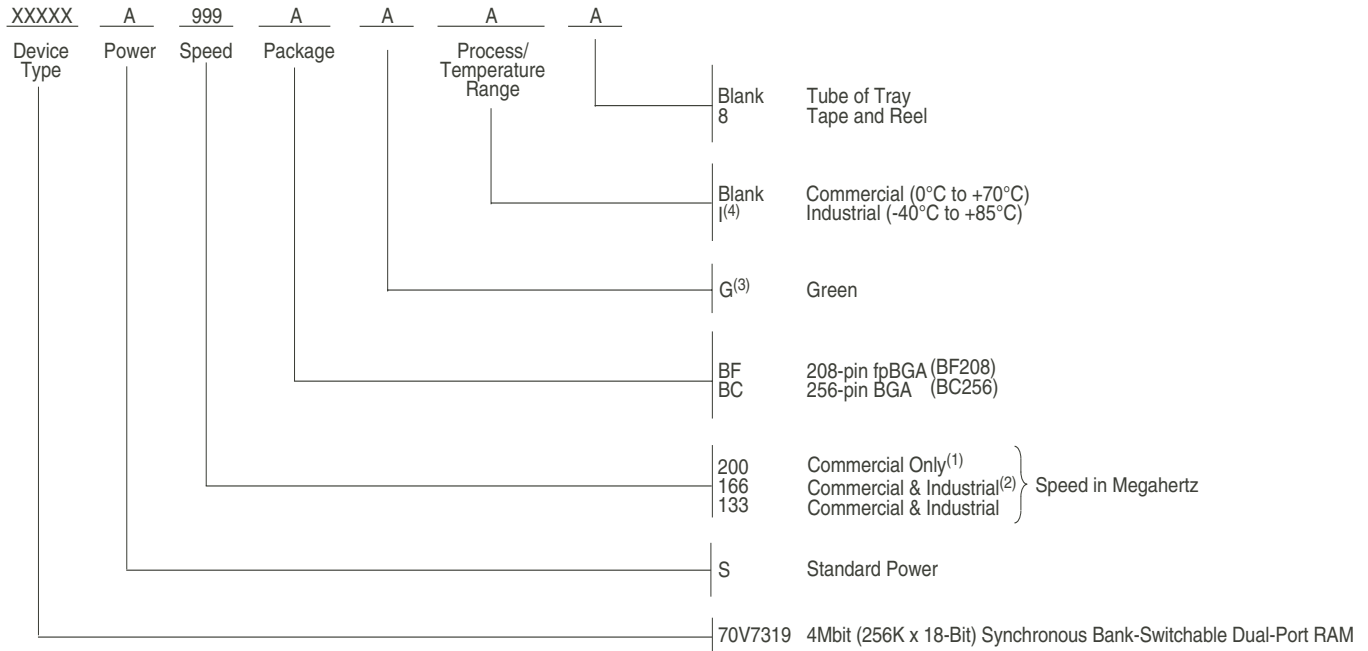
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs <sup>(1)</sup> . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs <sup>(2)</sup> and outputs <sup>(1)</sup> to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5629 tbl 15

### NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website ([www.idt.com](http://www.idt.com)), or by contacting your local IDT sales representative.

## Ordering Information



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### NOTES:

1. Available in BC-256 package only.
2. Industrial Temperature at 166Mhz not available in BF-208 package.
3. Green parts available. For specific speeds, packages and powers contact your local sales office.
4. Contact your local sales office for industrial temp range for other speeds, packages and powers.

## Datasheet Document History

- 01/05/00: Initial Public Offering
- 06/20/01: Page 1 Added JTAG information for TQFP package  
Page 4 & 22 Changed TQFP package from DA to DD  
Corrected Pin number on TQFP package from 100 to 110  
Page 20 Increased t<sub>CD</sub> from 20ns to 25ns
- 08/06/01: Page 4 Changed body size for DD package from 22mm x 22mm x 1.6mm to 20mm x 20mm x 1.4mm  
Page 9 Changed I<sub>SB3</sub> values for commercial and industrial DC Electrical Characteristics
- 11/20/01: Page 2, 3 & 4 Added date revision for pin configurations  
Page 11 Changed t<sub>OE</sub> value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05  
Page 1 & 22 Replaced ™ logo with ® logo
- 03/18/02: Page 1, 9, 11 & 22 Added 200MHz specification  
Page 9 Tightened power numbers in DC Electrical Characteristics  
Page 14 Changed waveforms to show INVALID operation if t<sub>CO</sub> < minimum specified  
Page 1 - 22 Removed "Preliminary" status
- 12/04/02: Page 9, 11 & 22 Designated 200Mhz speed grade available in BC-256 package only
- 01/16/04: Page 11 Added byte enable setup time and byte enable hold time parameters and values to all speed grades in the AC Electrical Characteristics Table
- 07/25/08: Page 9 Corrected a typo in the DC Chars table
- 01/29/09: Page 22 Removed "IDT" from orderable part number

**Datasheet Document History (con't)**

- 04/20/10: Page 1 Added green availability to features  
Page 21 Added green indicator to ordering information  
Removed the DD 144-pin TQFP (DD-144) Thin Quad Flatpack per PDN: F-08-01
- 06/15/15: Page 2, & 21 The package code for BF-208 changed to BF208 to match the standard package codes  
Page 2 & 3 Removed the date from all of the pin configurations BF208 & BC256  
Page 21 Added T&R indicator and updated footnotes to Ordering Information

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