

PSMN2R0-30BL

N-channel 30 V 2.1 m Ω logic level MOSFET in D2PAK Rev. 1 — 20 March 2012 Product

Product data sheet

1. **Product profile**

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see <u>Figure 1</u>	[1]	-	-	100	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	-	211	W
T _j	junction temperature			-55	-	175	°C
Static char	acteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 °C;$ see Figure 12; see Figure 11		-	2.51	2.9	mΩ
		$V_{GS} = 10 \text{ V; } I_D = 25 \text{ A; } T_j = 25 \text{ °C;}$ see Figure 11		-	1.79	2.1	mΩ
Dynamic c	haracteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; V_{DS} = 15 \text{ V};$		-	16	-	nC
Q _{G(tot)}	total gate charge	see <u>Figure 13</u> ; see <u>Figure 14</u>		-	55	-	nC
Avalanche	ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω ; unclamped		-	-	555	mJ

^[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

	•			
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain		mbb076 S
			SOT404 (D2PAK)	

^[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R0-30BL	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R0-30BL	PSMN2R0-30BL

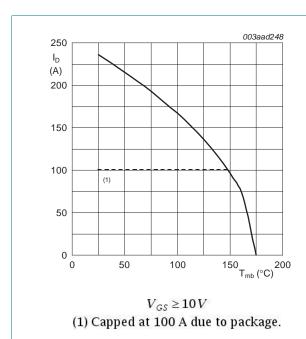
Limiting values

Limiting values Table 5.

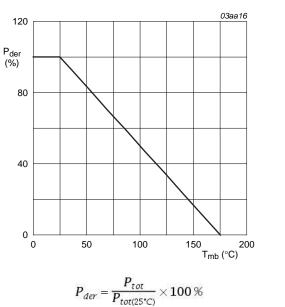
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _i ≥ 25 °C; T _i ≤ 175 °C		-	30	V
V_{DGR}	drain-gate voltage	$T_j \ge 25$ °C; $T_j \le 175$ °C; $R_{GS} = 20$ kΩ		-	30	V
V_{GS}	gate-source voltage			-20	20	V
I _D	drain current	$V_{GS} = 10 \text{ V; } T_{mb} = 100 \text{ °C; see } \frac{\text{Figure 1}}{}$	<u>[1]</u>	-	100	Α
		$V_{GS} = 10 \text{ V; } T_{mb} = 25 \text{ °C; see } \frac{\text{Figure 1}}{\text{Model}}$	<u>[1]</u>	-	100	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 ^{\circ}C$; see Figure 3		-	943	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 2</u>		-	211	W
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-dr	ain diode					
Is	source current	T _{mb} = 25 °C	<u>[1]</u>	-	100	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	943	Α
Avalanche	ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; V_{sup} ≤ 30 V; R_{GS} = 50 Ω; unclamped		-	555	mJ
		<u> </u>				

[1] Continuous current is limited by package.

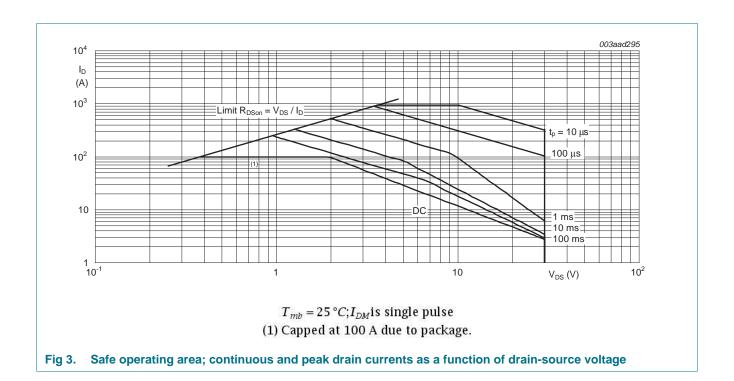


Normalized continuous drain current as a function of mounting base temperature



Normalized total power dissipation as a function of mounting base temperature

PSMN2R0-30BL



6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <u>Figure 4</u>	-	0.41	0.71	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	maximum foot print; mounted on a printed circuit board	-	50	-	K/W

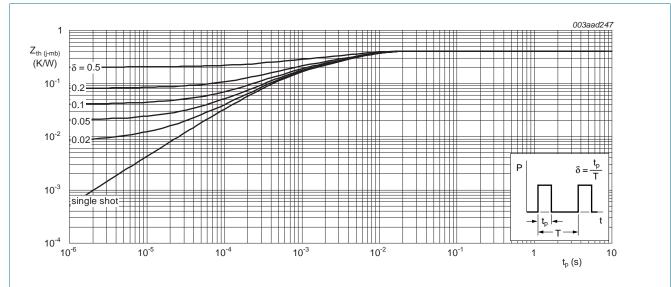


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	racteristics					
V _{(BR)DSS}	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ °C}$; see Figure 9; see Figure 10	1.3	1.7	2.15	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_j = 175$ °C; see Figure 10	0.5	-	-	V
		$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; $T_j = -55 \text{ °C}$; see Figure 10	-	-	2.45	V
I _{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.02	3	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ °C}$	-	-	70	μΑ
I _{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nΑ
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	10	100	nΑ
R _{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_{D} = 25 A; T_{j} = 25 °C; see <u>Figure 11</u>	-	2.47	2.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12; see Figure 11	-	3.4	4	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ see Figure 12; see Figure 11	-	2.51	2.9	mΩ
	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ see Figure 11	-	1.79	2.1	mΩ	
R _G	gate resistance	f = 1 MHz	-	0.78	-	Ω
Dynamic o	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	107	-	nC
		$I_D = 25 \text{ A}$; $V_{DS} = 15 \text{ V}$; $V_{GS} = 10 \text{ V}$; see Figure 13; see Figure 14	-	117	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$	-	55	-	nC
Q _{GS}	gate-source charge	see Figure 13; see Figure 14	-	17	-	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	11	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	6	-	nC
Q_{GD}	gate-drain charge		-	16	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$; $V_{DS} = 25 \text{ V}$; see <u>Figure 13</u> ; see <u>Figure 14</u>	-	2.6	-	V
C _{iss}	input capacitance	V _{DS} = 15 V; V _{GS} = 0 V; f = 1 MHz;	-	6810	-	pF
C _{oss}	output capacitance	T _j = 25 °C; see <u>Figure 15</u>	-	1410	-	pF
C _{rss}	reverse transfer capacitance		-	650	-	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 15 \text{ V}; R_L = 0.5 \Omega; V_{GS} = 4.5 \text{ V};$	-	63	-	ns
t _r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	125	-	ns
t _{d(off)}	turn-off delay time		-	111	-	ns
	fall time			59		ns

Table 7. Characteristics ...continued

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-dr	ain diode					
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 16</u>	-	0.76	1.2	V
t _{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A/}\mu\text{s}$;	-	49	-	ns
Q _r	recovered charge	$V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}$	-	66	-	nC

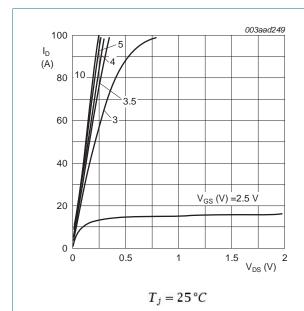
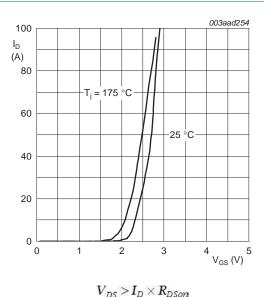


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



 $V_{DS} > I_D \wedge I_{DSon}$



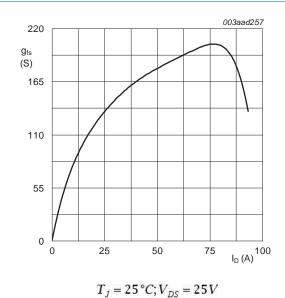
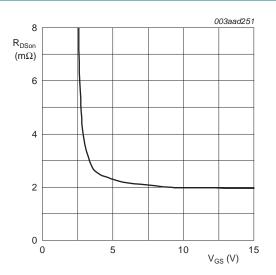


Fig 7. Forward transconductance as a function of drain current; typical values



 $T_j=25\,^{\circ}C; I_D=15A$

Fig 8. Drain source on-state resistance as a function of gate-source voltage; typical values

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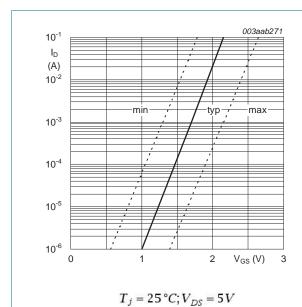


Fig 9. Sub-threshold drain current as a function of gate-source voltage

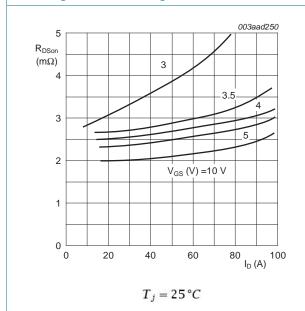
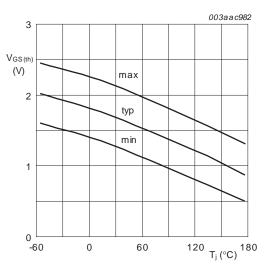


Fig 11. Drain-source on-state resistance as a function of drain current; typical values



 $I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature

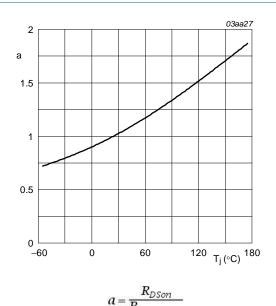
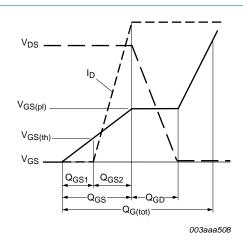


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

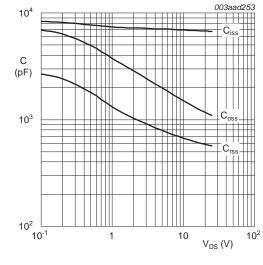


10 003aad255 V_{GS} (V) 8 V_{DS} = 15V 6 4 2 Q_G (nC) 120

 $T_j=25\,^{\circ}C; I_D=25A$

Fig 13. Gate charge waveform definitions





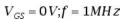


Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

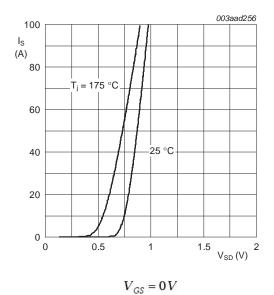
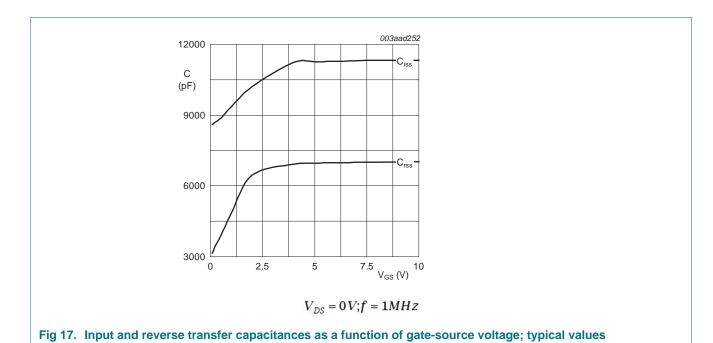


Fig 16. Source current as a function of source-drain voltage; typical values



8. Package outline

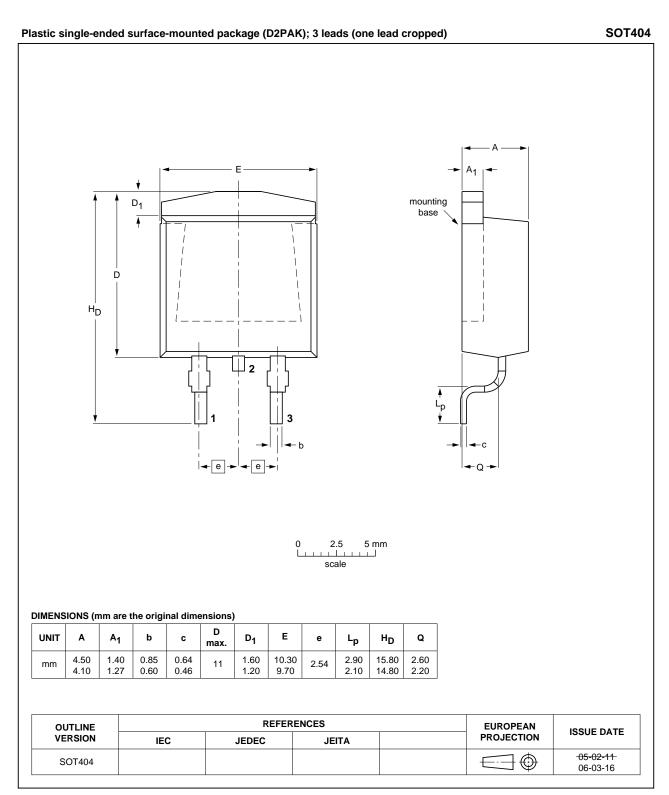


Fig 18. Package outline SOT404 (D2PAK)

Revision history

Table 8. **Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN2R0-30BL v.1	20120320	Product data sheet	-	-

10. Legal information

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Document status[1] [2]	Product status[3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Nexperia

N-channel 30 V 2.1 mΩ logic level MOSFET in D2PAK

12. Contents

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