GaN EiceDRIVER™ product family

Single-channel functional and reinforced isolated gate-drive ICs for high voltage enhancement-mode GaN HEMTs

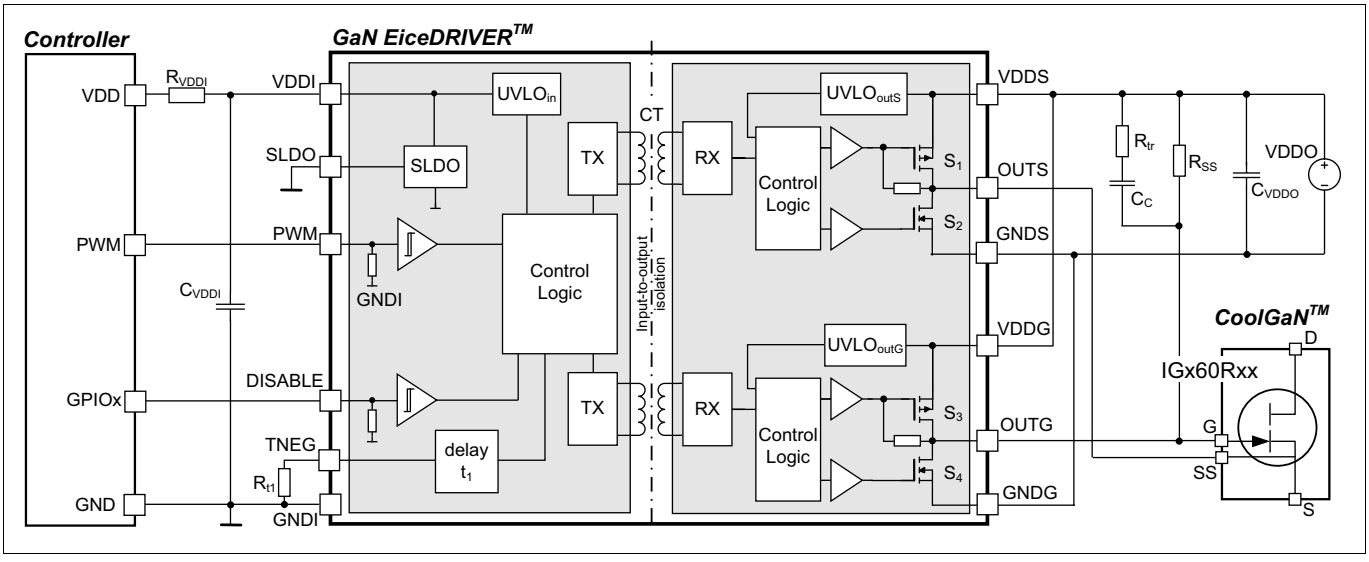
Features

- Dedicated gate driver ICs for Infineon's high voltage GaN power switches (CoolGaN™, X-GaN™)
  - low driving impedance (on-resistance 0.85 Ω source, 0.35 Ω sink)
  - resistor programmable gate current (typ. 10 mA) in steady "on" state
  - programmable negative gate voltage to completely avoid spurious turn-on
- Single output supply voltage (typ. 8 V, floating)
- Switching behavior independent of duty-cycle (2"off" voltage levels)
- Differential concept to ensure negative gate drive voltage under any condition
- Fast input-to-output propagation (37 ns) with excellent stability (+7/-6 ns)
- Galvanic input-to-output isolation based on coreless transformer (CT) technology
- Common mode transient immunity (CMTI) > 200 V/ns
- 3 package versions
  - 1EDF5673K: 13-pin LGA (5 x 5 mm, PG-TFLGA-13-1) for functional isolation (1.5 kV)
  - 1EDF5673F: 16-pin P-DSO (150 mil, PG-DSO-16-11) for functional isolation (1.5 kV)
  - 1EDS5663H: 16-pin P-DSO (300 mil, PG-DSO-16-30) for safe isolation (6 kV)
- Fully qualified according to JEDEC for Industrial Applications

Description

CoolGaN™ and similar GaN switches require a continuous gate current of a few mA in their "on" state. Besides, due to low threshold voltage and extremely fast switching transients, a negative "off" voltage level may be needed. The widely used RC-coupled gate driver fulfils these requirements, however it suffers from a duty-cycle dependence of switching dynamics and the lack of negative gate drive in specific situations.

Infineon's GaN EiceDRIVER™ solves these issues with very low effort. The two output stages shown below enable a zero "off" level to eliminate any duty-cycle dependence. In addition, the differential topology is able to provide negative gate drive without the need for a negative supply voltage. However, it requires a floating supply voltage not compatible with bootstrapping.



Potential applications

- High-voltage AC/DC conversion
- High-voltage DC/DC conversion

in server and telecom SMPS

Isolation and safety approval

- 1EDS5663H with reinforced isolation: certification by VDE, UL, CSA, CQC according to
  - DIN V VDE V 0884-10 (2006-12) with V_{IOTM} = 8 kV_{pk}, V_{IOSM} = 6.25 kV_{pk} (tested at 10 kV_{pk})
  - UL1577 (Ed. 5) with V_{ISO} = 5700 V_{RMS}
  - IEC60950 and IEC602386 system standards and corresponding CQC certificates
- 1EDF5673K and 1EDF5673F with functional isolation: production test with 1.5 kV for 10 ms

Product versions

In accordance with the isolation classification for primary and secondary side control, GaN EiceDRIVER™ is available in different package versions

Table 1 GaN EiceDRIVER™ product family overview

Part number	Package	Source/sink output resistance	Input-to-output isolation			
			Isolation class	Rating	Surge testing	Safety certification[1)]
1EDF5673K	LGA-13 5 x 5 mm	0.85 Ω / 0.35 Ω	functional	V_{IO} = 1.5 kV_{DC}	n.a	n.a
1EDF5673F	DSO-16 150 mil	0.85 Ω / 0.35 Ω	functional	V_{IO}= 1.5 kV_{DC}	n.a	n.a
1EDS5663H	DSO-16 300 mil	0.85 Ω / 0.35 Ω	reinforced (safe)	V_{IOTM} = 8 kV_{pk} (VDE0884-10) V_{ISO} = 5.7 kV_{RMS} (UL1577)	V_{IOSM} >10 kV_{pk} (IEC60065)	VDE0884-10 UL1577 IEC60950, 62386 (CQC)

1) certification pending

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1 Pin configuration and description

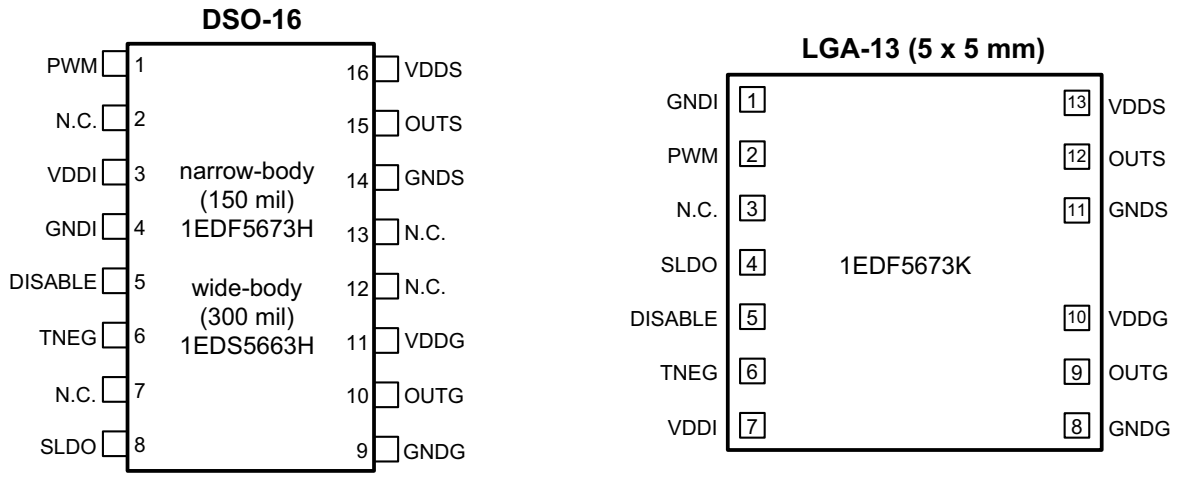


Figure 1 Pin configuration for DSO-16 and LGA-13 packages, top view

Table 2 Pin description

Pin DSO	Pin LGA	Symbol	Description
1	2	PWM	Input signal (default state Low) Controls switching sequence at OUTG and OUTS
2	3	N.C.	Do not connect
3	7	VDDI	Input supply voltage (+3.3 V)
4	1	GNDI	Input GND
5	5	DISABLE	Input signal (defaut state Low) Logic High is equivalent to a low state at PWM input
6	6	TNEG	Resistor programmable input to control the duration t_1 of negative "off" level (**Figure 4**); $t_1 = R_{t1}$ * 1.8 pF
7	7	N.C.	Not connected
8	4	SLDO	N.C. or connected to VDDI: applied voltate (3.3 V) directly used as input supply voltage Connected to GNDI: Internal shunt regulator activated
9	8	GNDG	Ground for OUTG
10	9	OUTG	Output connectd to GaN gate
11	10	VDDG	Positive supply for gate connected output stage
12	-	N.C.	Not connected
13	-	N.C.	Not connected
14	11	GNDS	Ground for OUTS (has to be connected with GNDG)
15	12	OUTS	Output connected to GaN source
16	13	VDDS	Positive supply voltage for source connected output stage (has to be connected with VDDG)

2 Background and system description

Although gallium nitride high electron mobility transistors (GaN HEMTs) with ohmic pGaN gate like Infineon's 600 V CoolGaN™ power switches are robust enhancement-mode ("normally-on") devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in **Figure 2**. In the steady "on" state a continuous gate current is required to achieve stable operating conditions. The switch is "normally-off", but the threshold voltage V_{th} is rather low (~ +1 V). This is why in certain applications a negative gate voltage $-V_N$, typically in the range of several volts, is required to safely keep the switch "off" (**Figure 2**b).

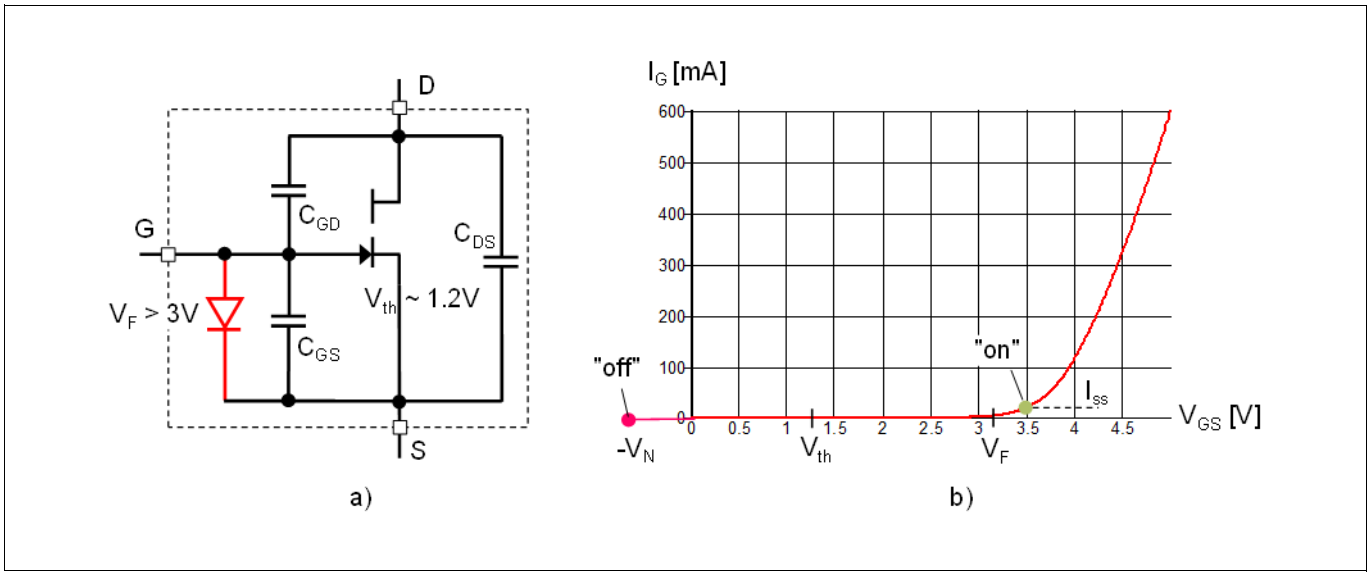


Figure 2 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

Obviously the transistor in **Figure 2** cannot be driven like a conventional MOSFET due to the need for a steady-state "on" current I_{ss} and a negative "off" voltage $-V_N$. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. To avoid a dedicated driver with 2 separate "on" paths and bipolar supply voltage, the solution depicted in **Figure 3** is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{on} and R_{off}, respectively, are connected to the gate via a coupling capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current, I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the "on"-state C_C is charged to the difference of driver supply V_{DDO} and diode voltage V_F. When switching to the "off" state, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value

(2.1)

$$-V_N = -\frac{C_C \cdot (V_{DDO} - V_F) - Q_{Gtot}}{C_C + C_{GS}}$$

with Q_{Gtot} denoting the total switching gate charge (e.g. 5 nC for a 70 mΩ transistor). V_N can thus be controlled by proper choice of V_{DDO} and C_C. During the "off" state the negative V_{GS} decreases, as C_C is discharged via R_{ss}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 s range. The negative gate voltage at the end of the "off" phase (V_{Nf} in **Figure 3**b) thus depends on the "off" duration. It lowers the effective driver voltage for the following switching "on" event, resulting in a dependence of switching dynamics on frequency and duty cycle as one drawback of this approach.

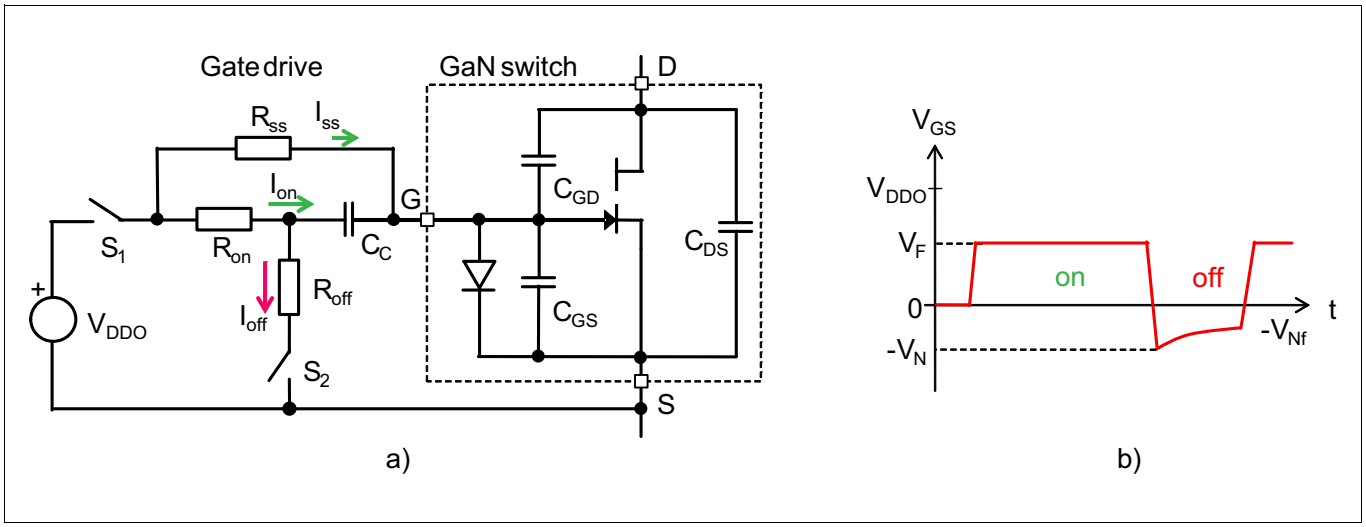


Figure 3 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

A second problem might happen if two switches are used alternately in a half-bridge configuration. In normal operation always one of the switches is "on", and before switching on the other one, it has to be switched off, thereby generating the negative gate voltage V_N. The usually short period with both switches "off" (dead time t_d) does not cause a significant increase of V_{GS}. If, however, there is by any reason a longer period with both switches in "off" state (e.g. during system start-up, burst mode operation etc.), both coupling capacitors (C_C) will be discharged. Thus, for the first switching pulse after such an extended non-switching period no negative voltage is available. This could lead to increased transistor stress or even instabilities due to spurious turn-on effects in half-bridge topologies.

To solve the problems described above, a shape of V_{GS} like the one in **Figure 4**b) would be required rather than the one in **Figure 4**a) which results from the simple RC circuit. As explained, a negative V_{GS} might be needed for safe "off" states during the switching transients, but it should be as low as possible. Due to the lack of a physical body diode any negative V_{GS} adds to the voltage drop of a GaN transistor in reverse polarity (diode operation) thereby increasing the conduction losses during dead time. Thus in the idealized waveform of **Figure 4**b) V_{GS} is switched to the minimum required V_N for a constant time t_1 longer than the system dead time t_d. After that V_{GS} is switched back to zero to ensure identical conditions for the next switch "on" event and to minimize losses from diode operation. If, however, an "off" state lasts for a time t_2 significantly longer than a normal switching period $1/f_{sw}$ (e.g. several µs), V_{GS} should be switched again to $-V_N$ to avoid the described "first pulse" problem.

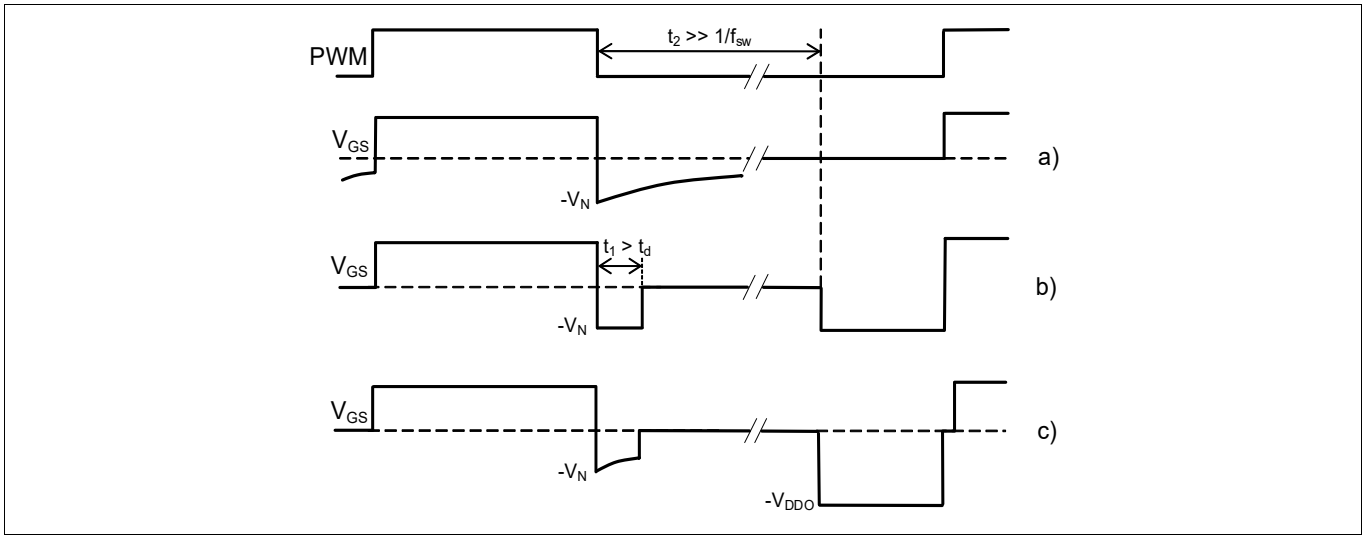


Figure 4 V_{GS} voltage waveforms with RC circuit (a), improved (b) and proposed shape (c)

The conceptual goal of the GaN EiceDRIVER™ is to provide the gate voltage of **Figure 4**b) or a functional equivalent without significantly increasing driving complexity. This is achieved by slightly modifying the gate drive waveform as depicted in **Figure 4**c). The "off" level after a long deadtime need not be the optimized negative voltage $-V_N$, it could also be the more negative level $-V_{DDO}$. As these "first pulse" situations happen very rarely compared with regular switching cycles, the resulting higher reverse voltage drop has negligible effect on switching losses.

Although going from the 3-level signal of **Figure 4**b) to the 4 levels of **Figure 4**c) seems to increase complexity at first sight, this is finally not true. Waveform **Figure 4**c) can be realized in a very convenient way, if V_N is generated by the RC network as described above. Then the differential driver concept of **Figure 5**a) with switch control signals as given in **Figure 5**b) is able to fulfil all discussed requirements with lowest effort: a single supply voltage, 4 switches and 4 connection pins are sufficient.

As mentioned, utilizing $-V_{DDO}$ instead of $-V_N$ only during extended "off"-phases has no impact on switching losses. However, care has to be taken when switching on again, because C_C is fully charged to V_{DDO} in this "first pulse" situation and no current flow is possible via the capacitive path. With the standard switching-on scheme (open S_1 / close S_2) the transient current thus would be limited to the small steady-state current. To achieve a faster turn-on, C_{GS} will be discharged prior to the "on"-transient by switching on S_3 for a short time t_3 before initiating the actual "on"-transient via S_1 and S_2. A t_3-duration of typically 20 ns is sufficient.

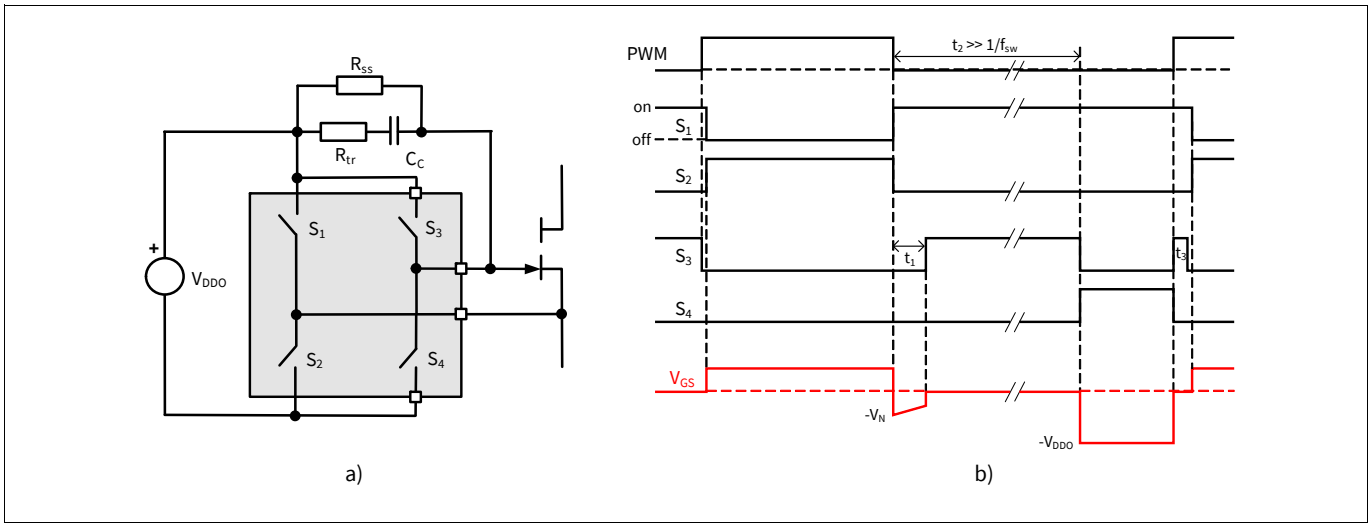


Figure 5 GaN EiceDRIVER™ concept (a) and switch control signals (b)

In the topology of **Figure 5**a) a single resistor R_{tr} is responsible for setting the maximum transient charging and discharging current. This is often acceptable. If it is not, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize different impedances for "on" and "off" transients, respectively. All relevant driving parameters are thus easily programmable by choosing V_{DDO}, R_{ss}, R_{tr}, R_{off} and C_C according to **Equation (2.1)** and the relations

(2.2)

$$I_{ss} = \frac{V_{DDO} - V_F}{R_{ss}}, \qquad I_{on,max} = \frac{V_{DDO}}{R_{tr}}, \qquad I_{off,max} = \frac{V_{th} + V_N}{R_{off} // R_{tr}}$$

3 Functional description

3.1 Block diagram

A simplified functional block diagram of the GaN EiceDRIVER™ is given in **Figure 6**. The 4 output transistors are placed on 2 separate dies. Isolation between input and outputs is achieved by means of two coreless transformer structures (CT) situated on the input die.

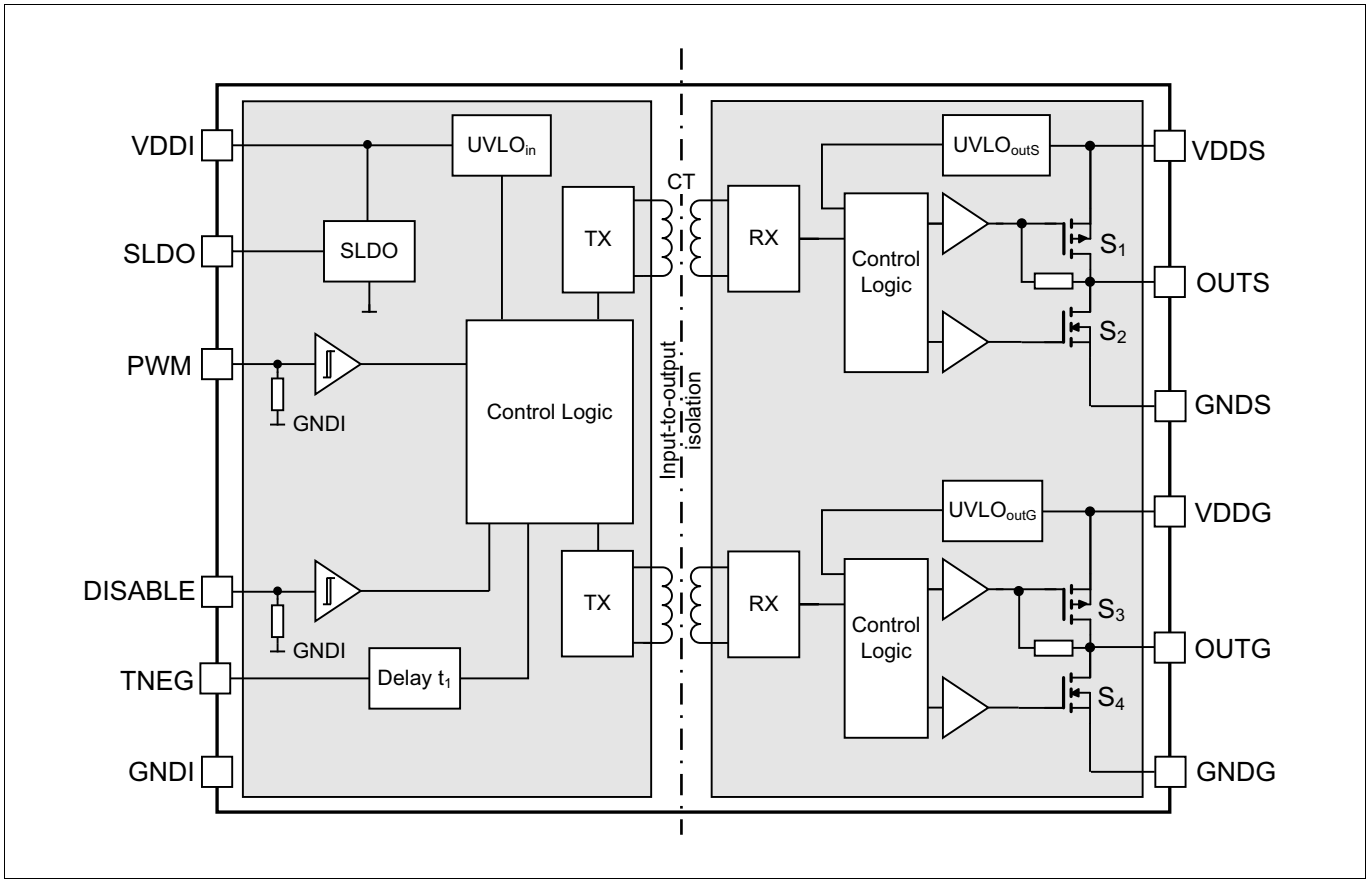


Figure 6 Block diagram

3.2 Isolation

The GaN EiceDRIVER™ is available in three package versions in accordance with different classes of input-to-output isolation voltage requirements

- 1EDF5673K in LGA-13 5 x 5 mm package for functional isolation (1.5 kV)
- 1EDF5673F in DSO-16 narrow-body (150 mil) package for functional isolation (1.5 kV)
- 1EDS5663H in DSO-16 wide-body (300 mil) package for reinforced safe isolation (6 kV)

In SMPS functional isolation is typical for high-voltage systems that are controlled from their primary side, whereas high-voltage switches controlled from the secondary side require safe isolation.

The safe isolation version 1EDS5663H is tested according to VDE0884-10 / IEC60747-17 standards as specified in **Table 15** to **Table 18**. As the CT forming this barrier is placed on the input die, a true "fail-safe" isolation is achieved, i.e. even in case of a destruction of the power switch the driver input remains safely isolated from the output.

3.3 Power supply

Due to the isolation between input and output side, two power domains with independent power management are required. Undervoltage Lockout (UVLO) functions for both input and output supplies ensure a defined start-up and robust functionality under all operating conditions.

3.3.1 Input supply voltage

The input die is supplied via VDDI with a nominal voltage of 3.3 V. Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the coreless transformer. Due to the chosen robust encoding scheme the average repetition rate of these pulses and thus the average supply current depends on the switching frequency f_{sw}. However, for f_{sw} < 500 kHz this effect is very small.

The input side can also be operated with supply voltages higher than 3.3 V. Then a shunt LDO voltage regulator (SLDO) is enabled by connecting pin SLDO to GND. The SLDO regulates the current through an external resistor R_{VDDI} connected between the external supply voltage VDD and pin VDDI as depicted in the typical application circuit on **Page 1** to generate the required voltage drop. For proper operation it has to be ensured that the current through R_{VDDI} always exceeds the maximum supply current $I_{VDDI,max}$ of the input chip. R_{VDDI} thus has to fulfil

(3.1)

$$R_{VDDI} < \frac{V_{DD} - 3.3V}{I_{VDDI,max}}$$

A typical choice for V_{DD} = 5 V could be R_{VDDI} = 470 Ω, resulting in sufficient margin between resistor current and maximum average operating current. As usual, the dynamic peak current is provided by a blocking cap (10 to 22 nF) between V_{DDI} and GNDI.

3.3.2 Output supply voltage

Both output dies and the respective output switches are supplied by a common voltage of typically 8 V between pins VDDS/G and GNDS/G. A ceramic bypass capacitance in the 20 to 100 nF range has to be placed close to the supply pins. The output supply must be floating with respect to the input supply system. This is not only required by the Kelvin source connection of the GaN switch (results in inductive voltage peaks between input and output ground during switching transient), but also by the differential driving concept as explained in **Chapter 2**.

Again the minimum operating supply voltage is set by an undervoltage lockout function ($UVLO_{out}$), operating independently of the input UVLO function.

3.4 Driver outputs

The rail-to-rail driver output stage realized with complementary MOS transistors is able to provide a typical 4 A sourcing and 8 A sinking current. Although these current levels are neither needed nor reached when driving GaN HEMTs (due to their low gate charge of only a few nC), the low on-resistance coming together with high driving current is nevertheless beneficial. With an R_{on} of 0.85 Ω for the sourcing pMOS and 0.35 Ω for the sinking nMOS transistor the driver can be considered as a nearly ideal switch. The gate drive parameters can thus be determined easily and accurately by the external components as described in **Chapter 2**. The p-channel sourcing transistor enables real rail-to-rail behavior without suffering from the voltage drop unavoidably associated with nMOS source follower stages.

3.5 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the outputs can be switched only, if both input and output supply voltages exceed the corresponding UVLO threshold voltages. Thus it can be guaranteed, that the switch transistors are not operated, if the driving voltage is too low for complete and fast switching on, thereby avoiding excessive power dissipation.

The UVLO levels for the output supply are set to a typical "on" value of 4.5 and 5.5 V (with 0.3 V hysteresis) for OUTG and OUTS, respectively, whereas $UVLO_{in}$ for VDDI is set to 2.85 V with 0.15 V hysteresis. The different UVLO levels for OUTG and OUTS help to safely avoid any erroneous turn-on of the GaN switch despite the low GaN threshold voltage. Special attention has been paid to cover all possible operating conditions, like start-up or arbitrary supply voltage situations:

- if V_{DDI} drops below $UVLO_{in}$, a "switch-to-low" command is sent to output OUTG, whereas OUTS is switched to "high"; this corresponds to the final state in extended "off" periods with $V_{GS} = -V_{DDO}$
- for V_{DD} lower than the output UVLO levels, an effective clamping concept has been realized by means of 100 kΩ resistors connecting the outputs OUTS and OUTG to the respective gates of the sourcing pMOS transistors in the output stage

As a result, safe operation of the GaN switch can be guaranteed under any circumstances.

3.6 CT communication and data transmission

A coreless transformer (CT) based communication module is used for PWM signal transfer between input and outputs. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog time-out at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

Besides, the repetition scheme is also used to signal a "first pulse" situation (**Figure 5**). If an "off"-state lasts longer than 32 µs, the repetition rate of the CT pulses is reduced to a value that causes the watchdog on the output chip to wake up and initiate a change in the "off" state acc. to **Figure 5** (switch S_3 to "off" and S_4 to "on" state).

3.7 Signal timing

From the above, the extended "off"-phase t_2 defining a "first pulse" situation, is fixed at a typical value of 32 µs. The other important timing parameter t_1, i.e. the duration of the negative "off"-voltage, can be programmed by a resistor R_{t1} connected from TNEG to GNDI according to $t_1 = R_{t1} * 1.8$ pF. As the main idea is to keep the switch in a safe "off" state during the switching transient, t_1 must be longer than the system dead time t_d, i.e. the maximum time between an "off"-command and the subsequent switching transient. The upper limit for t_1 obviously is the minimum "off"-period; thus there is usually sufficient margin in the choice of t_1.

However, it should be mentioned that the actual value of t_1 can be influenced by the switching transient itself due to small, but unavoidable coupling capacitances between output and input pins. Even with an optimized PCB layout, capacitances inside the package may cause a shortening of t_1 for the high-side switch in fast-switching half-bridges to approx. 50% of the static value. Nevertheless, as the effect is triggered by the transient of the switching node, the essential requirement, i.e.to apply the negative gate voltage during this transient, is always met and the described behavior does not cause any adverse effect in the system.

4 Electrical characteristics

4.1 Absolute maximum ratings

The absolute maximum ratings are listed in **Table 3**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	-0.3	–	3.7	V	SLDO inactive (N.C. or connected to VDDI)
Output supply voltage	V_{DDO}	-0.3	–	22	V	–
Voltage at pins PWM and DISABLE	V_{IN}	-0.3	–	17	V	–
		-5	–	–	V	< 50 ns for transient [1]
Voltage at pins TNEG and SLDO	V_{TNEG} V_{SLDO}	-0.3	–	V_{DDI} + 0.3	V	–
Voltage at pins OUTS, OUTG	$V_{OUTS/G}$	-0.3	–	V_{DDO} + 0.3	V	–
		-2	–	V_{DDO} + 1.5	V	< 200 ns [1]
Reverse current peak at pins OUTS, OUTG	I_{SRC_rev}	-5	–	–	A_{pk}	< 500 ns [1]
	I_{SNK_rev}	–	–	5	A_{pk}	
Non-destructive Common Mode Transient Immunity	CMTI	400	–	–	V/ns	outputs with respect to input
Junction temperature	T_J	-40	–	150	°C	–
Storage temperature	T_{STG}	-65	–	150	°C	–
Soldering temperature	T_{SOL}	–	–	260	°C	reflow / wave soldering [2]
ESD capability	V_{ESD_CDM}	–	–	0.5	kV	Charged Device Model (CDM) [3]
ESD capability	V_{ESD_HBM}	–	–	2	kV	Human Body Model (HBM) [4]

1) parameter verified by design, not tested in production
2) according to JESD22A111
3) according to JESD22-002
4) according to JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

4.2 Thermal characteristics

Table 4 Thermal characteristics at T_A= 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PG-TFLGA-13-1 package						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	112	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	44	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	66	–	K/W	–
Characterization parameter junction-top [4]	Ψ_{thJT25}	–	7.7	–	K/W	–
Characterization parameter junction-board [4]	Ψ_{thJB25}	–	5.6	–	K/W	–
PG-DSO-16-30 package						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	59	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	32	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	33	–	K/W	–
Characterization parameter junction-top [4]	Ψ_{thJT25}	–	8.9	–	K/W	–
Characterization parameter junction-board [4]	Ψ_{thJB25}	–	7.7	–	K/W	–
PG-DSO-16-11 package						
Thermal resistance junction-ambient [1]	R_{thJA25}	–	51	–	K/W	–
Thermal resistance junction-case (top) [2]	R_{thJC25}	–	25	–	K/W	–
Thermal resistance junction-board [3]	R_{thJB25}	–	36	–	K/W	–
Characterization parameter junction-top [4]	Ψ_{thJT25}	–	4.4	–	K/W	–
Characterization parameter junction-board [4]	Ψ_{thJB25}	–	5.4	–	K/W	–

1) obtained by simulating a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

2) obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

3) obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

4) estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining R_{th}, using a procedure described in JESD51-2a (sections 6 and 7).

4.3 Operating range

Table 5 Operating range

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3	–	3.5	V	SLDO inactive (N.C. or connected to VDDI)
Output supply voltage	V_{DDO}	6.5	8	20[1)]	V	Min. defined by UVLO
VDDI blocking capacitance	C_{VDDI}	–	–	22	nF	SLDO active (connected to GNDI)
Logic input voltage at pins PWM and DISABLE	V_{IN}	0	–	6.5	V	–
Voltage at pins TNEG and SLDO	V_{TNEG} V_{SLDO}	0	–	5	V	–
Junction temperature	T_J	-40	–	150[2)]	°C	
Ambient temperature	T_A	-40	–	85	°C	–

1) not recommended for CoolGaN™ HEMTs

2) continuous operation above 125°C may reduce lifetime

4.4 Electrical characteristics

Unless otherwise noted, min./max. values of characteristics are the lower and upper limits, respectively. They are valid within the full operating range. Typical values are given at T_J = 25°C with V_{DDI} = 3.3 V and V_{DDO} = 8 V

Table 6 Power supply

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDDI quiescent current	I_{VDDIqu}	–	1.5	–	mA	no switching
VDDO quiescent current	I_{VDDOqu}	–	1.3	–	mA	no switching

Table 7 Undervoltage Lockout

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Undervoltage Lockout input ($UVLO_{in}$) turn on threshold	$UVLO_{in}$	2.75	2.85	2.95	V	–
Undervoltage Lockout ($UVLO_{in}$) turn off threshold	$UVLO_{in-}$	–	2.7	–	V	–
$UVLO_{in}$ threshold hysteresis	$\Delta UVLO_{in}$	0.1	0.15	0.2	V	–
Undervoltage Lockout outputs ($UVLO_{outG/S}$) turn on threshold	$UVLO_{outG}$	4.7	5.0	5.3	V	–
	$UVLO_{outS}$	5.4	5.8	6.2	V	–
$UVLO_{out}$ turn off thresholds	$UVLO_{outG-}$	–	4.5	–	V	–
	$UVLO_{outS-}$	–	5.2	–	V	–
$UVLO_{out}$ threshold hysteresis	$\Delta UVLO_{outG}$	0.3	0.45	0.6	V	–
	$\Delta UVLO_{outS}$	0.4	0.6	0.8	V	–

Table 8 Logic inputs PWM and DISABLE

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INL}	1.7	2.0	2.3	V	independent of V_{DDI}
Input voltage threshold for transition HL	V_{INH}	–	1.2	–	V	independent of V_{DDI}
Input voltage hysteresis	ΔV_{IN}	0.4	0.8	1.2	V	–
Input pull down resistor	R_{IN}	–	150	–	kΩ	–

Table 9 Static output characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level (sourcing) output resistance	R_{on_SRC}	0.42	0.85	1.6	Ω	I_{SRC} = 50 mA
Peak sourcing output current	I_{SRC_pk}	–	4	1)	A	–
Low level (sinking) output resistance	R_{on_SNK}	0.18	0.35	0.75	Ω	I_{SNK} = 50 mA
Peak sinking output current	I_{SNK_pk}	2)	-8	–	A	–

1) actively limited to approx. 5.2 A_{pk}, not subject to production test - verified by design / characterization
2) actively limited to approx. -10.2 A_{pk}, not subject to production test - verified by design / characterization

Table 10 Dynamic characteristics, $T_{J,max}$ = 125°C (see Figure 7 and Figure 8)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PWM to OUTS propagation delay	t_{PDonS}	31	37	44	ns	load between OUTS and GNDS C_{LS} = 1.8 nF
	t_{PDoffS}	–	41	–		
PWM to OUTG propagation delay	t_{PDonG}	–	$t_{PDoffS} + t_1$	–	ns	load between OUTG and GNDG Z_{LG} = 1.8 nF // 20 Ω
	t_{PDoffG}	31	37	44	ns	
DISABLE to OUTS propagation delay	t_{PD_DISon} t_{PD_DISoff}	–	–	100	ns	C_{LS} = 1.8 nF
Rise time OUTS / OUTG	t_{rise}	–	6.5	12[1)]	ns	C_{LS} = C_{LG} = 1.8 nF, 10% to 90%
Fall time OUTS	t_{fall}	–	4.5	8[1)]	ns	C_{LS} = 1.8 nF, 90% to 10%
Minimum input pulse width that changes output state	t_{PW}	–	18	–	ns	–
Duration of negative gate “off” voltage	t_1	–	180	–	ns	R_{t1} = 100 kΩ
Minimum “off”time before entering “first pulse” mode	t_2	–	32[1)]	–	µs	–
Discharging time in “first pulse” mode	t_3	–	20[1)]	–	ns	–

1) verified by design, not tested in production

5 Timing diagrams

Figure 7 depicts rise, fall and delay times as observed at the capacitively loaded outputs OUTS and OUTG, resp. As OUTG is not actively switched to low, a resistor in parallel with the load capacitance has to be used for testing. In addition to the signal propagation delay t_{PDon}, the rising edge of OUTG is delayed by a time t_1 defining the duration of negative V_{GS}.

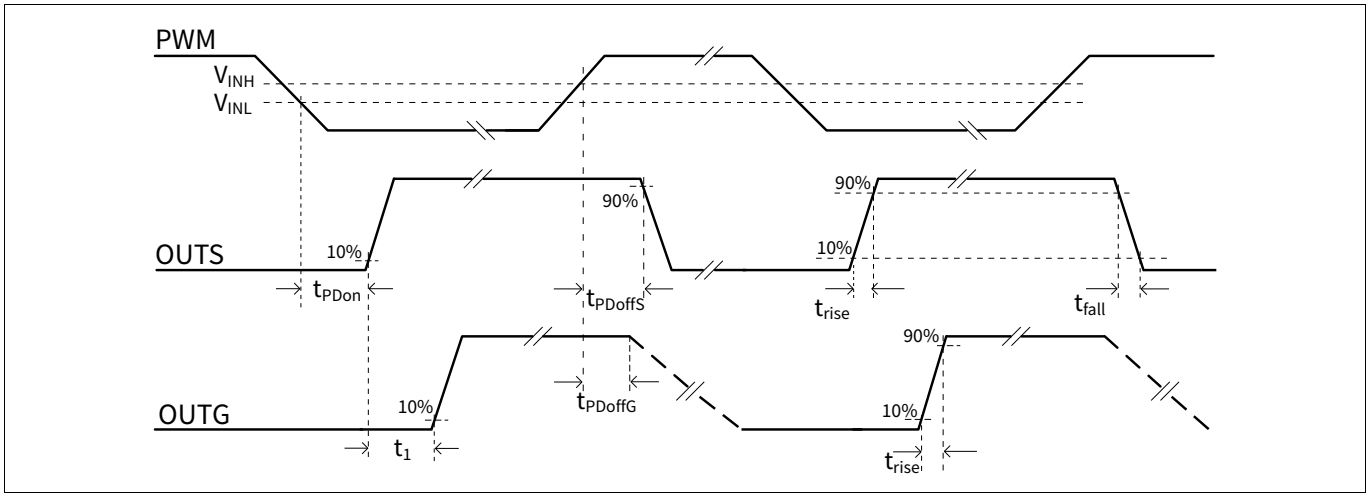


Figure 7 Propagation delay, rise and fall time

Figure 8 illustrates a complete switching sequence of the four switches forming the two output stages of GaN EiceDRIVER™ (delay, rise and fall times not shown). The sequence in the left part of **Figure 8** corresponds to the normal switching operation, whereas in the right part the "first pulse" situation is depicted. This situation is assumed to happen whenever there is no switching action for an extended period t_2. Clearly t_2 must be significantly longer than a regular switching period. A typical duration of 32 µs has been chosen, as GaN switches usually operate at switching frequencies significantly above 50 kHz (switching period below 20 µs).

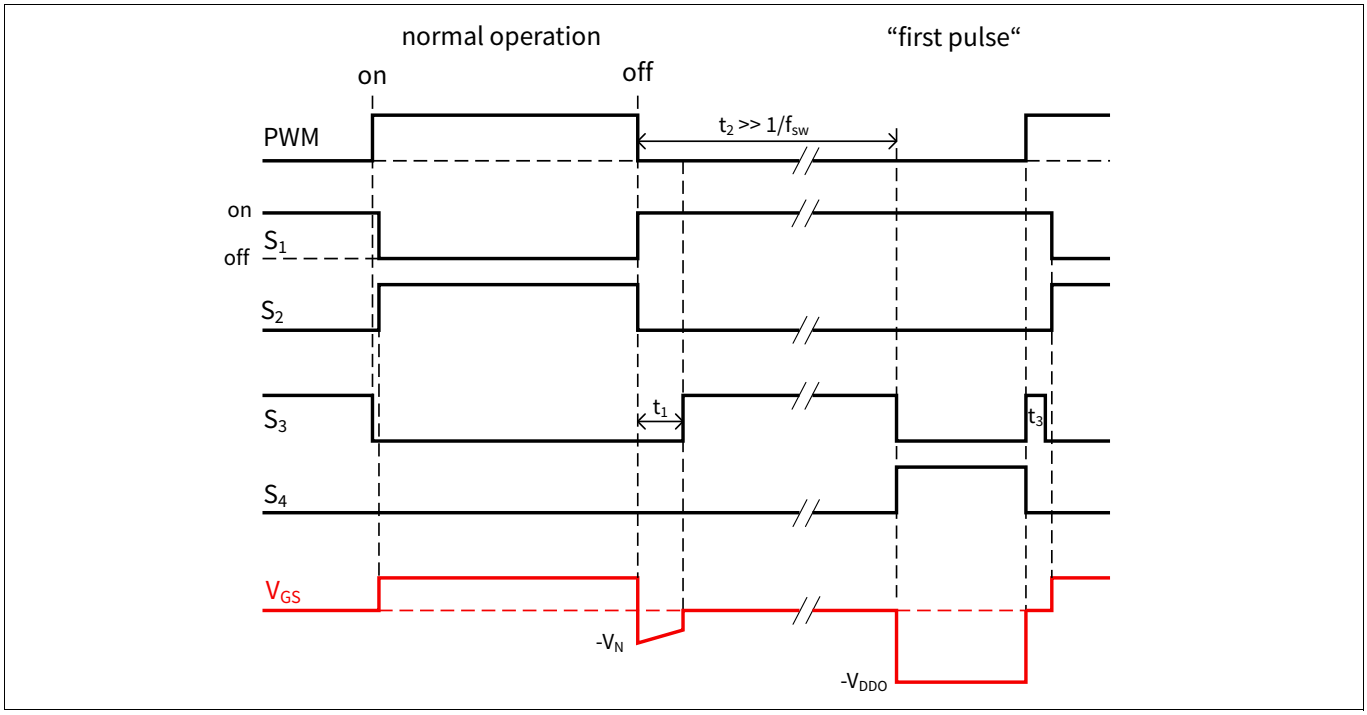
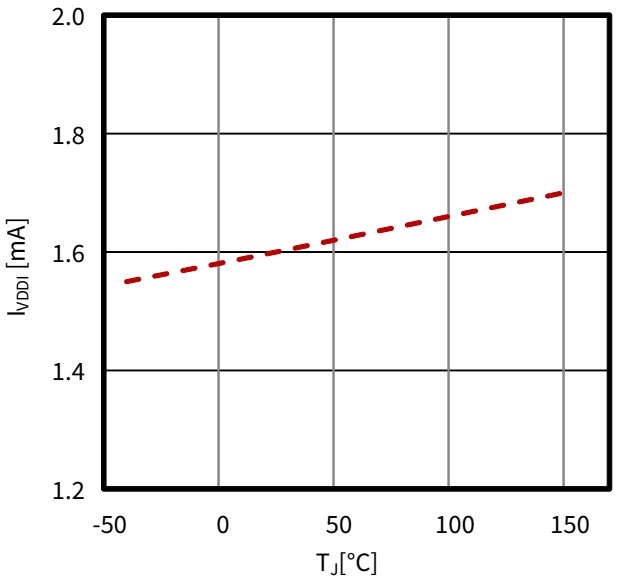


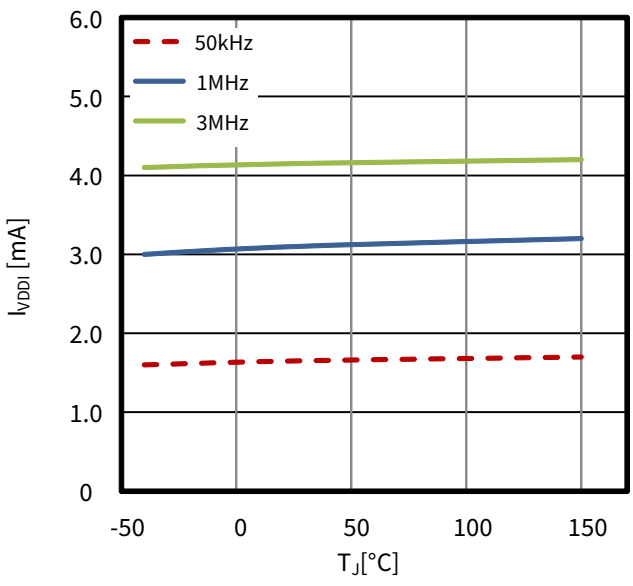
Figure 8 Input signal, output switch sequence and resulting V_{GS} for normal operation and "first pulse" situation

6 Typical characteristics

V_{DD}= 8 V, V_{DDI} = 3.3 V, T_A = 25°C, no load (unless otherwise noted)

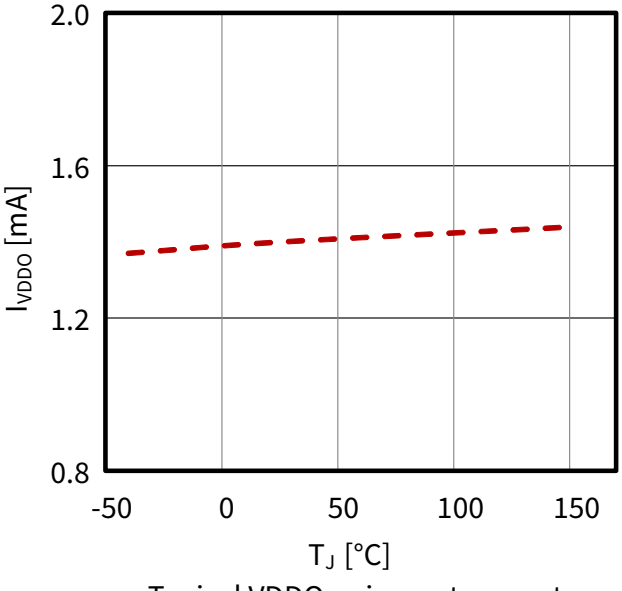


Typical VDDI quiescent current vs. temperature

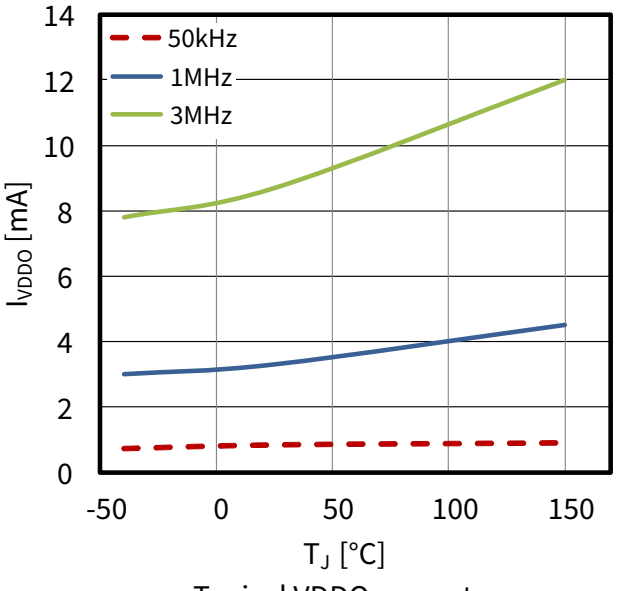


Typical VDDI current vs. temperature and frequency

Figure 9 Supply current VDDI



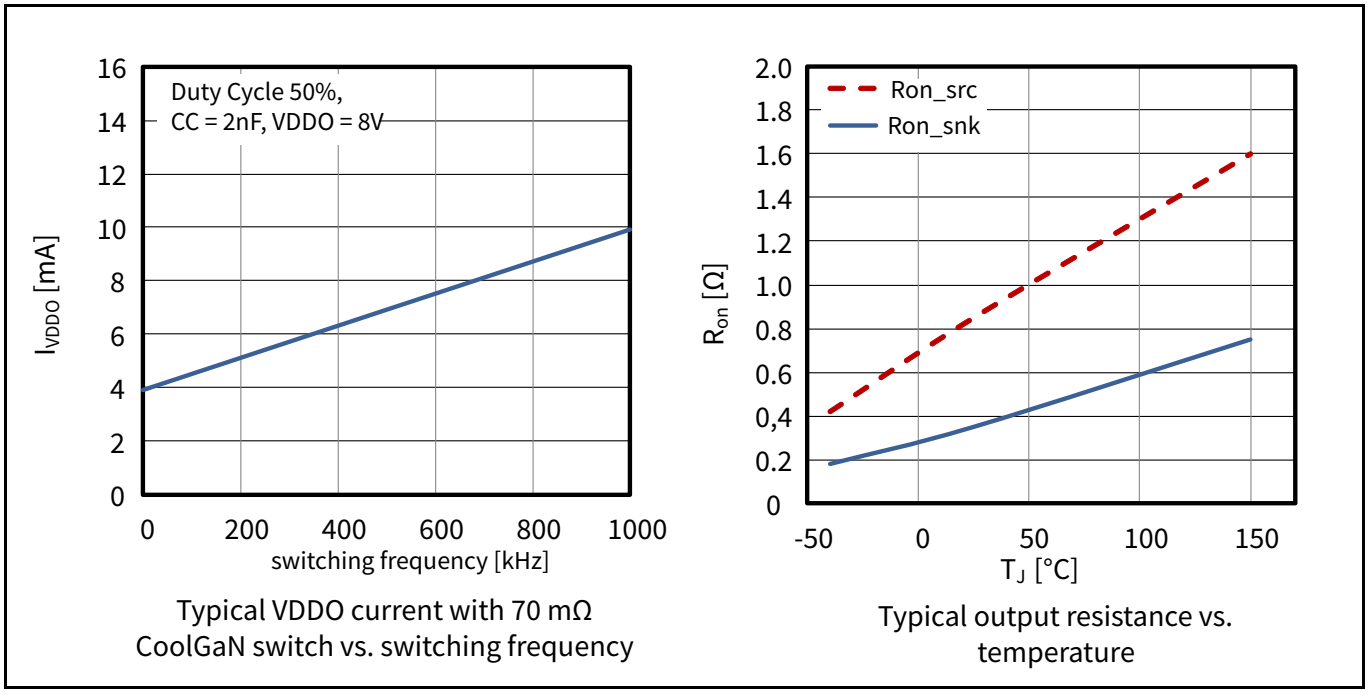
Typical VDDO quiescent currents vs. temperature



Typical VDDO current vs. temperature and frequency, no load

Figure 10 Supply current VDDO

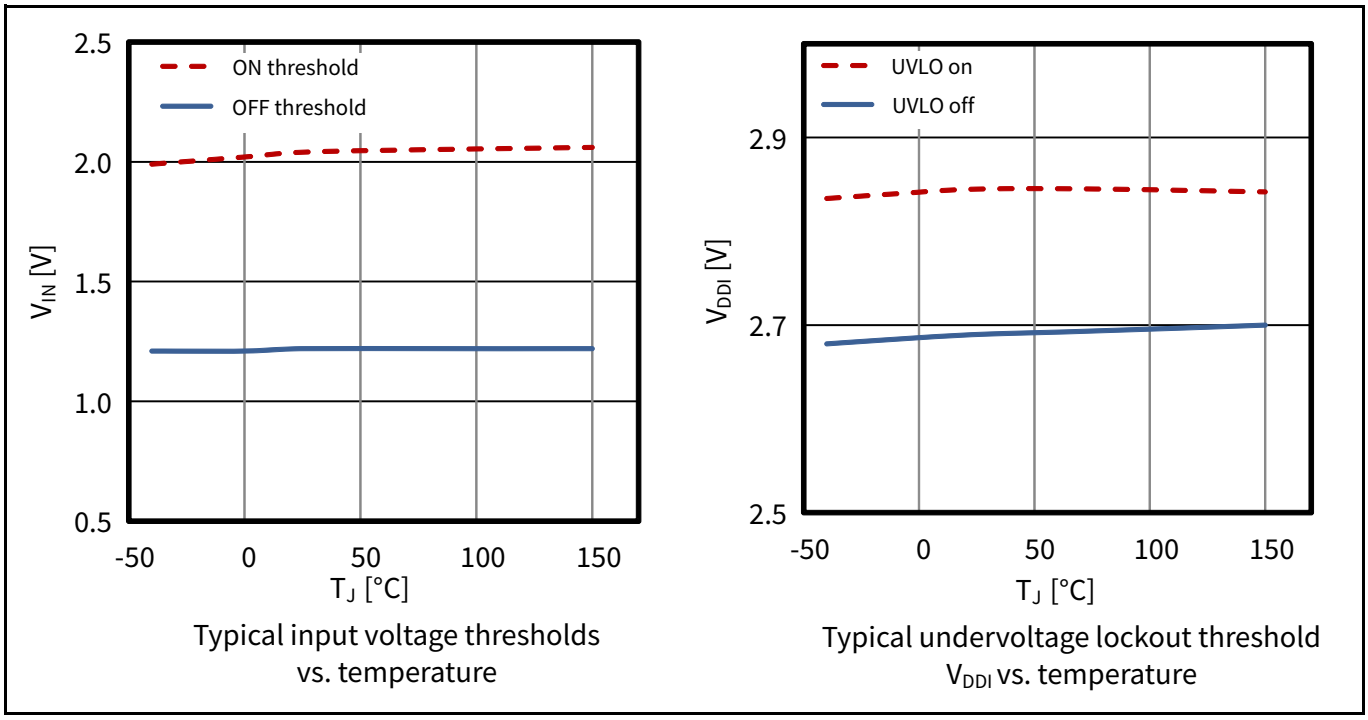
Typical characteristics



Typical VDDO current with 70 mΩ CoolGaN switch vs. switching frequency

Typical output resistance vs. temperature

Figure 11 Supply current VDDO (with load) and output resistance

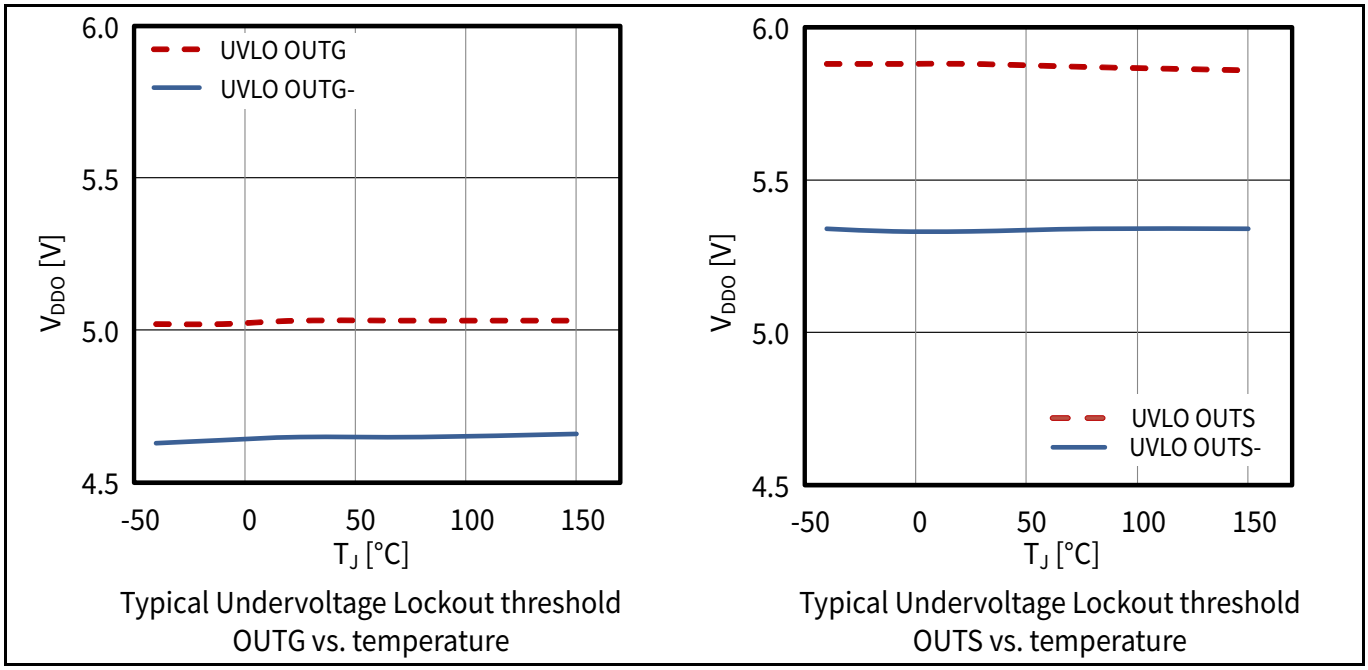


Typical input voltage thresholds vs. temperature

Typical undervoltage lockout threshold V_{DDI} vs. temperature

Figure 12 Logic input thresholds and V_{DDI} UVLO

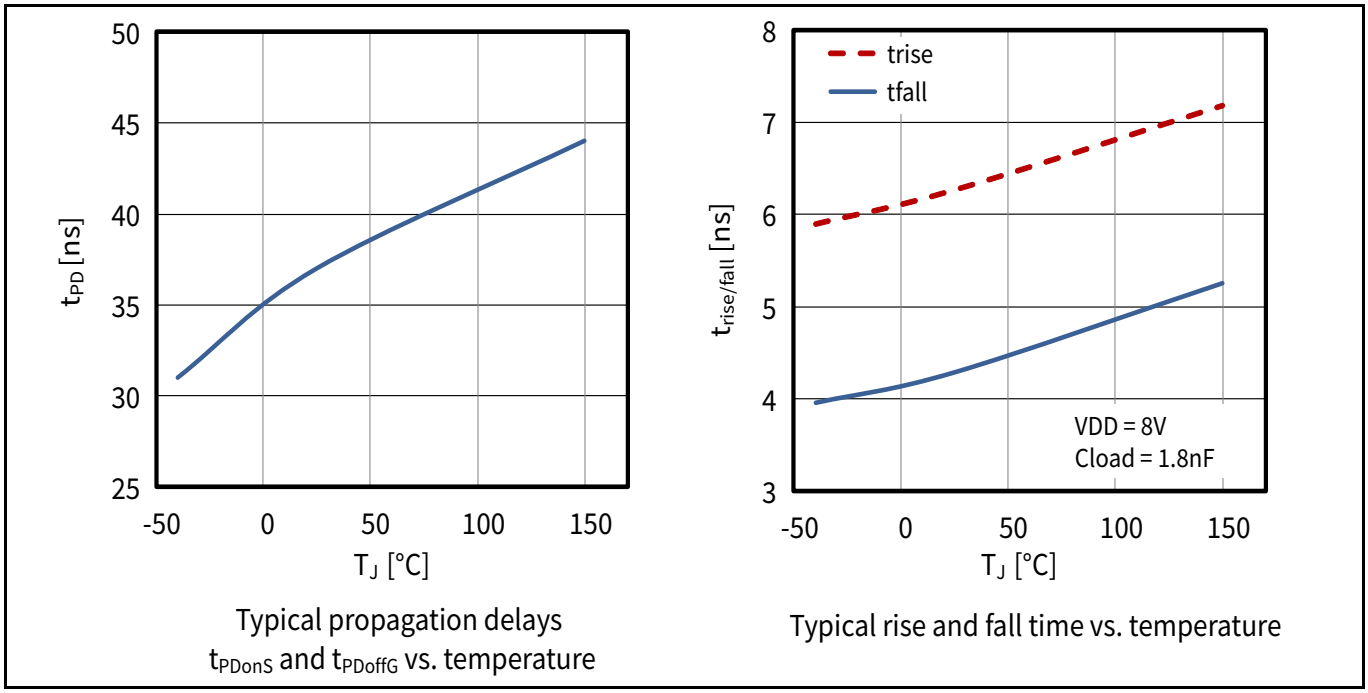
Typical characteristics



Typical Undervoltage Lockout threshold OUTG vs. temperature

Typical Undervoltage Lockout threshold OUTS vs. temperature

Figure 13 Output UVLO

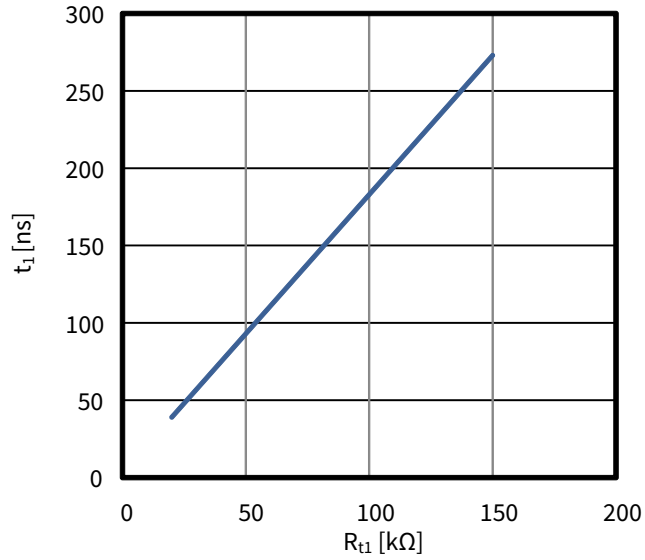


Typical propagation delays t_{PDonS} and t_{PDoffG} vs. temperature

Typical rise and fall time vs. temperature

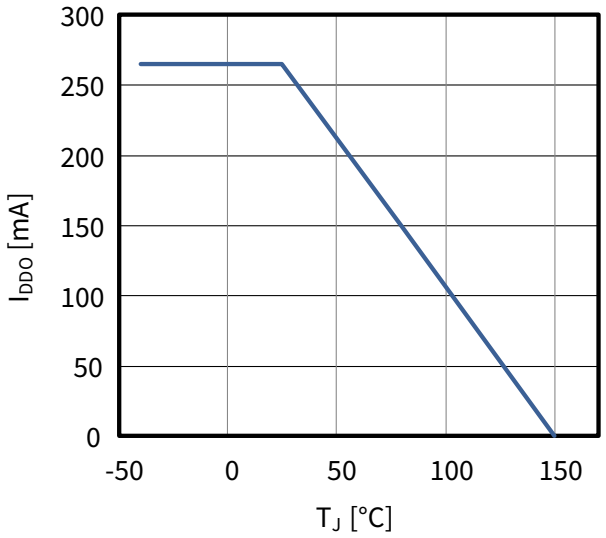
Figure 14 Propagation delay and rise / fall time

Typical characteristics

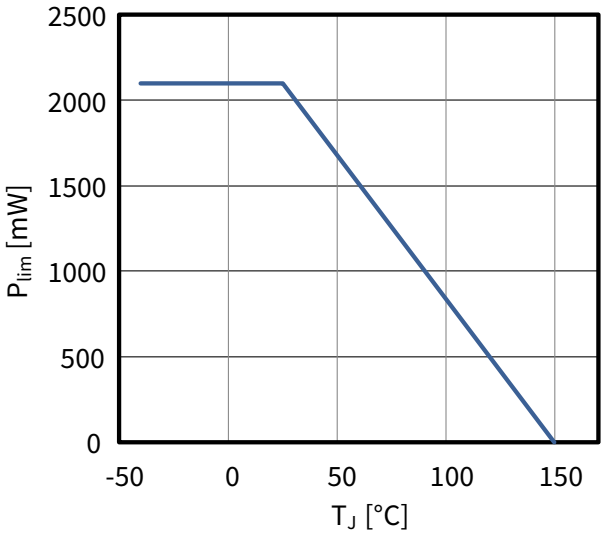


Typical negative "off" voltage duration t_1 vs R_{t1}

Figure 15 Typical negative "off" voltage duration t_1 vs. R_{t1}



Thermal derating for safety-related limiting current



Thermal derating for safety-related limiting power

Figure 16 Thermal derating curves

7 Isolation specifications

The following tables summarize the package-specific isolation characteristics and test methods. For reinforced isolation, the regulatory tests described in the component and system standards are applied; functional isolation is guaranteed by the specified in-house test methods.

As soon as the regulatory certificates are available, the reference and / or documents will become available for public download on the Infineon website.

As finally creepage and clearance distances are influenced by PCB layout, it is the customer's responsibility to verify the respective requirements on system level.

7.1 Functional isolation specifications

7.1.1 Functional isolation in PG-TFLGA-13-1 package (1EDF5673K)

Table 11 Functional isolation input-to-output (PG-TFLGA-13-1)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	V_{IO}	1500	–	–	V_{DC}	impulse test >10 ms, production tested
Maximum isolation working voltage	V_{IOWM}	460	–	–	V_{RMS}	according to IEC 60664-1 (PD 2; MG II)
Package clearance	CLR	–	3.4	–	mm	shortest distance over air, from any input pin to any output pin
Package creepage	CPG	–	3.4	–	mm	shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	200	–	–	V/ns	according to VDE V0884-10, static and dynamic test
Capacitance input-to-output	C_{IO}	–	2	–	pF	–
Resistance input-to-output	R_{IO}	–	>1000	–	MΩ	–

Table 12 Package characteristics (PG-TFLGA-13-1)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112

7.1.2 Functional isolation in NB PG-DSO-16-11 package (1EDF5673F)

Table 13 Functional isolation input-to-output (NB PG-DSO-16-11)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Functional isolation test voltage	V_{IO}	1500	–	–	V_{DC}	impulse test > 10 ms, sample tested
Maximum isolation working voltage	V_{IOWM}	510	–	–	V_{RMS}	according to IEC 60664-1 (PD2; MG II)[1)]
Package clearance	CLR	–	4.0	–	mm	shortest distance over air, from any input pin to any output pin
Package creepage	CPG	–	4.0	–	mm	shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	200	–	–	V/ns	according to VDE V0884-10, static and dynamic test
Capacitance input-to-output[1)]	C_{IO}	–	2	–	pF	–
Resistance input-to-output[1)]	R_{IO}	–	>1000	–	MΩ	–

1) verified by design, not tested in production

Table 14 Package characteristics (NB PG-DSO-16-11)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112

7.2 Reinforced isolation in WB PG-DSO-16-30 package (1EDS5663H)

Table 15 Input-to-output isolation specification according to VDE0884-10 (WB PG-DSO-16-30)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Maximum transient isolation voltage	V_{IOTM}	8000	–	–	V_{pk}	qualification for t = 60 s; production test with $V_{IOTM\_test} = V_{IOTM}$ * 1.2 for t =1 s
Maximum repetitive peak isolation voltage	V_{IORM}	1420	–	–	V_{pk}	Time Dependent Dielectric Breakdown test method
Maximum isolation working voltage	V_{IOWM}	1420	–	–	V_{DC}	
		1000	–	–	V_{RMS}	
Partial discharge voltage	V_{PD}	4500	–	–	V_{pk}	production test for t=1s, partial discharge Q_{PD} < 5 pC
Maximum surge isolation voltage	V_{IOSM}	6250	–	–	V_{pk}	V_{IOSM_test} = 1.6 x V_{IOSM} >10 kV_{pk}; sample tested [1]
Package clearance	CLR	–	8.0	–	mm	from any input pin to any output pin
Package creepage	CPG	–	8.0	–	mm	from any input pin to any output pin
Overvoltage category per IEC 60664-1 table F.1	–	I	–	IV		rated mains voltage ≤ 150 V_{RMS}
		I	–	III		≤ 300 V_{RMS}
		I	–	II		≤ 600 V_{RMS}
Capacitance input-to-output	C_{IO}	–	2	–	pF	–
Resistance input-to-output	R_{IO}	–	>1000	–	MΩ	–
Common Mode Transient Immunity	CMTI	200	–	–	V/ns	input to output static and dynamic; sample test

1) surge pulse tests applied according to IEC60065-10.1 (Ed 8.0 2014), 61000-4-5, 60060-1 waveforms (1.2 µs slope, 50 µs decay)

Table 16 Reinforced isolation package characteristics (WB PG-DSO-16-30)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	–	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	–	–	II	–	–	according to IEC 60112
Pollution degree	–	–	2	–	–	–
Climatic category	–	–	40/125/ 21	–	–	–

Table 17 Reinforced input-to-output isolation according to UL1577 Ed 5[1] (WB PG-DSO-16-30)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Withstand isolation voltage	V_{ISO}	5700	–	–	V_{RMS}	V_{ISO}= 5700 V_{RMS} for t = 60 s (qualification); V_{ISO_test} > 1.2 x V_{ISO} = 6840 *V* for t = 1 s

1) certification pending

7.3 Safety-limiting values

Table 18 Reinforced isolation safety-limiting values as outlined in VDE-0884-10 (WB PG-DSO-16-30)

Parameter	Side	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Safety supply power	Input	–	–	20.0	mW	R_{thJA} = 59 K/W[1], T_A = 25°C, T_J = 150°C
	Output	–	–	2100	mW	
	Total	–	–	2120	mW	
Safety supply current	Output	–	–	265	mA	R_{thJA} = 59 K/W[1], V_{DDO} = 8 V, T_A= 25°C, T_J = 150°C
Safety temperature	T_s	–	–	150	°C	T_s = $T_{J,max}$

1) Calculated with the R_{th} of WB-DSO-16-30 package (see **Table 4**)

According to VDE0884-10 and UL1577, safety-limiting values define the operating conditions under which the isolation barrier can be guaranteed to stay unaffected. This corresponds with the maximum allowed junction temperature, as temperature-induced failures might cause significant overheating and eventually damage the isolation barrier.

8 Application circuit

Figure 17 depicts a typical application for CoolGaN™ switches in a so called "totem-pole" PFC. It consists of a 70 mΩ GaN half-bridge controlled by two GaN EiceDRIVERs; the diode functions indicated in the power path are usually realized with low-R_{DSON} MOSFETs operating as synchronous rectifiers. 2.5 kW of power can be handled at very high efficiency (above 99%).

The topology in **Figure 17** differs from standard PFCs mainly by the fact that both GaN transistors are used alternately in switch and diode operation mode, depending on the polarity of the input voltage. This eliminates the need for rectifying the input voltage and therefore avoids a significant loss contributor. Such a topology cannot be realized with MOS-switches due to their inherent body diode and the associated large recovery charge.

Further details can be found in application note: **www.infineon.com/driving-coolgan**

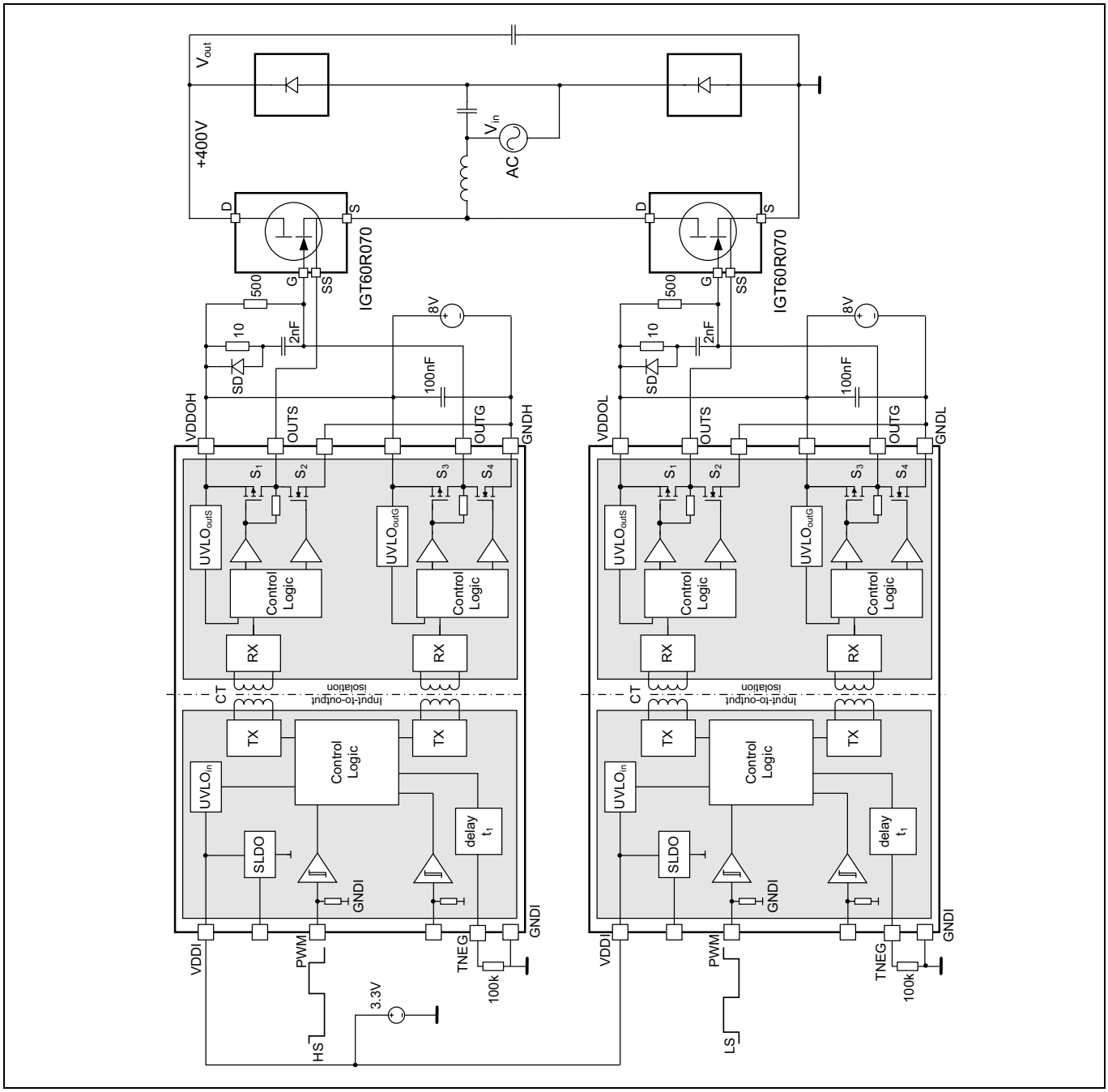


Figure 17 Typical application circuit for 2.5 kW GaN "totem-pole" PFC

9 Layout guidelines

For any fast-switching power system the PCB layout is crucial to achieve optimum performance. Among the many existing rules, recommendations, guidelines, tips and tricks, the following are of highest importance:

- minimize power loop inductance, the most critical limitation of switching speed due to the unavoidable voltage overshoots generated by fast current commutation
- use low-ESR decoupling capacitances for the driver supply voltages and place them as close as possible to the driver (in the layout proposals below the output capacitance has been split and connected to both supply pins)
- strictly avoid any additional coupling capacitance between input and output pins due to PCB layout (see **Chapter 3.7**)

Respective layout proposals for the immediate driver surroundings are given in **Figure 18**, **Figure 19** and **Figure 20** for the different available package types.

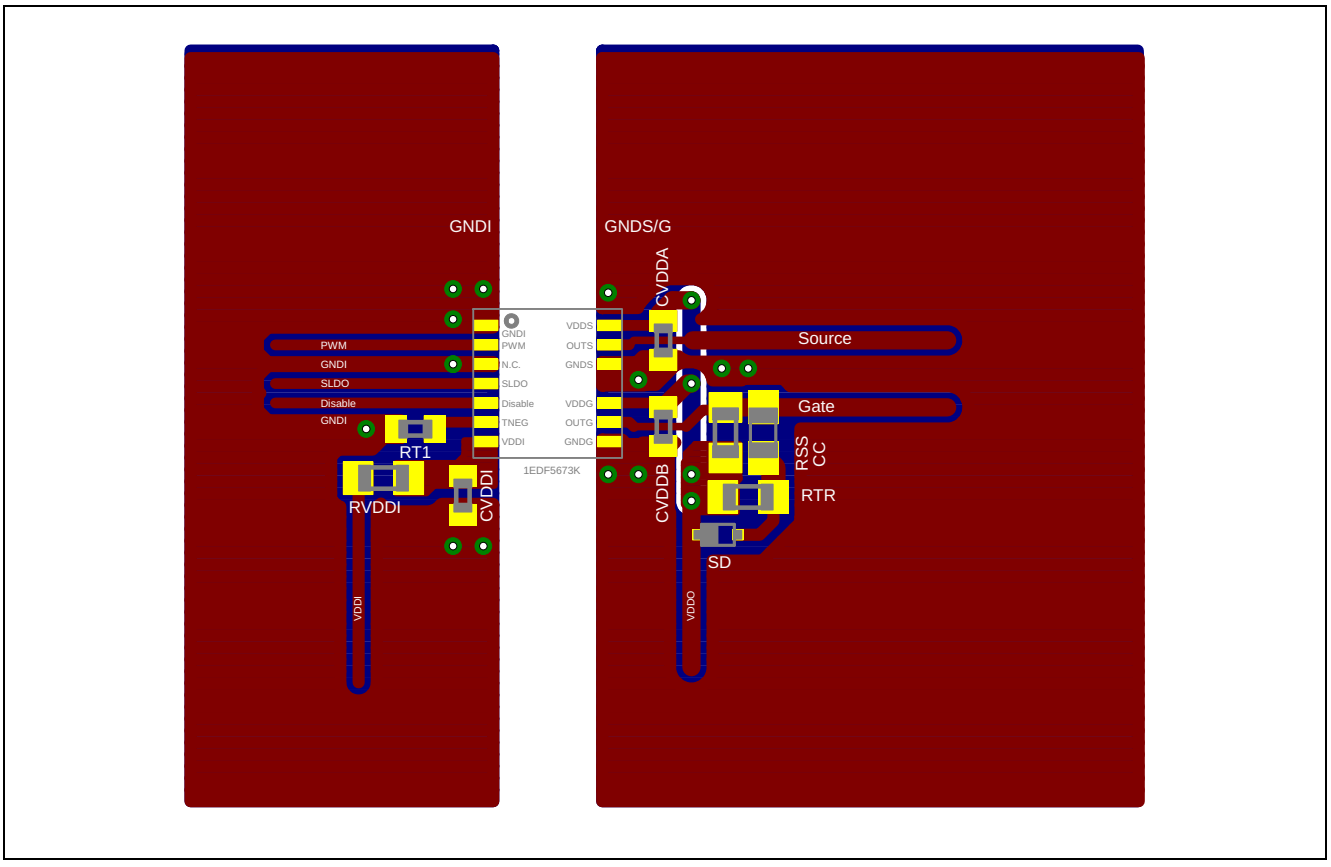


Figure 18 Layout recommendation for PG-TFLGA-13-1 package

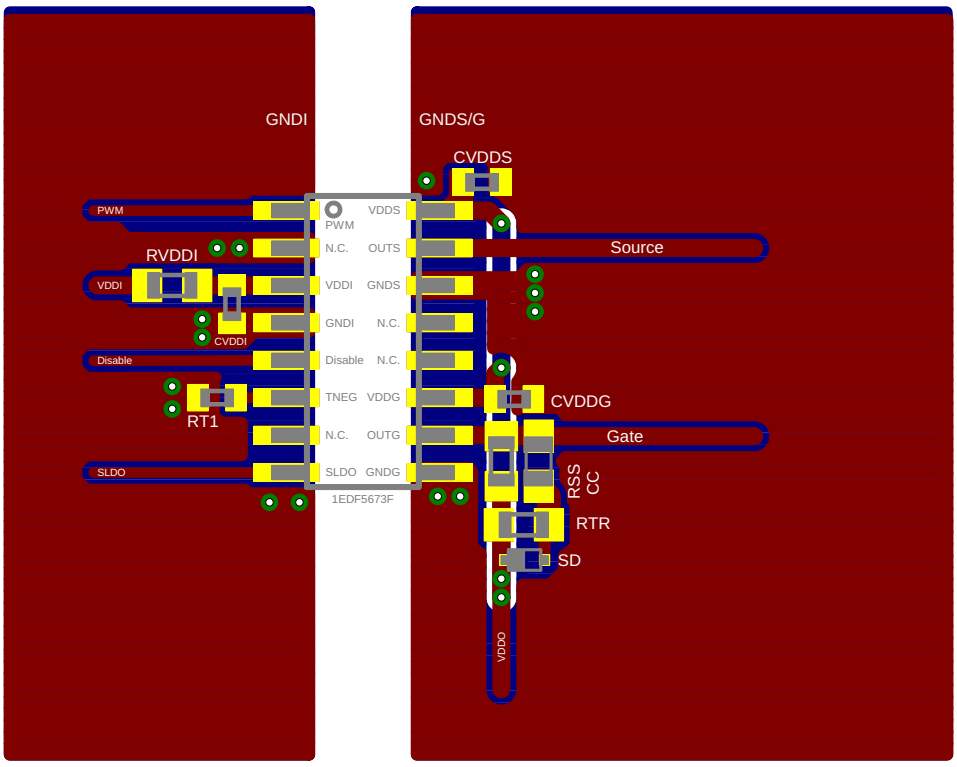


Figure 19 Layout recommendation for PG-DSO-16-11 package

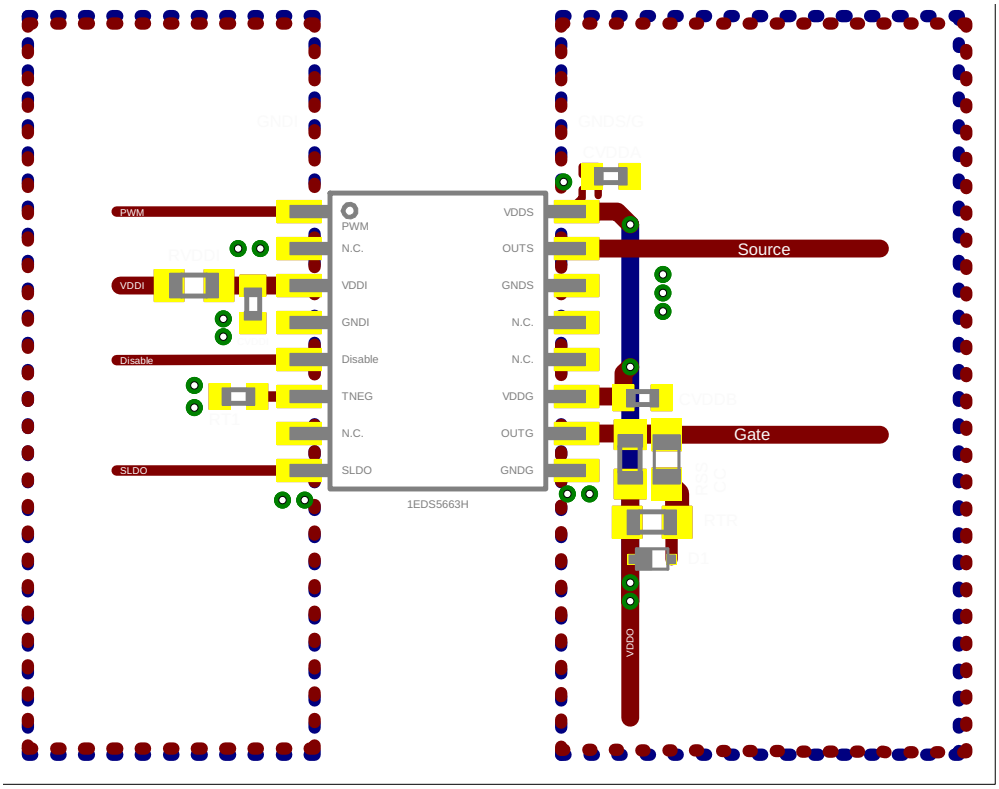


Figure 20 Layout recommendation for PG-DSO-16-30 package

10 Package information

The following package versions are available.

- an area optimized 5 x 5 mm² PG-TFLGA-13-1
- an NB PG-DSO-16-11 package with typ. 4 mm creepage input to output
- a WB PG-DSO-16-30 package with typ. 8 mm creepage input to output

Note: For further information on package types, recommendation for board assembly, please go to ***https://www.infineon.com/packages***

10.1 Package PG-TFLGA-13-1

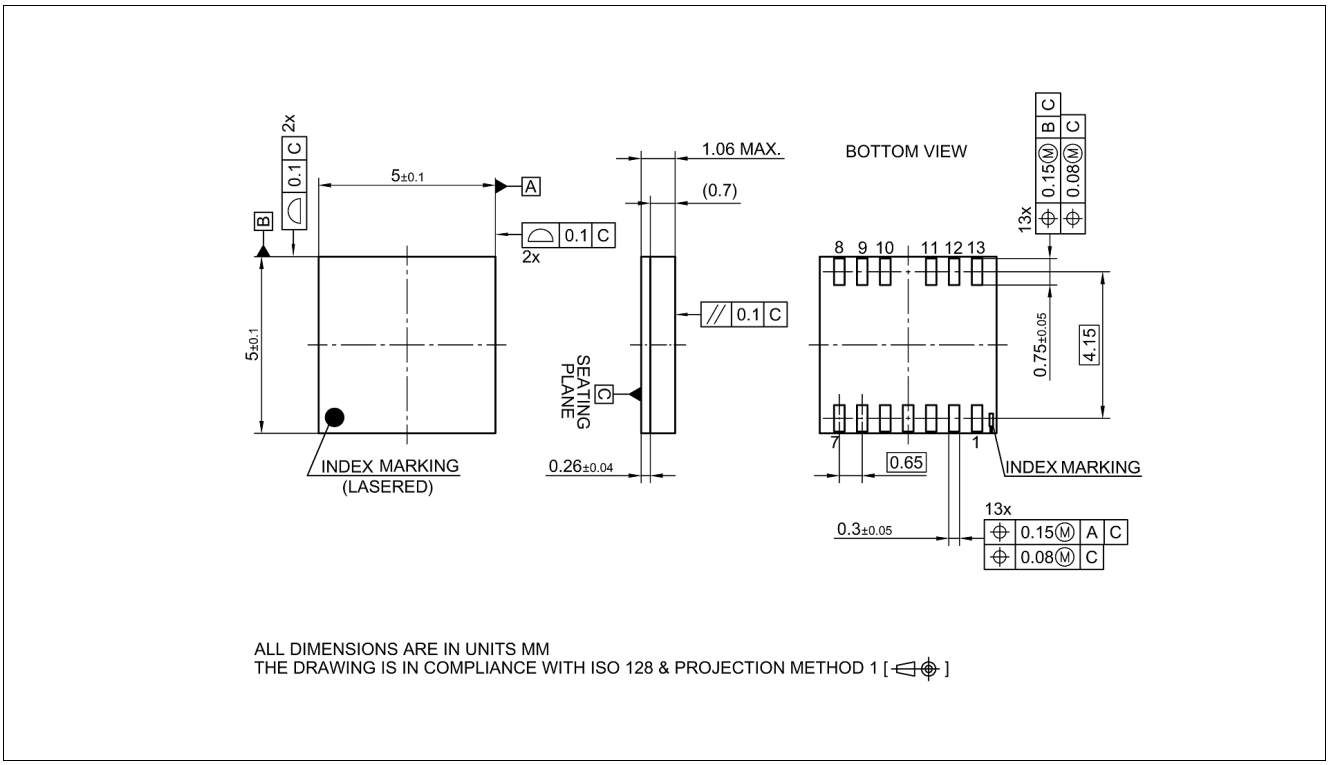


Figure 21 PG-TFLGA-13-1 outline

Package information

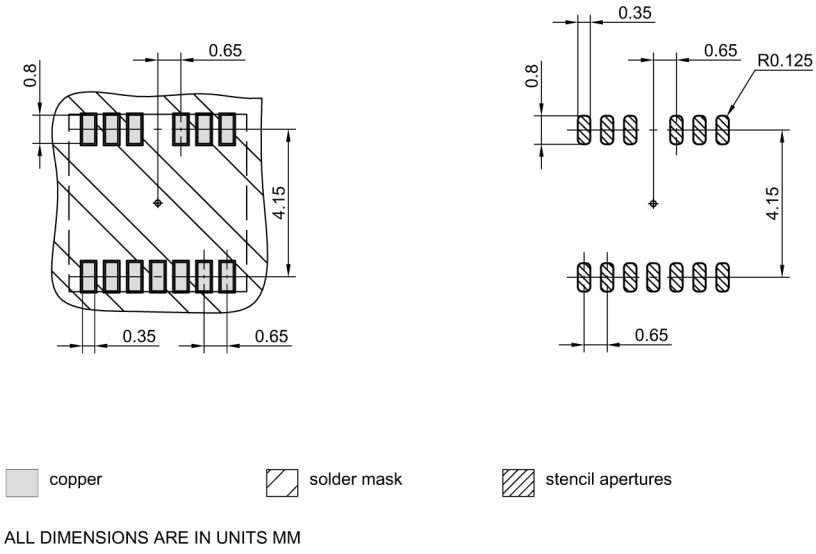


Figure 22 PG-TFLGA-13-1 footprint

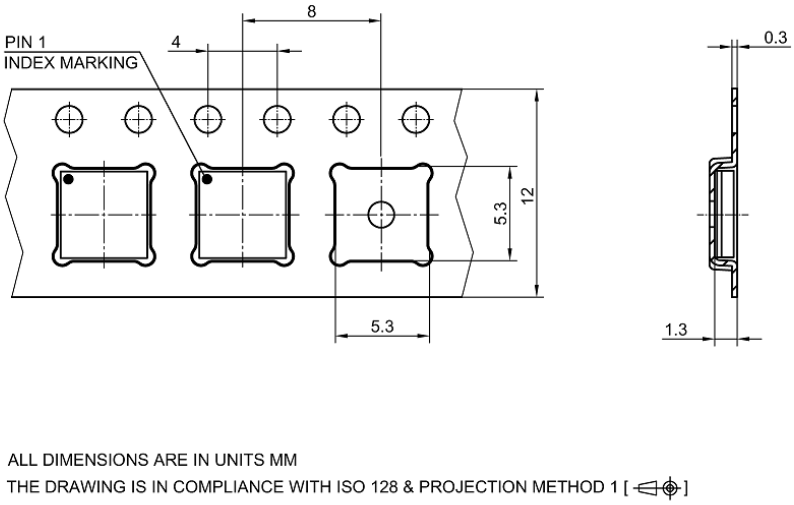


Figure 23 PG-TFLGA-13-1 packaging

10.2 Package PG-DSO-16-11

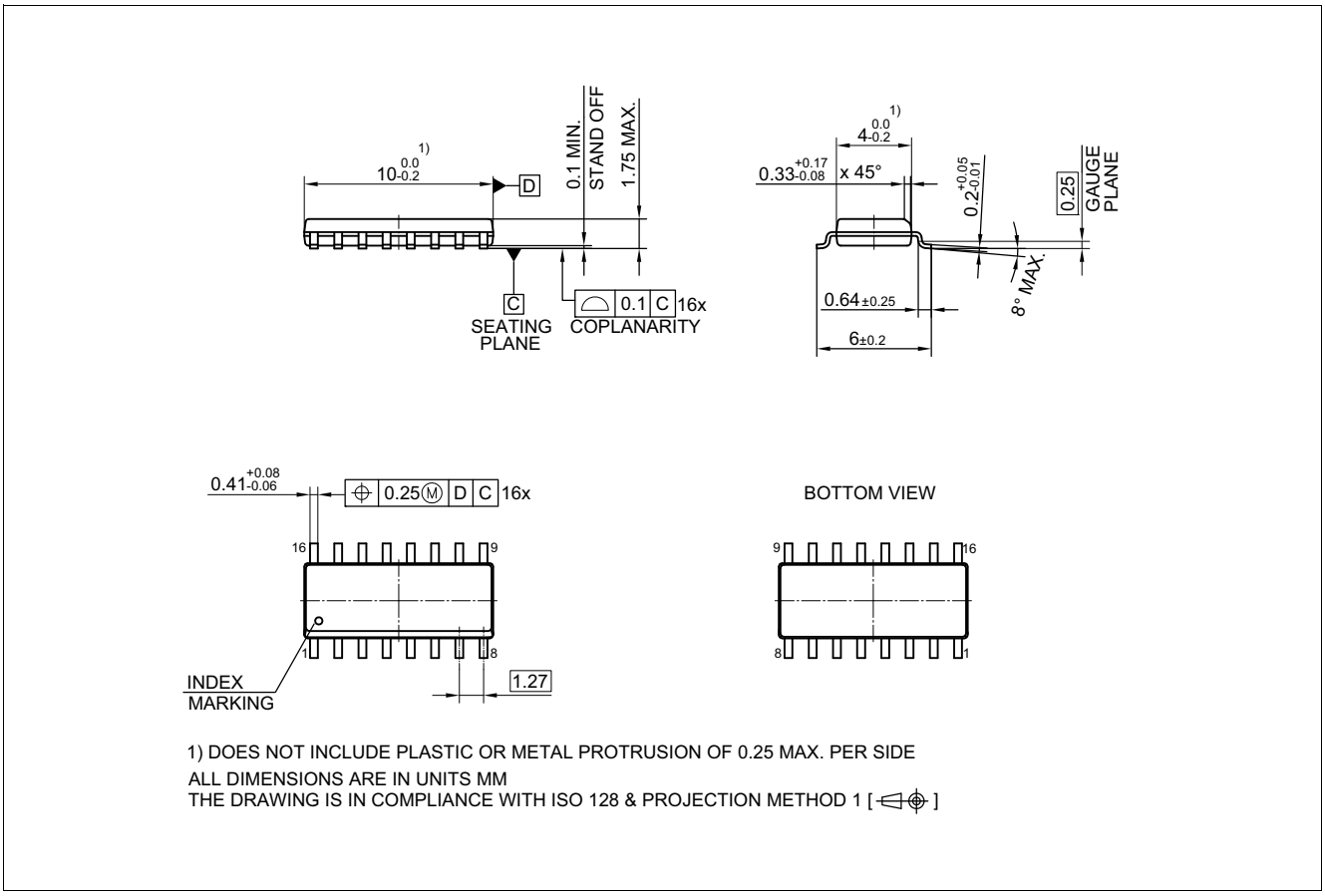


Figure 24 PG-DSO-16-11 outline

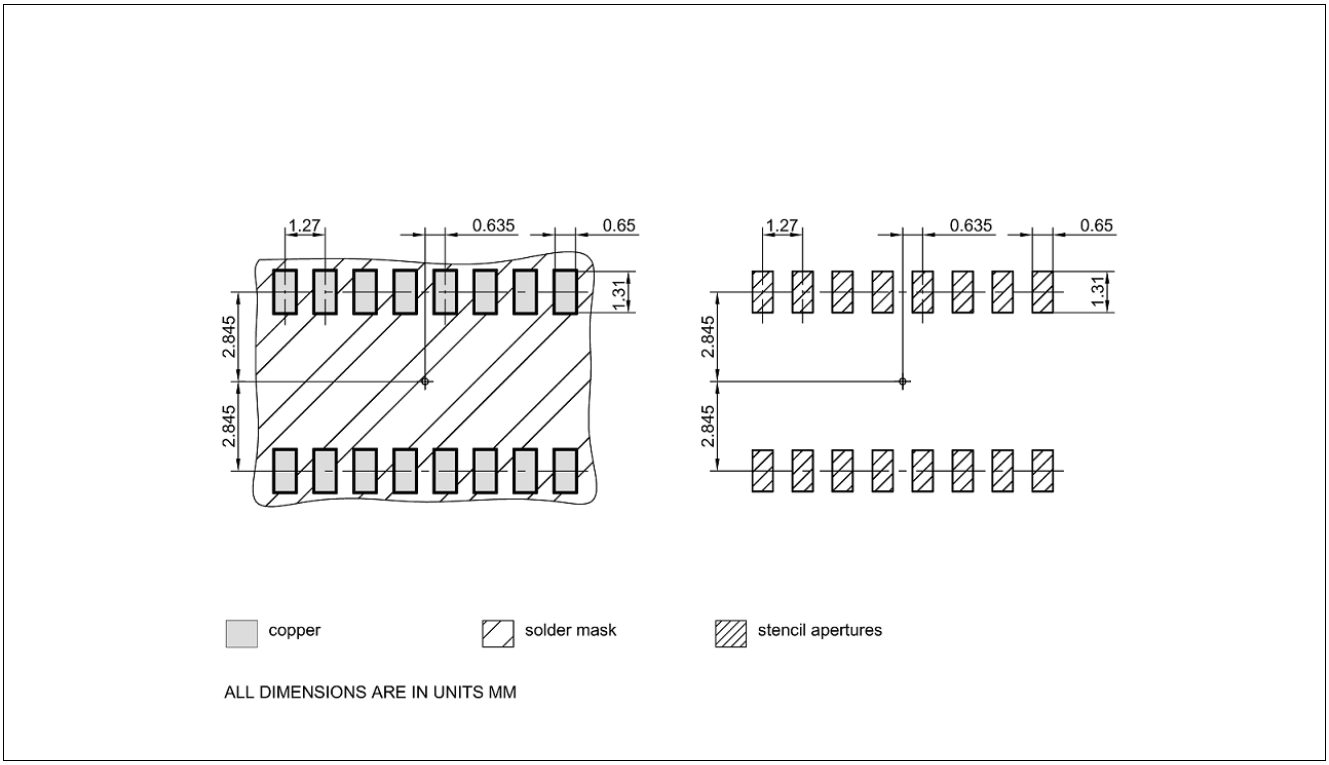


Figure 25 PG-DSO-16-11 footprint

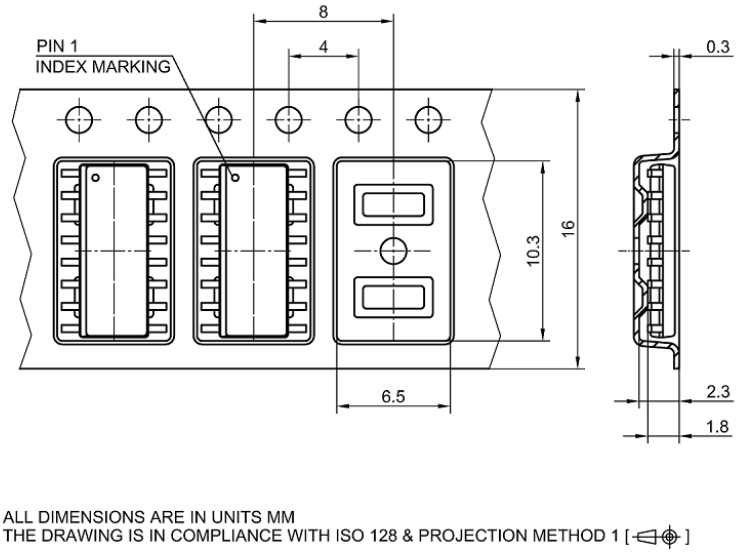


Figure 26 PG-DSO-16-11 packaging

10.3 Package PG-DSO-16-30

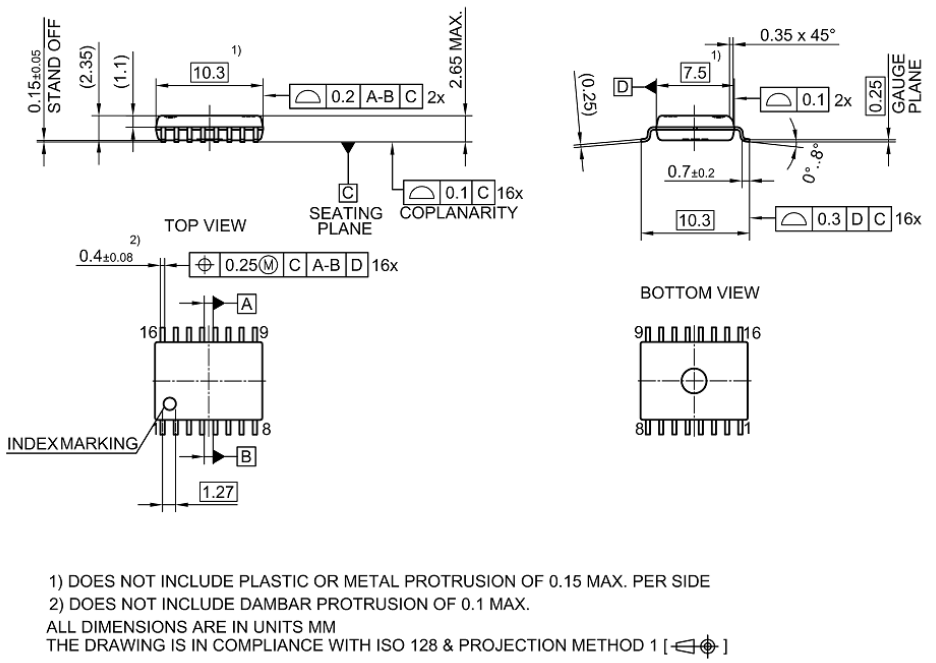


Figure 27 PG-DSO-16-30 outline

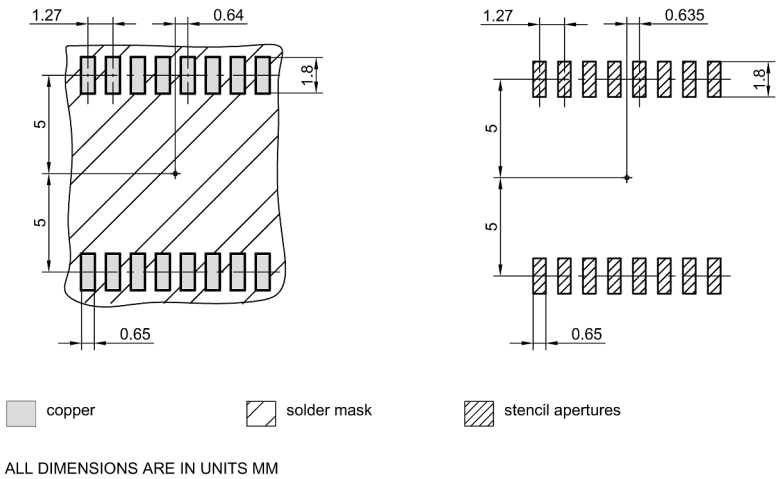


Figure 28 PG-DSO-16-30 footprint

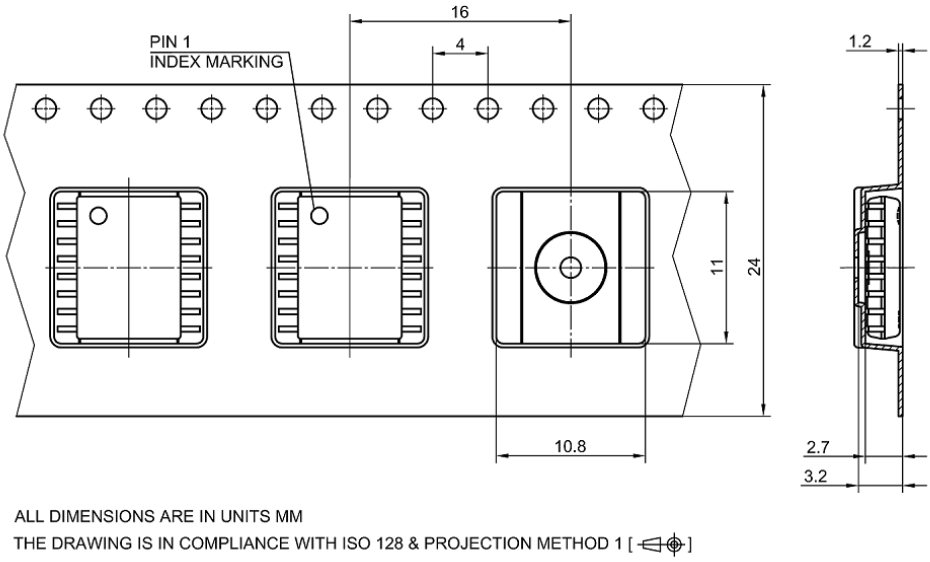


Figure 29 PG-DSO-16-30 packaging

11 Device numbers and markings

Table 19 Device numbers and markings

Part number	Package	Orderable part number (OPN)	Device marking
1EDF5673K	PG-TFLGA-13-1	1EDF5673KXUMA1	1F5673A
1EDF5673F	PG-DSO-16-11	1EDF5673FXUMA1	1F5673A
1EDS5663H	PG-DSO-16-30	1EDS5663HXUMA1	1S5663A

12 Revision History

Page or Item	Subjects (major changes since previous revision)
Rev. 2.00, 2018-11-07	
	Final datasheet created
Rev. 1.00, 2018-10-25	
	Initial version available

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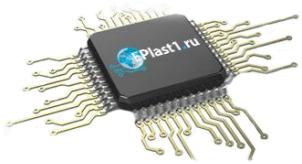

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