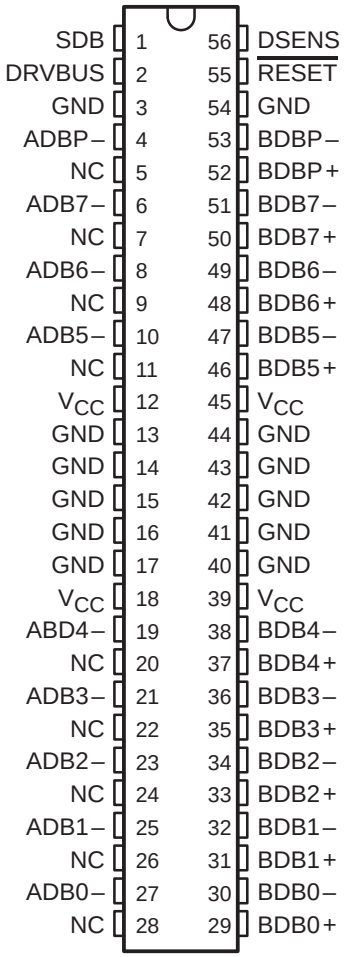
SLLS322A – NOVEMBER 1999 – REVISED JANUARY 2000

- **Provides High-Voltage Differential SCSI From Single-Ended Controller When Used With the SN75970B Control Transceiver**
- **Meets or Exceeds the Requirements of EIA Standard RS-485 and ISO-8482 Standards**
- **ESD Protection on Bus Pins to 12 kV**
- **Packaged in Shrink Small-Outline Package with 25 mil Terminal Pitch and Thin Small-Package with 20 mil Terminal Pitch**
- **Low Disabled-Supply Current 32 mA Typ**
- **Thermal Shutdown Protection**
- **Positive- and Negative-Current Limiting**
- **Power-Up/-Down Glitch Protection**
- **Open-Circuit Failsafe Receivers**

DGG OR DL PACKAGE
(TOP VIEW)



Pins 13 – 17 and 40 – 44 are connected together to the package lead frame and to signal ground.
NC – No internal connection

description

The SN75971B SCSI differential converter-data is a 9-channel RS-485 transceiver. When used in conjunction with its companion control transceiver, the SN75970B, the resulting chip set provides the superior electrical performance of differential SCSI from a single-ended SCSI bus or controller. A 16-bit Ultra-SCSI (or Fast-20) SCSI bus can be implemented with just three devices (two data and one control) in the space efficient, 56-pin, shrink small-outline package (SSOP) or thin shink small outline package (TSSOP) and a few external components. An 8-bit SCSI bus requires only one data and one control transceiver.

The SN75971B is available in a B2 (20 Mxfer) version and a B1 (10 Mxfer) version.

In a typical differential SCSI node, the SCSI controller provides an enable for each external RS-485 transceiver channel. This could require as many as 27 extra terminals for a 16-bit differential bus controller or relegate a 16-bit, single-ended controller to only an 8-bit differential bus. Using the standard nine SCSIcontrol signals, the SN75970B control transceiver decodes the state of the bus and enables the SN75971B data transceiver to transmit the single-ended SCSI input signals (A side) differentially to the cable or receive the differential cable signals (B side) and drive the single-ended outputs to the controller.

A reset function, which disables all outputs and clears internal latches, can be accomplished from two external inputs and two internally-generated signals. $\overline{\text{RESET}}$ (reset) and DSENS (differential sense) are available to external circuits for a bus reset or to disable all outputs should a single-ended cable be inadvertently connected to a differential connector. Internally-generated power-up and thermal-shutdown signals have the same affect when the supply voltage is below approximately 3.5 V or the junction temperature exceeds 175°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000, Texas Instruments Incorporated

description (continued)

The SCSI, differential, converter-data chip operates in two modes depending on the state of the DRVBUS input. With DRVBUS low, a bidirectional latch circuit sets the direction of data transfer. Each data bit has its own latch, and each bit's direction is independent of all other bits. When neither the single-ended nor the differential sides are asserted, the latch disables both A- and B-side output drivers. When the input to either side is asserted, the latch enables the opposite side's driver and sets data flow from the asserted input to the opposite side of the device. When the input deasserts, the latch maintains the direction until the receiver on the enabled driver detects a deassertion. The latch then returns to the initial state. No parity checking is done by this device; the parity signal passes through the device like other data signals do.

When DRVBUS is high, direction is determined by the SDB signal. However, a change in SDB does not always immediately change the direction. When DRVBUS first asserts, the direction indicated by SDB is latched and takes effect immediately. When SDB changes while DRVBUS is high, the drivers that were on immediately turn off. However, the other driver set does not turn on until the receivers sense a deasserted state on all nine data lines. This is done to prevent the active drivers from turning on until all other drivers are off and the terminators pull the lines to a deasserted state.

The single-ended SCSI bus interface consists of CMOS, bidirectional inputs and outputs. The drivers are rated to $\pm$16 mA of output current. The receiver inputs are pulled high with approximately 4 mA to eliminate the need for external pullup resistors for the open-drain outputs of most single-ended SCSI controllers. The single-ended side of the device is not intended to drive the SCSI bus directly.

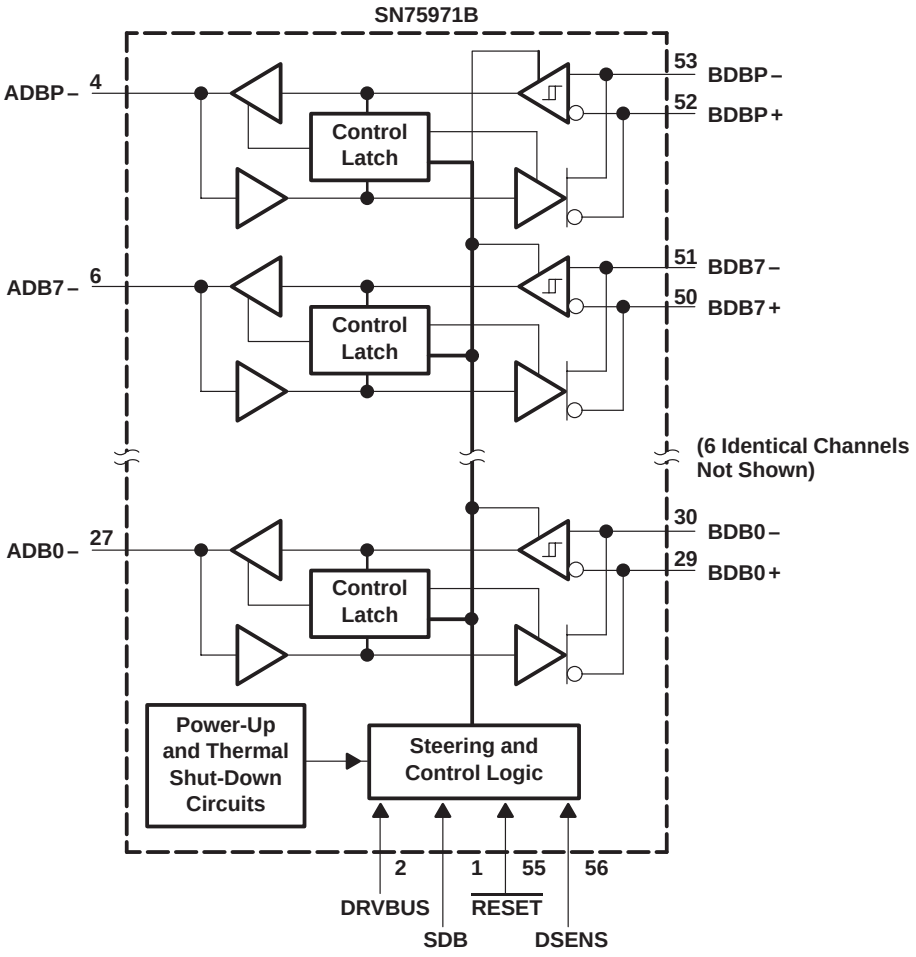
The differential SCSI bus interface consists of bipolar, bidirectional inputs and outputs that meet or exceed the requirements of EIA-485 and ISO 8482-1982/TIA TR30.2 referenced by American National Standard of Information Systems (ANSI) X3.131-1994 Small Computer System Interface-2 (SCSI-2) and SCSI-3 Fast-20 Parallel Interface (Fast-20) X3.277:1996.

The SN75971B is characterized for operation over the temperature range of 0°C to 70°C.

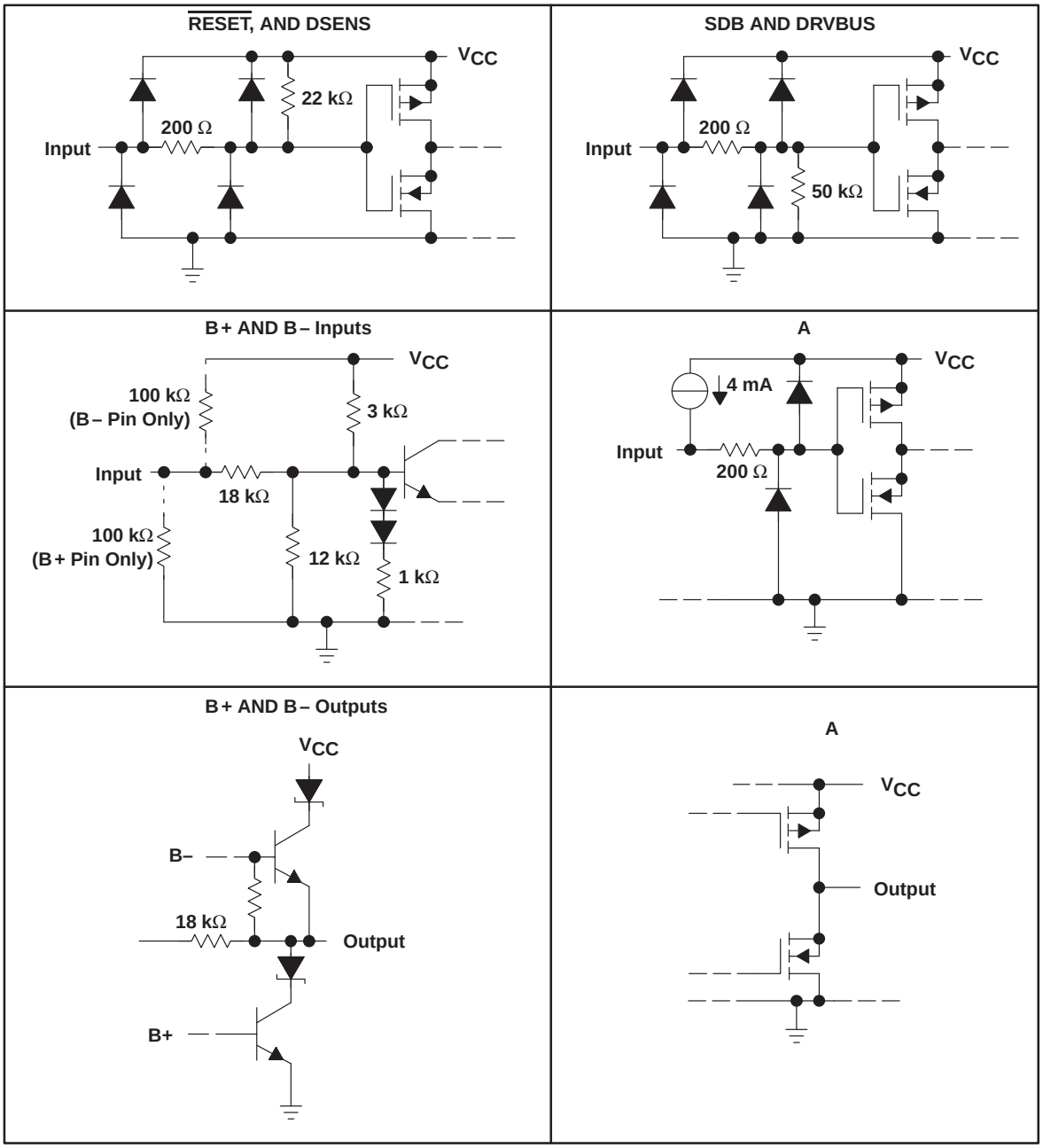
Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADBn–, where n = {0,1,2,3,4,5,6,7,P}	4, 6, 8, 10, 19, 21, 23, 25, 27	I/O, Single-ended SCSI voltage levels, Strong pullup	Bidirectional I/O for data and parity bits to and from the single-ended SCSI controller. As outputs, these terminals can source or sink 16 mA. As inputs, they are pulled up with about 4-mA to eliminate external resistors.
BDBn+, where n = {0,1,2,3,4,5,6,7,P}	29, 31, 33, 35, 37, 46, 48, 50, 52	I/O, RS-485, Weak pulldown	Bidirectional I/O for data and parity to and from the differential SCSI bus.
BDBn–, where n = {0,1,2,3,4,5,6,7,P}	30, 32, 34, 36, 38,47, 49, 51, 53	I/O, RS-485, Weak pulldown	Bidirectional I/O for the complement of data and parity to and from the differential SCSI bus.
DRVBUS	2	Input, TTL levels, Weak pulldown	A high-level logic signal from the control transceiver enables either the single-ended or differential drivers as directed by SDB.
DSENS	56	Input, TTL levels, Weak pullup	A low-level input initializes the internal latches and disables all drivers.
$\overline{\text{RESET}}$	55	Input, TTL levels, Weak pullup	A low-level input initializes the internal latches and disables all drivers.
SDB	1	Input, TTL levels, Weak pulldown	A high-level logic signal from the control transceiver sends data from the differential bus to the single-ended bus. A low-level signal reverses the flow.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.3 V to 7 V
Differential bus voltage range (B side) . . . . . –10 V to 15 V
Single-ended bus voltage range (A side and control inputs) . . . . . –0.3 V to 7 V
Continuous total power dissipation (see Note 2) . . . . . Internally Limited (see Dissipation Rating Table)
Electrostatic discharge (see Note 3): Class 2 A (all pins) . . . . . 4 kV
Class 2 B (all pins) . . . . . 400 V
Class 3 A (B-side and GND) . . . . . 12 kV
Class 3 B (B-side and GND) . . . . . 400 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
3. This absolute maximum rating is tested in accordance with MIL-STD-883C, Method 3015.7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	3333 mW	26.7 mW/°C	2133 mW
DL	3709 mW	29.7 mW/°C	2374 mW

‡ This is the inverse of the traditional junction-to-case thermal resistance ($R_{\theta JA}$) for High-K (per JEDEC) PCB installations.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}	A side and control	2			V
Low-level input voltage, V_{IL}	A side and control			0.8	V
Voltage at any bus terminal (separately or common-mode), V_O or V_I	B side			12 –7	V
High-level output current, I_{OH}	A side			–16	mA
Low-level output current, I_{OL}	A side			16	mA
Operating case temperature, T_C		0		125	°C
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{OD(H)}$	Driver high-level differential output voltage		See Figure 1		–1	–2.2		V
$V_{OD(L)}$	Driver low-level differential output voltage		See Figure 1		1	1.8		V
V_{OH}	High-level output voltage	A side	V_{ID} = –200 mV,	I_{OH} = –16 mA	2.5	4.2		V
		B side	I_{OH} = –60 mA			3.4		
V_{OL}	Low-level output voltage	A side	V_{ID} = 200 mV,	I_{OL} = 16 mA		0.4	0.8	V
		B side	I_{OL} = 60 mA			1.6		
V_{IT+}	Receiver positive-going differential input threshold voltage	B side	I_{OH} = –16 mA	See Figure 2			0.2	V
V_{IT-}	Receiver negative-going differential input threshold voltage		I_{OL} = 16 mA	See Figure 2	–0.2§			V
V_{hys}	Receiver input hysteresis voltage (V_{IT+} – V_{IT-})				35	45		mV
I_I	Bus input current	B or $\overline{B}$	V_I = 12 V, Other input at 0 V	V_{CC} = 5 V		0.6	1	mA
				V_{CC} = 0		0.7	1	
			V_I = –7 V, Other input at 0 V	V_{CC} = 5 V		–0.5	–0.8	mA
				V_{CC} = 0		–0.4	–0.8	
I_{IH}	High-level input current	A side	V_{IH} = 2 V		–2	–5	–8	mA
		$\overline{RESET}$, DSENS				–70	–100	µA
		SDB, DRVBUS					25	
I_{IL}	Low-level input current	A side	V_{IL} = 0.8 V			–6	–9	mA
		$\overline{RESET}$, DSENS				–66	–100	µA
		SDB, DRVBUS					±30	
I_{OS}	Short-circuit output current	B side	V_O = 5 V and 0				±250	mA
I_{OZ}	High-impedance-state output current	A side			–2	–5	–8	
						–6	–9	
		B side				See I_I		
I_{CC}	Supply current	Disabled	$\overline{RESET}$ at 0.8 V,	Others open		38	46	mA
		B to A Enabled	SDB and DRVBUS at 2 V, All other inputs open,	V_{ID} = –1 V, No load		39	50	
		A to B Enabled	SDB at 0.8 V, All other inputs open,	DRVBUS at 2 V, No load		32	66	
C_O	Output capacitance		V_I = 0.6 sin($2\pi \times 10^6$t) + 1.5 V,	BDBn to GND		18	21	pF
C_{pd}	Power dissipation capacitance‡		B to A,	One channel		40		pF
			A to B,	One channel		100		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ C_{pd} determines the no-load dynamic current consumption, $I_S = C_{pd} \times V_{CC} \times f + I_{CC}$.
§ The algebraic convention with the least positive (more negative) limit is designated minimum, is used in this data sheet for the differential input voltage only.

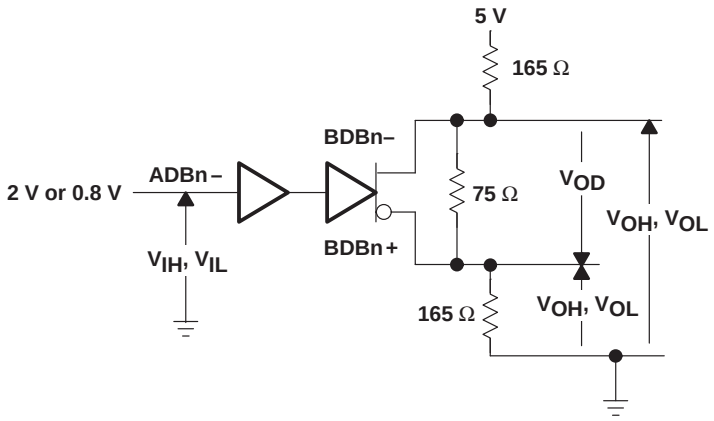
switching characteristics over recommended of operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}, t_{d2}	Delay time, A to B, high- to low-level or low- to high-level output	SN75971B1	See Figures 3 and 4	3	14	ns
			V_{CC} = 5 V, T_A = 25°C, See Figures 3 and 4	4	12	
			V_{CC} = 5 V, T_A = 70°C, See Figures 3 and 4	4.9	12.9	
		SN75971B2	See Figures 3 and 4	5	12	
			V_{CC} = 5 V, T_A = 25°C, See Figures 3 and 4	6.2	10.2	
			V_{CC} = 5 V, T_A = 70°C, See Figures 3 and 4	6.9	10.9	
t_{d3}, t_{d4}	Delay time, B to A, high- to low-level or low- to high-level output	SN75971B1	See Figures 5 and 6	5.4	18.1	ns
			V_{CC} = 5 V, T_A = 25°C, See Figures 5 and 6	6.5	15.4	
			V_{CC} = 5 V, T_A = 70°C, See Figures 5 and 6	7.2	16.1	
		SN75971B2	See Figures 5 and 6	7.7	15	
			V_{CC} = 5 V, T_A = 25°C, See Figures 5 and 6	8.7	13.2	
			V_{CC} = 5 V, T_A = 70°C, See Figures 5 and 6	9.4	13.9	
$t_{sk(pp)}$	Skew, part-to-part†	SN75971B1	A to B See Figures 5 and 6		8	ns
			B to A See Figures 5 and 6		9	
		SN75971B2	A to B See Figures 5 and 6		4	
			B to A See Figures 5 and 6		5	
$t_{sk(p)}$	Pulse skew‡				4	ns
t_{dis1}	Disable time, A to B		See Figures 3 and 4		200	ns
t_{dis2}	Disable time, B to A		See Figures 5 and 6		35	ns
t_{en1}	Enable time, A to B		See Figures 3 and 4		65	ns
t_{en2}	Enable time, B to A		See Figures 5 and 6		65	ns
$t_{en(TX)}$	Enable time, receive-to-transmit		See Figure 7		142	ns

† Part-to-part skew is the magnitude of the difference in propagation delay times between any two devices when both operate with the same supply voltages, the same temperature, and the same loads.

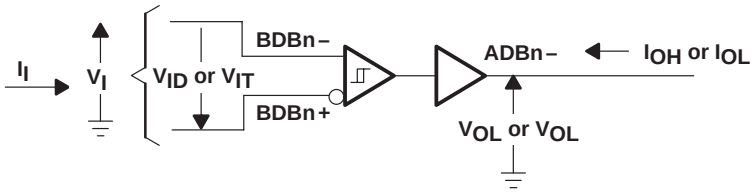
‡ Pulse skew is the difference between the high-to-low and low-to-high propagation delay times of any single channel.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Resistance values are in ohms with a tolerance of ± 5%.
B. All input voltage levels are held to within 0.01 V.
C. The logical function is set with SDB at 0.8 V, DRVBUS at 3.5 V, and all others left open.

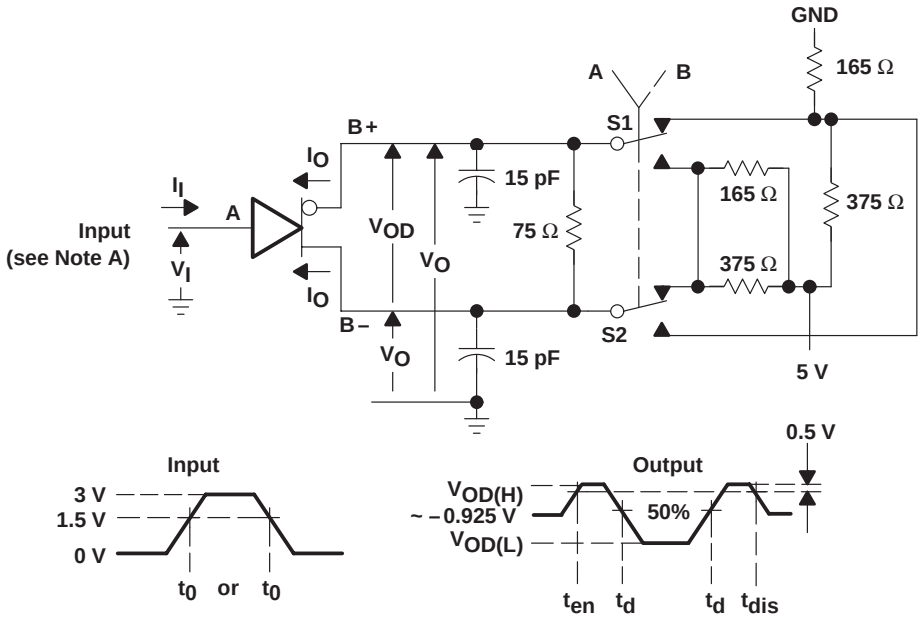
Figure 1. Differential Driver V_{OD}, V_{OH}, and V_{OL} Test Circuit



NOTES: A. Resistance values are in ohms with a tolerance of ± 5%.
B. All input voltage levels are held to within 0.01 V.
C. The logical function is set with SDB and DRVBUS at 3.5 V, and all others left open.

Figure 2. Single-Ended Driver V_{OH}, V_{OL}, V_{IT+}, and V_{IT-} Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 45% < duty cycle < 50%, t_r ≤ 1 ns, t_f ≤ 1 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Resistance values are in ohms with a tolerance of ± 5%.
D. All input voltage levels are held to within 0.01 V.

Figure 3. A to B Propagation Delay Time Test Circuit

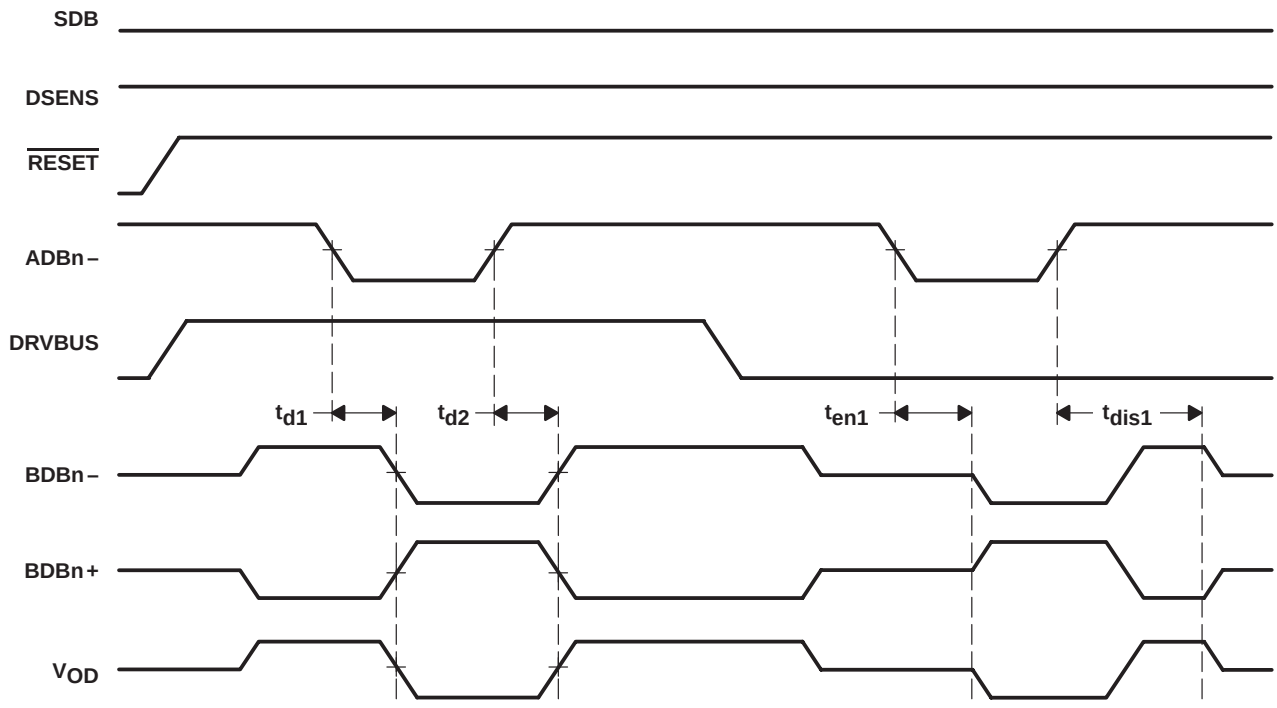
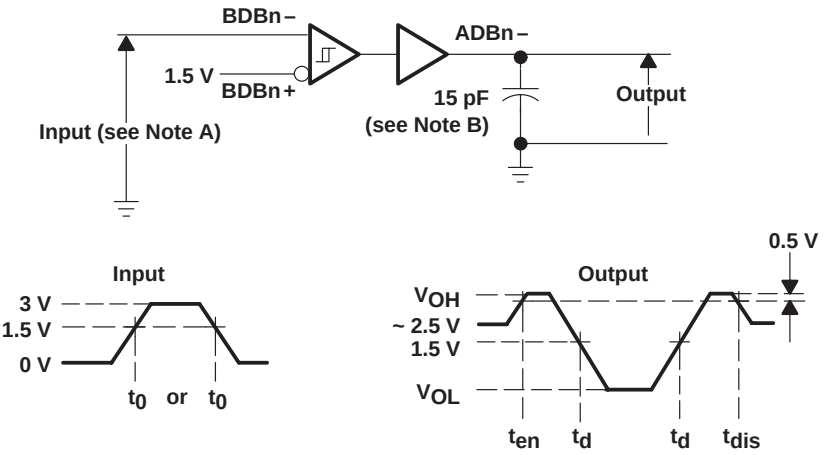


Figure 4. A to B Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 45% < duty cycle < 50%, t_r ≤ 1 ns, t_f ≤ 1 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. Resistance values are in ohms with a tolerance of ± 5%.
D. All input voltage levels are held to within 0.01 V.

Figure 5. B to A Propagation Delay Time Test Circuit

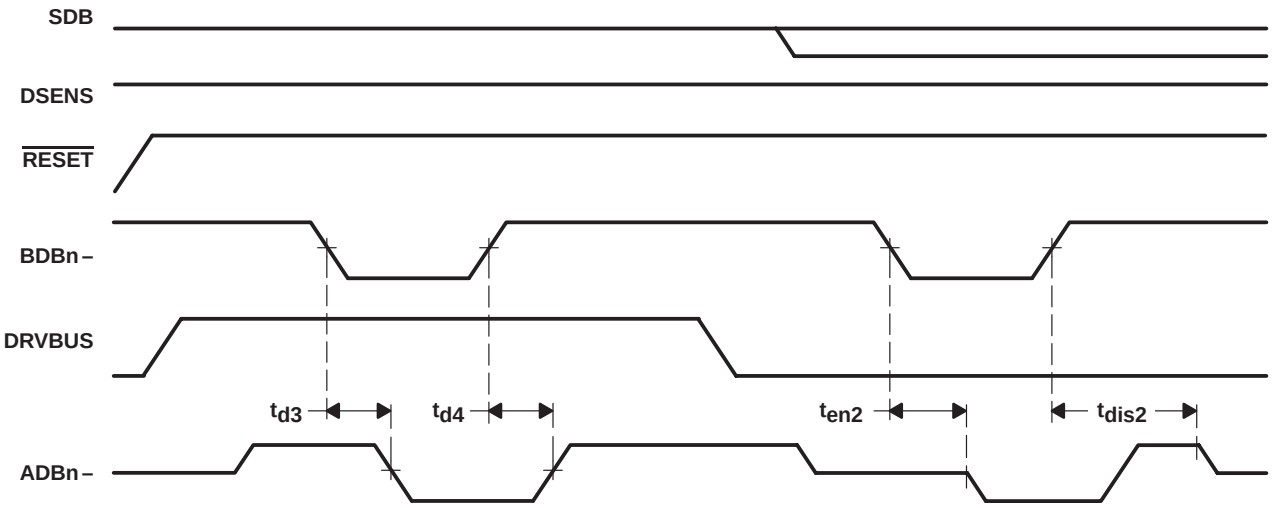


Figure 6. B to A Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

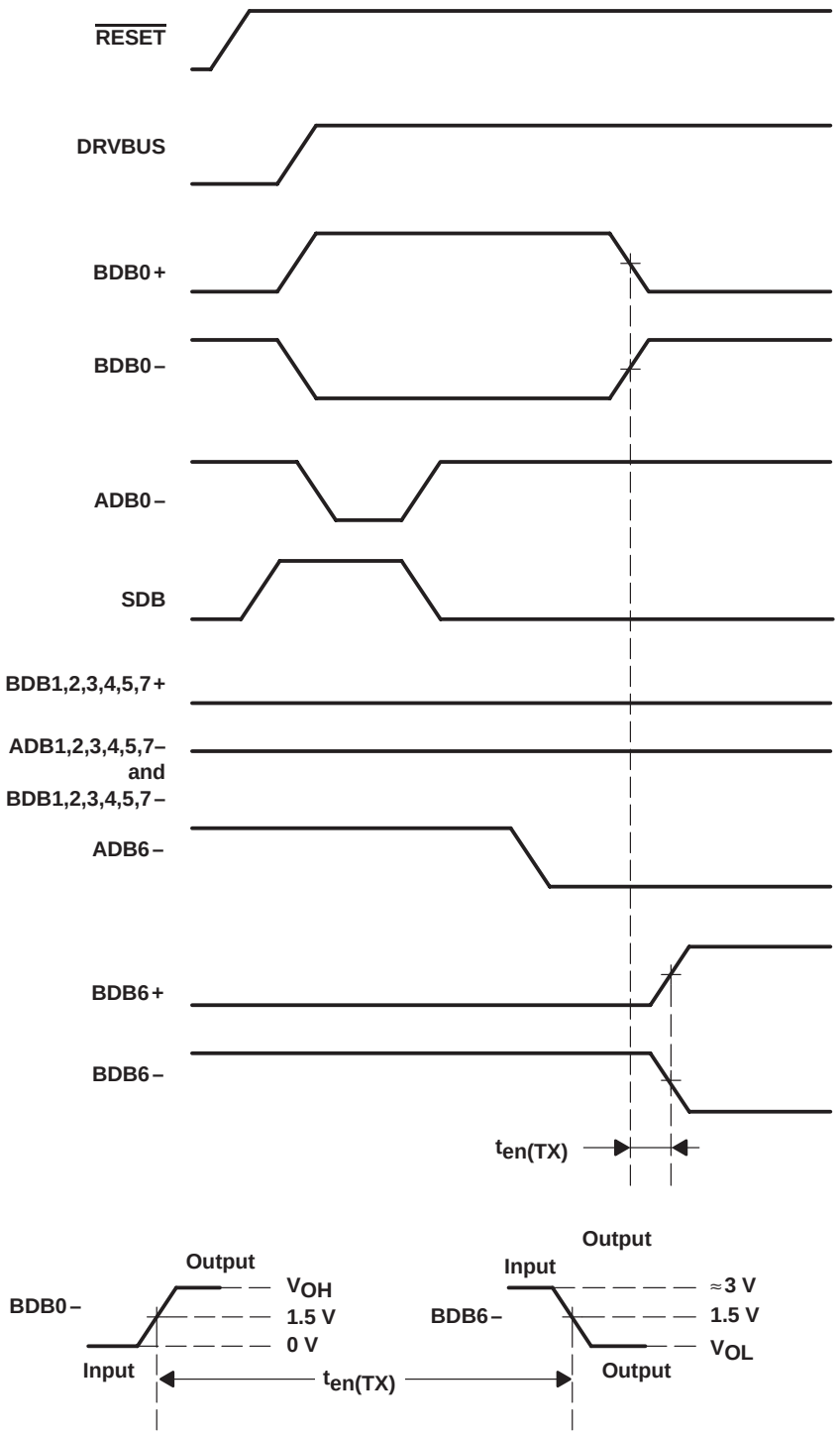
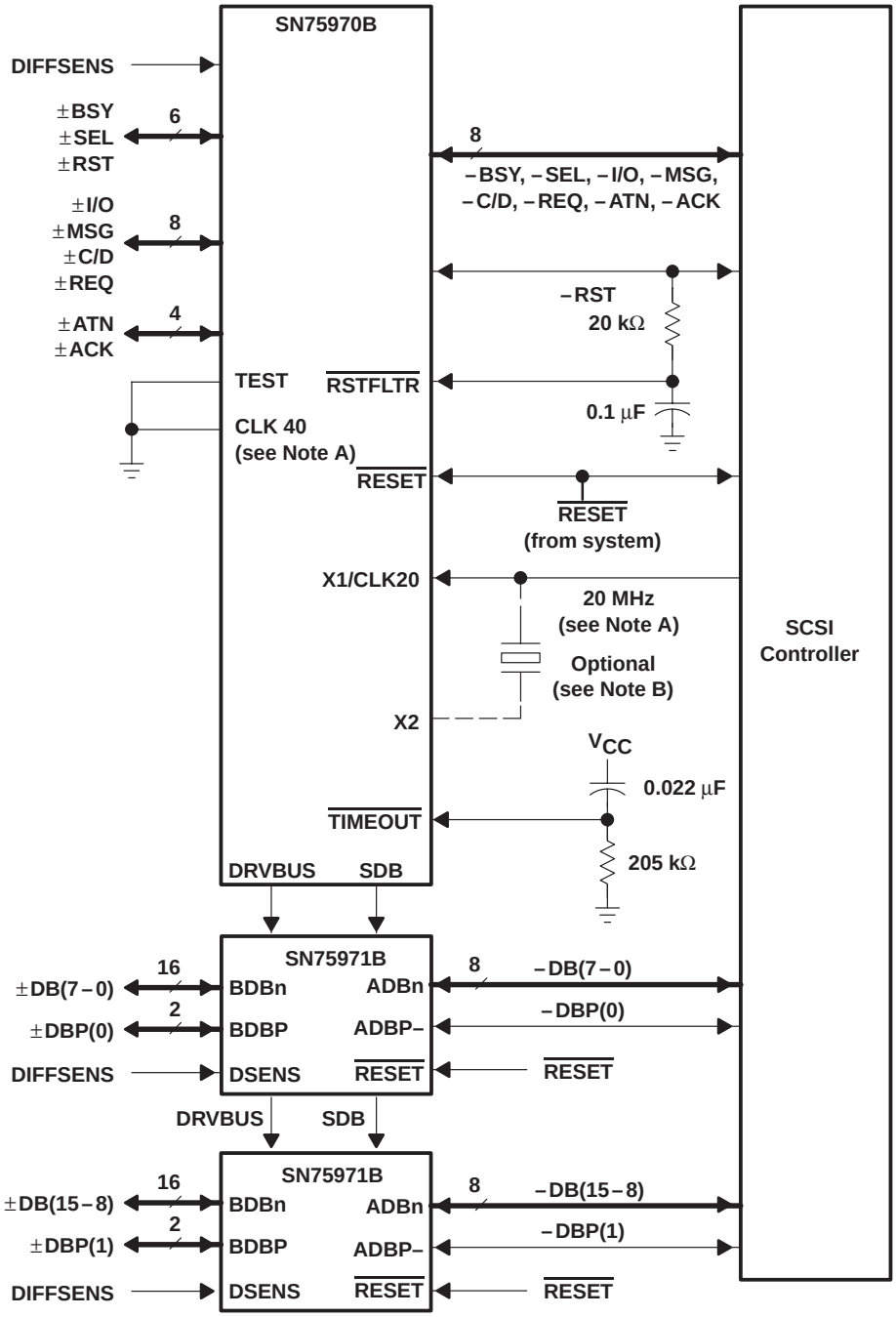


Figure 7. Receive-to-Transmit ($t_{en(TX)}$) Timing Waveforms

APPLICATION INFORMATION



NOTES: A. When using the 40-MHz clock input, X1 must be connected to V_{CC}.
B. The oscillator cell of the SN75970B is for a series-resonant crystal and requires approximately 10 pF (including fixture capacitance) from X1 and X2 to ground in order to function.

Figure 8. Typical Application of the SN75970B and SN75971B

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75971B1DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B1	Samples
SN75971B1DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B1	Samples
SN75971B2DGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B2	Samples
SN75971B2DGGG4	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B2	Samples
SN75971B2DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B2	Samples
SN75971B2DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75971B2	Samples
SN75971BDGG	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI			
SN75971BDL	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated

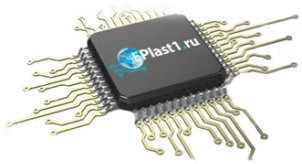
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.