12-Bit, 10Msps, Sampling ADC

FEATURES

- **10Msps Sample Rate**
- **Single 5V Supply or ±5V Supplies**
- **71dB S/(N + D) and 83dB SFDR at Nyquist**
- **100MHz Full-Power Bandwidth Sampling**
- **Input PGA**
- Integral Nonlinearity Error <0.35LSB
- Differential Nonlinearity <0.25LSB
- ±2.048V, ±1.024V and ±0.512V Bipolar Input Range
- Out-of-Range Indicator
- True Differential Inputs with 75dB CMRR
- Power Dissipation: 250mW
- 28-Pin Narrow SSOP Package

APPLICATIONS

- Telecommunications
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- High Speed Data Acquisition
- Spectral Analysis
- Imaging Systems

DESCRIPTION

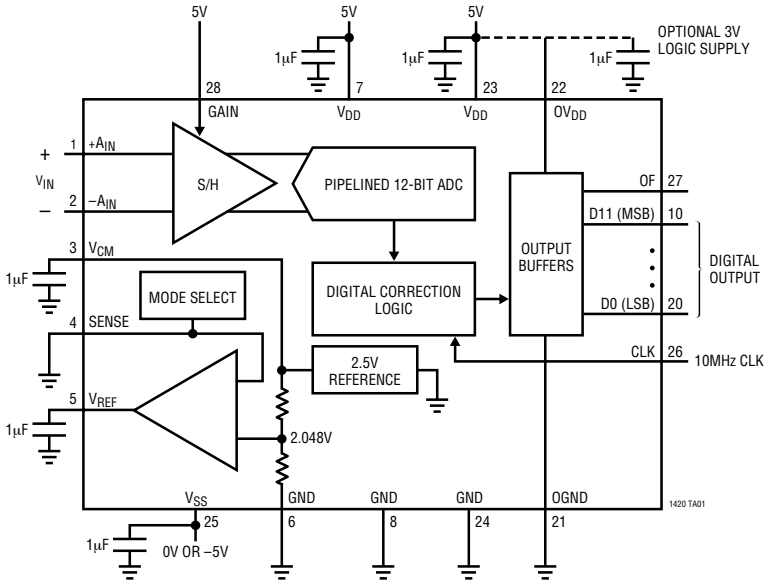
The LTC®1420 is a 10Msps, 12-bit sampling A/D converter that draws only 250mW from either single 5V or dual ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold, a precision reference and a PGA input circuit.

The LTC1420 has a flexible input circuit that allows full-scale input ranges of ±2.048V ±1.024V and ±0.512V. The input common mode voltage is arbitrary, though a 2.5V reference is provided for single supply applications. The input PGA has a digitally selectable 1x or 2x gain.

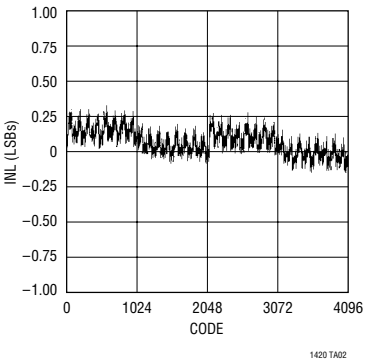
Maximum DC specs include ±1LSB INL and ±1LSB DNL over temperature. Outstanding AC performance includes 71dB S/(N + D) and 83dB SFDR at the Nyquist input frequency of 5MHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 100MHz bandwidth. The 75dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source. A separate output logic supply allows direct connection to 3V components.

TYPICAL APPLICATION



Typical INL Curve

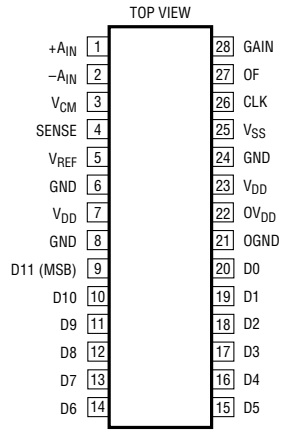


ABSOLUTE MAXIMUM RATINGS

$0V_{DD} = V_{DD}$ (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Input Voltage
(Note 4) ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Digital Output Voltage ..... (V_{SS} – 0.3V) to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC1420C ..... 0°C to 70°C
LTC1420I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 80°C/W

ORDER PART NUMBER
LTC1420CGN
LTC1420IGN

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With Internal 4.096V Reference. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●		±0.35	±1	LSB
Differential Linearity Error		●		±0.25	±1	LSB
Offset Error	(Note 8)	 ●		±5	12 16	LSB LSB
Full-Scale Error				±10	30	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0			±15		ppm/°C

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9) $+A_{IN} – (–A_{IN})$	V_{REF} = 4.096V (SENSE = 0V), GAIN = 5V (1×) V_{REF} = 4.096V (SENSE = 0V), GAIN = 0V (2×) V_{REF} = 2.048V (SENSE = V_{REF}), GAIN = 5V (1×) V_{REF} = 2.048V (SENSE = V_{REF}), GAIN = 0V (2×) External V_{REF} (SENSE = 5V), GAIN = 5V (1×) External V_{REF} (SENSE = 5V), GAIN = 0V (2×)	● ● ● ● ● ●		±2.048 ±1.024 ±1.024 ±0.512 ±V_{REF}/2 ±V_{REF}/4		V V V V V V
I_{IN}	Analog Input Leakage Current		●			±20	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			12 6		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time				30		ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–250		ps
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				0.6		ps
CMRR	Analog Input Common Mode Rejection Ratio	–2.048V < ($–A_{IN}$ = $+A_{IN}$) < 2.048V			75		dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, V_{SS} = –5V, f_{SAMPLE} = 10MHz, V_{REF} = 4.096V. +A_{IN} = –0.1dBFS single ended input, –A_{IN} = 0V. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1MHz Input Signal 5MHz Input Signal	● ●	68.5 68	71.4 71.0		dB dB
THD	Total Harmonic Distortion	1MHz Input Signal, First 5 Harmonics 5MHz Input Signal, First 5 Harmonics	● ●		–84 –81	–77 –73	dB dB
SFDR	Peak Harmonic or Spurious Noise	1MHz Input Signal 5MHz Input Signal	● ●		–85 –83	–78.5 –75	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–80		dB
	Full-Power Bandwidth				100		MHz
	Input Referred Noise	±2.048V Input Range ±1.024V Input Range, 2x Mode (SENSE = GAIN = 0V)			0.22 0.33		LSB_{RMS} LSB_{RMS}
	Overvoltage Recovery Time	1.5x FS Input to 0 (Settling to 1LSB)			15		ns
	Full-Scale Step Acquisition Time	Settling to 1LSB			15		ns

INTERNAL REFERENCE CHARACTERISTICS

T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0	2.475	2.50	2.525	V
V_{CM} Output Tempco	I_{OUT} = 0		±15		ppm/°C
V_{CM} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V –5.25V ≤ V_{SS} ≤ –4.75V		0.6 0.03		mV/V mV/V
V_{CM} Output Resistance	0.1mA ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA		8		Ω
V_{REF} Output Voltage	SENSE = GND, I_{OUT} = 0 SENSE = V_{REF}, I_{OUT} = 0 SENSE = V_{DD}		4.096 2.048 Drive V_{REF} with External Reference		V V V
V_{REF} Output Tempco			±15		ppm/°C

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage (Clock Pin)	V_{DD} = 5.25V, V_{SS} = 0V V_{DD} = 5.25V, V_{SS} = –5V	● ●	2.4 3.5			V V
V_{IL}	Low Level Input Voltage (Clock Pin)	V_{DD} = 4.75V, V_{SS} = 0V V_{DD} = 4.75V, V_{SS} = –5V	● ●			0.8 1	V V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				1.8		pF
V_{OH}	High Level Output Voltage	0V_{DD} = 4.75V, I_O = –10µA 0V_{DD} = 4.75V, I_O = –200µA 0V_{DD} = 2.7V, I_O = –10µA 0V_{DD} = 2.7V, I_O = –200µA	 ● ●	 4.0 2.3	4.74 4.71 2.6 	 	V V V V
V_{OL}	Low Level Output Voltage	0V_{DD} = 4.75V, I_O = 160µA 0V_{DD} = 4.75V, I_O = 1.6mA 0V_{DD} = 2.7V, I_O = 160µA 0V_{DD} = 2.7V, I_O = 1.6mA	 ● ●		0.05 0.10 0.05 0.10	 0.4 0.4	V V V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			50		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			35		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage	(Note 10)		4.75		5.25	V
OV_{DD}	Output Supply Voltage	(Note 10)		2.7		5.25	V
V_{SS}	Negative Supply Voltage	Dual Supply Mode Single Supply Mode		–5.25	 0	–4.75	V V
I_{DD}	Positive Supply Current		●		48	58	mA
I_{SS}	Negative Supply Current		●		1.4	2.5	mA
P_D	Power Dissipation		●		250	300	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Specifications are guaranteed for both dual supply and single supply operation. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SAMPLE}	Maximum Sampling Frequency		●	0.02		10	MHz
t_{CONV}	Conversion Time		●		70	90	ns
t_{ACQ}	Acquisition Time		●	10	30		ns
t_H	CLK High Time		●	20	50		ns
t_L	CLK Low Time		●	20	50		ns
t_{AP}	Aperature Delay of Sample-and-Hold				–250		ps

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with GND and OGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latchup. GAIN is not clamped to V_{DD}. When CLK is taken above V_{DD}, it will be clamped by an internal diode. The CLK pin can handle input currents of greater than 100mA above V_{DD} without latchup.

Note 5: V_{DD} = 5V, V_{SS} = –5V or 0V, f_{SAMPLE} = 10MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Dynamic specifications are guaranteed for dual supply operation with a single-ended $+A_{IN}$ input and $–A_{IN}$ grounded. For single supply dynamic specifications, refer to the Typical Performance Characteristics.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

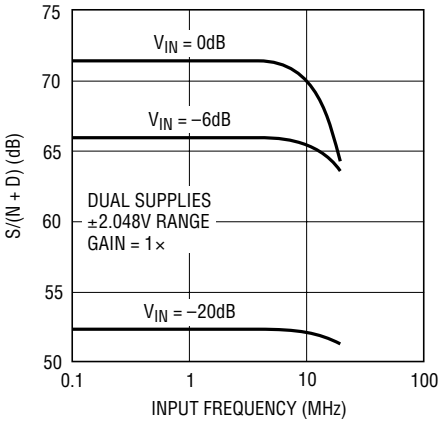
Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

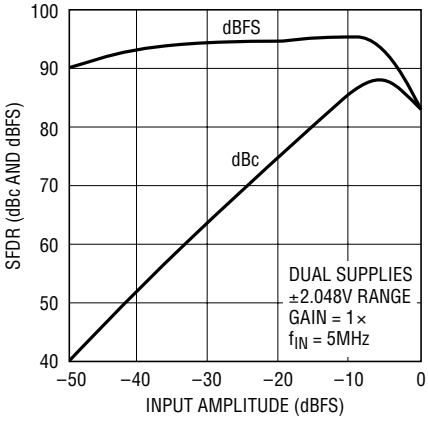
Note 10: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

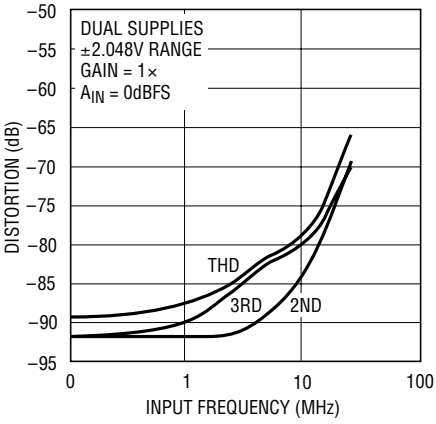
S/(N+D) vs Input Frequency and Amplitude



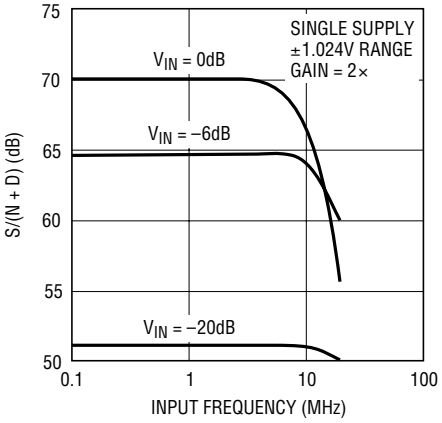
Spurious-Free Dynamic Range vs Input Amplitude



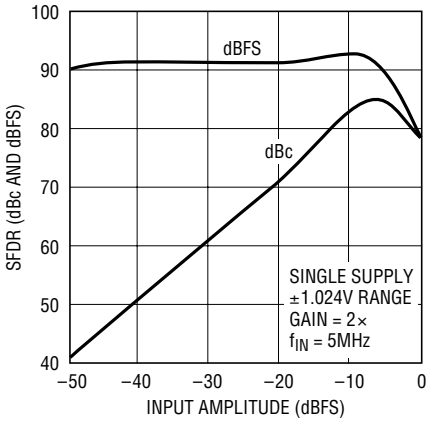
Distortion vs Input Frequency



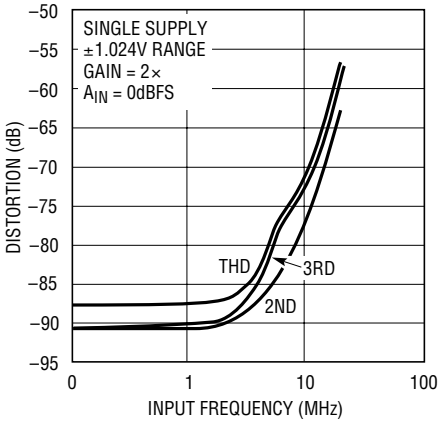
S/(N+D) vs Input Frequency and Amplitude



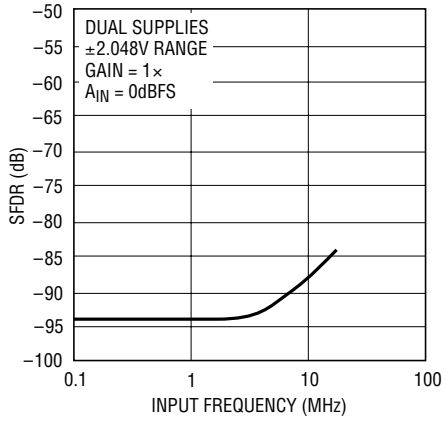
Spurious-Free Dynamic Range vs Input Amplitude



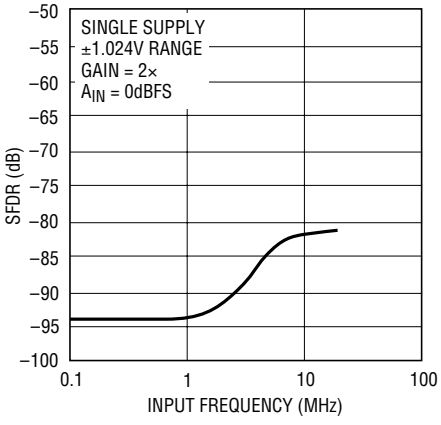
Distortion vs Input Frequency



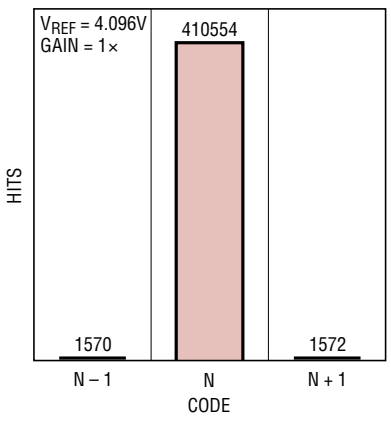
SFDR vs Input Frequency, Differential Input



SFDR vs Input Frequency, Differential Input

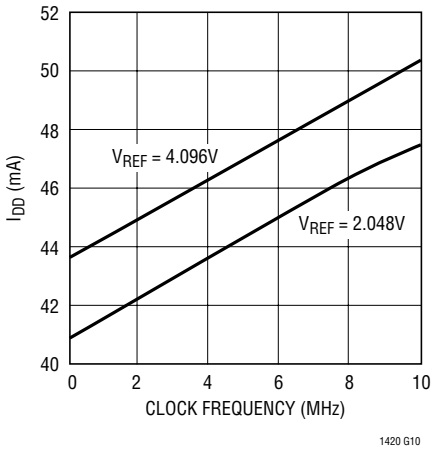


Grounded Input Histogram

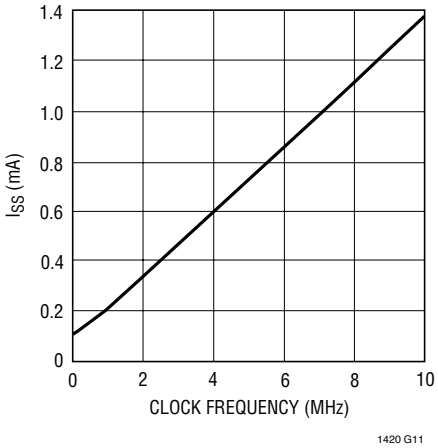


TYPICAL PERFORMANCE CHARACTERISTICS

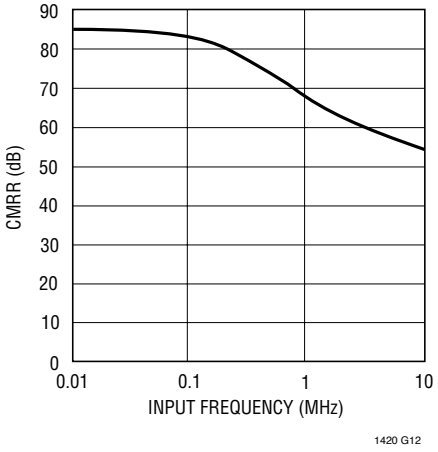
I_{DD} vs Clock Frequency



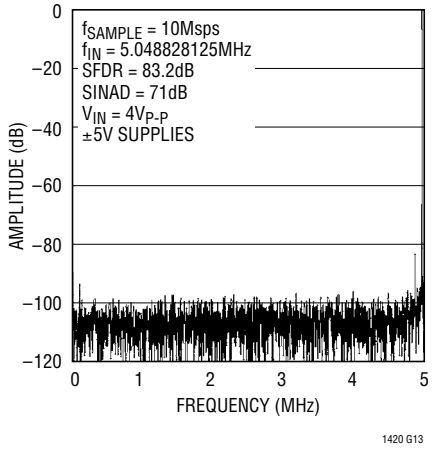
I_{SS} vs Clock Frequency



CMRR vs Input Frequency



LTC1420 Nonaveraged 4096 Point FFT



PIN FUNCTIONS

+A_{IN} (Pin 1): Positive Analog Input.

–A_{IN} (Pin 2): Negative Analog Input.

V_{CM} (Pin 3): 2.5V Reference Output.Optional input common mode for single supply operation. Bypass to GND with a 1µF to 10µF ceramic.

SENSE (Pin 4): Reference Programming Pin. Ground selects V_{REF} = 4.096V. Short to V_{REF} for 2.048V. Connect SENSE to V_{DD} to drive V_{REF} with an external reference.

V_{REF} (Pin 5): DAC Reference. Bypass to GND with a 1µF to 10µF ceramic.

GND (Pin 6): DAC Reference Ground.

V_{DD} (Pin 7): Analog 5V Supply. Bypass to GND with a 1µF to 10µF ceramic.

GND (Pin 8): Analog Power Ground.

D11 to D0 (Pins 9 to 20): Data Outputs. The output format is two's complement.

OGND (Pin 21): Output Logic Ground. Tie to GND.

OV_{DD} (Pin 22): Positive Supply for the Output Logic. Connect to Pin 23 for 5V logic. If not shorted to Pin 23, bypass to GND with a 1µF ceramic.

PIN FUNCTIONS

V_{DD} (Pin 23): Analog 5V Supply. Bypass to GND with a 1μF ceramic.

GND (Pin 24): Analog Power Ground.

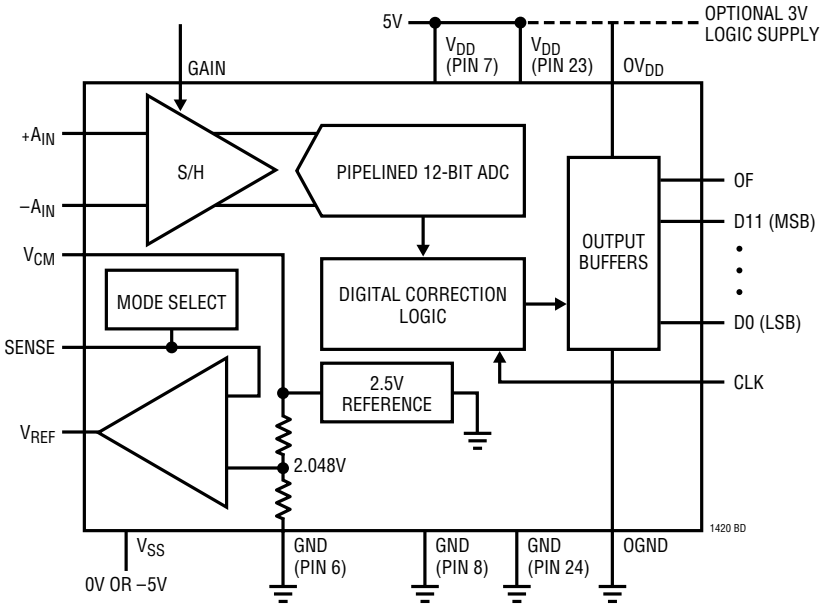
V_{SS} (Pin 25): Negative Supply. Can be –5V or 0V. If V_{SS} is not shorted to GND, bypass to GND with a 1μF ceramic.

CLK (Pin 26): Conversion Start Signal. This active high signal starts a conversion on its rising edge.

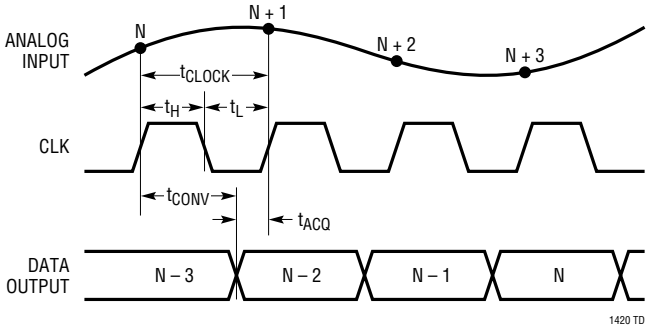
OF (Pin 27): Overflow Output. This signal is high when the digital output is 011111111111 or 100000000000.

GAIN (Pin 28): Gain Select for Input PGA. 5V selects an input gain of 1, 0V selects a gain of 2.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM



APPLICATIONS INFORMATION

Conversion Details

The LTC1420 is a high performance 12-bit A/D converter that operates up to 10Msps. It is a complete solution with an on-chip sample-and-hold, a 12-bit pipelined CMOS ADC, a low drift programmable reference and an input programmable gain amplifier. The digital output is parallel, with a 12-bit two's complement output and an out-of-range (overflow) bit.

The rising edge of the CLK begins a conversion. The differential analog inputs are simultaneously sampled and passed on to the pipelined A/D. After two more conversion starts (plus a 70ns conversion time) the digital outputs are updated with the conversion result and will be ready for capture on the third rising clock edge. Thus, even though a new conversion is begun every time CLK goes high, each result takes three clock cycles to reach the output.

The analog signals that are passed from stage to stage in the pipelined A/D are stored on capacitors. The signals on these capacitors will be lost if the delay between conversions is too long. For accurate conversion results, the part should be clocked faster than 20kHz.

In some pipelined A/D converters if there is no clock present, dynamic logic on the chip will droop and the power consumption sharply increases. The LTC1420 doesn't have this problem. If the part is not clocked for 500µs, an internal timer will refresh the dynamic logic. Thus, the clock can be turned off for long periods of time to save power.

Power Supplies

The LTC1420 will operate from either a single 5V or dual ±5V supply, making it easy to interface the analog input to single or dual supply systems. The digital output drivers have their own power supply pin (OV_{DD}) which can be set from 3V to 5V, allowing direct connection to either 3V or 5V digital systems. For single supply operation, V_{SS} should be connected to analog ground. For dual supply operation, V_{SS} should be connected to –5V. Both V_{DD} pins should be connected to a clean 5V analog supply. (Don't connect V_{DD} to a noisy system digital supply.)

Analog Input Ranges

The LTC1420 has a flexible analog input with a wide selection of input ranges. The input range is always differential and is set by the voltages at the V_{REF} and the GAIN pins (Figure 1). The input range of the A/D core is fixed at $\pm V_{REF}/2$. The reference voltage, V_{REF}, is either set by the on-chip voltage reference or directly driven by an external voltage. The GAIN pin is a digital input that controls the gain of a preamplifier in the sample-and-hold circuit. The gain of this PGA can be set to 1× or 2×. Table 1 gives the input range in terms of V_{REF} and GAIN.

Table 1

GAIN PIN	PGA GAIN	INPUT RANGE ($V_{IN} = A_{IN}^+ - A_{IN}^-$)
5V (Logic H)	1×	$-V_{REF}/2 < V_{IN} < V_{REF}/2$
0V (Logic L)	2×	$-V_{REF}/4 < V_{IN} < V_{REF}/4$

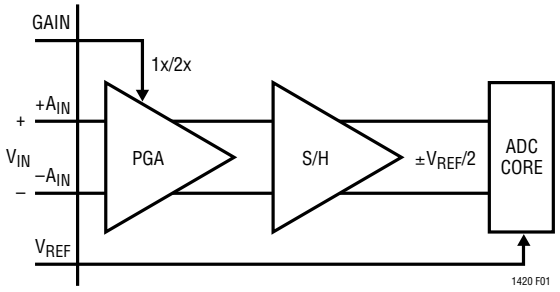


Figure 1. Analog Input Circuit

Internal Reference

Figure 2 shows a simplified schematic of the LTC1420 reference circuitry. An on-chip temperature compensated bandgap reference (V_{CM}) is factory trimmed to 2.500V. The voltage at the V_{REF} pin sets the input span of the ADC to $\pm V_{REF}/2$. An internal voltage divider converts V_{CM} to 2.048V, which is connected to a reference amplifier. The reference programming pin, SENSE, controls how the reference amplifier drives the V_{REF} pin. If SENSE is tied to ground, the reference amplifier feedback is connected to the R1/R2 voltage divider, thus making V_{REF} = 4.096V. If SENSE is tied to V_{REF}, the reference amplifier feedback is connected to SENSE thus making V_{REF} = 2.048V. If SENSE is tied to V_{DD}, the reference amplifier is disconnected from

APPLICATIONS INFORMATION

V_{REF} and V_{REF} can be driven by an external voltage. With two additional resistors, V_{REF} can be set to any voltage between 2.048V and 4.5V.

An external reference or a DAC can be used to drive V_{REF} over a 0V to 5V range (Figures 3a and 3b). The input impedance of the V_{REF} pin is 1k, so a buffer may be required for high accuracy. Driving V_{REF} with a DAC is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio.

Both the V_{CM} and V_{REF} pins must be bypassed with capacitors to ground. For best performance, 1µF or larger ceramic capacitors are recommended. For the case of external circuitry driving V_{REF}, a smaller capacitor can be used at V_{REF} so the input range can be changed quickly. In this case, a 0.05µF or larger ceramic capacitor is acceptable.

The V_{CM} pin is a low output impedance 2.5V reference that can be used by external circuitry. For single 5V supply applications it is convenient to connect $-A_{IN}$ directly to the V_{CM} pin.

Driving the Analog Inputs

The differential inputs of the LTC1420 are easy to drive. The inputs may be driven differentially or single-ended (i. e., the $-A_{IN}$ input is held at a fixed value). The $-A_{IN}$ and $+A_{IN}$ inputs are simultaneously sampled and any common mode signal is reduced by the high common mode rejection of the sample-and-hold circuit. Any common mode input value is acceptable as long as the input pins stay between V_{DD} and V_{SS}. During conversion, the analog inputs are high impedance. At the end of conversion, the inputs draw a small current spike while charging the sample-and-hold.

For superior dynamic performance in dual supply mode, the LTC1420 should be operated with the analog inputs centered at ground, and in single supply mode the inputs should be centered at 2.5V. If required, the analog inputs can be driven differentially via a transformer. Refer to Table 2 for a summary of the analog input and reference configurations and their relative advantages.

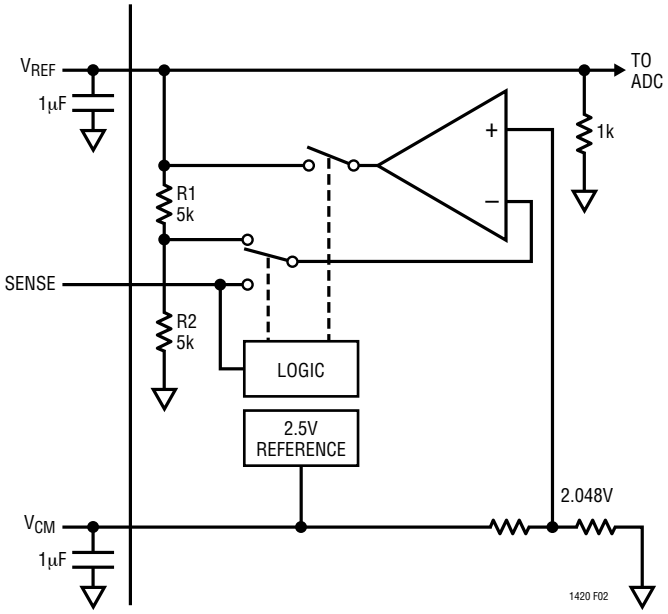


Figure 2. Reference Circuit

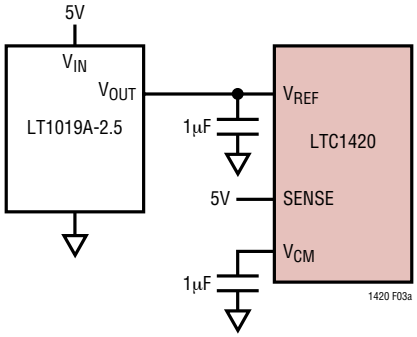


Figure 3a. Using the LT1019-2.5 As an External Reference; Input Range = ±1.25V

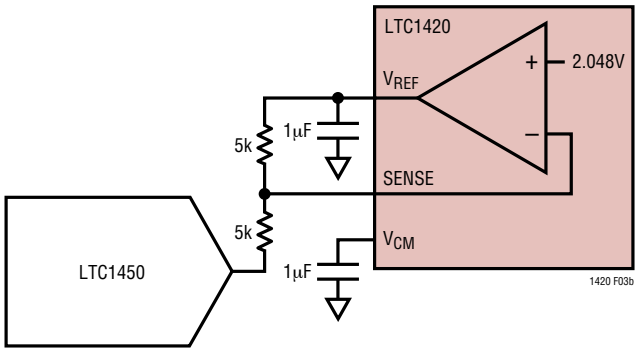


Figure 3b. Driving V_{REF} with a DAC

APPLICATIONS INFORMATION

Table 2. Comparison of Analog Input Configurations

SUPPLIES	COUPLING	V_{REF}	GAIN	A_{IN}^+	A_{IN}^-	COMMENTS
±5V	DC	4.096V	1×	±2.048	0	Best SNR, THD
5V	DC	4.096V	2×	2.5 ± 1.024	2.5	Best SINAD, THD for Single Supply
5V	DC	2.048V	1×	2.5 ± 1.024	2.5	Worse Noise than Above Case
5V	DC	4.096V	1×	2.5 ± 2.048	2.5	Best Single Supply Noise, THD Is Not Optimal
5V	DC	4.096V	1×	0 to 4.096	2.048	Same As Above
±5V	AC (Transformer)	4.096V	1×	±1.024	±1.024	Very Best SNR, THD
5V	AC (Transformer)	4.096V	1×	2.5 ± 1.024	2.5 ± 1.024	Very Best SNR, THD for Single Supply

DC Coupling the Input

In most applications the analog input signal can be directly coupled to the LTC1420 inputs. If the input signal is centered around ground, such as when dual supply op amps are used, simply connect $-A_{IN}$ to ground and connect V_{SS} to –5V (Figure 4). In a single power supply system with the input signal centered around 2.5V, connect $-A_{IN}$ to V_{CM} and V_{SS} to ground (Figure 5). If the input signal is not centered around ground or 2.5V, the voltage for $-A_{IN}$ must be generated externally by a resistor divider or a voltage reference (Figure 6).

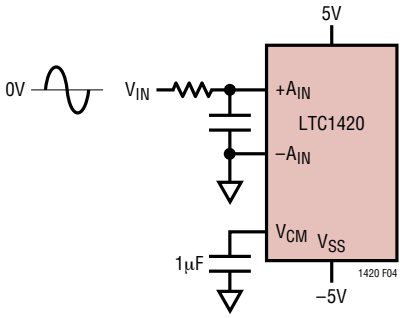


Figure 4. DC Coupling a Ground Centered Signal (Dual Supply System)

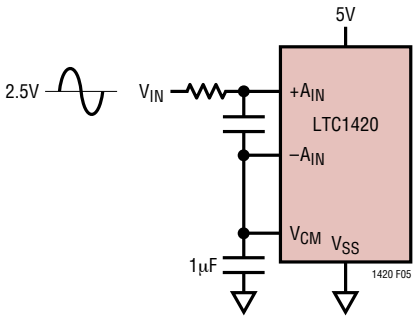


Figure 5. DC Coupling a Signal Centered Around 2.5V (Single Supply System)

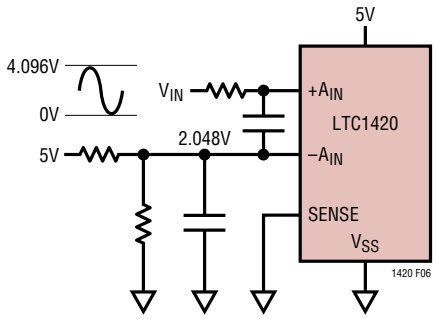


Figure 6. DC Coupling a 0V to 4.096V Signal

AC Coupling the Input

The analog inputs to the LTC1420 can also be AC coupled through a capacitor, though in most cases it is simpler to directly couple the input to the ADC. Figure 7 shows an example where the input signal is centered around ground and the ADC operates from a single 5V supply. Note that the performance would improve if the ADC was operated from a dual supply and the input was directly coupled (as in Figure 4). With AC coupling the DC resistance to ground should be roughly matched for $+A_{IN}$ and $-A_{IN}$ to maintain offset accuracy.

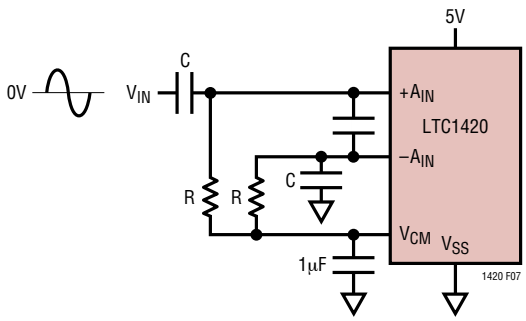


Figure 7. AC Coupling to the LTC1420. Note That the Input Signal Can Almost Always Be Directly Coupled with Better Performance

APPLICATIONS INFORMATION

Differential Operation

The THD and SFDR performance of the LTC1420 can be improved by using a center tap RF transformer to drive the inputs differentially. Though the signal can no longer be DC coupled, the improvement in dynamic performance makes this an attractive solution for some applications. Typical connections for single and dual supply systems are shown in Figures 8a and 8b. Good choices for transformers are the Mini Circuits T1-1T (1:1 turns ratio) and T4-6T (1:4 turns ratio). For best results, the transformer should be located close to the LTC1420 on the printed circuit board.

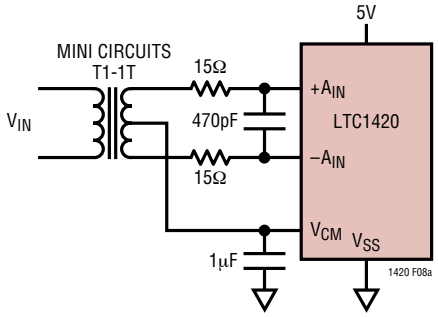


Figure 8a. Single Supply Transformer Coupled Input

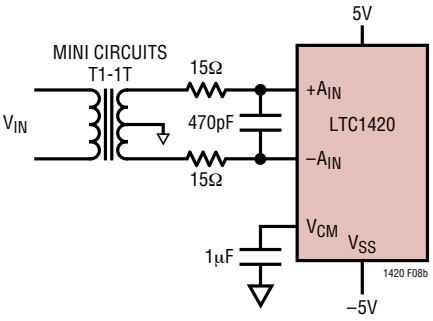


Figure 8b. Dual Supply Transformer Coupled Input

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 100MHz, then the output impedance at 100MHz must be less than 100Ω.

The second requirement is that the closed-loop bandwidth must be greater than 100MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1420 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1420 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 100MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications.

For example, Figure 9 shows a 470pF capacitor from $+A_{IN}$ to $-A_{IN}$ and a 30Ω source resistor to limit the input bandwidth to 11.3MHz. The 470pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the amplifier driving V_{IN} from the ADC's small current glitch. In undersampling applications, an input capacitor this large may prohibitively limit the input bandwidth. If this is the case, use as large an input capacitance as possible. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

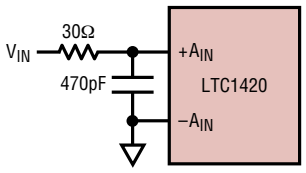


Figure 9. RC Input Filter

APPLICATIONS INFORMATION

Digital Outputs and Overflow Bit (OF)

Figure 10 shows the ideal input/output characteristics for the LTC1420. The output data is two's complement binary for all input ranges and for both single and dual supply operation. One LSB = V_{REF}/4096. To create a straight binary output, invert the MSB (D11). The overflow bit (OF) indicates when the analog input is outside the input range of the converter. OF is high when the output code is 1000 0000 0000 or 0111 1111 1111.

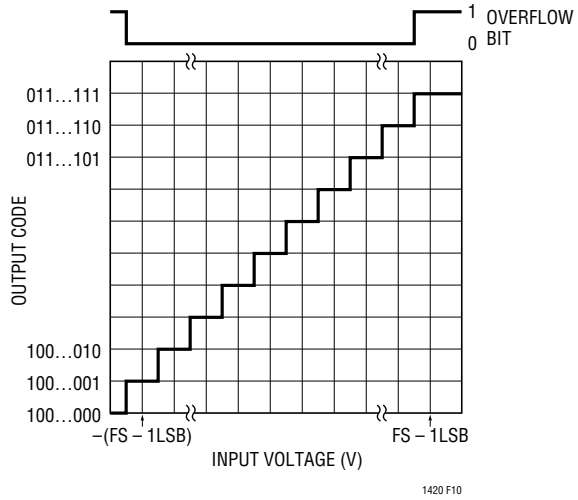


Figure 10. LTC1420 Transfer Characteristics

Full-Scale and Offset Adjustment

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error should be adjusted before full-scale error. Figure 11 shows a method for error adjustment for a dual supply, 4.096V application. For zero offset error apply –0.5mV (i. e., –0.5LSB) at +A_{IN} and adjust R1 until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, apply an input voltage of 2.0465V (FS – 1.5LSBs) at +A_{IN} and adjust R2 until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

Digital Output Drivers

The LTC1420 output drivers can interface to logic operating from 3V to 5V by setting OV_{DD} to the logic power supply. If 5V output is desired, OV_{DD} can be shorted to V_{DD} and share its decoupling capacitor. Otherwise, OV_{DD} requires its own 1µF decoupling capacitor. To prevent digital noise from affecting performance, the load capacitance on the digital outputs should be minimized. If large capacitive loads are required (>30pF), external buffers or 100Ω resistors in series with the digital outputs are suggested.

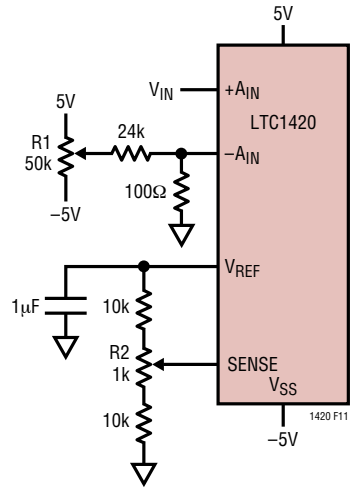


Figure 11. Offset and Full-Scale Adjust Circuit

Timing

The conversion start is controlled by the rising edge of the CLK pin. Once a conversion is started, it cannot be stopped or restarted until the conversion cycle is complete. Output data is updated at the end of conversion, or about 70ns after a conversion is begun. There is an additional two cycle pipeline delay, so the data for a given conversion is output two full clock cycles plus 70ns after the convert start. Thus, output data can be latched on the third CLK rising edge after the rising edge that samples the input.

Clock Input

The LTC1420 only uses the rising edge of the CLK pin for internal timing, and CLK doesn't necessarily need to have a 50% duty cycle. For optimal AC performance, the rise time of the CLK should be less than 5ns. If the available clock has a rise time slower than 5ns, it can be locally sped up with a logic gate. With single supply operation, the clock can be driven with 5V CMOS, 3V CMOS or TTL logic levels. With dual power supplies, the clock should be driven with 5V CMOS levels.

As with all fast ADCs, the noise performance of the LTC1420 is sensitive to clock jitter when high speed inputs

APPLICATIONS INFORMATION

are present. The SNR performance of an ADC when the performance is limited by jitter is given by:

$$SNR = -20\log(2\pi f_{IN} t_J)dB$$

where f_{IN} is the frequency of an input sine wave and t_J is the root-mean-square jitter due to the clock, the analog input and the A/D aperture jitter. To minimize clock jitter, use a clean clock source such as a crystal oscillator, treat the clock signals as sensitive analog traces and use dedicated packages with good supply bypassing for any clock drivers.

Board Layout

To obtain the best performance from the LTC1420, a printed circuit board with a ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be placed under and around the ADC. Pins 6, 8 and 24 (GND), Pin 21 (OGND) and all other analog grounds should be connected to this ground plane. In single supply mode, Pin 25 (V_{SS}) should also be connected to this ground plane. All bypass capacitors for the LTC1420 should also be connected to this ground plane (Figure 12). The digital system ground should be connected to the analog ground plane at only one point, near the OGND pin.

The analog ground plane should be as close to the ADC as possible. Care should be taken to avoid making holes in the analog ground plane under and around the part. To accomplish this, we recommend placing vias for power and signal traces outside the area containing the part and the decoupling capacitors (Figure 13).

Supply Bypassing

High quality, low series resistance ceramic 1µF capacitors should be used at both V_{DD} pins, V_{CM} and V_{REF}. If V_{SS} is connected to –5V it should also be bypassed to ground with 1µF. In single supply operation, V_{SS} should be shorted to the ground plane as close to the part as possible. If OV_{DD} is not shorted to Pin 23 (V_{DD}), it also requires a 1µF decoupling capacitor to ground. Surface mount capacitors such as the AVX 0805ZC105KAT provide excellent bypassing in a small board space. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

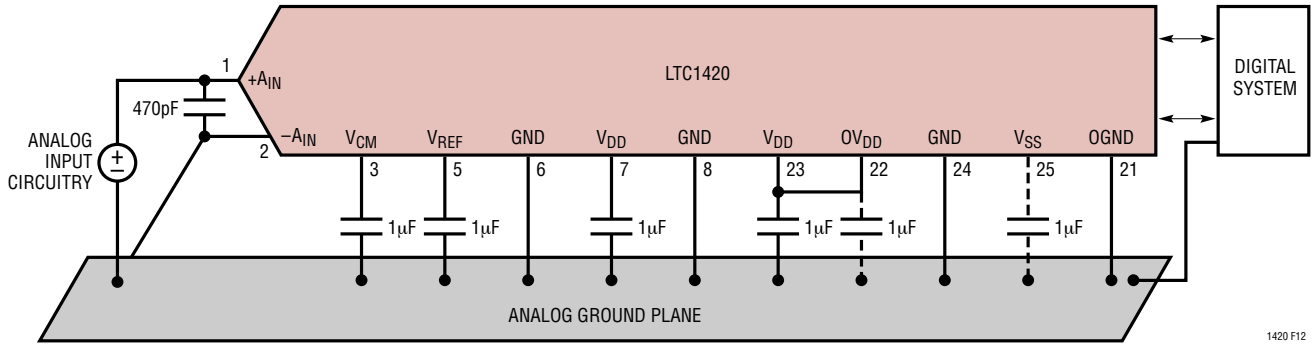


Figure 12. Power Supply Grounding

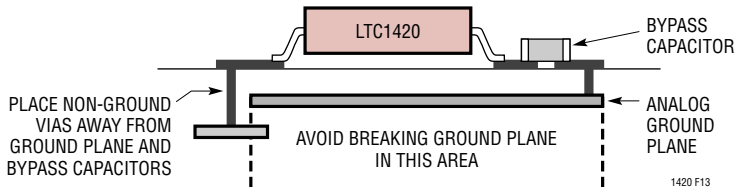


Figure 13. Cross Section of LTC1420 Printed Circuit Board

APPLICATIONS INFORMATION

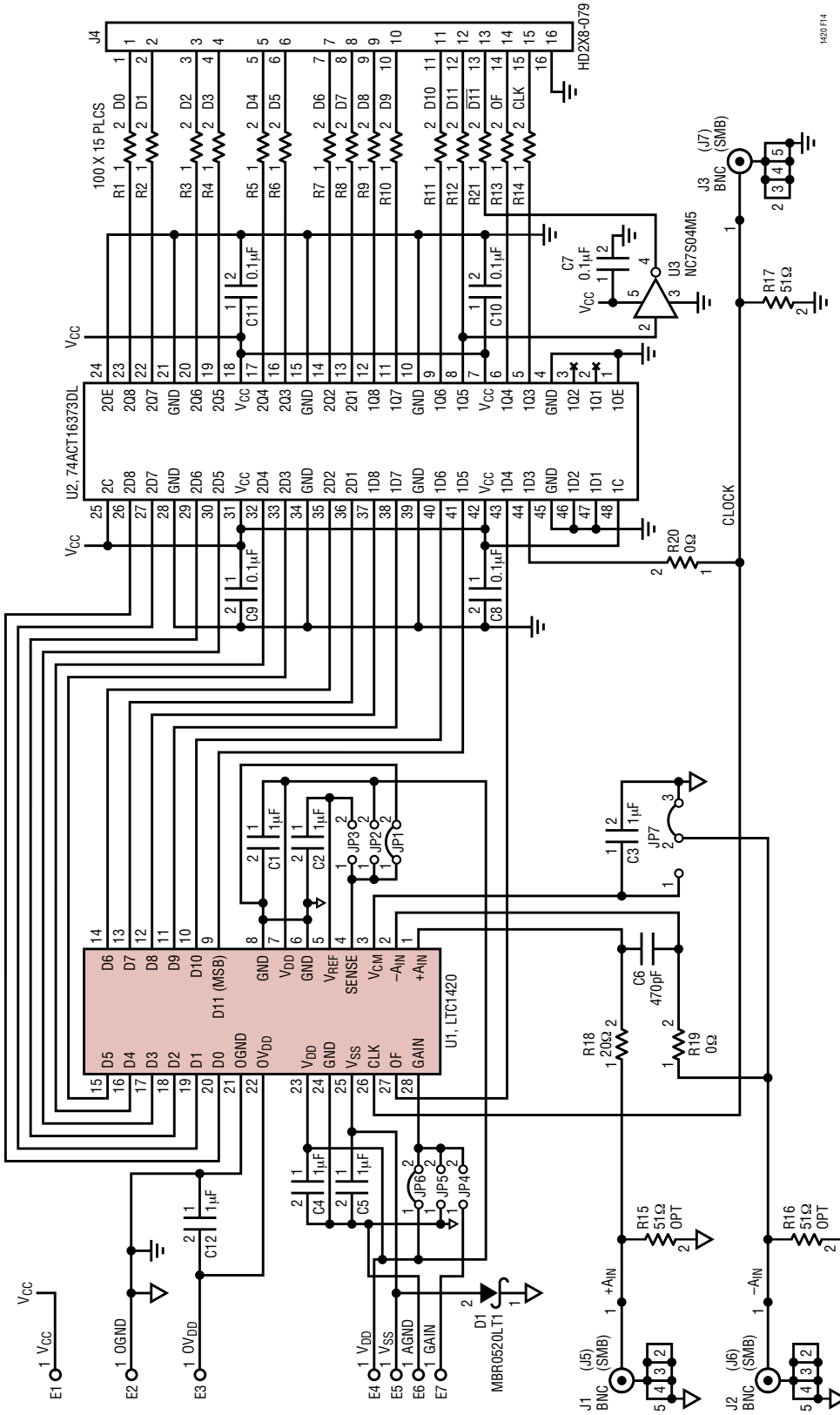


Figure 14. LTC1420 Demo Board Schematic

APPLICATIONS INFORMATION

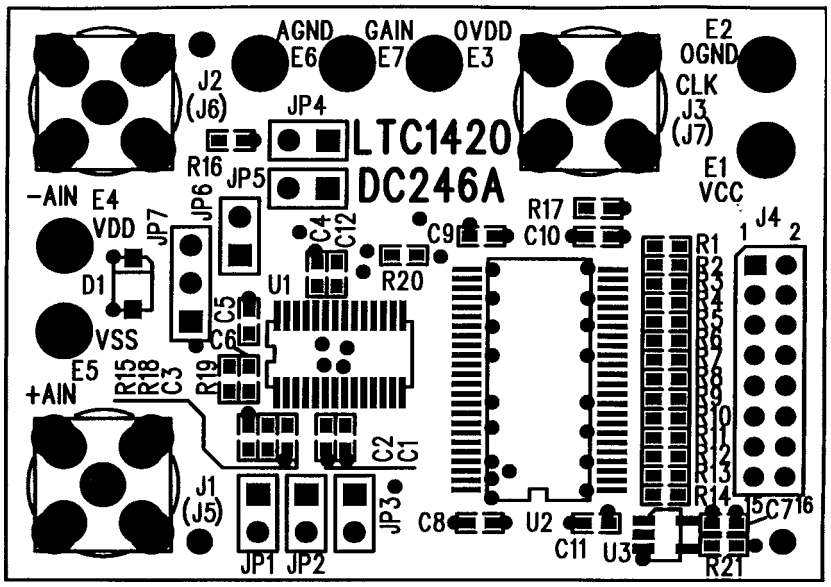


Figure 15. Top Silkscreen Layer for LTC1420 Demo Board

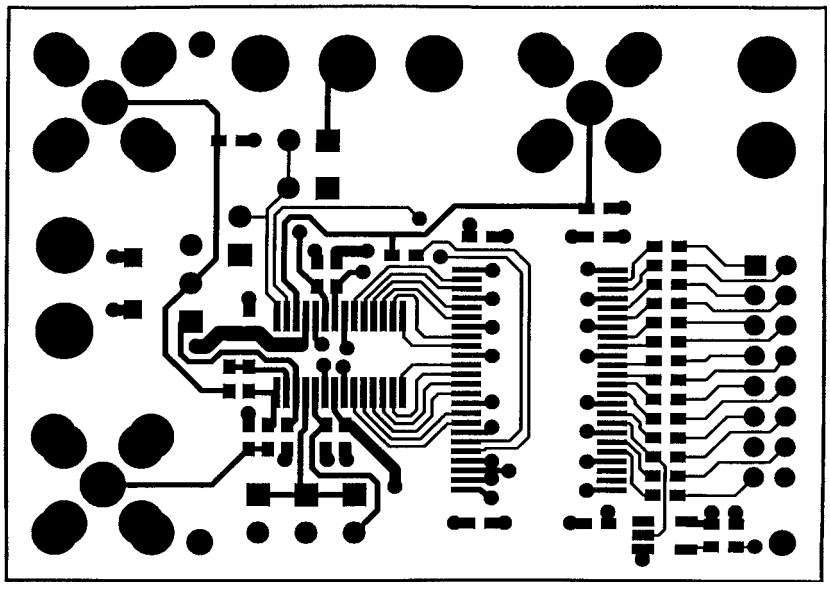


Figure 16. Top Layer for LTC1420 Demo Board

APPLICATIONS INFORMATION

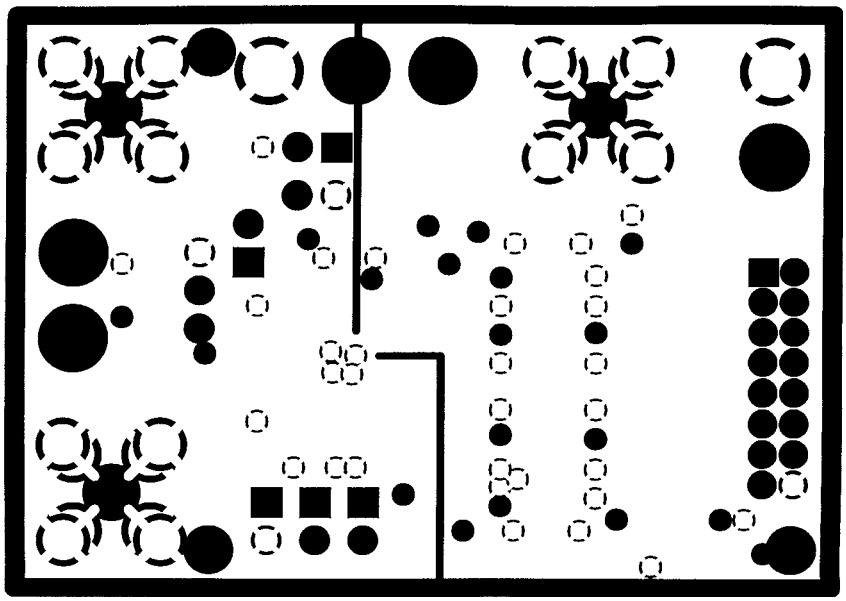


Figure 17. Ground Plane Layer for LTC1420 Demo Board

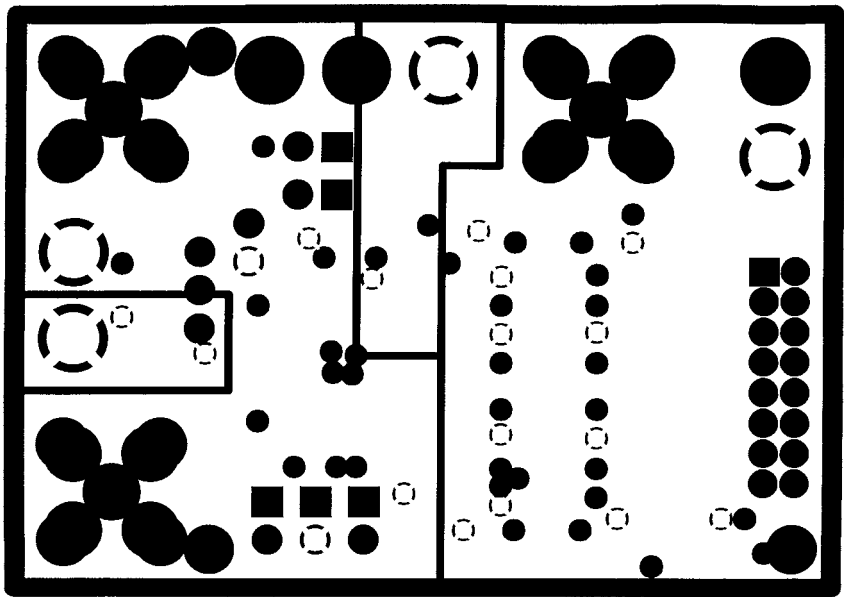


Figure 18. Power Plane Layer for LTC1420 Demo Board

APPLICATIONS INFORMATION

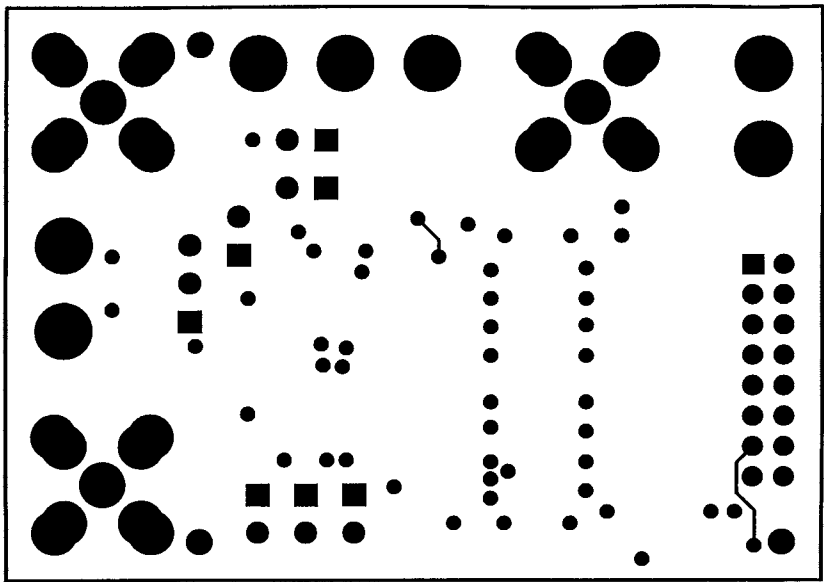
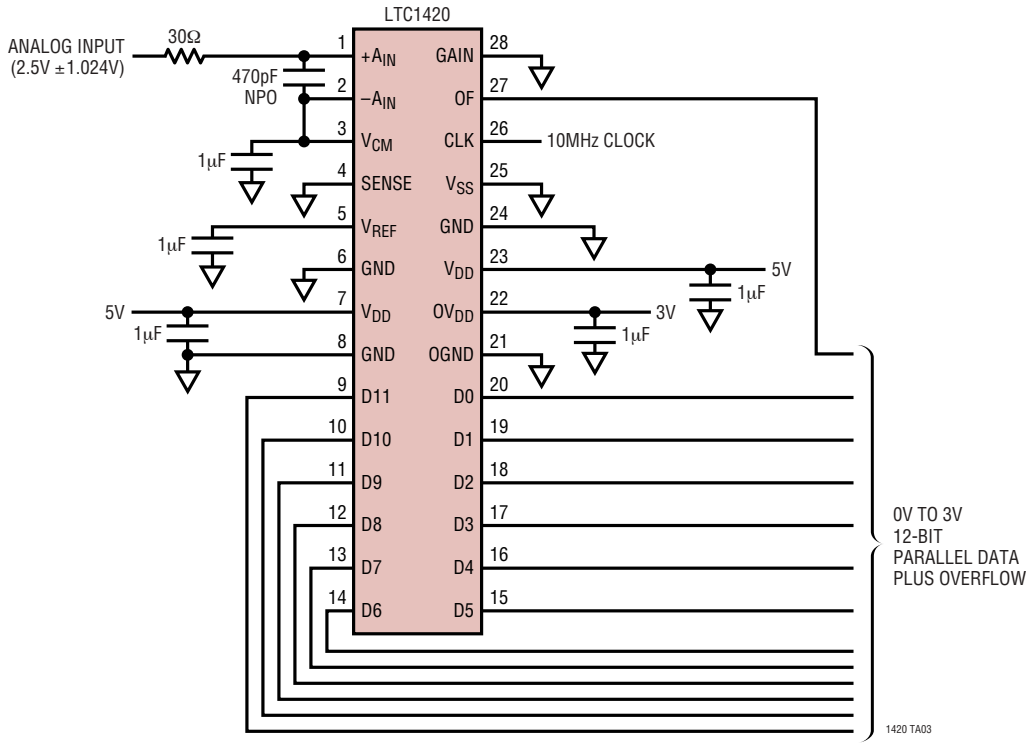


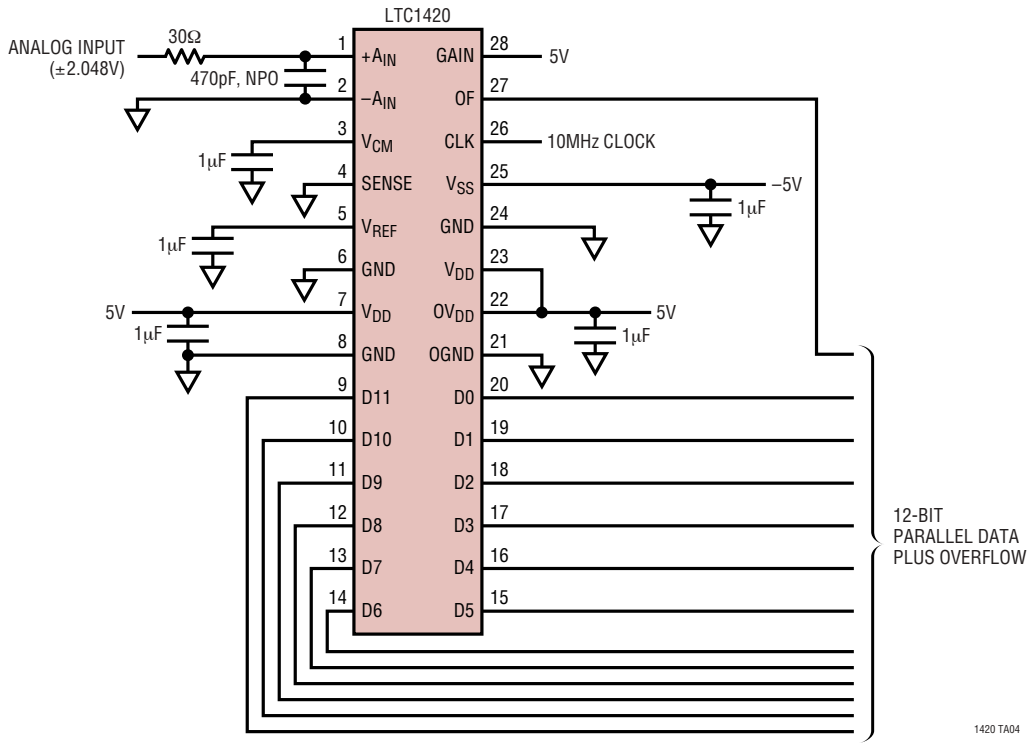
Figure 19. Bottom Layer for LTC1420 Demo Board

TYPICAL APPLICATIONS

Single Supply, 10Msps, 12-Bit ADC with 3V Logic Outputs

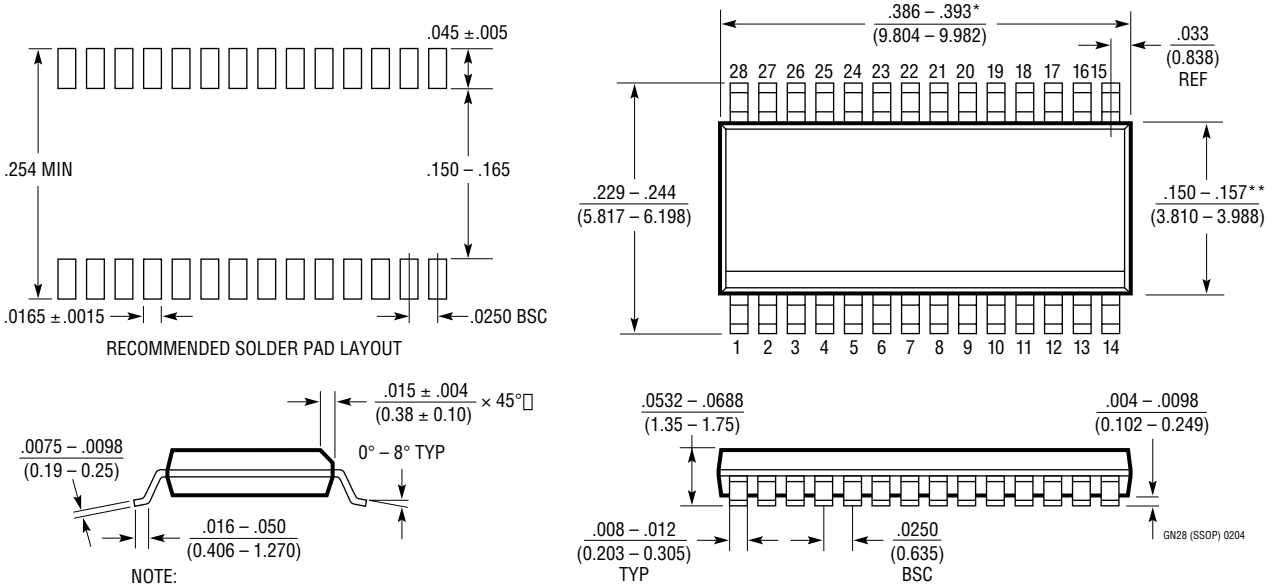


Dual Supply, 10Msps, 12-Bit ADC with 71dB SINAD



PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



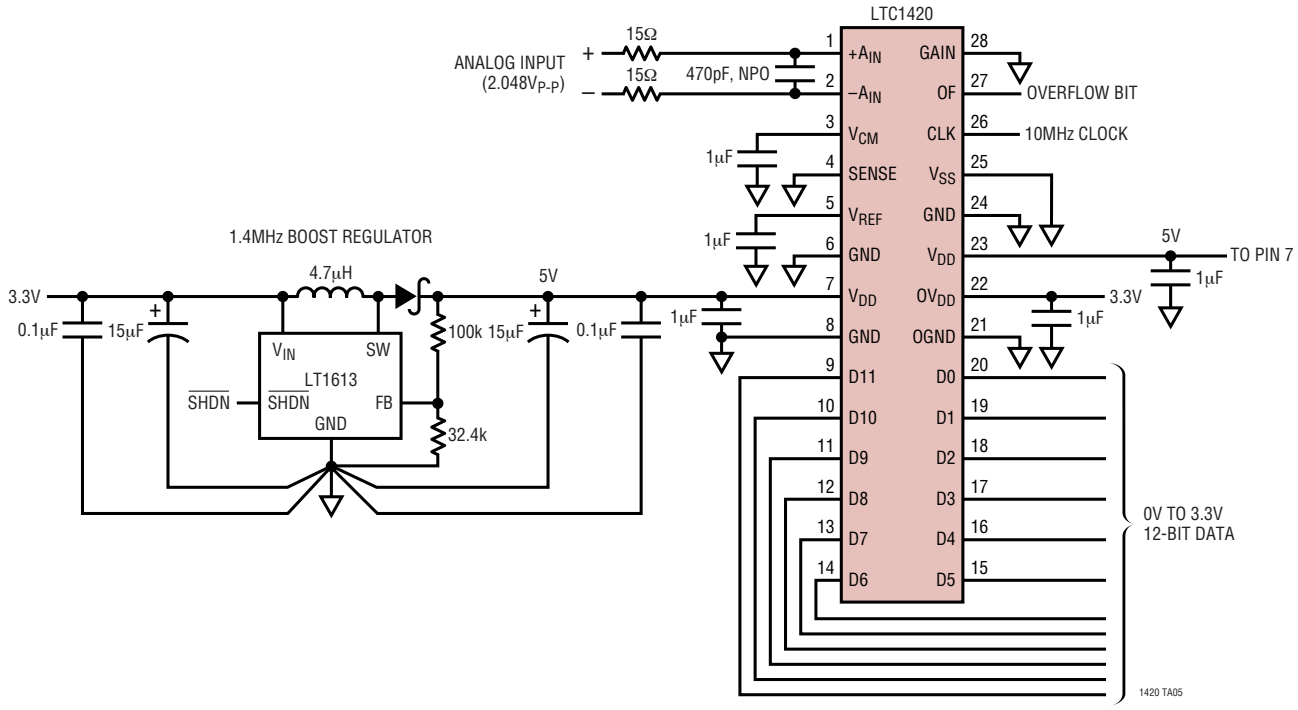
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

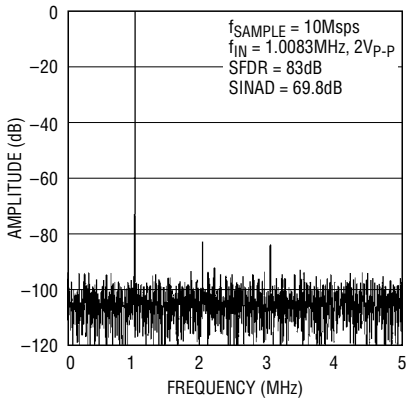
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Single 3.3V Supply, 10Msps, 12-Bit ADC



4096 Point FFT of Above Circuit with a 1MHz Input. Note That There Are No Spurs From the 1.4MHz Boost Regulator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1405	12-Bit, 5Msps, Sampling ADC with Parallel Output	Pin Compatible with the LTC1420
LTC1412	12-Bit, 3Msps, Sampling ADC with Parallel Output	Best Dynamic Performance, SINAD = 72dB at Nyquist
LTC1415	Single 5V, 12-Bit, 1.25Msps with Parallel Output	55mW Power Dissipation, 72dB SINAD
LT1019	Precision Bandgap Reference	0.05% Max Initial Accuracy, 5ppm/°C Max Drift

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
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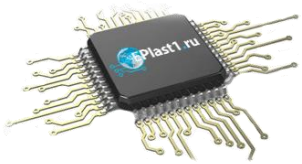
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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