

FEATURES:

- **Organized as 2M x16 or 4M x8**
- **Dual Bank Architecture for Concurrent Read/Write Operation**
 - 32 Mbit Bottom Sector Protection (in the smaller bank)
 - GLS36VF3203: 8 Mbit + 24 Mbit
 - 32 Mbit Top Sector Protection (in the smaller bank)
 - GLS36VF3204: 24 Mbit + 8 Mbit
- **Single 2.7-3.6V for Read and Write Operations**
- **Superior Reliability**
 - Endurance: 100,000 cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption:**
 - Active Current: 6 mA typical
 - Standby Current: 4 μ A typical
 - Auto Low Power Mode: 4 μ A typical
- **Hardware Sector Protection/WP# Input Pin**
 - Protects 8 KWord in the smaller bank by driving WP# low and unprotects by driving WP# high
- **Hardware Reset Pin (RST#)**
 - Resets the internal state machine to reading array data
- **Byte# Pin**
 - Selects 8-bit or 16-bit mode
- **Sector-Erase Capability**
 - Uniform 2 KWord sectors
- **Chip-Erase Capability**
- **Block-Erase Capability**
 - Uniform 32 KWord blocks
- **Erase-Suspend / Erase-Resume Capabilities**
- **Security ID Feature**
 - Greenliant: 128 bits
 - User: 256 Bytes
- **Fast Read Access Time**
 - 70 ns
- **Latched Address and Data**
- **Fast Erase and Program (typical):**
 - Sector-Erase Time: 18 ms
 - Block-Erase Time: 18 ms
 - Chip-Erase Time: 35 ms
 - Program Time: 7 μ s
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bit
 - Data# Polling
 - Ready/Busy# pin
- **CMOS I/O Compatibility**
- **Conforms to Common Flash Memory Interface (CFI)**
- **JEDEC Standards**
 - Flash EEPROM Pinouts and command sets
- **Packages Available**
 - 48-ball TFBGA (6mm x 8mm)
 - 48-lead TSOP (12mm x 20mm)

PRODUCT DESCRIPTION

The GLS36VF320x are 2M x16 or 4M x8 CMOS Concurrent Read/Write Flash Memory manufactured with high performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The devices write (Program or Erase) with a 2.7-3.6V power supply and conform to JEDEC standard pinouts for x8/x16 memories.

Featuring high performance Word-Program, these devices provide a typical Program time of 7 μ sec and use the Toggle Bit, Data# Polling, or RY/BY# to detect the completion of the Program or Erase operation. To protect against inadvertent write, the devices have on-chip hardware and Soft-

ware Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

These devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, the devices significantly improve performance and reliability, while lowering power consumption. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation

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is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high-density, surface-mount requirements, these devices are offered in 48-ball TFBGA and 48-lead TSOP packages. See Figures 2 and 3 for pin assignments.

Device Operation

Memory operation functions are initiated using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.

Auto Low Power Mode

These devices also have the **Auto Lower Power** mode which puts them in a near standby mode within 500 ns after data has been accessed with a valid Read operation. This reduces the I_{DD} active Read current to 4 µA typically. While CE# is low, the devices exit Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty.

Concurrent Read/Write Operation

The dual bank architecture of these devices allows the Concurrent Read/Write operation whereby the user can read from one bank while programming or erasing in the other bank. For example, reading system code in one bank while updating data in the other bank.

Concurrent Read/Write State

| Bank 1 | Bank 2 |
|--------------|--------------|
| Read | No Operation |
| Read | Write |
| Write | Read |
| Write | No Operation |
| No Operation | Read |
| No Operation | Write |

Note: For the purposes of this table, write means to perform Block- or Sector-Erase or Program operations as applicable to the appropriate bank.

Read Operation

The Read operation is controlled by CE# and OE#; both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in a high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 4).

Program Operation

These devices are programmed on a word-by-word or byte-by-byte basis depending on the state of the BYTE# pin. Before programming, one must ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Address and data are loaded.

During the Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first.

3. The internal Program operation is initiated after the rising edge of the fourth WE# or CE#, which-

ever occurs first. The Program operation, once initiated, will be completed typically within 7 μ s.

See Figures 5 and 6 for WE# and CE# controlled Program operation timing diagrams and Figure 20 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

Sector- (Block-) Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Sector- or Block-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 10 and 11 for timing waveforms.

Chip-Erase Operation

The devices provide a Chip-Erase operation, which allows the user to erase all sectors/blocks to the “1” state. This is useful when a device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid Read is Toggle Bit or Data# Polling. Any commands issued during the Chip-Erase operation are ignored. See Table 7 for the command sequence, Figure 9 for timing diagram, and Figure 23 for the flowchart. When WP# is low, any attempt to Chip-Erase will be ignored.

Erase-Suspend/Erase-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode no more than 10 μ s after the Erase-Suspend command had been issued. (T_{ES} maximum latency equals 10 μ s.) Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ₂ toggling and DQ₆ at “1”. While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend. The Software ID Entry command can also be executed. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the last byte sequence.

Write Operation Status Detection

These devices provide one hardware and two software means to detect the completion of a Write (Program or Erase) cycle in order to optimize the system Write cycle time. The hardware detection uses the Ready/Busy# (RY/BY#) output pin. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Ready/Busy# (RY/BY#), a Data# Polling (DQ₇), or Toggle Bit (DQ₆) Read may be simultaneous with the completion of the Write cycle. If this occurs, the system may get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both Reads are valid, then the Write cycle has completed, otherwise the rejection is valid.

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Ready/Busy# (RY/BY#)

The devices include a Ready/Busy# (RY/BY#) output signal. RY/BY# is an open drain output pin that indicates whether an Erase or Program operation is in progress. Since RY/BY# is an open drain output, it allows several devices to be tied in parallel to V_{DD} via an external pull-up resistor. After the rising edge of the final WE# pulse in the command sequence, the RY/BY# status is valid.

When RY/BY# is actively pulled low, it indicates that an Erase or Program operation is in progress. When RY/BY# is high (Ready), the devices may be read or left in standby mode.

Byte/Word (BYTE#)

The device includes a BYTE# pin to control whether the device data I/O pins operate x8 or x16. If the BYTE# pin is at logic "1" (V_{IH}) the device is in x16 data configuration: all data I/O pins DQ₀-DQ₁₅ are active and controlled by CE# and OE#.

If the BYTE# pin is at logic "0", the device is in x8 data configuration: only data I/O pins DQ₀-DQ₇ are active and controlled by CE# and OE#. The remaining data pins DQ₈-DQ₁₄ are at Hi-Z, while pin DQ₁₅ is used as the address input A₋₁ for the Least Significant Bit of the address bus.

Data# Polling (DQ₇)

When the devices are in an internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Data# Polling (DQ₇) timing diagram and Figure 21 for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or CE#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of sixth WE# (or CE#) pulse. DQ₆ will be set to "1" if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or CE#) pulse of a Write operation. See Figure 8 for Toggle Bit timing diagram and Figure 21 for a flowchart.

TABLE 1: Write Operation Status

| Status | | DQ ₇ | DQ ₆ | DQ ₂ | RY/BY# |
|--------------------|--|-------------------|-----------------|-----------------|--------|
| Normal Operation | Standard Program | DQ ₇ # | Toggle | No Toggle | 0 |
| | Standard Erase | 0 | Toggle | Toggle | 0 |
| Erase-Suspend Mode | Read From Erase Suspended Sector/Block | 1 | 1 | Toggle | 1 |
| | Read From Non-Erase Suspended Sector/Block | Data | Data | Data | 1 |
| | Program | DQ ₇ # | Toggle | N/A | 0 |

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Note: DQ₇, DQ₆, and DQ₂ require a valid address when reading status information. The address must be in the bank where the operation is in progress in order to read the operation status. If the address is pointing to a different bank (not busy), the device will output array data.

Data Protection

The devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The devices provide hardware block protection which protects the outermost 8 KWord in the smaller bank. The block is protected when WP# is held low. When WP# is held low and a Block-Erase command is issued to the protected block, the data in the outermost 8 KWord/16 KByte section will be protected. The rest of the block will be erased. See Tables 3 and 4 for Block-Protection location.

A user can disable block protection by driving WP# high. This allows data to be erased or programmed into the protected sectors. WP# must be held high prior to issuing the Write command and remain stable until after the entire Write operation has completed. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the devices to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 17) and all output pins are set to High-Z. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 16).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Software Data Protection (SDP)

These devices provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of the six-byte sequence. The devices are shipped with the Software Data Protection permanently enabled. See Table 7 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value during any SDP command sequence.

Common Flash Memory Interface (CFI)

These devices also contain the CFI information to describe the characteristics of the devices. In order to enter the CFI Query mode, the system must write the three-byte sequence, same as the Software ID Entry command with 98H (CFI Query command) to address BK_X555H in the last byte sequence. In order to enter the CFI Query mode, the system can also use the one-byte sequence with BK_X55H on Address and 98H on Data Bus. See Figure 13 for CFI Entry and Read timing diagram. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 8 through 10. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Security ID

The GLS36VF320x devices offer a 136-word Security ID space. The Secure ID space is divided into two segments—one 128-bit factory programmed segment and one 128-word (256-byte) user-programmed segment. The first segment is programmed and locked at Greenliant with a unique, 128-bit number. The user segment is left unprogrammed for the customer to program as desired. To program the user segment of the Security ID, the user must use the Security ID Program command. End-of-Write status is checked by reading the toggle bits. Data# Polling is not used for Security ID End-of-Write detection. Once programming is complete, the Sec ID should be locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Note that regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased. The Secure ID space can be queried

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by executing a three-byte command sequence with Query Sec ID command (88H) at address 555H in the last byte sequence. See Figure 15 for timing diagram. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 7 for more details.

Product Identification

The Product Identification mode identifies the devices and manufacturer. For details, see Table 2 for software operation, Figure 12 for the Software ID Entry and Read timing diagram and Figure 22 for the Software ID Entry command sequence flowchart. The addresses A_{20} and A_{18} indicate a bank address. When the addressed bank is switched to Product Identification mode, it is possible to read another address from the same bank without issuing a new Software ID Entry command. The Software ID Entry command may be written to an address within a bank that is in Read Mode or in Erase-Suspend mode. The Software ID Entry command may not be written while the device is programming or erasing in the other bank.

TABLE 2: Product Identification

| | Address | Data |
|-------------------|-----------------------|-------|
| Manufacturer's ID | BK _X 0000H | 00BFH |
| Device ID | | |
| GLS36VF3203 | BK _X 0001H | 7354H |
| GLS36VF3204 | BK _X 0001H | 7353H |

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Note: BK_X = Bank Address (A_{20} - A_{18})

Product Identification Mode Exit/CFI Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 7 for the software command code, Figure 14 for timing waveform and Figure 22 for a flowchart.

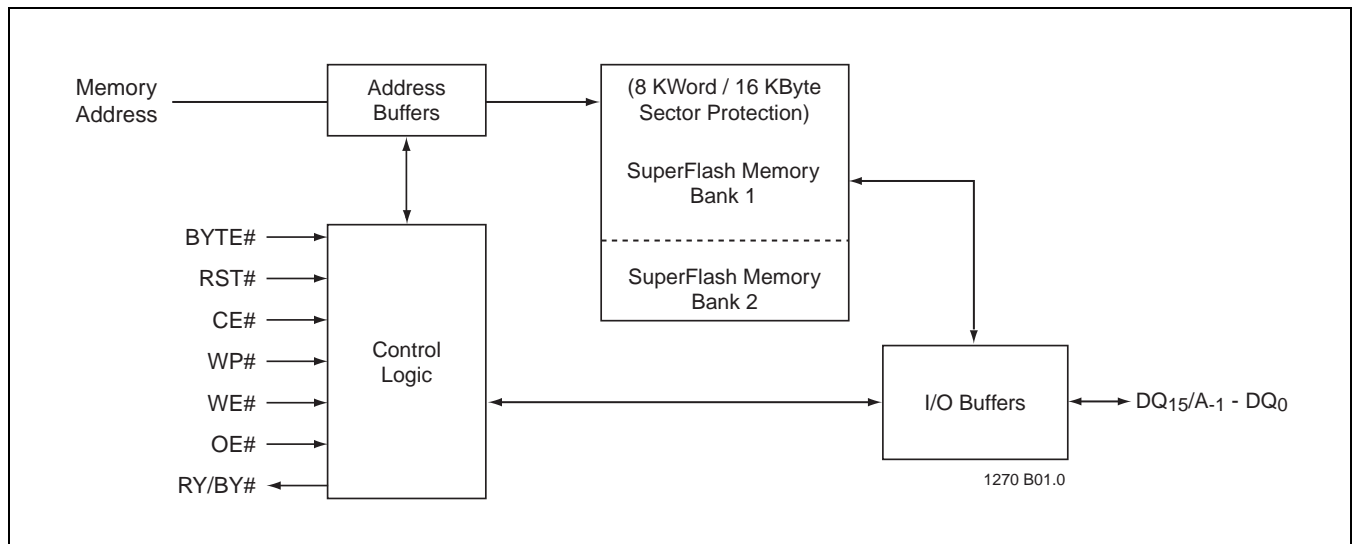


FIGURE 1: Functional Block Diagram

TABLE 3: GLS36VF3203, 2M x16 CSF Bottom Dual-Bank Memory Organization (1 of 3)

| GLS36VF3203 | Block | Block Size | Address Range x8 | Address Range x16 |
|-------------|-------|---------------|------------------|-------------------|
| Bank 1 | BA0 | 8 KW / 16 KB | 000000H–003FFFFH | 000000H–001FFFFH |
| | | 24 KW / 48 KB | 004000H–00FFFFH | 002000H–007FFFFH |
| | BA1 | 32 KW / 64 KB | 010000H–01FFFFH | 008000H–00FFFFH |
| | BA2 | 32 KW / 64 KB | 020000H–02FFFFH | 010000H–017FFFFH |
| | BA3 | 32 KW / 64 KB | 030000H–03FFFFH | 018000H–01FFFFH |
| | BA4 | 32 KW / 64 KB | 040000H–04FFFFH | 020000H–027FFFFH |
| | BA5 | 32 KW / 64 KB | 050000H–05FFFFH | 028000H–02FFFFH |
| | BA6 | 32 KW / 64 KB | 060000H–06FFFFH | 030000H–037FFFFH |
| | BA7 | 32 KW / 64 KB | 070000H–07FFFFH | 038000H–03FFFFH |
| | BA8 | 32 KW / 64 KB | 080000H–08FFFFH | 040000H–047FFFFH |
| | BA9 | 32 KW / 64 KB | 090000H–09FFFFH | 048000H–04FFFFH |
| | BA10 | 32 KW / 64 KB | 0A0000H–0AFFFFH | 050000H–057FFFFH |
| | BA11 | 32 KW / 64 KB | 0B0000H–0BFFFFH | 058000H–05FFFFH |
| | BA12 | 32 KW / 64 KB | 0C0000H–0CFFFFH | 060000H–067FFFFH |
| | BA13 | 32 KW / 64 KB | 0D0000H–0DFFFFH | 068000H–06FFFFH |
| | BA14 | 32 KW / 64 KB | 0E0000H–0EFFFFH | 070000H–077FFFFH |
| | BA15 | 32 KW / 64 KB | 0F0000H–0FFFFFH | 078000H–07FFFFH |

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TABLE 3: GLS36VF3203, 2M x16 CSF Bottom Dual-Bank Memory Organization (Continued) (2 of 3)

| GLS36VF3203 | Block | Block Size | Address Range x8 | Address Range x16 |
|--------------------|--------------|-------------------|-------------------------|--------------------------|
| Bank 2 | BA16 | 32 KW / 64 KB | 100000H—10FFFFH | 080000H—087FFFH |
| | BA17 | 32 KW / 64 KB | 110000H—11FFFFH | 088000H—08FFFFH |
| | BA18 | 32 KW / 64 KB | 120000H—12FFFFH | 090000H—097FFFH |
| | BA19 | 32 KW / 64 KB | 130000H—13FFFFH | 098000H—09FFFFH |
| | BA20 | 32 KW / 64 KB | 140000H—14FFFFH | 0A0000H—0A7FFFH |
| | BA21 | 32 KW / 64 KB | 150000H—15FFFFH | 0A8000H—0AFFFFH |
| | BA22 | 32 KW / 64 KB | 160000H—16FFFFH | 0B0000H—0B7FFFH |
| | BA23 | 32 KW / 64 KB | 170000H—17FFFFH | 0B8000H—0BFFFFH |
| | BA24 | 32 KW / 64 KB | 180000H—18FFFFH | 0C0000H—0C7FFFH |
| | BA25 | 32 KW / 64 KB | 190000H—19FFFFH | 0C8000H—0CFFFFH |
| | BA26 | 32 KW / 64 KB | 1A0000H—1AFFFFH | 0D0000H—0D7FFFH |
| | BA27 | 32 KW / 64 KB | 1B0000H—1BFFFFH | 0D8000H—0DFFFFH |
| | BA28 | 32 KW / 64 KB | 1C0000H—1CFFFFH | 0E0000H—0E7FFFH |
| | BA29 | 32 KW / 64 KB | 1D0000H—1DFFFFH | 0E8000H—0EFFFFH |
| | BA30 | 32 KW / 64 KB | 1E0000H—1EFFFFH | 0F0000H—0F7FFFH |
| | BA31 | 32 KW / 64 KB | 1F0000H—1FFFFFH | 0F8000H—0FFFFFH |
| | BA32 | 32 KW / 64 KB | 200000H—20FFFFH | 100000H—107FFFH |
| | BA33 | 32 KW / 64 KB | 210000H—21FFFFH | 108000H—10FFFFH |
| | BA34 | 32 KW / 64 KB | 220000H—22FFFFH | 110000H—117FFFH |
| | BA35 | 32 KW / 64 KB | 230000H—23FFFFH | 118000H—11FFFFH |
| | BA36 | 32 KW / 64 KB | 240000H—24FFFFH | 120000H—127FFFH |
| | BA37 | 32 KW / 64 KB | 250000H—25FFFFH | 128000H—12FFFFH |
| | BA38 | 32 KW / 64 KB | 260000H—26FFFFH | 130000H—137FFFH |
| | BA39 | 32 KW / 64 KB | 270000H—27FFFFH | 138000H—13FFFFH |
| | BA40 | 32 KW / 64 KB | 280000H—28FFFFH | 140000H—147FFFH |
| | BA41 | 32 KW / 64 KB | 290000H—29FFFFH | 148000H—14FFFFH |

TABLE 3: GLS36VF3203, 2M x16 CSF Bottom Dual-Bank Memory Organization (Continued) (3 of 3)

| GLS36VF3203 | Block | Block Size | Address Range x8 | Address Range x16 |
|---------------|-------|---------------|------------------|-------------------|
| Bank 2 | BA42 | 32 KW / 64 KB | 2A0000H—2AFFFFH | 150000H—157FFFH |
| | BA43 | 32 KW / 64 KB | 2B0000H—2BFFFFH | 158000H—15FFFFH |
| | BA44 | 32 KW / 64 KB | 2C0000H—2CFFFFH | 160000H—167FFFH |
| | BA45 | 32 KW / 64 KB | 2D0000H—2DFFFFH | 168000H—16FFFFH |
| | BA46 | 32 KW / 64 KB | 2E0000H—2EFFFFH | 170000H—177FFFH |
| | BA47 | 32 KW / 64 KB | 2F0000H—2FFFFFH | 178000H—17FFFFH |
| | BA48 | 32 KW / 64 KB | 300000H—30FFFFH | 180000H—187FFFH |
| | BA49 | 32 KW / 64 KB | 310000H—31FFFFH | 188000H—18FFFFH |
| | BA50 | 32 KW / 64 KB | 320000H—32FFFFH | 190000H—197FFFH |
| | BA51 | 32 KW / 64 KB | 330000H—33FFFFH | 198000H—19FFFFH |
| | BA52 | 32 KW / 64 KB | 340000H—34FFFFH | 1A0000H—1A7FFFH |
| | BA53 | 32 KW / 64 KB | 350000H—35FFFFH | 1A8000H—1AFFFFH |
| | BA54 | 32 KW / 64 KB | 360000H—36FFFFH | 1B0000H—1B7FFFH |
| | BA55 | 32 KW / 64 KB | 370000H—37FFFFH | 1B8000H—1BFFFFH |
| | BA56 | 32 KW / 64 KB | 380000H—38FFFFH | 1C0000H—1C7FFFH |
| | BA57 | 32 KW / 64 KB | 390000H—39FFFFH | 1C8000H—1CFFFFH |
| | BA58 | 32 KW / 64 KB | 3A0000H—3AFFFFH | 1D0000H—1D7FFFH |
| | BA59 | 32 KW / 64 KB | 3B0000H—3BFFFFH | 1D8000H—1DFFFFH |
| | BA60 | 32 KW / 64 KB | 3C0000H—3CFFFFH | 1E0000H—1E7FFFH |
| | BA61 | 32 KW / 64 KB | 3D0000H—3DFFFFH | 1E8000H—1EFFFFH |
| | BA62 | 32 KW / 64 KB | 3E0000H—3EFFFFH | 1F0000H—1F7FFFH |
| | BA63 | 32 KW / 64 KB | 3F0000H—3FFFFFH | 1F8000H—1FFFFFH |

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TABLE 4: GLS36VF3204, 2M x16 CSF Top Dual-Bank Memory Organization (1 of 2)

| GLS36VF3204 | Block | Block Size | Address Range x8 | Address Range x16 |
|--------------------|--------------|-------------------|-------------------------|--------------------------|
| Bank 2 | BA0 | 32 KW / 64 KB | 000000H—00FFFFH | 000000H—007FFFH |
| | BA1 | 32 KW / 64 KB | 010000H—01FFFFH | 008000H—00FFFFH |
| | BA2 | 32 KW / 64 KB | 020000H—02FFFFH | 010000H—017FFFH |
| | BA3 | 32 KW / 64 KB | 030000H—03FFFFH | 018000H—01FFFFH |
| | BA4 | 32 KW / 64 KB | 040000H—04FFFFH | 020000H—027FFFH |
| | BA5 | 32 KW / 64 KB | 050000H—05FFFFH | 028000H—02FFFFH |
| | BA6 | 32 KW / 64 KB | 060000H—06FFFFH | 030000H—037FFFH |
| | BA7 | 32 KW / 64 KB | 070000H—07FFFFH | 038000H—03FFFFH |
| | BA8 | 32 KW / 64 KB | 080000H—08FFFFH | 040000H—047FFFH |
| | BA9 | 32 KW / 64 KB | 090000H—09FFFFH | 048000H—04FFFFH |
| | BA10 | 32 KW / 64 KB | 0A0000H—0AFFFFH | 050000H—057FFFH |
| | BA11 | 32 KW / 64 KB | 0B0000H—0BFFFFH | 058000H—05FFFFH |
| | BA12 | 32 KW / 64 KB | 0C0000H—0CFFFFH | 060000H—067FFFH |
| | BA13 | 32 KW / 64 KB | 0D0000H—0DFFFFH | 068000H—06FFFFH |
| | BA14 | 32 KW / 64 KB | 0E0000H—0EFFFFH | 070000H—077FFFH |
| | BA15 | 32 KW / 64 KB | 0F0000H—0FFFFFH | 078000H—07FFFFH |
| | BA16 | 32 KW / 64 KB | 100000H—10FFFFH | 080000H—087FFFH |
| | BA17 | 32 KW / 64 KB | 110000H—11FFFFH | 088000H—08FFFFH |
| | BA18 | 32 KW / 64 KB | 120000H—12FFFFH | 090000H—097FFFH |
| | BA19 | 32 KW / 64 KB | 130000H—13FFFFH | 098000H—09FFFFH |
| | BA20 | 32 KW / 64 KB | 140000H—14FFFFH | 0A0000H—0A7FFFH |
| | BA21 | 32 KW / 64 KB | 150000H—15FFFFH | 0A8000H—0AFFFFH |
| | BA22 | 32 KW / 64 KB | 160000H—16FFFFH | 0B0000H—0B7FFFH |
| | BA23 | 32 KW / 64 KB | 170000H—17FFFFH | 0B8000H—0BFFFFH |
| | BA24 | 32 KW / 64 KB | 180000H—18FFFFH | 0C0000H—0C7FFFH |
| | BA25 | 32 KW / 64 KB | 190000H—19FFFFH | 0C8000H—0CFFFFH |
| | BA26 | 32 KW / 64 KB | 1A0000H—1AFFFFH | 0D0000H—0D7FFFH |
| | BA27 | 32 KW / 64 KB | 1B0000H—1BFFFFH | 0D8000H—0DFFFFH |
| | BA28 | 32 KW / 64 KB | 1C0000H—1CFFFFH | 0E0000H—0E7FFFH |
| | BA29 | 32 KW / 64 KB | 1D0000H—1DFFFFH | 0E8000H—0EFFFFH |
| | BA30 | 32 KW / 64 KB | 1E0000H—1EFFFFH | 0F0000H—0F7FFFH |
| | BA31 | 32 KW / 64 KB | 1F0000H—1FFFFFH | 0F8000H—0FFFFFH |
| | BA32 | 32 KW / 64 KB | 200000H—20FFFFH | 100000H—107FFFH |
| | BA33 | 32 KW / 64 KB | 210000H—21FFFFH | 108000H—10FFFFH |
| | BA34 | 32 KW / 64 KB | 220000H—22FFFFH | 110000H—117FFFH |
| | BA35 | 32 KW / 64 KB | 230000H—23FFFFH | 118000H—11FFFFH |
| | BA36 | 32 KW / 64 KB | 240000H—24FFFFH | 120000H—127FFFH |
| | BA37 | 32 KW / 64 KB | 250000H—25FFFFH | 128000H—12FFFFH |
| | BA38 | 32 KW / 64 KB | 260000H—26FFFFH | 130000H—137FFFH |
| | BA39 | 32 KW / 64 KB | 270000H—27FFFFH | 138000H—13FFFFH |
| | BA40 | 32 KW / 64 KB | 280000H—28FFFFH | 140000H—147FFFH |
| | BA41 | 32 KW / 64 KB | 290000H—29FFFFH | 148000H—14FFFFH |
| | BA42 | 32 KW / 64 KB | 2A0000H—2AFFFFH | 150000H—157FFFH |

TABLE 4: GLS36VF3204, 2M x16 CSF Top Dual-Bank Memory Organization (Continued) (2 of 2)

| GLS36VF3204 | Block | Block Size | Address Range x8 | Address Range x16 |
|---------------|-------|---------------|------------------|-------------------|
| Bank 2 | BA43 | 32 KW / 64 KB | 2B0000H–2BFFFFH | 158000H–15FFFFH |
| | BA44 | 32 KW / 64 KB | 2C0000H–2CFFFFH | 160000H–167FFFFH |
| | BA45 | 32 KW / 64 KB | 2D0000H–2DFFFFH | 168000H–16FFFFH |
| | BA46 | 32 KW / 64 KB | 2E0000H–2EFFFFH | 170000H–177FFFFH |
| | BA47 | 32 KW / 64 KB | 2F0000H–2FFFFFH | 178000H–17FFFFH |
| Bank 1 | BA48 | 32 KW / 64 KB | 300000H–30FFFFH | 180000H–187FFFFH |
| | BA49 | 32 KW / 64 KB | 310000H–31FFFFH | 188000H–18FFFFH |
| | BA50 | 32 KW / 64 KB | 320000H–32FFFFH | 190000H–197FFFFH |
| | BA51 | 32 KW / 64 KB | 330000H–33FFFFH | 198000H–19FFFFH |
| | BA52 | 32 KW / 64 KB | 340000H–34FFFFH | 1A0000H–1A7FFFFH |
| | BA53 | 32 KW / 64 KB | 350000H–35FFFFH | 1A8000H–1AFFFFH |
| | BA54 | 32 KW / 64 KB | 360000H–36FFFFH | 1B0000H–1B7FFFFH |
| | BA55 | 32 KW / 64 KB | 370000H–37FFFFH | 1B8000H–1BFFFFH |
| | BA56 | 32 KW / 64 KB | 380000H–38FFFFH | 1C0000H–1C7FFFFH |
| | BA57 | 32 KW / 64 KB | 390000H–39FFFFH | 1C8000H–1CFFFFH |
| | BA58 | 32 KW / 64 KB | 3A0000H–3AFFFFH | 1D0000H–1D7FFFFH |
| | BA59 | 32 KW / 64 KB | 3B0000H–3BFFFFH | 1D8000H–1DFFFFH |
| | BA60 | 32 KW / 64 KB | 3C0000H–3CFFFFH | 1E0000H–1E7FFFFH |
| | BA61 | 32 KW / 64 KB | 3D0000H–3DFFFFH | 1E8000H–1EFFFFH |
| | BA62 | 32 KW / 64 KB | 3E0000H–3EFFFFH | 1F0000H–1F7FFFFH |
| | BA63 | 24 KW / 48 KB | 3F0000H–3FBFFFFH | 1F8000H–1FDFFFFH |
| | | 8 KW / 16 KB | 3FC000H–3FFFFFFH | 1FE000H–1FFFFFFH |

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Data Sheet

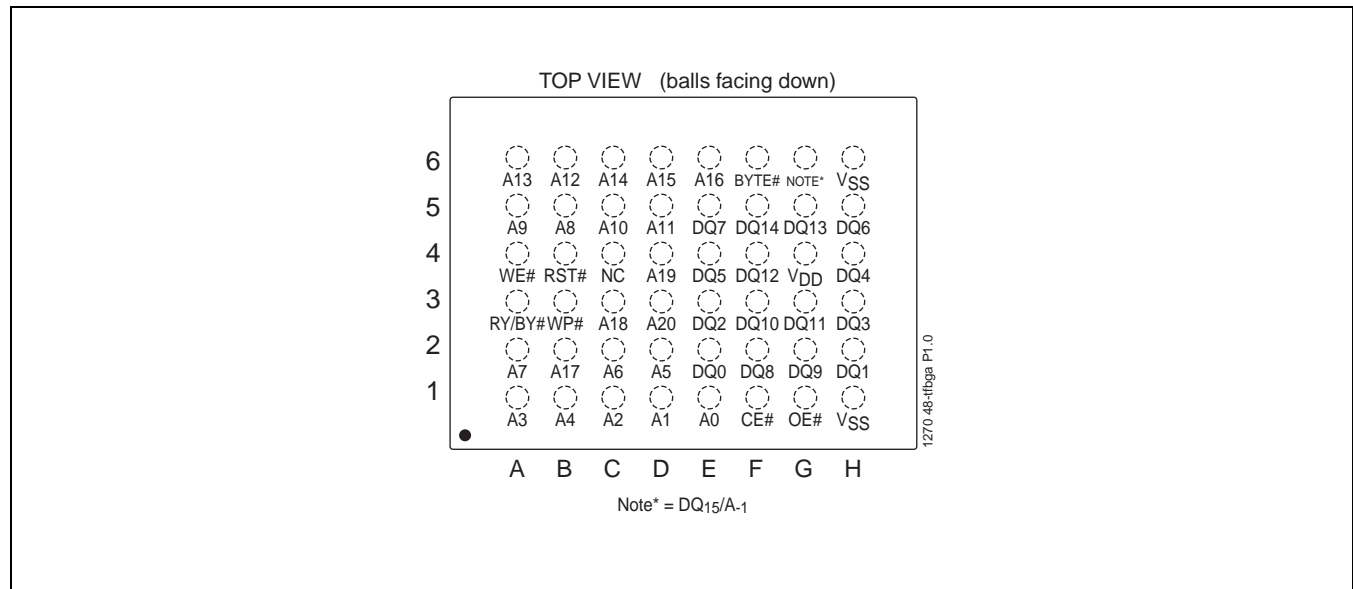


FIGURE 2: Pin Assignments for 48-ball TFBGA (6mm x 8mm)

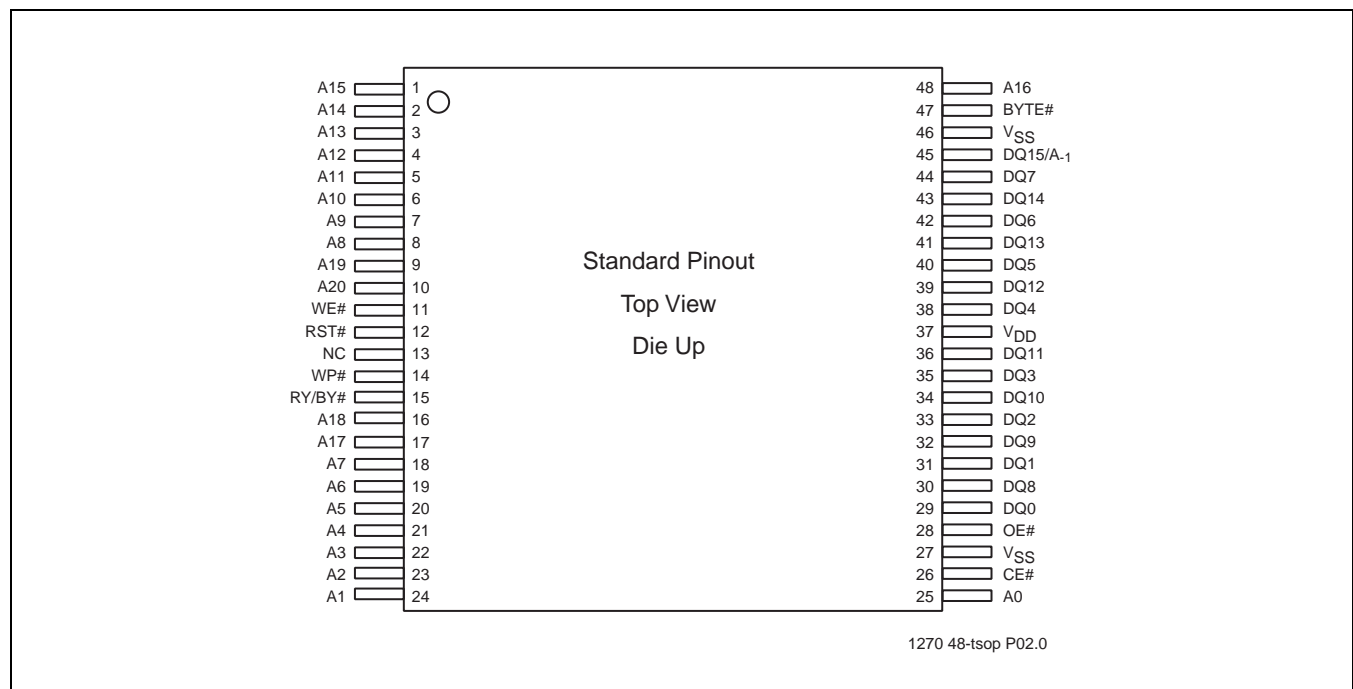


FIGURE 3: Pin Assignments for 48-lead TSOP (12mm x 20mm)

TABLE 5: Pin Description

| Symbol | Name | Functions |
|-----------------------------------|-----------------------------------|--|
| A ₂₀ -A ₀ | Address Inputs | To provide memory addresses. During Sector-Erase and Hardware Sector Protection, A ₂₀ -A ₁₁ address lines will select the sector. During Block-Erase A ₂₀ -A ₁₅ address lines will select the block. |
| DQ ₁₄ -DQ ₀ | Data Input/Output | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# or CE# is high. |
| DQ ₁₅ /A ₋₁ | Data Input/Output and LBS Address | DQ ₁₅ is used as data I/O pin when in x16 mode (BYTE# = "1") A ₋₁ is used as the LSB address pin when in x8 mode (BYTE# = "0") |
| CE# | Chip Enable | To activate the device when CE# is low. |
| OE# | Output Enable | To gate the data output buffers |
| WE# | Write Enable | To control the Write operations |
| RST# | Hardware Reset | To reset and return the device to Read mode |
| RY/BY# | Ready/Busy# | To output the status of a Program or Erase operation RY/BY# is a open drain output, so a 10K Ω - 100K Ω pull-up resistor is required to allow RY/BY# to transition high indicating the device is ready to read. |
| WP# | Write Protect | To protect and unprotect top or bottom 8 KWord (4 outermost sectors) from Erase or Program operation. |
| BYTE# | Word/Byte Configuration | To select 8-bit or 16-bit mode. |
| V _{DD} | Power Supply | To provide 2.7-3.6V power supply voltage |
| V _{SS} | Ground | |
| NC | No Connection | Unconnected pins |

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TABLE 6: Operation Modes Selection

| Mode | CE# | OE# | WE# | RST# | DQ ₇ -DQ ₀ | DQ ₁₅ -DQ ₈ | | Address |
|------------------------|------------------|-----------------|-----------------|------------------|---|---|--|--|
| | | | | | | BYTE# = V _{IH} | BYTE# = V _{IL} | |
| Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | D _{OUT} | D _{OUT} | DQ ₁₄ -DQ ₈ = High Z | A _{IN} |
| Program | V _{IL} | V _{IH} | V _{IL} | V _{IH} | D _{IN} | D _{IN} | DQ ₁₅ = A ₋₁ | A _{IN} |
| Erase | V _{IL} | V _{IH} | V _{IL} | V _{IH} | X ¹ | X | High Z | Sector or Block address, 555H for Chip-Erase |
| Standby | V _{IHC} | X | X | V _{IHC} | High Z | High Z | High Z | X |
| Write Inhibit | X | V _{IL} | X | V _{IH} | High Z / D _{OUT} | High Z / D _{OUT} | High Z | X |
| | X | X | V _{IH} | V _{IH} | High Z / D _{OUT} | High Z / D _{OUT} | High Z | X |
| Product Identification | | | | | | | | |
| Software Mode | V _{IL} | V _{IL} | V _{IH} | V _{IH} | Manufacturer's ID (BFH) Device ID ² | Manufacturer's ID (00H) Device ID ² | High Z High Z | See Table 7 |
| Reset | X | X | X | V _{IL} | High Z | High Z | High Z | X |

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1. X can be V_{IL} or V_{IH}, but no other value.

2. Device ID = GLS36VF3203 = 7354H, GLS36VF3204 = 7353H

Data Sheet

TABLE 7: Software Command Sequence

| Command Sequence | 1st Bus Write Cycle | | 2nd Bus Write Cycle | | 3rd Bus Write Cycle | | 4th Bus Write Cycle | | 5th Bus Write Cycle | | 6th Bus Write Cycle | |
|--|-------------------------------------|-------------------|---------------------|-------------------|--------------------------------------|-------------------|---------------------|-------------------|---------------------|-------------------|------------------------------|-------------------|
| | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² | Addr ¹ | Data ² |
| Word-Program | 555H | AAH | 2AAH | 55H | 555H | A0H | WA ³ | Data | | | | |
| Sector-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA _X ⁴ | 50H |
| Block-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | BA _X ⁴ | 30H |
| Chip-Erase | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| Erase-Suspend | XXXH | B0H | | | | | | | | | | |
| Erase-Resume | XXXH | 30H | | | | | | | | | | |
| Query Sec ID ⁵ | 555H | AAH | 2AAH | 55H | 555H | 88H | | | | | | |
| User Security ID Word-Program | 555H | AAH | 2AAH | 55H | 555H | A5H | SIWA ⁶ | Data | | | | |
| User Security ID Program Lock-out ⁷ | 555H | AAH | 2AAH | 55H | 555H | 85H | XXXH | 0000H | | | | |
| Software ID Entry ^{8,9} | 555H | AAH | 2AAH | 55H | BK _X ⁴ 555H | 90H | | | | | | |
| CFI Query Entry ⁹ | 555H | AAH | 2AAH | 55H | BK _X ⁴ 555H | 98H | | | | | | |
| CFI Query Entry ⁹ | BK _X ⁴ 55H | 98H | | | | | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit ^{10,11} | 555H | AAH | 2AAH | 55H | 555H | F0H | | | | | | |
| Software ID Exit/ CFI Exit/ Sec ID Exit ^{10,11} | XXH | F0H | | | | | | | | | | |

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- Address format A₁₀-A₀ (Hex), Addresses A₂₀-A₁₁ can be V_{IL} or V_{IH}, but no other value (unless otherwise stated), for the command sequence when in x16 mode.
When in x8 mode, Addresses A₂₀-A₁₂, Address A₁, and DQ₁₄-DQ₈ can be V_{IL} or V_{IH}, but no other value (unless otherwise stated), for the command sequence.
- DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence
- WA = Program word address
- SA_X for Sector-Erase; uses A₂₀-A₁₁ address lines
BA_X for Block-Erase; uses A₂₀-A₁₅ address lines
BK_X for Bank Address; uses A₂₀-A₁₈ address lines
- For GLS36VF3203 the Security ID Address Range is: (x16 mode) = 100000H to 100087H, (x8 mode) = 100000H to 10010FH
Greenliant ID is read at Address Range (x16 mode) = 100000H to 100007H (x8 mode) = 100000H to 10000FH
User ID is read at Address Range (x16 mode) = 100008H to 100087H (x8 mode) = 100010H to 10010FH
Lock status is read at Address 1000FFH (x16) or 1001FFH (x8). Unlocked: DQ3 = 1 / Locked: DQ3 = 0.
For GLS36VF3204 the Security ID Address Range is: (x16 mode) = 000000H to 000087H, (x8 mode) = 000000H to 00010FH
Greenliant ID is read at Address Range (x16 mode) = 000000H to 000007H (x8 mode) = 000000H to 00000FH
User ID is read at Address Range (x16 mode) = 000008H to 000087H (x8 mode) = 000010H to 00010FH
Lock Status is read at Address 0000FFH (x16) or 0001FFH (x8). Unlocked: DQ3 = 1 / Locked: DQ3 = 0
- SIWA = Valid Word addresses for user Sec ID
For GLS36VF3203 User ID valid Address Range is (x16 mode) = 100008H-100087H (x8 mode) = 100010H-10010FH.
For GLS36VF3204 User ID valid Address Range is (x16 mode) = 000008H-000087H (x8 mode) = 000010H-00010FH.
All 4 cycles of User Security ID Program and Program Lock-out must be completed before going back to Read-Array mode.
- The User Security ID Program Lock-out command must be executed in x16 mode (BYTE# = V_{IH}).
- The device does not remain in Software Product Identification mode if powered down.
- A₂₀, A₁₉, and A₁₈ = BK_X (Bank Address): address of the bank that is switched to Software ID/CFI Mode
With A₁₇-A₁ = 0; Greenliant Manufacturer's ID = 00BFH, is read with A₀ = 0
GLS36VF3203 Device ID = 7354H, is read with A₀ = 1
GLS36VF3204 Device ID = 7353H, is read with A₀ = 1
- Both Software ID Exit operations are equivalent
- If users never lock after programming, User Sec ID can be programmed over the previously unprogrammed bits (data=1) using the User Sec ID mode again (the programmed "0" bits cannot be reversed to "1").

TABLE 8: CFI Query Identification String¹

| Address x16 Mode | Address x8 Mode | Data ² | Description |
|---------------------|--------------------|-------------------------|--|
| 10H 11H 12H | 20H 22H 24H | 0051H 0052H 0059H | Query Unique ASCII string "QRY" |
| 13H 14H | 26H 28H | 0002H 0000H | Primary OEM command set |
| 15H 16H | 2AH 2CH | 0000H 0000H | Address for Primary Extended Table |
| 17H 18H | 2EH 30H | 0000H 0000H | Alternate OEM command set (00H = none exists) |
| 19H 1AH | 32H 34H | 0000H 0000H | Address for Alternate OEM extended Table (00H = none exists) |

T8.1 1270

1. Refer to CFI publication 100 for more details.
2. In x8 mode, only the lower byte of data is output.

TABLE 9: System Interface Information

| Address x16 Mode | Address x8 Mode | Data ¹ | Description |
|---------------------|--------------------|-------------------|--|
| 1BH | 36H | 0027H | V _{DD} Min (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1CH | 38H | 0036H | V _{DD} Max (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts |
| 1DH | 3AH | 0000H | V _{PP} min (00H = no V _{PP} pin) |
| 1EH | 3CH | 0000H | V _{PP} max (00H = no V _{PP} pin) |
| 1FH | 3EH | 0004H | Typical time out for Program 2 ^N μ s (2 ⁴ = 16 μ s) |
| 20H | 40H | 0000H | Typical time out for min size buffer program 2 ^N μ s (00H = not supported) |
| 21H | 42H | 0004H | Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ = 16 ms) |
| 22H | 44H | 0006H | Typical time out for Chip-Erase 2 ^N ms (2 ⁶ = 64 ms) |
| 23H | 46H | 0001H | Maximum time out for Program 2 ^N times typical (2 ¹ x 2 ⁴ = 32 μ s) |
| 24H | 48H | 0000H | Maximum time out for buffer program 2 ^N times typical |
| 25H | 4AH | 0001H | Maximum time out for individual Sector-/Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms) |
| 26H | 4CH | 0001H | Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁶ = 128 ms) |

T9.0 1270

1. In x8 mode, only the lower byte of data is output.

Data Sheet

TABLE 10: Device Geometry Information

| Address x16 Mode | Address x8 Mode | Data ¹ | Description |
|--------------------------|--------------------------|----------------------------------|--|
| 27H | 4EH | 0016H | Device size = 2 ^N Bytes (16H = 22; 2 ²² = 4 MByte) |
| 28H 29H | 50H 52H | 0002H 0000H | Flash Device Interface description; 0002H = x8/x16 asynchronous interface |
| 2AH 2BH | 54H 56H | 0000H 0000H | Maximum number of bytes in multi-byte write = 2 ^N (00H = not supported) |
| 2CH | 58H | 0002H | Number of Erase Sector/Block sizes supported by device |
| 2DH 2EH 2FH 30H | 5AH 5CH 5EH 60H | 003FH 0000H 0000H 0001H | Block Information (y + 1 = Number of blocks; z x 256B = block size) y = 63 + 1 = 64 blocks (003FH = 63) z = 256 x 256 Bytes = 64 KByte/block (0100H = 256) |
| 31H 32H 33H 34H | 62H 64H 66H 68H | 00FFH 0003H 0010H 0000H | Sector Information (y + 1 = Number of sectors; z x 256B = sector size) y = 1023 + 1 = 1024 sectors (03FFH = 1023) z = 16 x 256 Bytes = 4 KByte/sector (0010H = 16) |

T10.2 1270

1. In x8 mode, only the lower byte of data is output.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

| | |
|---|------------------------|
| Temperature Under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| D. C. Voltage on Any Pin to Ground Potential | -0.5V to $V_{DD}+0.5V$ |
| Transient Voltage (<20 ns) on Any Pin to Ground Potential | -2.0V to $V_{DD}+2.0V$ |
| Package Power Dissipation Capability ($T_A = 25^\circ C$) | 1.0W |
| Surface Mount Solder Reflow Temperature | 260°C for 10 seconds |
| Output Short Circuit Current | 50 mA |

Operating Range

| Range | Ambient Temp | V_{DD} |
|------------|----------------|----------|
| Extended | -20°C to +85°C | 2.7-3.6V |
| Industrial | -40°C to +85°C | 2.7-3.6V |

AC Conditions of Test

| | |
|----------------------------|----------------------|
| Input Rise/Fall Time | 5 ns |
| Output Load | $C_L = 30\text{ pF}$ |
| See Figures 18 and 19 | |

Data Sheet

TABLE 11: DC Operating Characteristics $V_{DD} = 2.7-3.6V$

| Symbol | Parameter | Freq | Limits | | | Test Conditions |
|------------|--|--------------|--------------|-----|---------|---|
| | | | Min | Max | Units | |
| I_{DD}^1 | Active V_{DD} Current Read | | | | | $CE\#=V_{IL}$, $WE\#=OE\#=V_{IH}$ |
| | | 5 MHz | | 15 | mA | |
| | | 1 MHz | | 4 | mA | |
| | Program and Erase Concurrent Read/Write | | | 30 | mA | $CE\#=WE\#=V_{IL}$, $OE\#=V_{IH}$ |
| | | 5 MHz | | 45 | mA | $CE\#=V_{IL}$, $OE\#=V_{IH}$ |
| | | 1 MHz | | 35 | mA | |
| I_{SB} | Standby V_{DD} Current | | | 20 | μA | $CE\#, RST\#=V_{DD}\pm 0.3V$ |
| I_{ALP} | Auto Low Power V_{DD} Current | | | 20 | μA | $CE\#=0.1V$, $V_{DD}=V_{DD} \text{ Max}$ $WE\#=V_{DD}-0.1V$ Address inputs= $0.1V$ or $V_{DD}-0.1V$ |
| I_{RT} | Reset V_{DD} Current | | | 20 | μA | $RST\#=GND$ |
| I_{LI} | Input Leakage Current | | | 1 | μA | $V_{IN} = GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ |
| I_{LIW} | Input Leakage Current on $WP\#$ pin and $RST\#$ pin | | | 10 | μA | $WP\#=GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ $RST\#=GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ |
| I_{LO} | Output Leakage Current | | | 1 | μA | $V_{OUT} = GND$ to V_{DD} , $V_{DD}=V_{DD} \text{ Max}$ |
| V_{IL} | Input Low Voltage | | | 0.8 | V | $V_{DD}=V_{DD} \text{ Min}$ |
| V_{ILC} | Input Low Voltage (CMOS) | | | 0.3 | V | $V_{DD}=V_{DD} \text{ Max}$ |
| V_{IH} | Input High Voltage | $0.7 V_{DD}$ | $V_{DD}+0.3$ | | V | $V_{DD}=V_{DD} \text{ Max}$ |
| V_{IHC} | Input High Voltage (CMOS) | $V_{DD}-0.3$ | $V_{DD}+0.3$ | | V | $V_{DD}=V_{DD} \text{ Max}$ |
| V_{OL} | Output Low Voltage | | | 0.2 | V | $I_{OL}=100 \mu A$, $V_{DD}=V_{DD} \text{ Min}$ |
| V_{OH} | Output High Voltage | $V_{DD}-0.2$ | | | V | $I_{OH}=-100 \mu A$, $V_{DD}=V_{DD} \text{ Min}$ |

T11.1 1270

1. Address input = V_{ILT}/V_{IHT} , $V_{DD}=V_{DD} \text{ Max}$ (See Figure 18)

TABLE 12: Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|------------------|-----------------------------|---------|---------|
| $T_{PU-READ}^1$ | Power-up to Read Operation | 100 | μs |
| $T_{PU-WRITE}^1$ | Power-up to Write Operation | 100 | μs |

T12.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: Capacitance ($T_A = 25^\circ C$, $f=1 \text{ Mhz}$, other pins open)

| Parameter | Description | Test Condition | Maximum |
|-------------|---------------------|----------------|---------|
| $C_{I/O}^1$ | I/O Pin Capacitance | $V_{I/O} = 0V$ | 10 pF |
| C_{IN}^1 | Input Capacitance | $V_{IN} = 0V$ | 10 pF |

T13.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 14: Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|-------------|----------------|-----------------------|--------|---------------------|
| N_{END}^1 | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| T_{DR}^1 | Data Retention | 100 | Years | JEDEC Standard A103 |
| I_{LTH}^1 | Latch Up | $100 + I_{DD}$ | mA | JEDEC Standard 78 |

T14.0 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 15: Read Cycle Timing Parameters $V_{DD} = 2.7-3.6V$

| Symbol | Parameter | Min | Max | Units |
|----------------|---------------------------------|-----|-----|---------|
| T_{RC} | Read Cycle Time | 70 | | ns |
| T_{CE} | Chip Enable Access Time | | 70 | ns |
| T_{AA} | Address Access Time | | 70 | ns |
| T_{OE} | Output Enable Access Time | | 35 | ns |
| T_{CLZ}^1 | CE# Low to Active Output | 0 | | ns |
| T_{OLZ}^1 | OE# Low to Active Output | 0 | | ns |
| T_{CHZ}^1 | CE# High to High-Z Output | | 16 | ns |
| T_{OHZ}^1 | OE# High to High-Z Output | | 16 | ns |
| T_{OH}^1 | Output Hold from Address Change | 0 | | ns |
| T_{RP}^1 | RST# Pulse Width | 500 | | ns |
| T_{RHR}^1 | RST# High before Read | 50 | | ns |
| $T_{RY}^{1,2}$ | RST# Pin Low to Read Mode | | 20 | μs |

T15.1 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
This parameter does not apply to Chip-Erase operations.

TABLE 16: Program/Erase Cycle Timing Parameters

| Symbol | Parameter | Min | Max | Units |
|----------------|----------------------------------|-----|-----|---------|
| T_{BP} | Program Time | | 10 | μs |
| T_{AS} | Address Setup Time | 0 | | ns |
| T_{AH} | Address Hold Time | 40 | | ns |
| T_{CS} | WE# and CE# Setup Time | 0 | | ns |
| T_{CH} | WE# and CE# Hold Time | 0 | | ns |
| T_{OES} | OE# High Setup Time | 0 | | ns |
| T_{OEH} | OE# High Hold Time | 10 | | ns |
| T_{CP} | CE# Pulse Width | 40 | | ns |
| T_{WP} | WE# Pulse Width | 40 | | ns |
| T_{WPH}^1 | WE# Pulse Width High | 30 | | ns |
| T_{CPH}^1 | CE# Pulse Width High | 30 | | ns |
| T_{DS} | Data Setup Time | 30 | | ns |
| T_{DH}^1 | Data Hold Time | 0 | | ns |
| T_{IDA}^1 | Software ID Access and Exit Time | | 150 | ns |
| T_{SE} | Sector-Erase | | 25 | ms |
| T_{BE} | Block-Erase | | 25 | ms |
| T_{SCE} | Chip-Erase | | 50 | ms |
| T_{ES} | Erase-Suspend Latency | | 10 | μs |
| $T_{BY}^{1,2}$ | RY/BY# Delay Time | | 90 | ns |
| T_{BR}^1 | Bus Recovery Time | | 0 | μs |

T16.1 1270

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase, and Program operations.
This parameter does not apply to Chip-Erase operations.

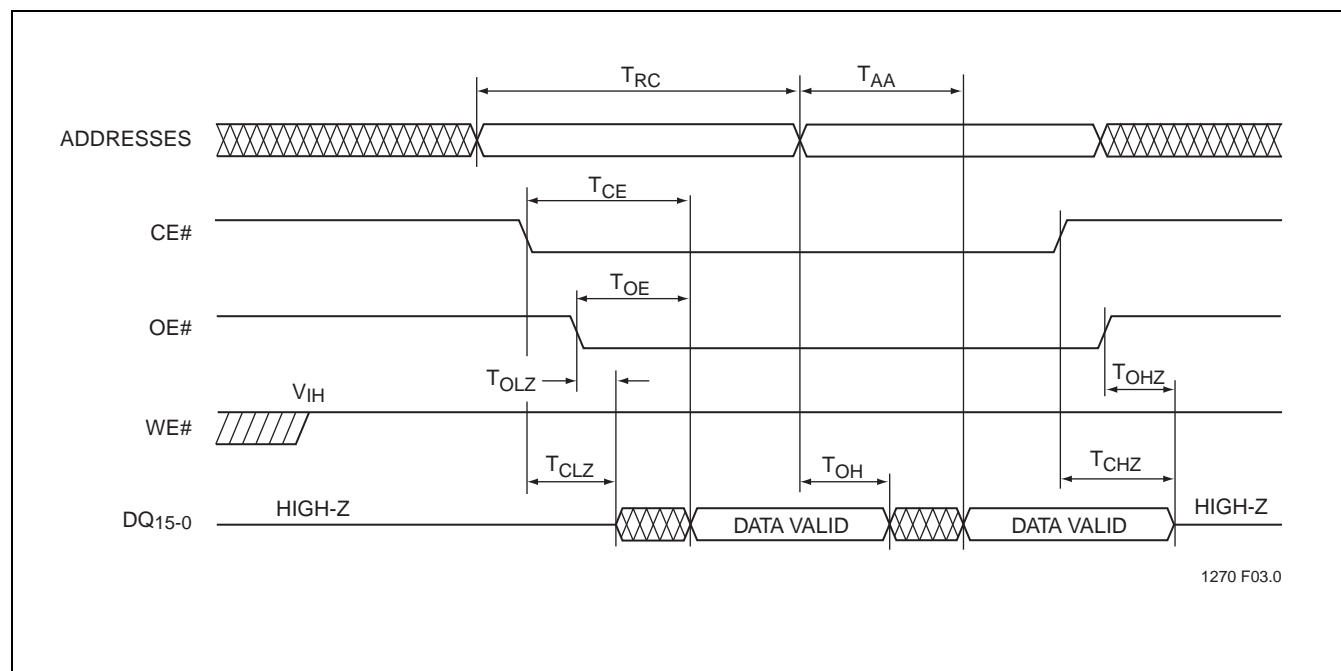


FIGURE 4: Read Cycle Timing Diagram

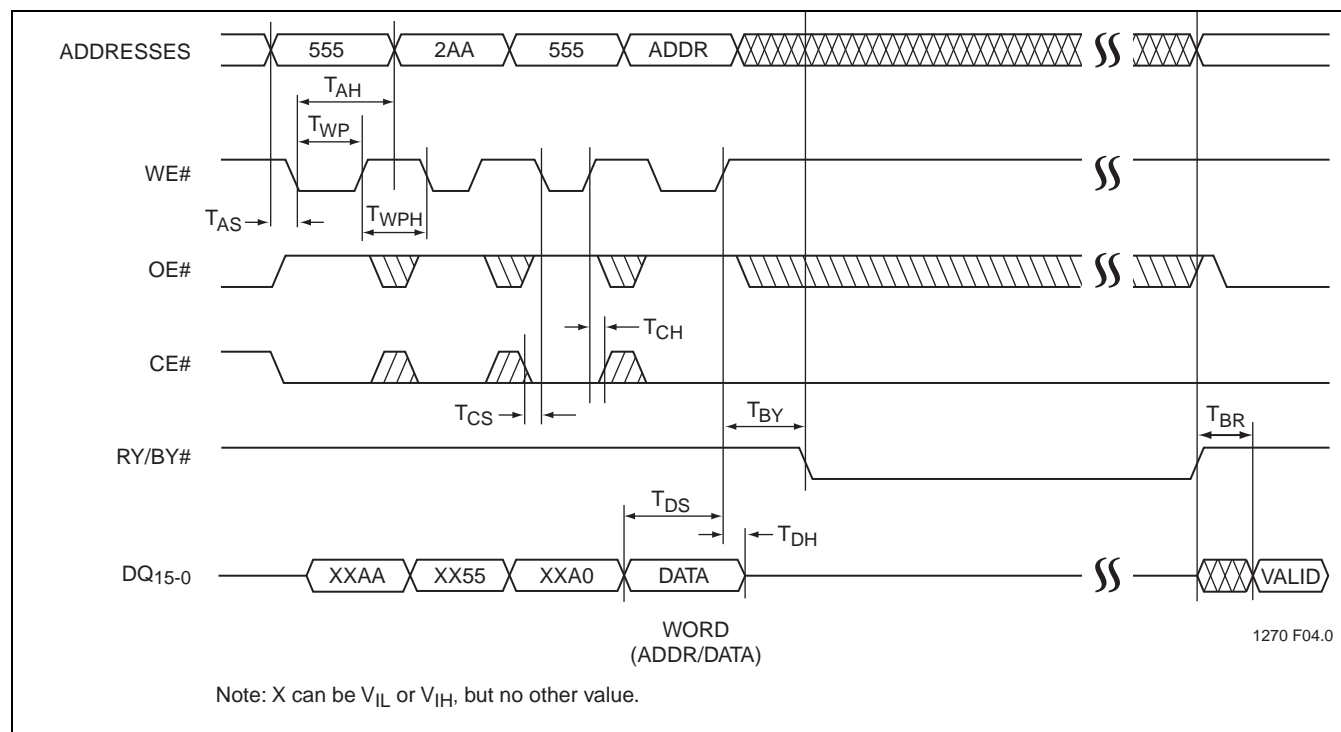


FIGURE 5: WE# Controlled Program Cycle Timing Diagram

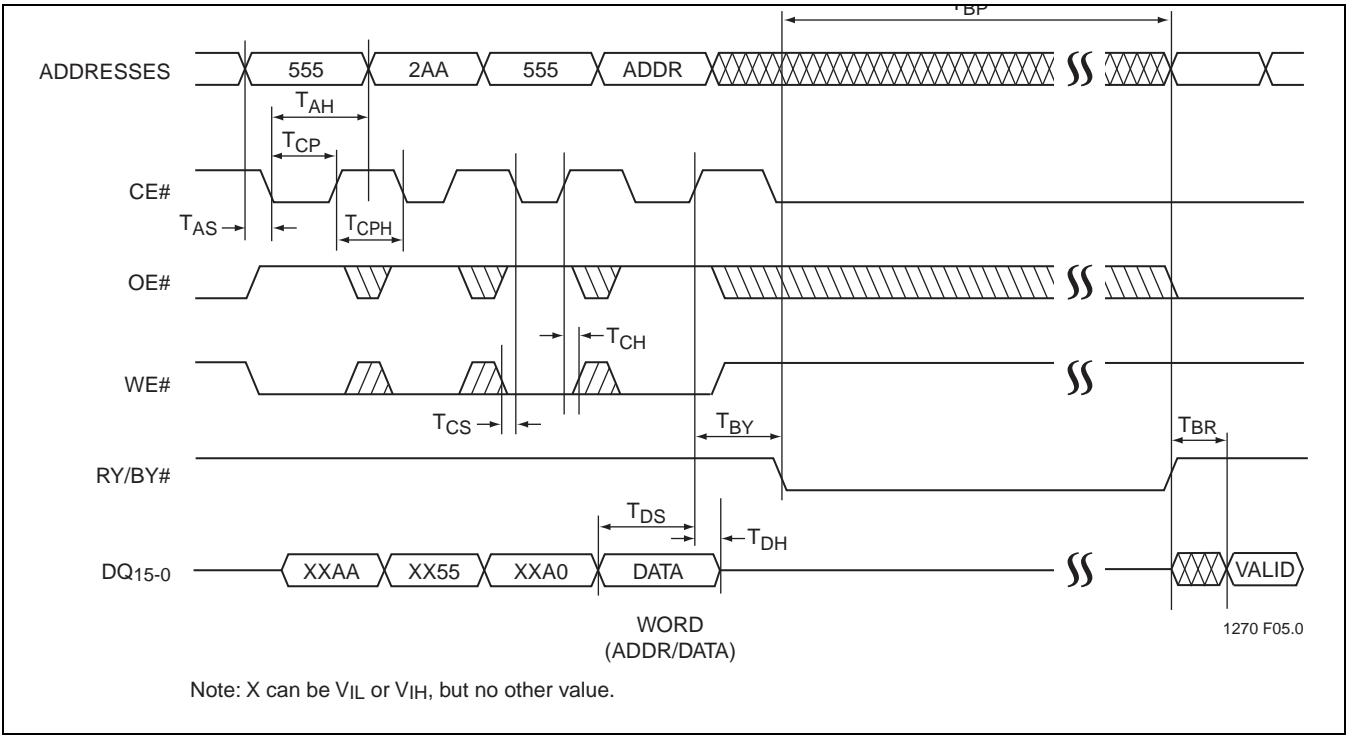


FIGURE 6: CE# Controlled Program Cycle Timing Diagram

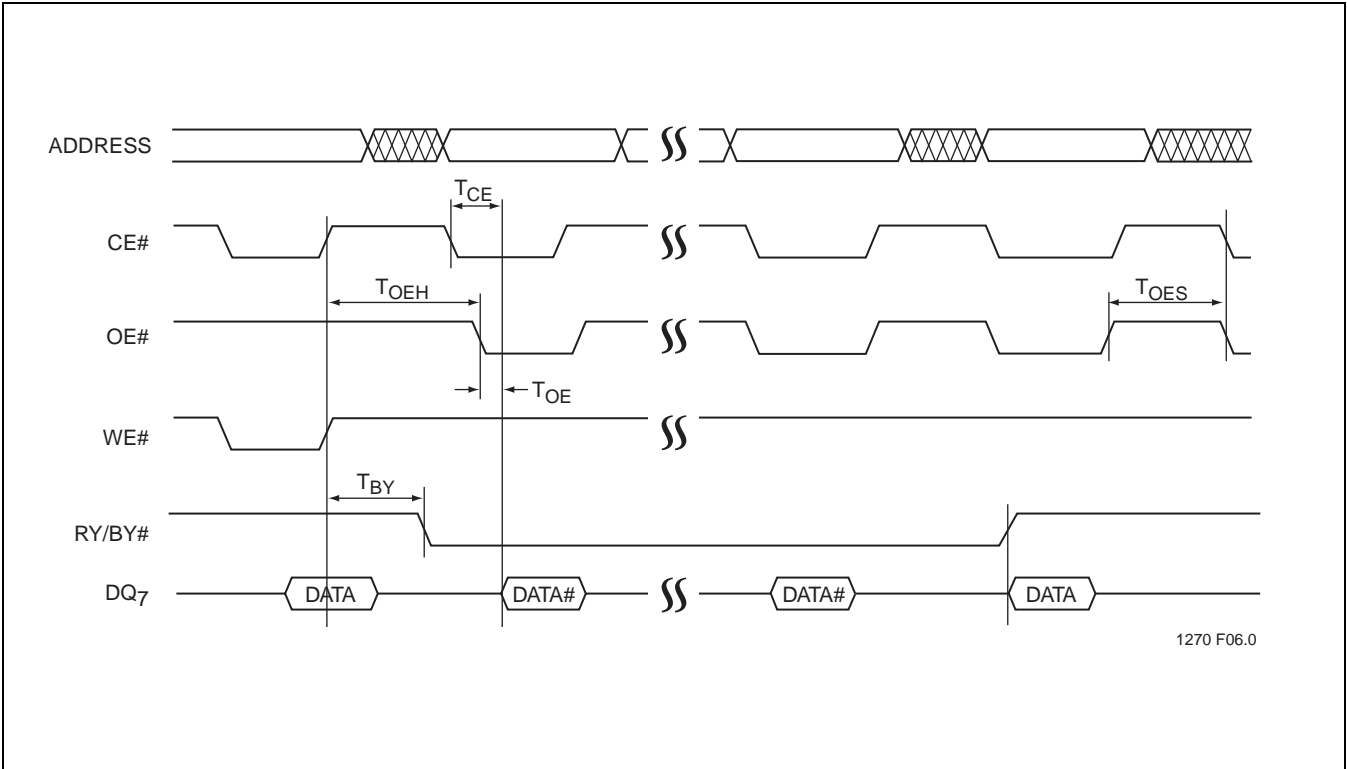


FIGURE 7: Data# Polling Timing Diagram

Data Sheet

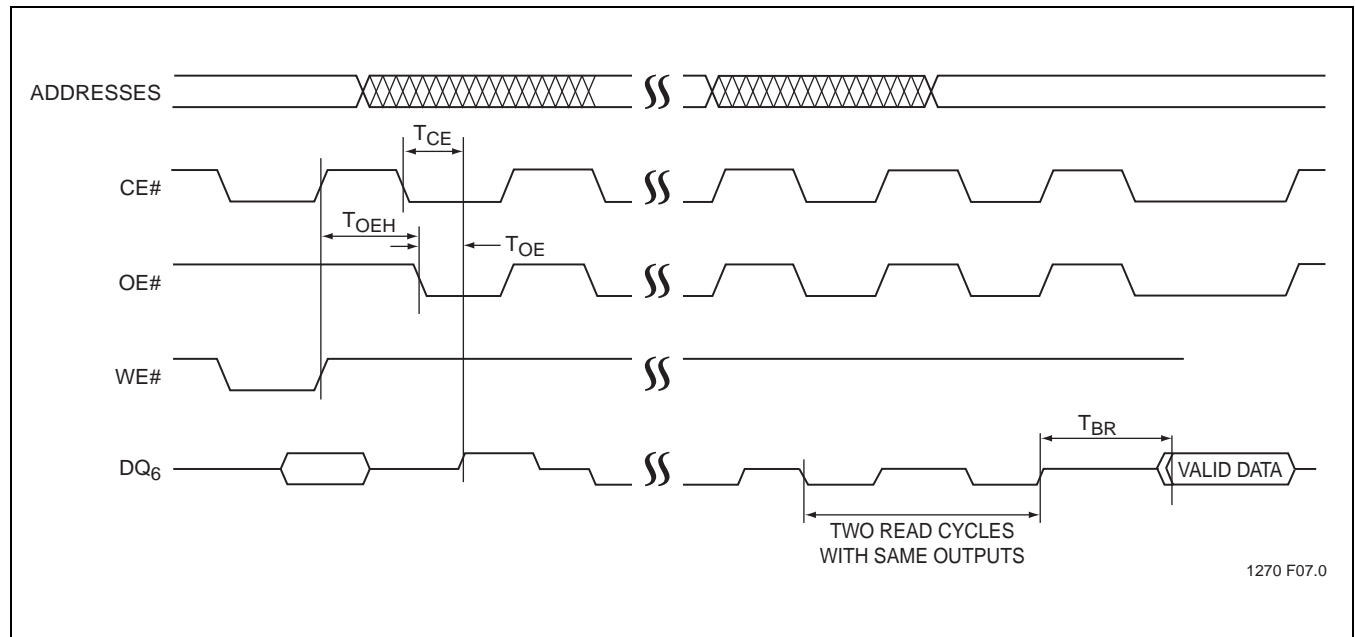


FIGURE 8: Toggle Bit Timing Diagram

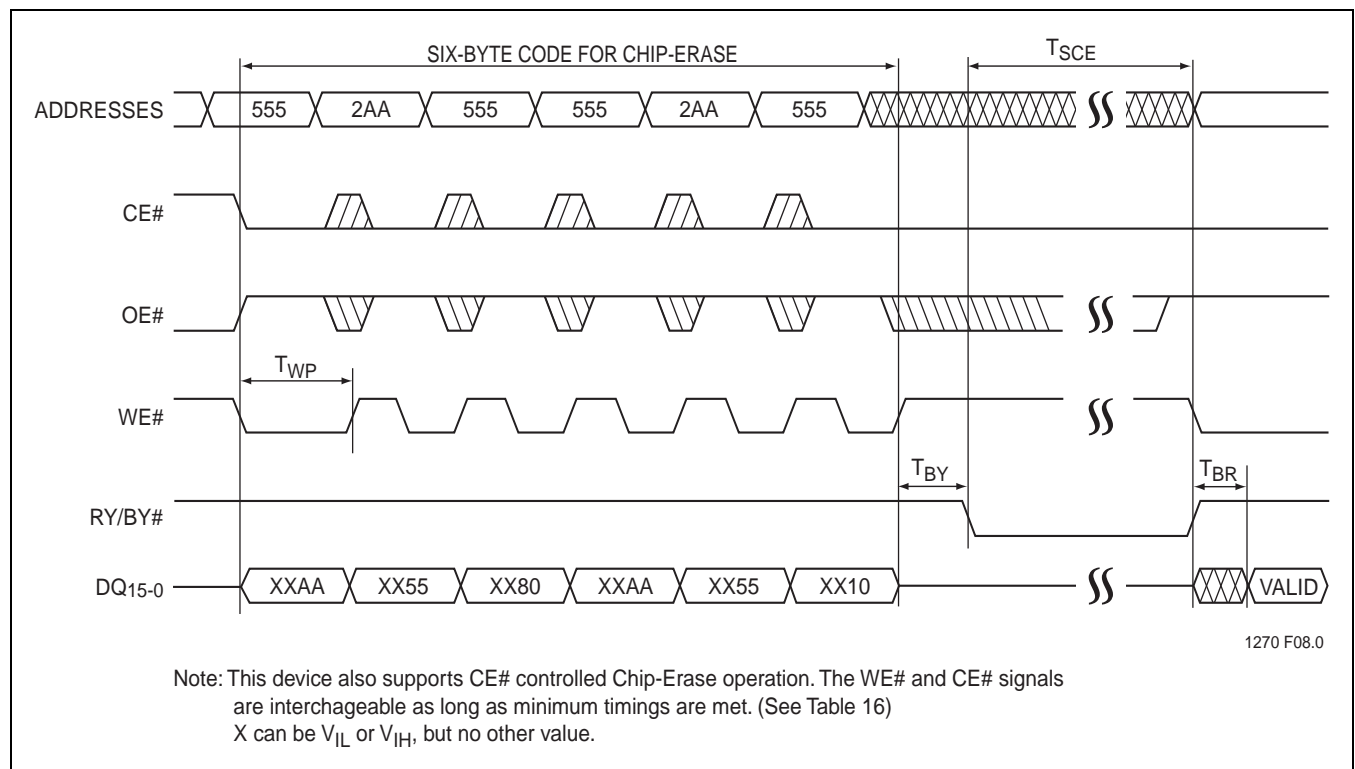


FIGURE 9: WE# Controlled Chip-Erase Timing Diagram

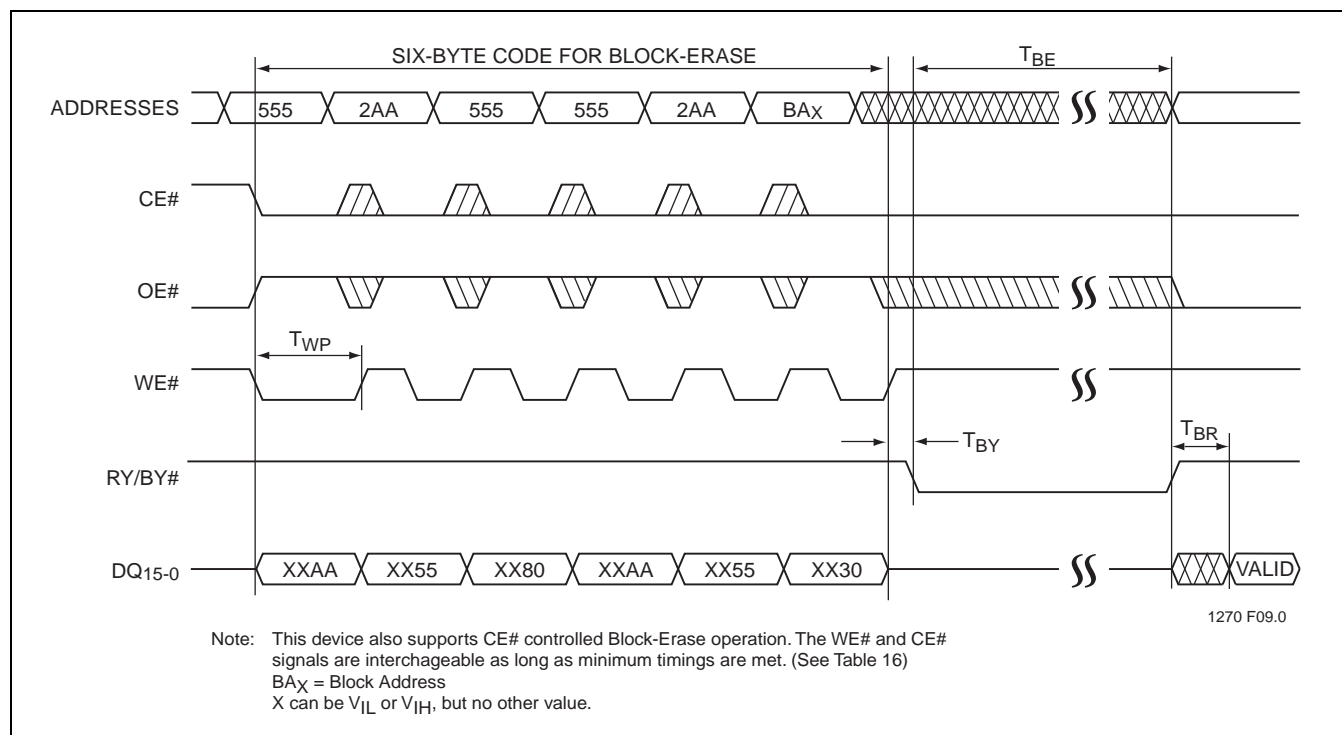


FIGURE 10: WE# Controlled Block-Erase Timing Diagram

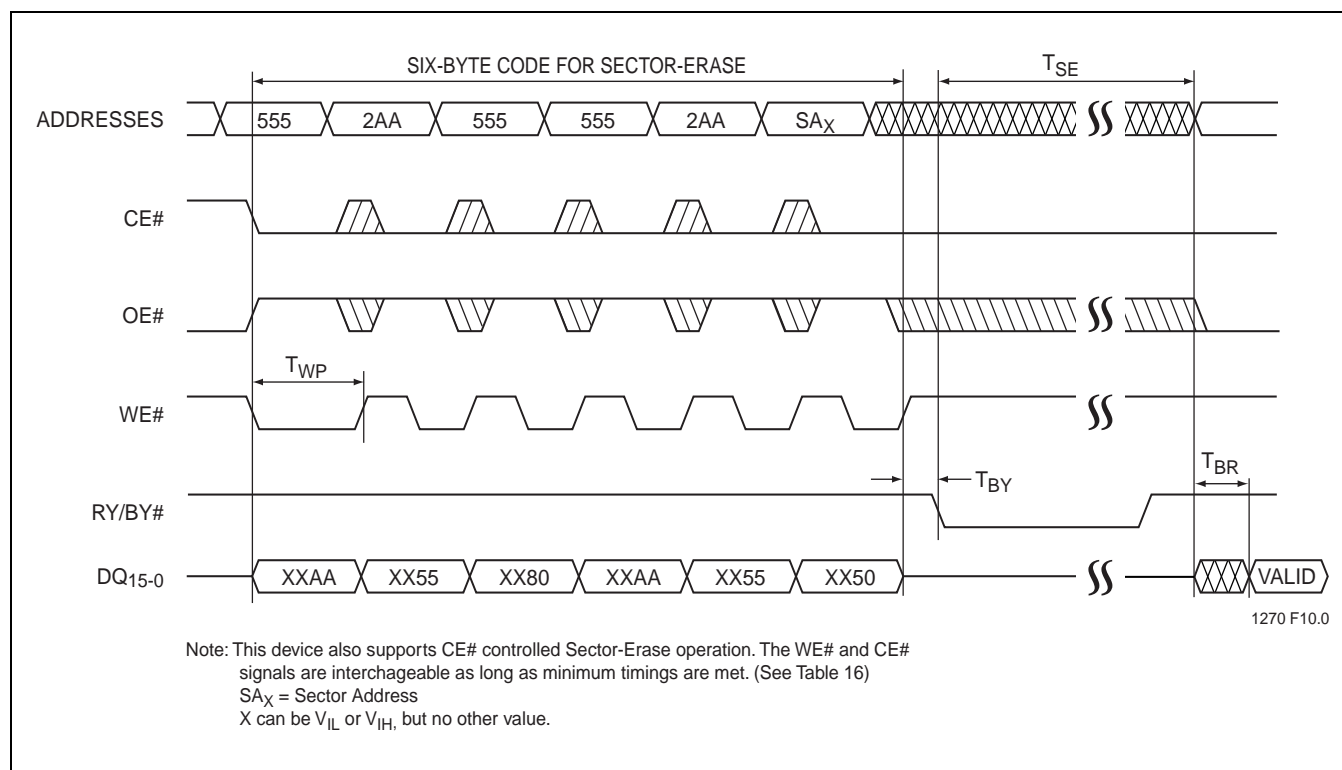


FIGURE 11: WE# Controlled Sector-Erase Timing Diagram

Data Sheet

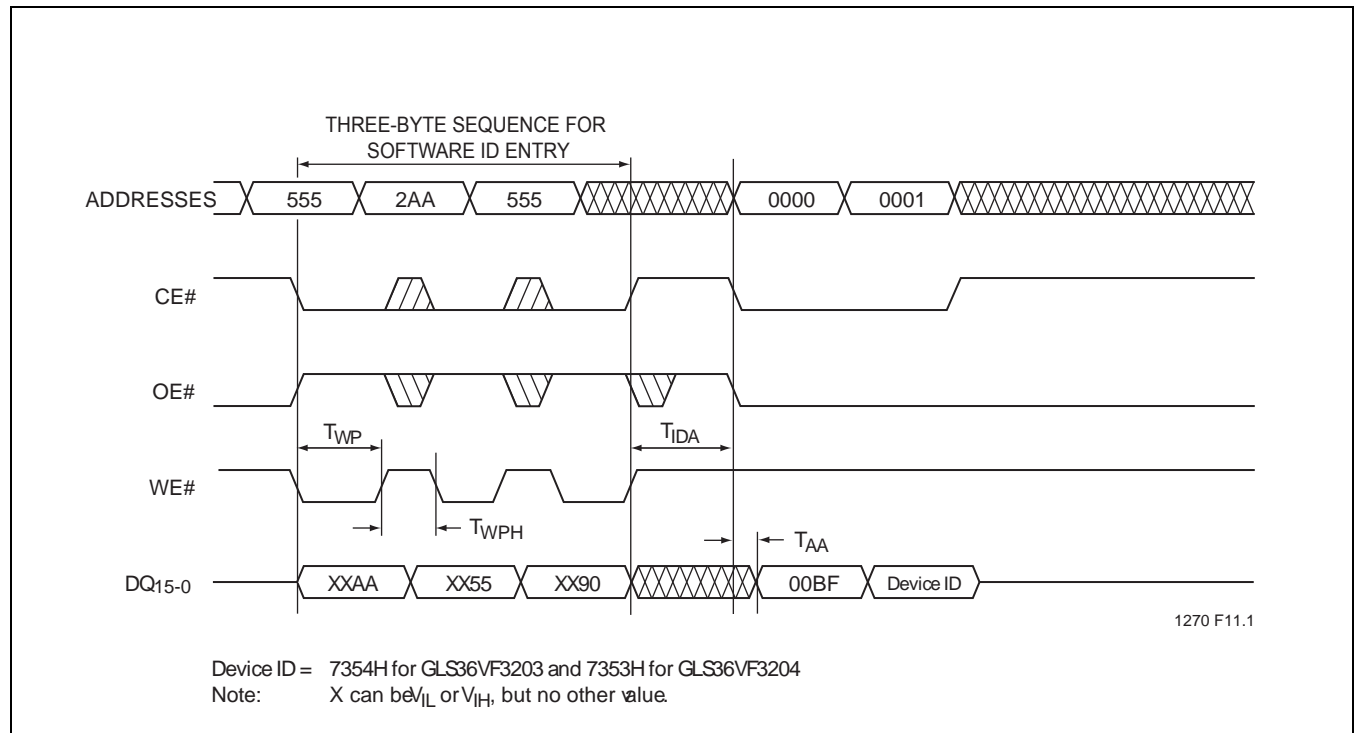


FIGURE 12: Software ID Entry and Read

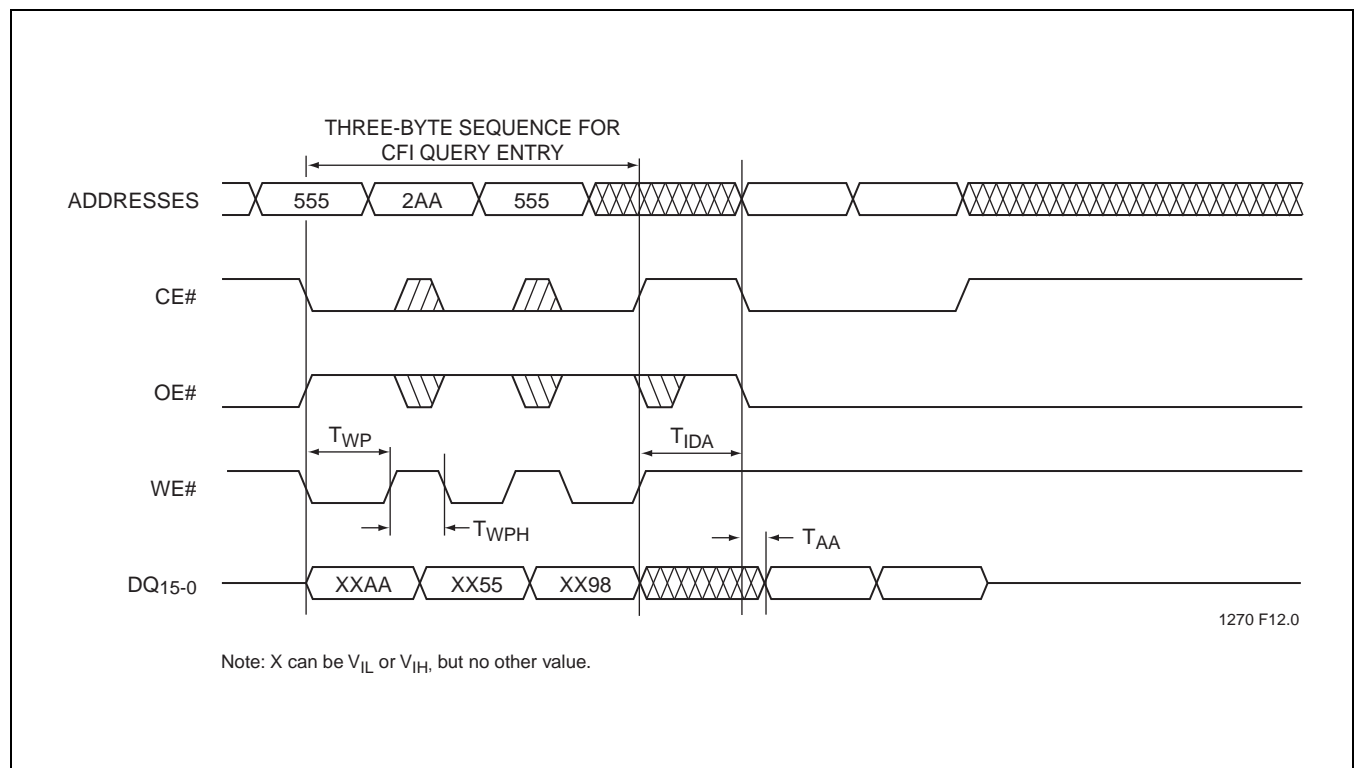


FIGURE 13: CFI Entry and Read

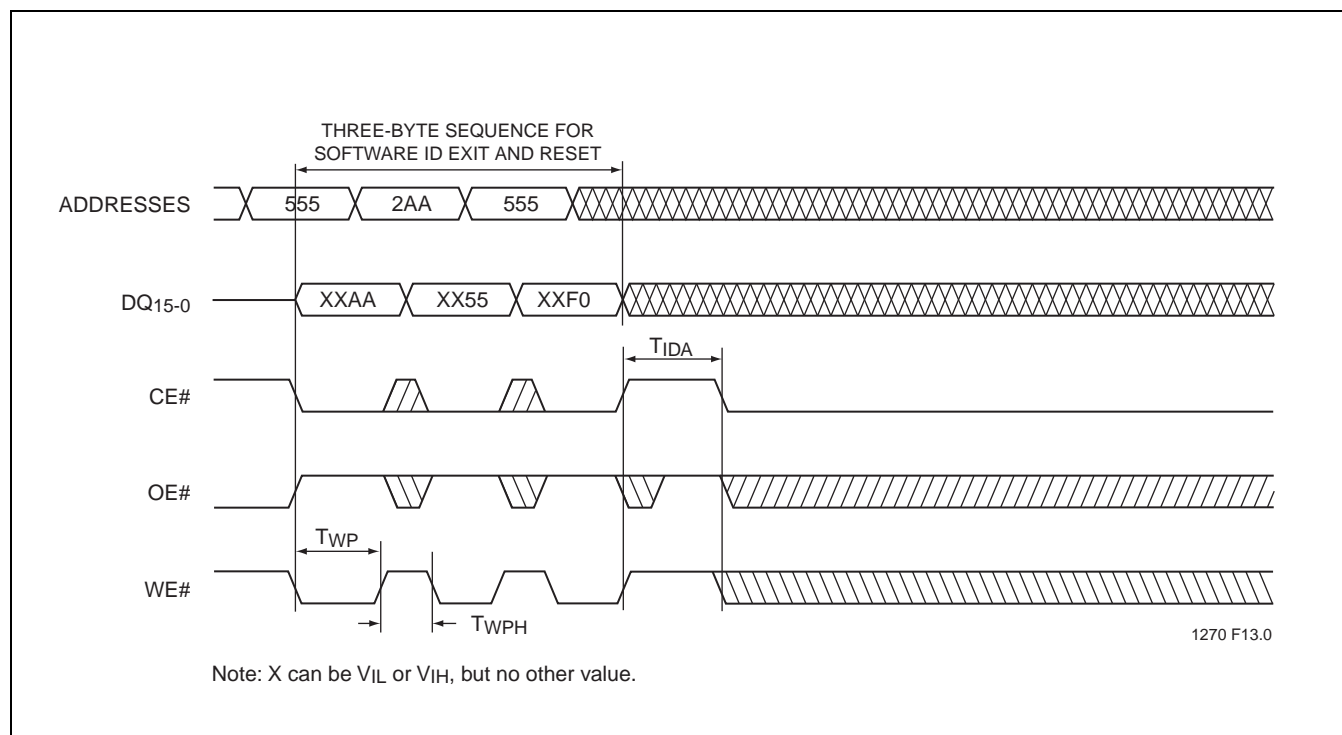


FIGURE 14: Software ID Exit/CFI Exit

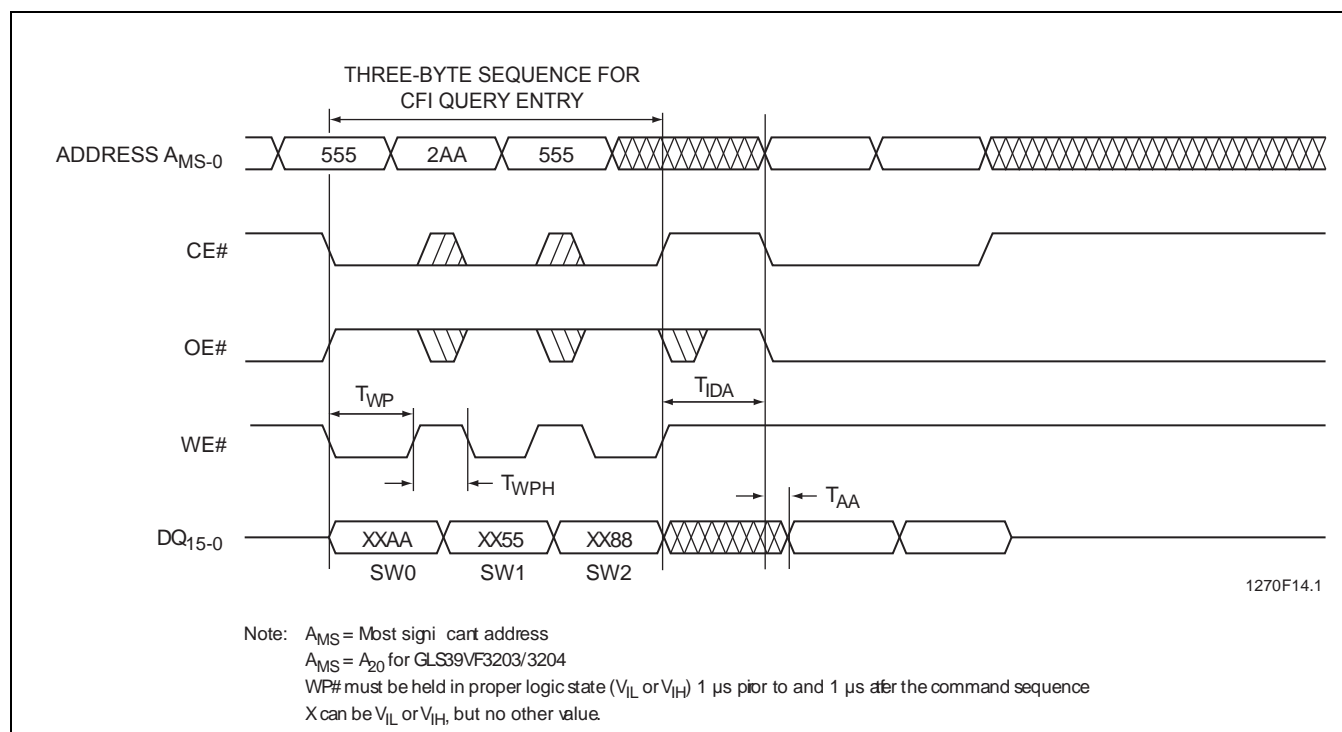


FIGURE 15: Sec ID Entry

Data Sheet

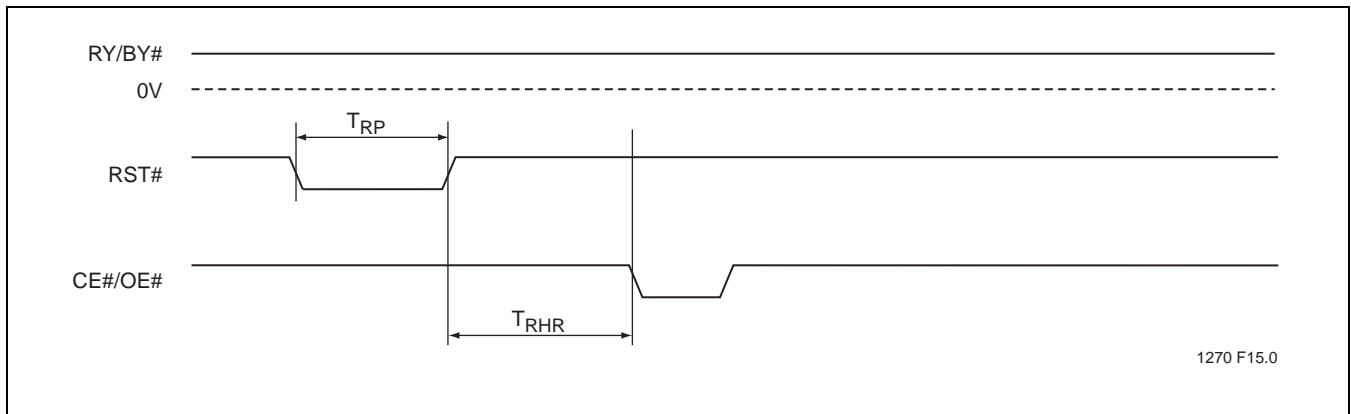


FIGURE 16: RST# Timing Diagram (When no internal operation is in progress)

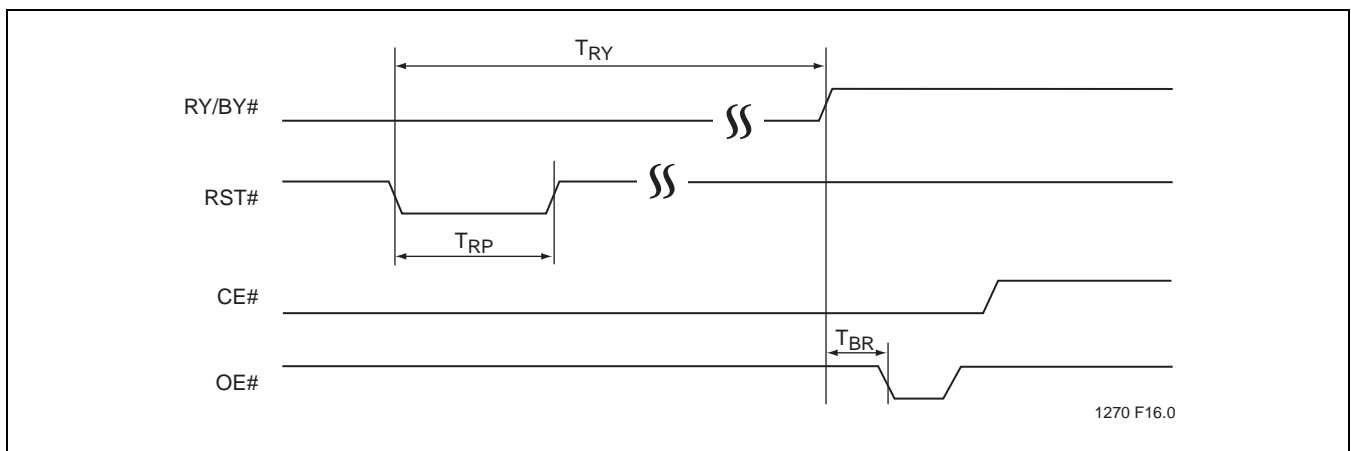
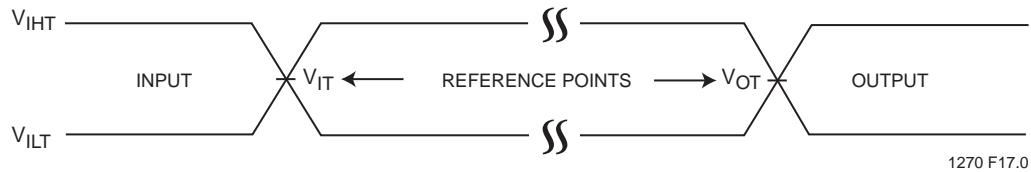


FIGURE 17: RST# Timing Diagram (During Sector- or Block-Erase operation)



AC test inputs are driven at V_{IHT} ($0.9 V_{DD}$) for a logic "1" and V_{ILT} ($0.1 V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} ($0.5 V_{DD}$) and V_{OT} ($0.5 V_{DD}$). Input rise and fall times (10% \leftrightarrow 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - V_{INPUT} HIGH Test
 V_{ILT} - V_{INPUT} LOW Test

FIGURE 18: AC Input/Output Reference Waveforms

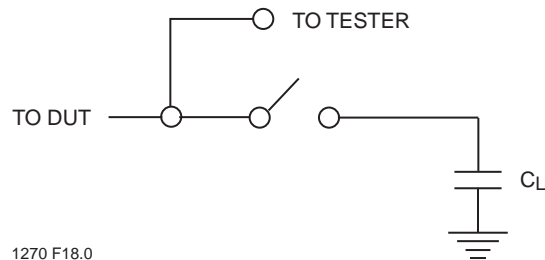
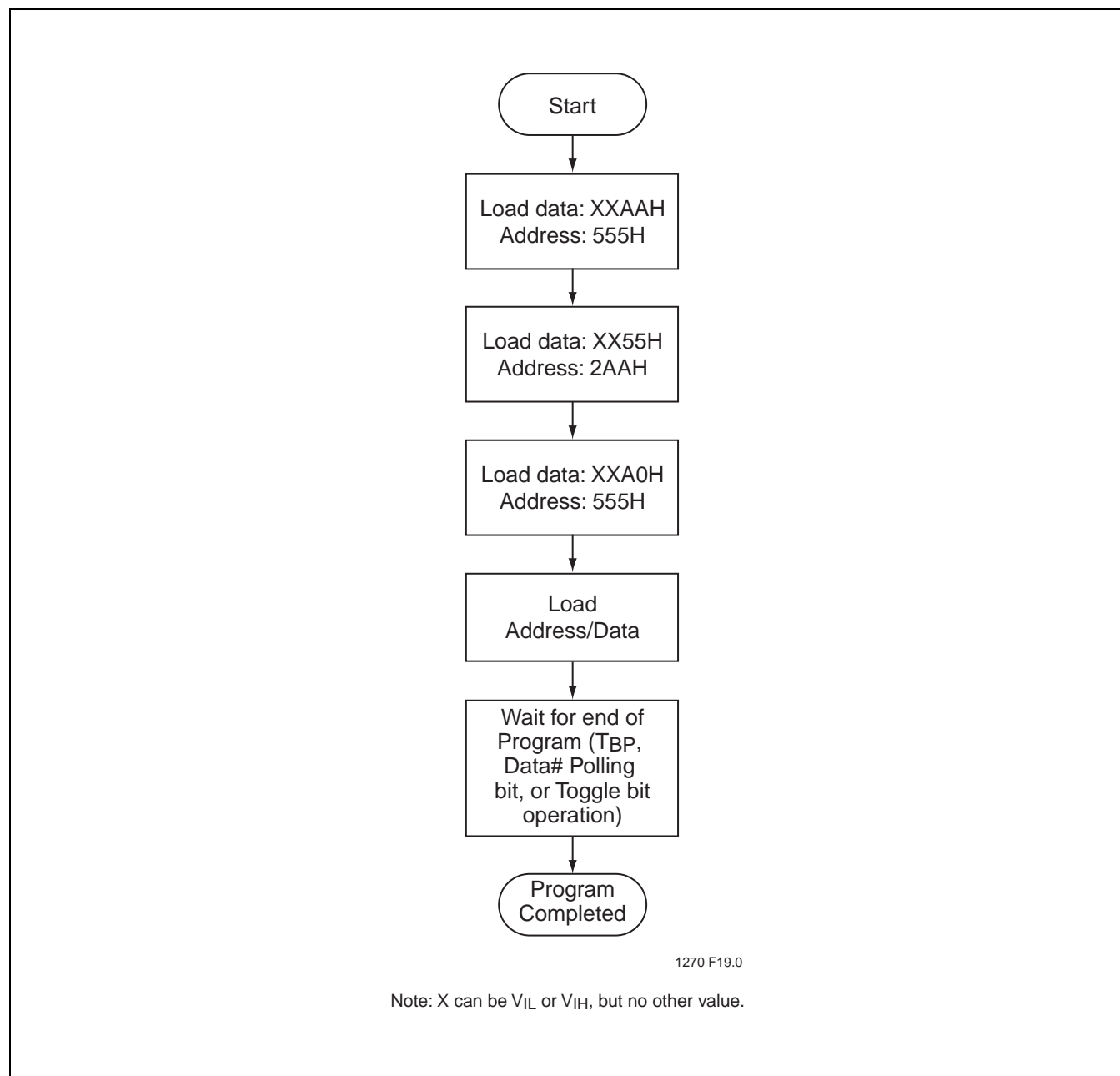


FIGURE 19: A Test Load Example

Data Sheet


FIGURE 20: Word-Program Algorithm

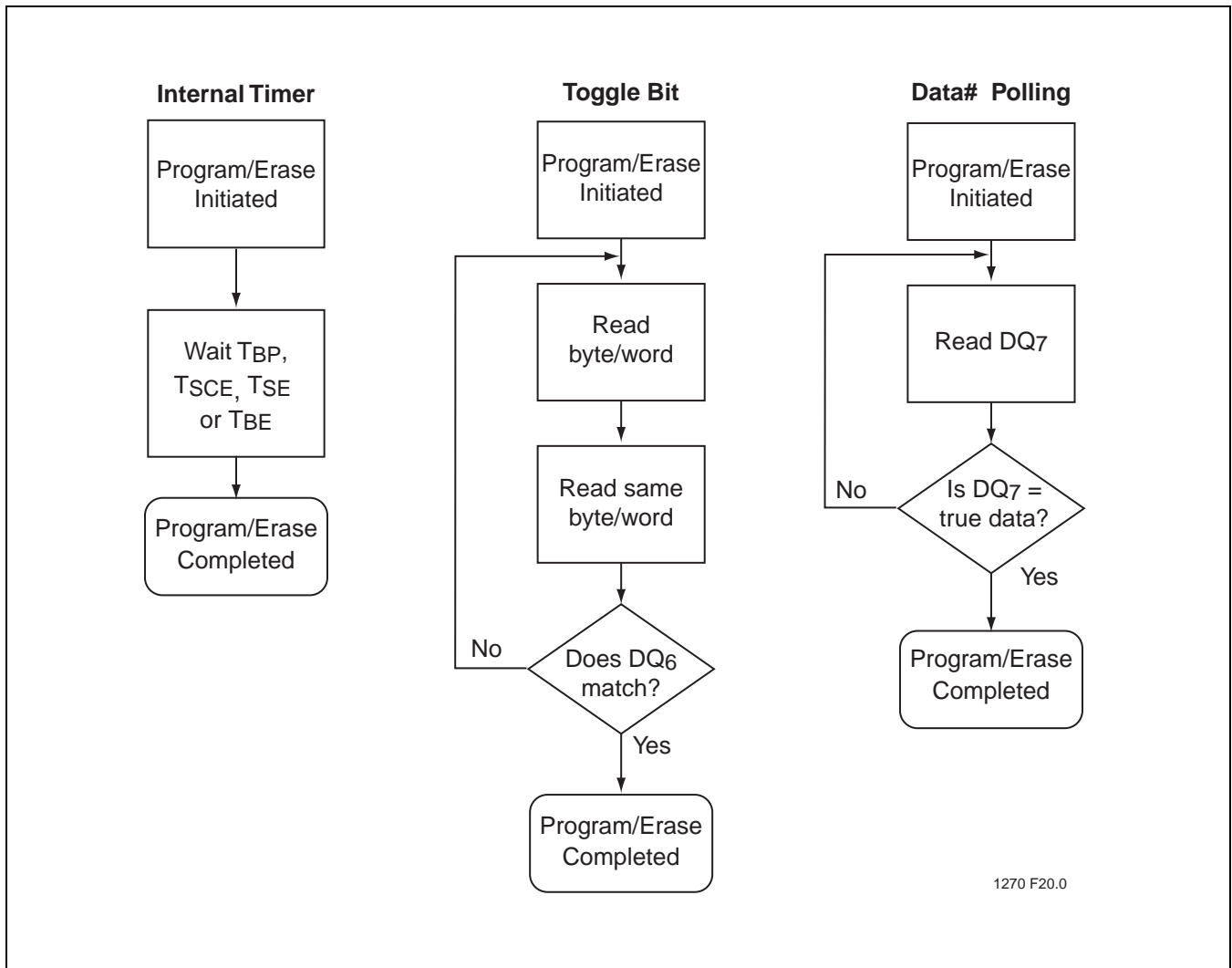


FIGURE 21: Wait Options

Data Sheet

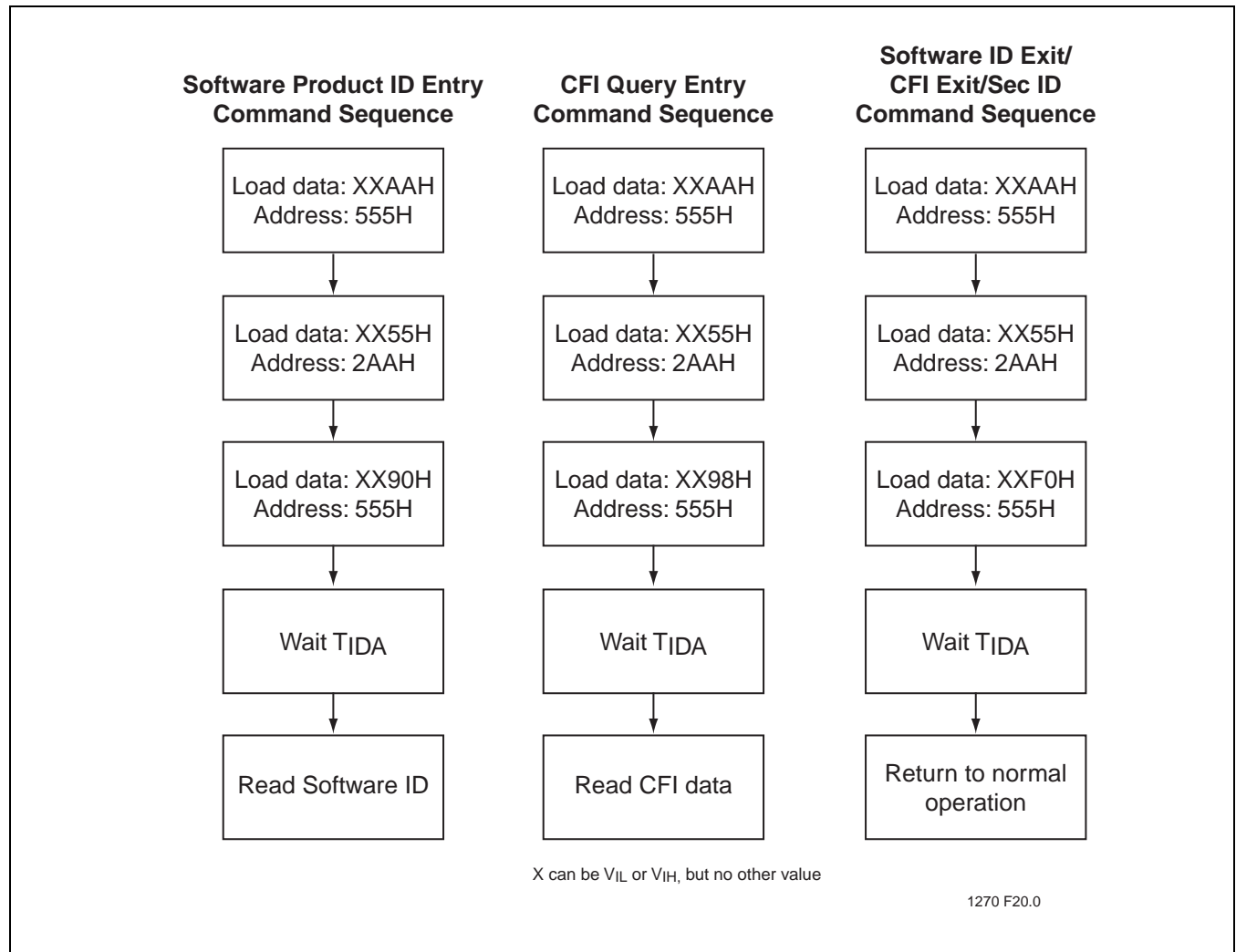


FIGURE 22: Software Product ID/CFI/Sec ID Entry Command Flowcharts

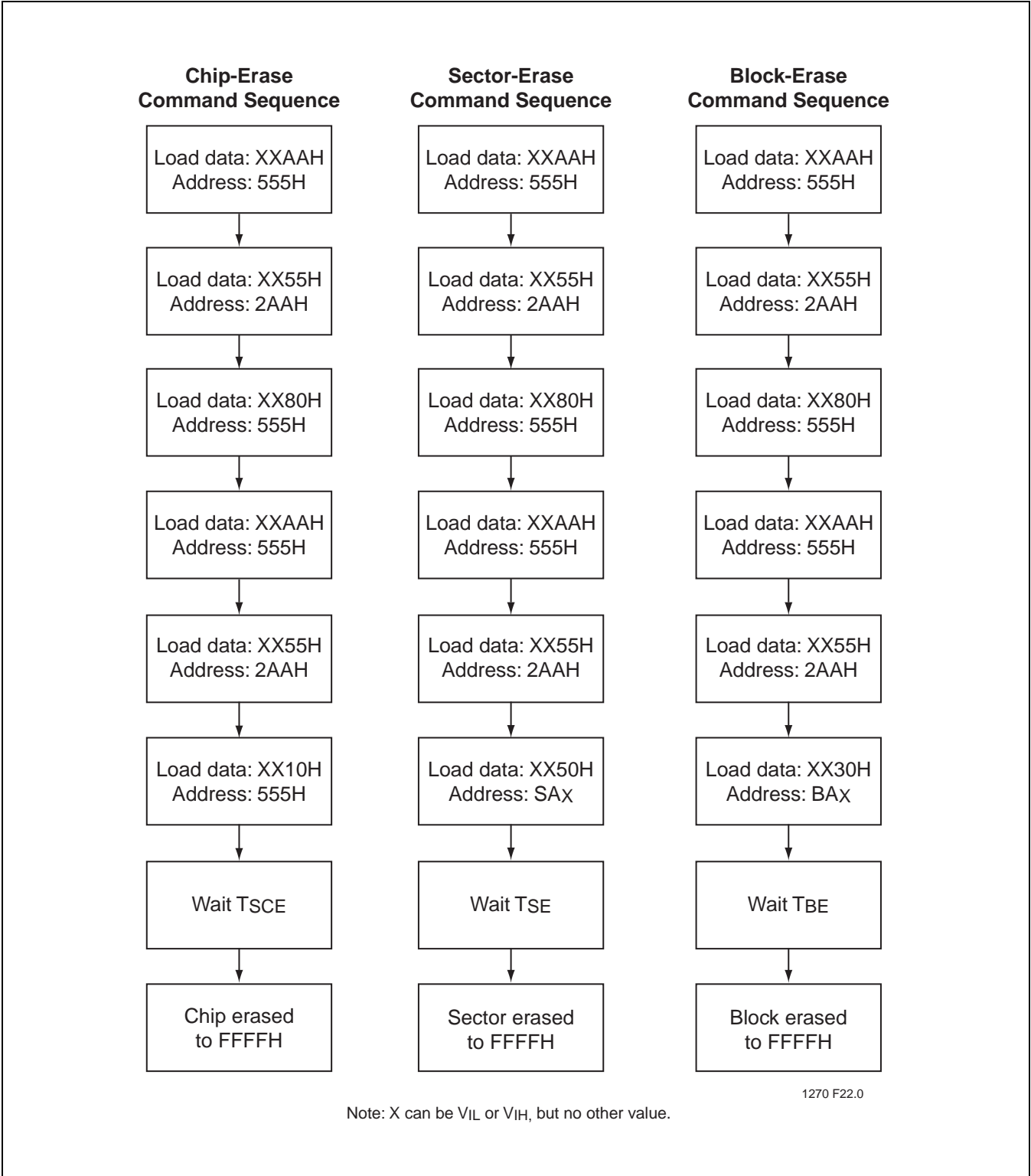
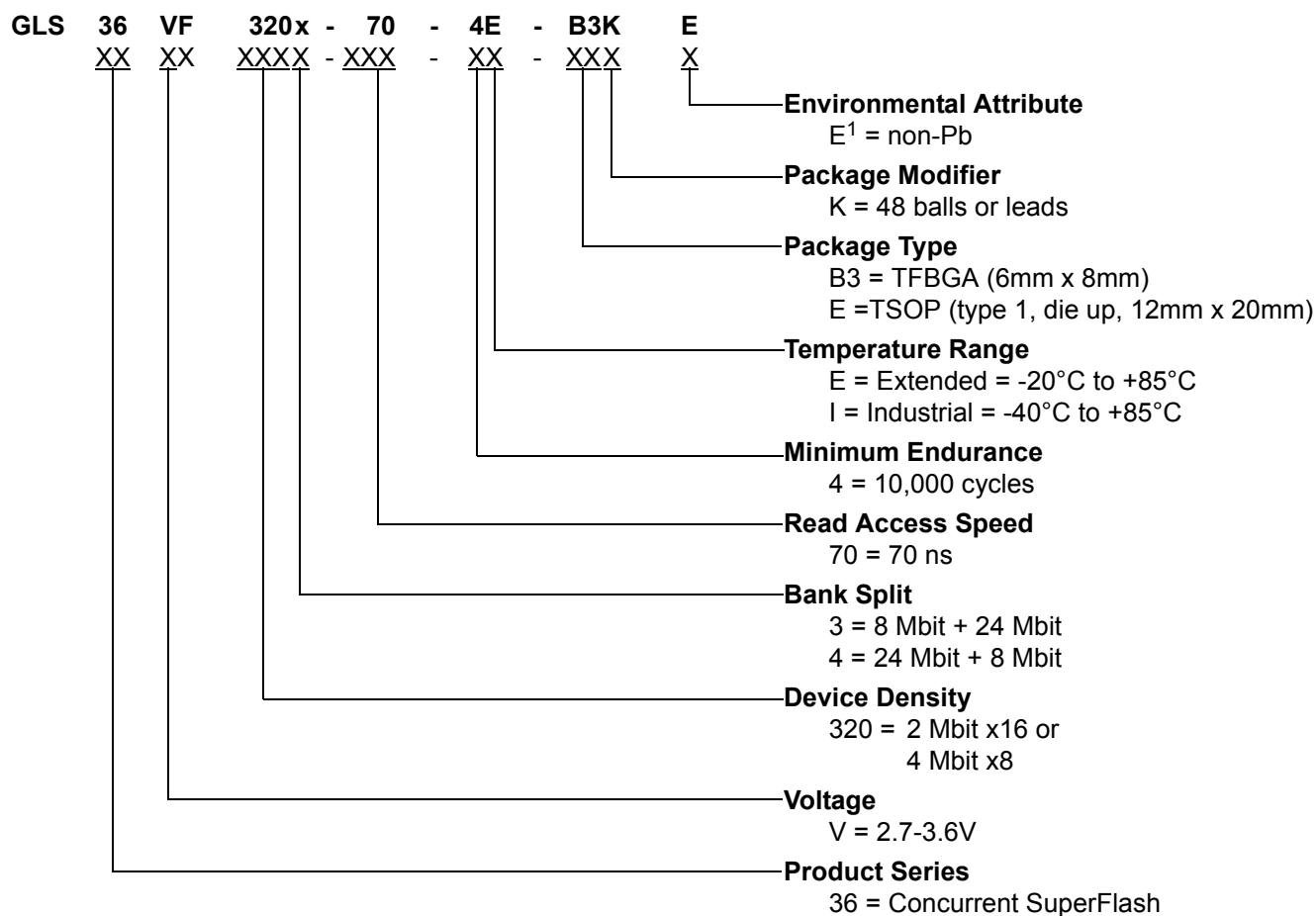


FIGURE 23: Erase Command Sequence

Data Sheet

PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder.
Greenliant non-Pb solder devices are "RoHS Compliant".

Valid combinations for GLS36VF3203

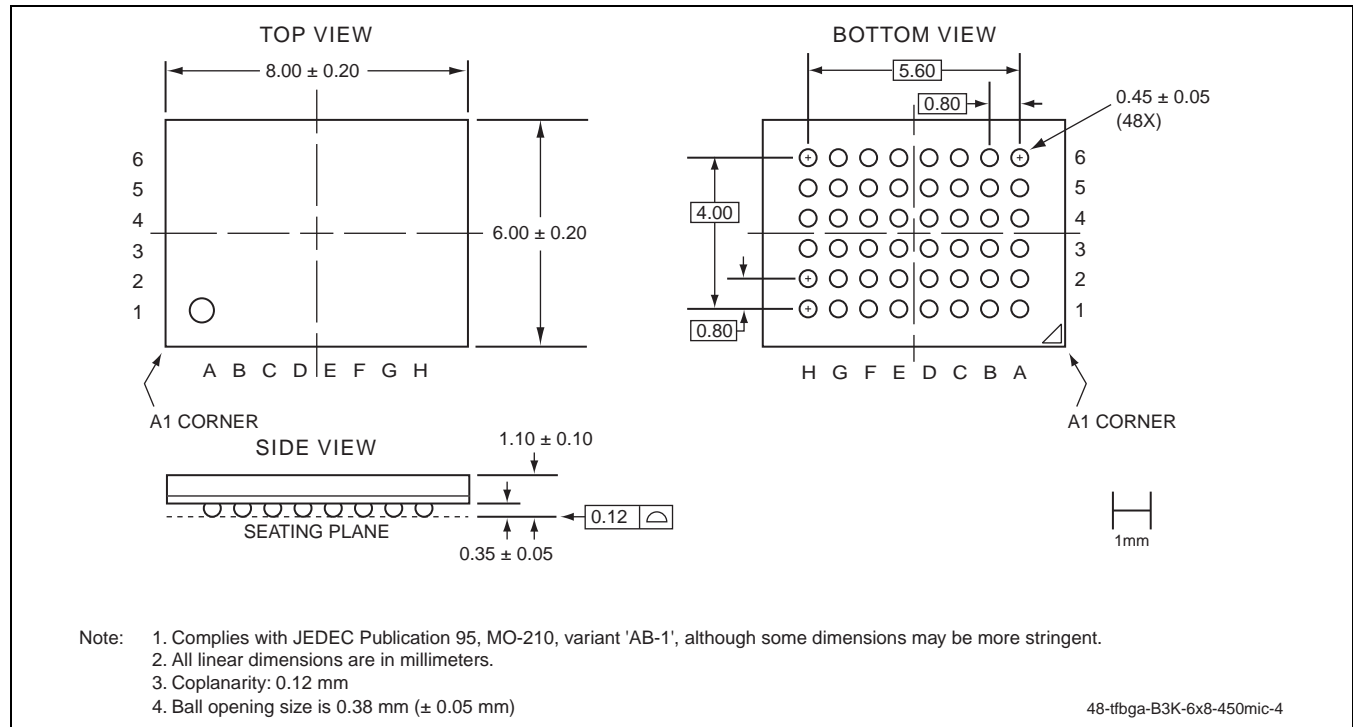
| | |
|------------------------|-----------------------|
| GLS36VF3203-70-4E-B3KE | GLS36VF3203-70-4E-EKE |
| GLS36VF3203-70-4I-B3KE | GLS36VF3203-70-4I-EKE |

Valid combinations for GLS36VF3204

| | |
|------------------------|-----------------------|
| GLS36VF3204-70-4E-B3KE | GLS36VF3204-70-4E-EKE |
| GLS36VF3204-70-4I-B3KE | GLS36VF3204-70-4I-EKE |

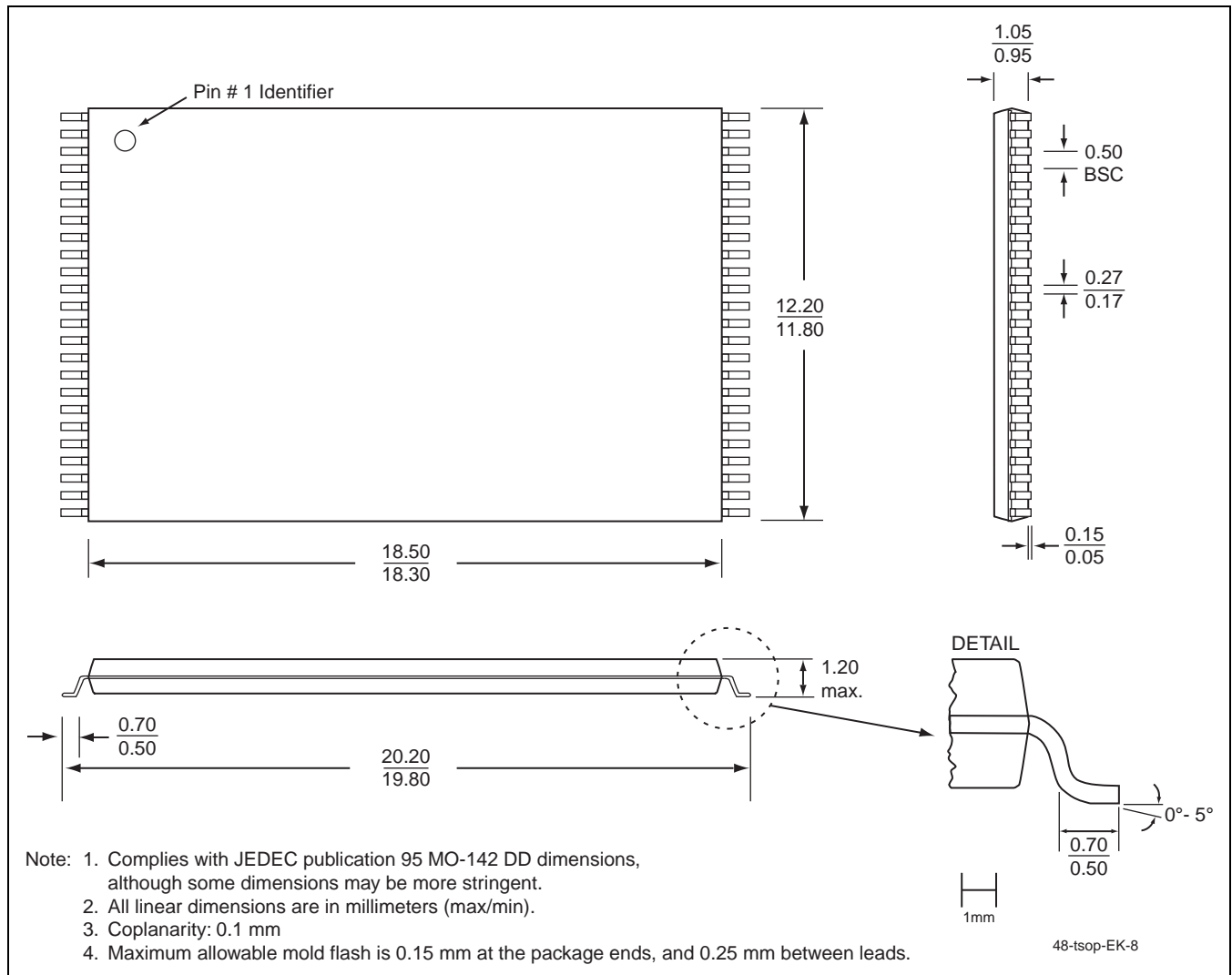
Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS



48-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 6MM X 8MM
GREENLIANT PACKAGE CODE: B3K

Data Sheet



48-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 12MM X 20MM
GREENLIANT PACKAGE CODE: EK

TABLE 17: Revision History

| Number | Description | Date |
|--------|---|----------|
| 00 | <ul style="list-style-type: none"> Initial release of data sheet | Feb 2005 |
| 01 | <ul style="list-style-type: none"> Updated “Erase-Suspend/Erase-Resume Operations” on page 3 Updated footnote 5 and added footnote 7 to Table 7 on page 14 Updated CFI Query Identification in Table 8 on page 15 Updated Device Geometry Information in Table 10 on page 16 Updated T_{ES} parameter from 20 μs to 10 μs in Table 16 on page 19 In “Product Ordering Information” on page 32 <ul style="list-style-type: none"> Removed all MPNs for packages containing Pb (B3K/EK) Removed all commercial temperature MPNs Added extended temperature MPNs for all devices | Sep 2005 |
| 02 | <ul style="list-style-type: none"> Removed Industrial Grade reference Changed to Data Sheet Removed non-Pb reference Updated Bank information Changes TOE from 30ns to 35ns, Table 15, page 18 | May 2006 |
| 03 | <ul style="list-style-type: none"> Re-added Industrial Grade reference | Jul 2006 |
| 04 | <ul style="list-style-type: none"> Edited T_{by} TY/BY# Delay Time in Table 15 on page 19 from 90ns Min to 90ns Max | Nov 2009 |
| 05 | <ul style="list-style-type: none"> Transferred from SST to Greenliant | May 2010 |

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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