



QPF4530

Wi-Fi Front End Module

Product Overview

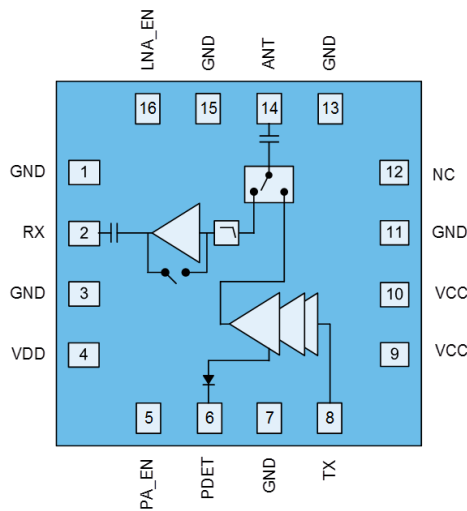
The Qorvo® QPF4530 is an integrated front end module (FEM) designed for Wi-Fi 802.11ax systems. The compact form factor and integrated matching minimizes layout area in the application.

Performance is focused on optimizing the PA for a 3.3V supply voltage that conserves power consumption while maintaining the highest linear output power and leading edge throughput. Receive path matches the optimal technologies to maximize Rx sensitivity through noise figure performance that is consistent over a wider variety of conditions.

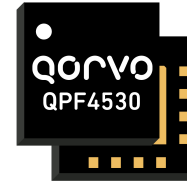
The receive path is pinned out so external filtering can be added in the optimal position. Integrated die level filtering for 2nd and 3rd harmonics as well as 2.4 GHz rejection for DBDC operation are included. A DC power detector which has voltage output provides feedback for close loop applications.

The QPF4530 integrates a 5 GHz power amplifier (PA), regulator, single pole two throw switch (SP2T) and bypassable low noise amplifier (LNA) into a single device

Functional Block Diagram



Top View



16 Pin 3x3 mm QFN Package

Key Features

- 5150 – 5925 MHz
- P_{OUT} = +15dBm MCS11 HE80 -43dB Dynamic EVM
- P_{OUT} = +18dBm MCS9 VHT80 -35dB Dynamic EVM
- P_{OUT} = +19dBm MCS7 HT20/40 -30dB Dynamic EVM
- P_{OUT} = +21dBm MCS0 HT20 Spectral Mask Compliance
- Optimized for +3.3 V Operation
- 0.5W Power Consumption at P_{OUT} +17dBm
- 30 dB Tx Gain
- 2 dB Noise Figure
- 15 dB Rx Gain & 7 dB Bypass Loss
- 37 dB 2.4 GHz Rejection on Rx Path
- Integrated DC Power Detector

Applications

- Access Points
- Wireless Routers
- Client Equipment
- Customer Premise Equipment
- Internet of Things

Ordering Information

Part Number	Description
QPF4530SB	Sample bag with 5 pieces
QPF4530SQ	Sample bag with 25 pieces
QPF4530SR	7" reel with 100 pieces
QPF4530TR13-5K	13" reel with 5,000 pieces
QPF4530PCK-01	Assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Conditions	Rating
DC Supply Voltage		-0.5 to +6 V
Control Voltage	PA_EN & LNA_EN	-0.5 to +6 V
Storage Temperature		-40 to 150 °C
Junction Temperature	MTTF > 1.5x10 ⁶ hours MTTF > 1.0x10 ⁶ hours	160 °C 170 °C
RF Input Power at TX	Into 50 Ω Load for 802.11a/n/ac/ax (No Damage), Transmit Mode	+10 dBm
RF Input Power at ANT	(No Damage), Receive LNA On Mode	+10 dBm
RF Input Power at ANT	(No Damage), Receive Bypass Mode	+25 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. This is an InGaP device designed for high duty cycle applications with T_j>30 °C over ambient.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Frequency	5150		5850	MHz
Extended Operating Frequency	4900		5925	MHz
Device Voltage (V _{CC} & V _{DD})	+3	+3.3	+3.6	V
Control Voltage – High	+1.7	+3	V _{CC}	V
Control Voltage - Low	0		+0.4	V
T _{OPERATING} *	-40		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. * T_{OPERATING} is temperature at package ground.

Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Transmit (TX-ANT) Mode	Unless otherwise noted: V_{CC}=3.3V, T=+25°C, PA_EN=High, LNA_EN=Low				
11ax HE80 Output Power	MCS11 1024QAM		15		dBm
Dynamic EVM				-43	dB
11ax HE80 Output Power	MCS11 1024QAM		16		dBm
Dynamic EVM				-40	dB
11ac VHT80 Output Power	MCS9 256QAM	16.5	18		dBm
Dynamic EVM				-35	dB
11n HT20/40 Output Power	MCS7 64QAM	17.5	19		dBm
Dynamic EVM				-30	dB
Margin to VHT80 Spectral Mask	P _{OUT} = +19.5 dBm, 11ac MCS0		3		dBc
Margin to HT20 Spectral Mask	P _{OUT} = +21 dBm, 11n MCS0		3		dBc
Gain		29	30		dB
Gain Flatness	Across any 80 MHz Channel	-0.25		+0.25	dB
Out of Band Gain	f = 3300-3800MHz			-5	dB
	f > 7000MHz			15	dB
TX Port Return Loss		7	14		dB

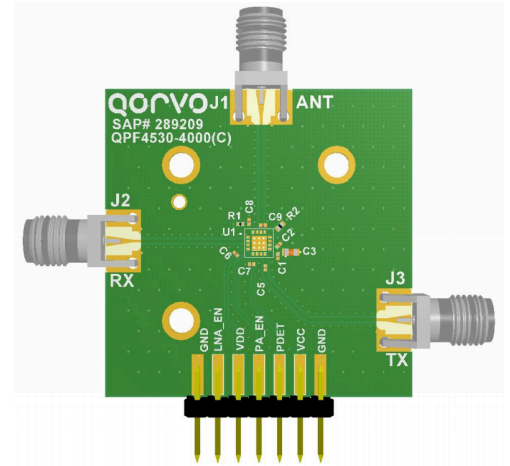
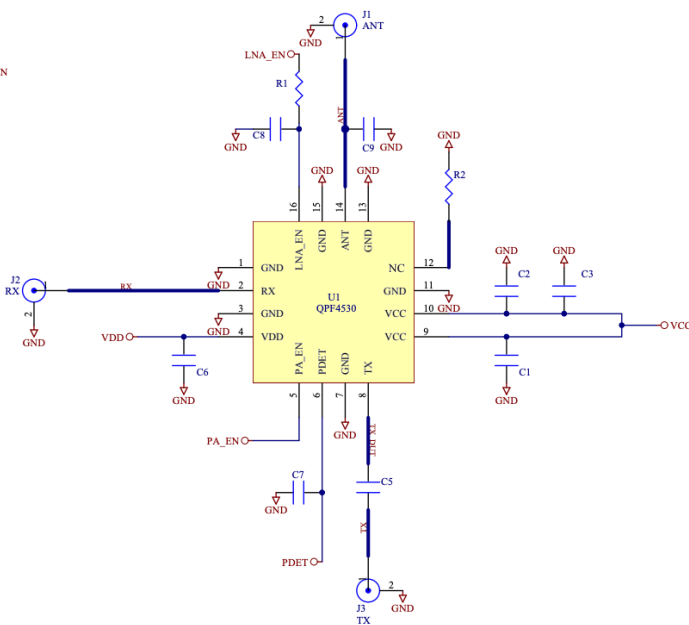
Parameter	Conditions	Min.	Typ.	Max.	Units
ANT Port Return Loss		7	15		dB
Quiescent Current	RF Off		95		mA
Operating Current	P _{OUT} = +15 dBm P _{OUT} = +18 dBm P _{OUT} = +21 dBm		135 155 195	150 175 215	mA
2 nd Harmonics	P _{OUT} = +21 dBm 802.11a 6 Mbps		-35	-30	dBm/MHz
3 rd Harmonics	P _{OUT} = +21 dBm 802.11a 6 Mbps		-40	-35	dBm/MHz
ANT-RX Isolation			40		dB
DC Power Detect Voltage	RF Off		0.25		V
	P _{OUT} = +15 dBm		0.46		V
	P _{OUT} = +18 dBm		0.58		V
	P _{OUT} = +21 dBm		0.75		V
RECEIVE (ANT-RX) LNA ON MODE		Unless otherwise noted: V_{CC}=3.3V, T=+25°C, PA_EN=Low, LNA_EN=High			
Gain		13.5	15		dB
Gain Flatness Across any 80 MHz Channel		-0.25		+0.25	dB
Out of Band Gain	f = 2400-2500 MHz		-37		dB
Noise Figure			2	2.2	dB
RX Port Return Loss		7	13		dB
ANT Port Return Loss		6	9		dB
Input P _{1dB}			-5		dBm
Input IP3			+9		dBm
Rx Operating Current			17		mA
RECEIVE (ANT-RX) BYPASS MODE		Unless otherwise noted: V_{CC}=3.3V, T=+25°C, PA_EN=Low, LNA_EN=Low			
Bypass Loss			7		dB
Loss Flatness Across any 80 MHz Channel		-0.15		+0.15	dB
Out of Band Gain	f = 2400-2500 MHz		-32		dB
RX Port Return Loss		10	12		dB
ANT Port Return Loss		6	8		dB
Input P _{1dB}			+20		dBm
Input IP3			+40		dBm
GENERAL SPECIFICATIONS		Unless otherwise noted: V_{CC}=3.3V, T=+25°C			
Control Current - High			30		μA
Control Current - Low			5		μA
Switching Time	Transmit to LNA On or Bypass Mode			500	nS
	LNA On to Bypass Mode			200	nS
	Bypass to LNA On Mode			200	nS
	LNA On or Bypass to Transmit Mode			500	nS
TX Output P _{1dB}	CW		+27		dBm
PA Stability - Output VSWR	CW No Spurious above -41.25dBm/MHz		4:1		
Output Power Range		0		21	dBm
Thermal Resistance, θ _{jc}	Junction to case		49		°C/W

Logic Truth Table

Mode	PA_EN	LNA_EN
Bypass	Low	Low
Transmit	High	Low
LNA On	Low	High
Not Used	High	High

Evaluation Board Schematic and Layout

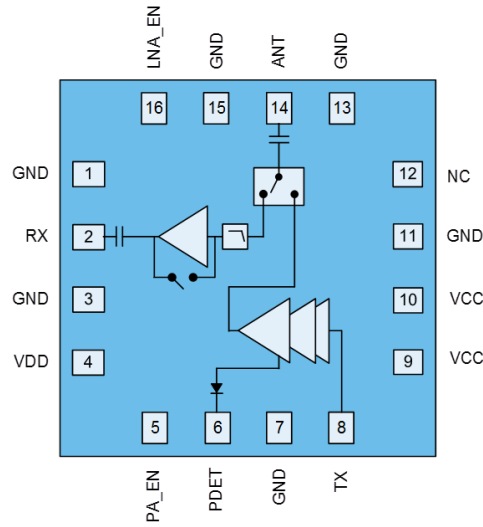
1	→ GND
2	→ VCC
3	→ PDET
4	→ PA_EN
5	→ VDD
6	→ LNA_EN
7	→ GND



Bill of Material

Ref. Des.	Value	Description	Manuf.	Part number
-	-	Printed Circuit Board		
U1	-	5GHz Wi-Fi Front End Module	Qorvo	QPF4530
C9	0.1 pF	Capacitor, Chip, +/-0.05pF, 25V, C0G, 0201	Murata	GRM0335C1ER10WA01D
C3	4.7 μF	Capacitor, Chip, 10%, 6.3V, X5R, 0603	Murata	GRM188R60J475KE19D
C6, C8	1000 pF	Capacitor, Chip, 10%, 16V, X7R, 0201		
C1	100 pF	Capacitor, Chip, 5%, 25V, C0G, 0201		
C5	10 pF	Capacitor, Chip, +/-0.05pF, 25V, C0G, 0201		
C2	150 pF	Capacitor, Chip, 10%, 16V, X7R, 0201		
R1	0 Ω	Resistor, Chip, 5%, 1/20W, 0201	Kamaya	RMC1/20JPPA15
R2	49.9 Ω	Resistor, Chip, 1%, 1/10W, 0402	Panasonic IDS	ERJ-2RKF49R9X
C7	-	Do Not Install		

Pin Configuration and Description

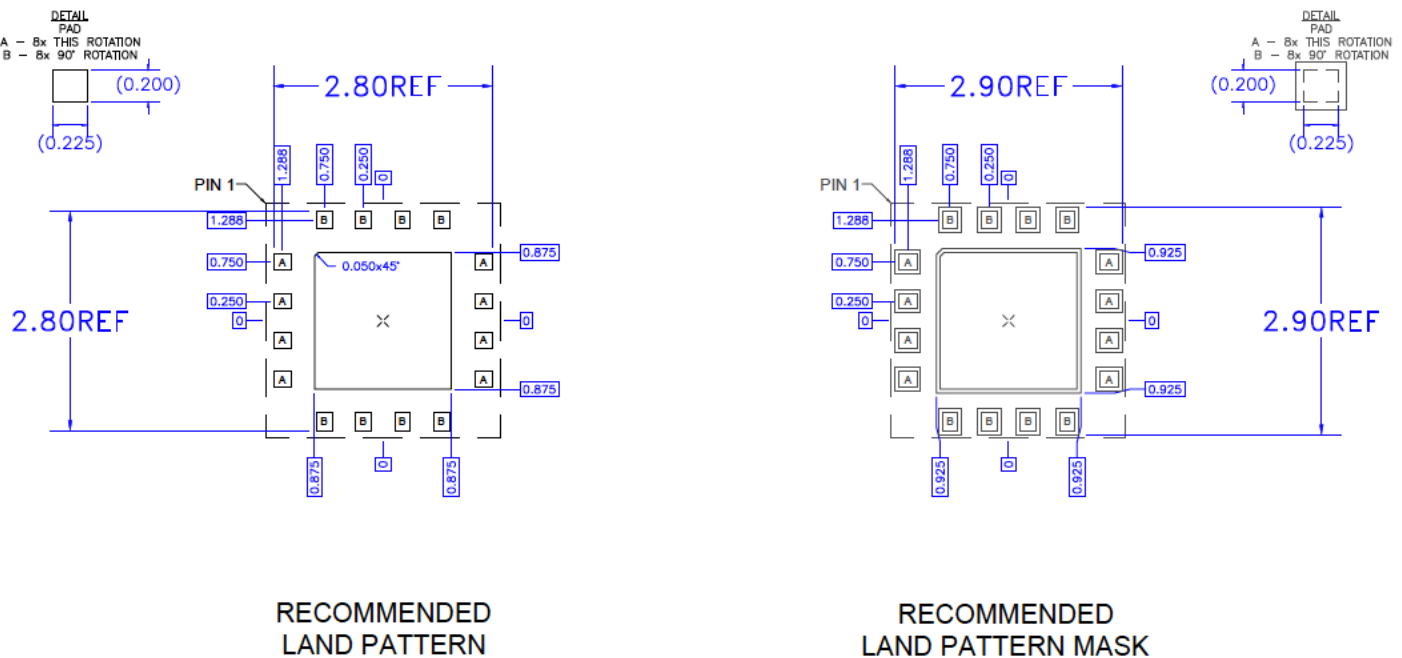
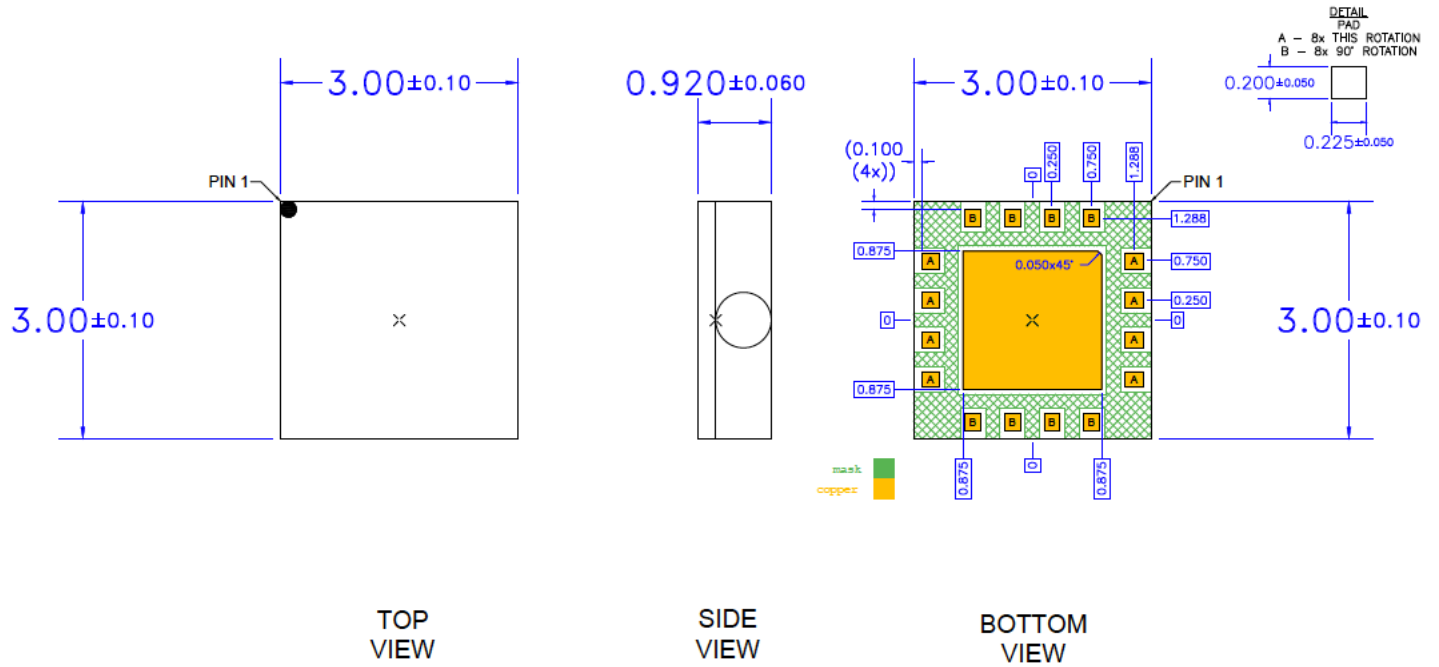


Top View

Pin Number	Label	Description
1	GND	Ground connection.
2	RX	RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked.
3	GND	Ground connection.
4	VDD	LNA & regulator supply voltage.
5	PA_EN	Control pin.
6	PDET	DC power detector. Provides an output voltage proportional to the RF output power level
7	GND	Ground connection.
8	TX	RF input. Internally matched to 50 Ω and DC shorted. No DC leakage from this pin. If DC is present on the trace to TX, then a series DC block is recommended.
9	VCC	Supply voltage
10	VCC	Supply voltage
11	GND	Ground connection.
12	NC	RF power detector. Provides an RF output proportional to the RF output power level. This pin must be terminated with 50 Ω when not used.
13	GND	Ground connection.
14	ANT	RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked.
15	GND	Ground connection.
16	LNA_EN	Control pin.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Mechanical Information

Dimensions and PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B (500V)	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3 (1kV)	JESD22-C101
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electroless Ni/Electroless Pd/Immersion Au (ENEPIG)

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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- Техническая поддержка проекта;
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