Features

September 2005

- 256 x 256 channel non-blocking switch
- Programmable frame integrity for wideband channels
- Automatic identification of ST-BUS/GCI interface backplanes
- Per channel tristate control
- Patented message mode
- Non-multiplexed microprocessor interface
- Single +5 volt supply
- Available in DIP-40, PLCC-44 and QFP-44 packages
- Pin compatible with MT8980 device

Applications

- Medium size digital switch matrices
- Hyperchannel switching (e.g., ISDN H0)
- ST-BUS/MVIP™ interface functions
- Serial bus control and monitoring
- Centralized voice processing systems
- Data multiplexer

Ordering Information

MT8985AE	40 Pin PDIP	Tubes
MT8985AP	44 Pin PLCC	Tubes
MT8985AL	44 Pin MQFP	Trays
MT8985APR	44 Pin PLCC	Tape & Reel
MT8985AP1	44 Pin PLCC*	Tubes
MT8985APR1	44 Pin PLCC*	Tape & Reel
MT8985AE1	40 Pin PDIP*	Tubes
MT8985AL1	44 Pin MQFP*	Trays

*Pb Free Matte Tin

-40°C to +85°C

Description

The MT8985 Enhanced Digital Switch device is an upgraded version of the popular MT8980D Digital Switch (DX). It is pin compatible with the MT8980D and retains all of the MT8980D's functionality. This VLSI device is designed for switching PCM-encoded voice or data, under microprocessor control, in digital exchanges, PBXs and any ST-BUS/MVIP environment. It provides simultaneous connections for up to 256 64 kb/s channels. Each of the eight serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s stream. As the main function in switching applications, the device provides per-channel selection between variable or constant throughput delays. The constant throughput delay feature allows grouped channels such as ISDN H0 to be switched through the device maintaining its sequence integrity. The MT8985 is ideal for medium sized mixed voice/data switch and voice processing applications.

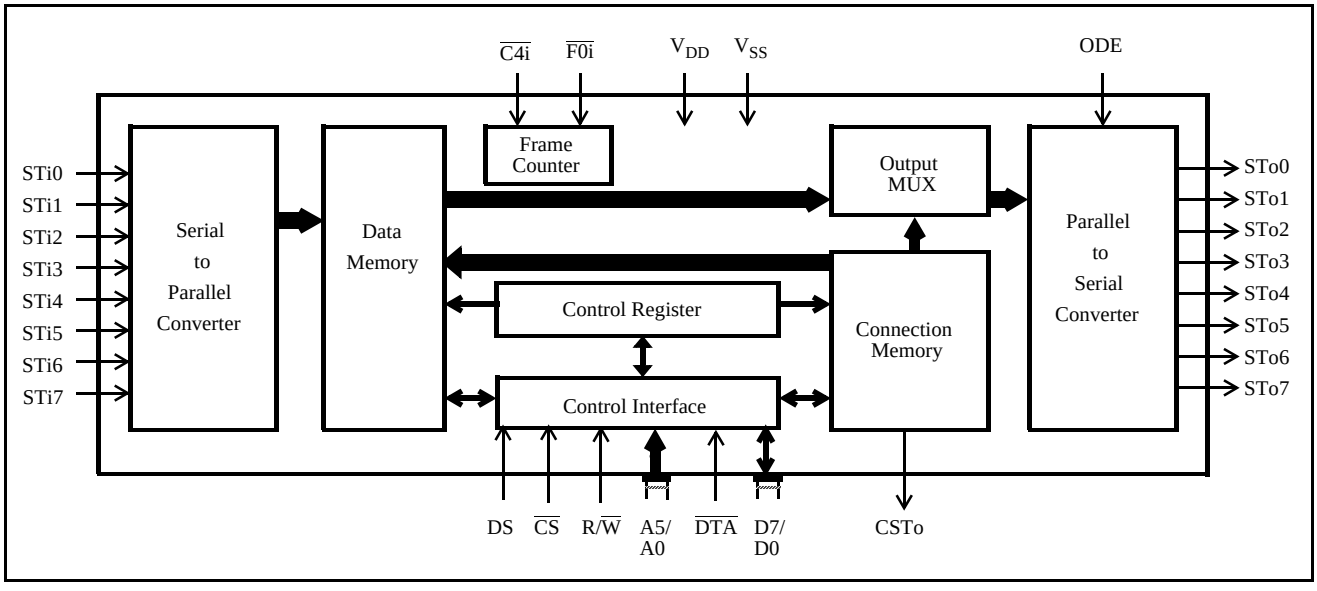


Figure 1 - Functional Block Diagram

Changes Summary

The following table captures the changes from the May 2005 issue.

Page	Item	Change
7	Figure 3 - “Address Memory Map“	• corrected Address Memory Map

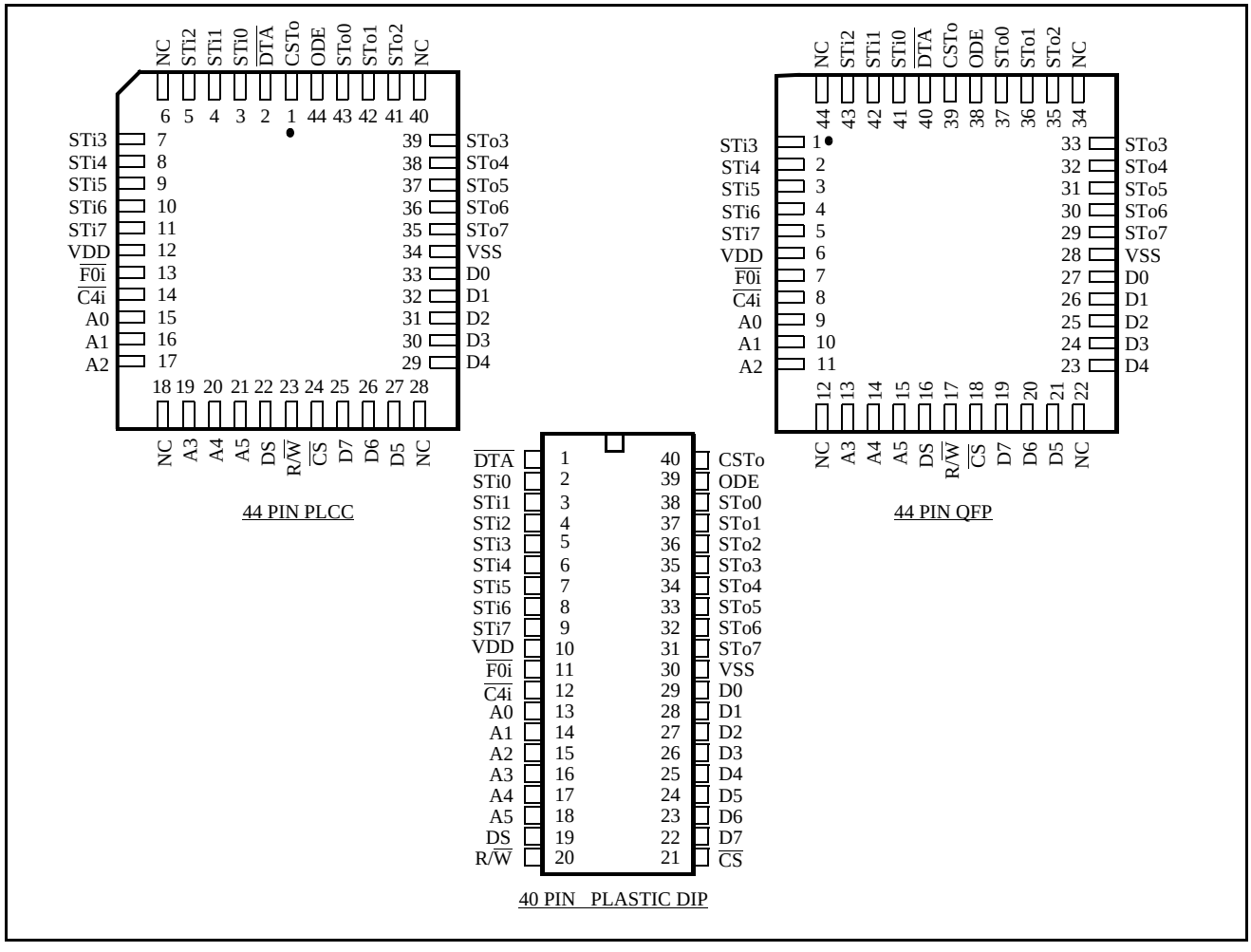


Figure 2 - Pin Connections

Pin Description

Pin #			Name	Description
40 DIP	44 PLCC	44 QFP		
1	2	40	$\overline{DTA}$	**Data Acknowledgement** (Open Drain Output). This active low output indicates that a data bus transfer is complete. A pull-up resistor is required at this output.
2-9	3-5 7-11	41-43 1-5	STi0-STi7	**ST-BUS Input 0 to 7 (Inputs).** Serial data input streams. These streams have 32 channels at data rates of 2.048 Mbit/s.
10	12	6	V_{DD}	+5 Volt Power Supply rail.
11	13	7	$\overline{F0i}$	**Frame Pulse (Input):** This input accepts and automatically identifies frame synchronization signals formatted according to different backplane specifications such as ST-BUS and GCI.
12	14	8	$\overline{C4i}$	**Clock (Input).** 4.096 MHz serial clock for shifting data in and out of the data streams.
13-18	15-17 19-21	9-11 13-15	A0-A5	**Address 0 to 5 (Inputs).** These lines provide the address to MT8985 internal registers.
19	22	16	DS	**Data Strobe (Input).** This is the input for the active high data strobe on the microprocessor interface. This input operates with $\overline{CS}$ to enable the internal read and write generation.
20	23	17	R/$\overline{W}$	**Read/Write (Input).** This input controls the direction of the data bus lines (D0-D7) during a microprocessor access.
21	24	18	$\overline{CS}$	**Chip Select (Input).** Active low input enabling a microprocessor read or write of control register or internal memories.
22-29	25-27 29-33	19-21 23-27	D7-D0	**Data Bus 7 to 0 (Bidirectional).** These pins provide microprocessor access to data in the internal control register, connect memory high, connect memory low and data memory.
30	34	28	V_{SS}	**Ground Rail.**
31-38	35-39 41-43	29-33 35-37	STo7-STo0	**ST-BUS Outputs 7 to 0 (Three-state Outputs).** Serial data output streams. These streams are composed of 32 channels at data rates of 2.048 Mbit/s.
39	44	38	ODE	**Output Drive Enable (Input).** This is an output enable for the STo0 to STo7 serial outputs. If this input is low STo0-7 are high impedance. If this input is high each channel may still be put into high impedance by software control.
40	1	39	CSTo	**Control ST-BUS Output (Output).** This output is a 2.048 Mb/s line which contains 256 bits per frame. The level of each bit is controlled by the contents of the CSTo bit in the Connect Memory high locations.
	6, 18, 28, 40	12,22 34, 44	NC	No Connection.

Functional Description

With the integration of voice, video and data services into the same network, there has been an increasing demand for systems which ensure that data at N x 64 Kbit/s rates maintain frame sequence integrity while being transported through time slot interchange circuits. Existing requirements demand time slot interchange devices performing switching with constant throughput delay while guaranteeing minimum delay for voice channels.

The MT8985 device provides both functions and allows existing systems based on the MT8980D to be easily upgraded to maintain the data integrity while multiple channel data are transported. The device is designed to switch 64 kbit/s PCM or N x 64 kbit/s data. The MT8985 can provide both frame integrity for data applications and minimum throughput switching delay for voice applications on a per channel basis.

By using Zarlink Message mode capability, the microprocessor can access input and output time slots on a per channel basis to control devices such as the Zarlink MT8972, ISDN Transceivers and T1/CEPT trunk interfaces through the ST-BUS interface. Different digital backplanes can be accepted by the MT8985 device without user's intervention. The MT8985 device provides an internal circuit that automatically identifies the polarity and format of frame synchronization input signals compatible to ST-BUS and GCI interfaces.

Device Operation

A functional block diagram of the MT8985 device is shown in Figure 1. The serial ST-BUS streams operate continuously at 2.048 Mb/s and are arranged in 125 μs wide frames each containing 32 8-bit channels. Eight input (STi0-7) and eight output (STo0-7) serial streams are provided in the MT8985 device allowing a complete 256 x 256 channel non-blocking switch matrix to be constructed. The serial interface clock for the device is 4.096 MHz, as required in ST-BUS and GCI specifications.

Data Memory

The received serial data is converted to parallel format by the on-chip serial to parallel converters and stored sequentially in a 256-position Data Memory. The sequential addressing of the Data Memory is generated by an internal counter that is reset by the input 8 kHz frame pulse ($\overline{F0i}$) marking the frame boundaries of the incoming serial data streams.

Depending on the type of information to be switched, the MT8985 device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. For voice applications, the variable delay mode can be selected ensuring minimum throughput delay between input and output data. In multiple or grouped channel data applications, the constant delay mode can be selected maintaining the integrity of the information through the switch.

Data to be output on the serial streams may come from two sources: Data Memory or Connect Memory. Locations in the Connect Memory, which is split into HIGH and LOW parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input (connection mode) or it can be originated from the microprocessor (message mode). If a channel is configured in connection mode, the source of the output data is the Data Memory. If a channel is configured in message mode, the source of the output data is the Connect Memory Low. Data destined for a particular channel on the serial output stream is read from the Data or Connect Memory Low during the previous channel time slot. This allows enough time for memory access and internal parallel to serial conversion.

Connection and Message Modes

In connection mode, the addresses of input source for all output channels are stored in the Connect memory Low. The Connect Memory Low locations are mapped to each location corresponding to an output 64 kb/s channel. The contents of the Data memory at the selected address are then transferred to the parallel to serial converters. By having the output channel to specify the input channel through the connect memory, the user can route the same input channel to several output channels, allowing broadcasting facility in the switch.

In message mode the CPU writes data to the Connect Memory Low locations which correspond to the output link and channel number. The contents of the Connect Memory Low are transferred to the parallel to serial converter one channel before it is to be output. The Connect Memory Low data is transmitted each frame to the output until it is changed by the CPU.

The per-channel functions available in the MT8985 are controlled by the Connect Memory High bits, which determine whether individual output channels are selected into specific conditions such as: message or connection mode, variable or constant throughput delay modes, output drivers enabled or in three-state condition. In addition, the Connect Memory High provides one bit to allow the user to control the state of the CSTo output pin.

If an output channel is set to three-state condition, the TDM serial stream output will be placed in high impedance during that channel time. In addition to the per-channel three-state control, all channels on the TDM outputs can be placed in high impedance at one time by pulling the ODE input pin in LOW. This overrides the individual per-channel programming on the Connect Memory High bits.

The Connect Memory data is received via the Microprocessor Interface at D0-D7 lines. The addressing of the MT8985 internal registers, Data and Connect memories is performed through address input pins and some bits of the device's Control register. The higher order address bits come from the Control register, which may be written or read through the microprocessor interface. The lower order address bits come directly from the external address line inputs. For details on the device addressing, see Software Control and Control register description.

Serial Interface Timing

The MT8985 master clock ($\overline{C4i}$) is a 4.096 MHz allowing serial data link configuration at 2.048 Mb/s to be implemented. The MT8985 frame synchronization pulse can be formatted according to ST-BUS or GCI interface specifications; i.e., the frame pulse can be active in HIGH (GCI) or LOW (ST-BUS). The MT8985 device automatically detects the presence of an input frame pulse and identifies the type of backplane present on the serial interface. Upon determining the correct interface connected to the serial port, the internal timing unit establishes the appropriate serial data bit transmit and sampling edges. In ST-BUS mode, every second falling edge of the 4.096 MHz clock marks a bit boundary and the input data is clocked in by the rising edge, three quarters of the way into the bit cell. In GCI mode, every second rising edge of the 4.096 MHz clock marks the bit boundary while data sampling is performed during the falling edge, at three quarters of the bit boundaries.

Delay through the MT8985

The transfer of information from the input serial streams to the output serial streams results in a delay through the MT8985 device. The delay through the MT8985 device varies according to the mode selected in the V/C bit of the connect memory high.

Variable Delay Mode

The delay in this mode is dependent only on the combination of source and destination channels and it is not dependent on the input and output streams. The minimum delay achievable in the MT8985 device is 3 time slots. In the MT8985 device, the information that is to be output in the same channel position as the information is input (position n), relative to frame pulse, will be output in the following frame (channel n, frame n+1). The same occurs if the input channel has to be output in the two channels succeeding (n+1 and n+2) the channel position as the information is input.

The information switched to the third timeslot after the input has entered the device (for instance, input channel 0 to output channel 3 or input channel 30 to output channel 1), is always output three channels later.

Any switching configuration that provides three or more timeslots between input and output channels, will have a throughput delay equal to the difference between the output and input channels; i.e., the throughput delay will be less than one frame. Table 1 shows the possible delays for the MT8985 device in Variable Delay mode:

Input Channel	Output Channel	Throughput Delay
n	m=n, n+1 or n+2	m-n + 32 timeslots
n	m>n+2	m-n time slots
n	m<n	32-(n-m) time slots

Table 1 - Channel Delay for the Variable Mode Delay

Constant Delay Mode

In this mode frame integrity is maintained in all switching configurations by making use of a multiple Data-Memory buffer technique where input channels written in any of the buffers during frame N will be read out during frame N+2. In the MT8985, the minimum throughput delay achievable in Constant Delay mode will be 32 time slots; for example, when input time slot 32 (channel 31) is switched to output time slot 1 (channel 0). Likewise, the maximum delay is achieved when the first time slot in a frame (channel 0) is switched to the last time slot in the frame (channel 31), resulting in 94 time slots of delay.

To summarize, any input time slot from input frame N will be always switched to the destination time slot on output frame N+2. In Constant Delay mode, the device throughput delay is calculated according to the following formula:

DELAY = [32 + (32 - IN) + (OUT - 1)];
(expressed in number of time slots)

Where: IN is the number of the input time slot (from 1 to 32).

OUT is the number of the output time slot (from 1 to 32).

Microprocessor Port

The MT8985 microprocessor port has pin compatibility with Zarlink MT8980 Digital Switch device providing a non-multiplexed bus architecture. The parallel port consists of an 8 bit parallel data bus (D0-D7), six address input lines (A0-A5) and four control lines ($\overline{CS}$, DS, R/$\overline{W}$ and $\overline{DTA}$). This parallel microport allows the access to the Control registers, Connection Memory High, Connection Memory Low and the Data Memory. All locations are read/written except for the data memory which can be read only.

Accesses from the microport to the connection memory and the data memory are multiplexed with accesses from the input and output TDM ports. This can cause variable Data Acknowledge delays ($\overline{DTA}$). In the MT8985 device, the $\overline{DTA}$ output provides a maximum acknowledgement delay of 800 ns for read/write operations in the Connection Memory. However, for operations in the Data Memory (Message Mode), the maximum acknowledgement delay can be 1220 ns.

A5	A4	A3	A2	A1	A0	LOCATION
0	0	0	0	0	0	Control Register
1	0	0	0	0	0	Channel 0
1	0	0	0	0	1	Channel 1
1	•	•	•	•	•	•
1	•	•	•	•	•	•
1	•	•	•	•	•	•
1	•	•	•	•	•	•
1	•	•	•	•	•	•
1	1	1	1	1	1	Channel 31

Figure 3 - Address Memory Map

Note: "x" Don't care

Software Control

The address lines on the microprocessor interface give access to the MT8985 internal registers and memories. If the A5,A1,A0 address line inputs are LOW, then the MT8985 Internal Control Register is addressed (see Figure 3). If A5 input line is HIGH, then the remaining address input lines are used to select Memory subsections of 32 locations corresponding to the number of channels per input or output stream. As explained in the Control register description, the address input lines and the Stream Address bits (STA) of the Control register give the user the capability of selecting all positions of the MT8985 Data and Connect memories.

The data in the Control register consists of Split memory and Message mode bits, Memory select and Stream Address bits (see Figure 4). The memory select bits allow the Connect Memory HIGH or LOW or the Data Memory to be chosen, and the Stream Address bits define an internal memory subsections corresponding to input or output ST-BUS streams. Bit 7 (Split Memory) of the Control register allows split memory operation whereby reads are from the Data memory and writes are to the Connect Memory LOW.

The Message Enable bit (bit 6) places every output channel on every output stream in message mode; i.e., the contents of the Connect Memory LOW (CML) are output on the ST-BUS output streams once every frame unless the ODE input pin is LOW. If ME bit is HIGH, then the MT8985 behaves as if bits 2 (Message Channel) and 0 (Output Enable) of every Connect Memory HIGH (CMH) locations were set to HIGH, regardless of the actual value. If ME bit is LOW, then bit 2 and 0 of each Connect Memory HIGH location operates normally. In this case, if bit 2 of the CMH is HIGH, the associated ST-BUS output channel is in Message mode. If bit 2 of the CMH is LOW, then the contents of the CML define the source information (stream and channel) of the time slot that is to be switched to an output.

If the ODE input pin is LOW, then all serial outputs are high-impedance. If ODE is HIGH, then bit 0 (Output Enable) of the CMH location enables (if HIGH) or disables (if LOW) the output drivers for the corresponding individual ST-BUS output stream and channel.

The contents of bit 1 (CSTo) of each Connection Memory High location (see Figure 5) is output on CSTo pin once every frame. The CSTo pin is a 2048 Mbit/s output which carries 256 bits. If CSTo bit is set HIGH, the corresponding bit on CSTo output is transmitted in HIGH. If CSTo bit is LOW, the corresponding bit on the CSTo output is transmitted in LOW. The contents of the 256 CSTo bits of the CMH are transmitted sequentially on to the CSTo output pin and are synchronous to the ST-BUS streams. To allow for delay in any external control circuitry the contents of the CSTo bit is output one channel before the corresponding channel on the ST-BUS streams. For example, the contents of CSTo bit in position 0 (ST0, CH0) of the CMH, is transmitted synchronously with ST-BUS channel 31, bit 7. The contents of CSTo bit in position 32 (ST1, CH0) of the CMH is transmitted during ST-BUS channel 31 bit 6. Bit V/C (Variable/Constant Delay) on the Connect Memory High locations allow per-channel selection between Variable and Constant throughput delay capabilities.

7	6	5	4	3	2	1	0
SM	ME	X	MS1	MS0	STA2	STA1	STA0

BIT	NAME	DESCRIPTION
7	SM	**Split Memory.** When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. The Memory Select bits need to be set to specify the memory for the operations. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	ME	**Message Enable.** When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when in High Impedance. When 0, the Connection Memory bits for each channel determine what is output.
4-3	MS1-MS0	**Memory Select Bits.** The memory select bits operate as follows: 0-0 - Not to be used 0-1 - Data Memory (read only from the CPU) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2-0	STA2-0	**Stream Address Bits 2-0.** The number expressed in binary notation on these bits refers to the input or output ST-BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 4 - Control Register Bits

x = Don’t care

Initialization of the MT8985

On initialization or power up, the contents of the Connection Memory High can be in any state. This is a potentially hazardous condition when multiple MT8985 ST-BUS outputs are tied together to form matrices, as these outputs may conflict. The ODE pin should be held low on power up to keep all outputs in the high impedance condition.

7	6	5	4	3	2	1	0
X	$\overline{V}$/C	X	X	X	MC	CSTo	OE

BIT	NAME	DESCRIPTION
6	$\overline{V}$/C	**Variable/Constant Throughput Delay Mode.** This bit is used to select between Variable (LOW) and Constant Delay (HIGH) modes on a per-channel basis.
2	MC	**Message Channel.** When 1, the contents of the corresponding location in Connection Memory Low are output on the corresponding channel and stream. When 0, the contents of the programmed location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	CSTo	**CSTo Bit.** This bit drives a bit time on the CSTo output pin.
0	OE	**Output Enable.** This bit enables the output drivers on a per-channel basis. This allows individual channels on individual streams to be made high-impedance, allowing switch matrices to be constructed. A HIGH enables the driver and a LOW disables it.

Figure 5 - Connection Memory High Bits

x = Don't care

7	6	5	4	3	2	1	0
SAB2	SAB1	SAB0	CAB4	CAB3	CAB2	CAB1	CAB0

BIT	NAME	DESCRIPTION
7-5	SAB2-0*	**Source Stream Address bits.** These three bits are used to select eight source streams for the connection. Bit 7 of each word is the most significant bit.
4-0*	CAB4-0*	**Source Channel Address bits 0-4.** These five bits are used to select 32 different source channels for the connection (The ST-BUS stream where the channel is present is defined by bits SAB2-0). Bit 4 is the most significant bit.
*	If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.	

Figure 6 - Connection Memory Low Bits

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the matrices, and put all other channels into the high impedance state. Care should be taken that no two connected ST-BUS outputs drive the bus simultaneously. When this process is complete, the microprocessor controlling the matrices can bring the ODE signal high to relinquish high impedance state control to the CMH_b0s.

Applications

Typical Exchange, PBX or Multiplexer

Figure 7 shows a typical implementation of line cards being interconnected through a central routing matrix that can scale up in channel capacity to accommodate different number of ports depending on the application. In a configuration where the switched services utilize concatenated or grouped time slots to carry voice, data and video (channels of 128, 256 Kb/s, ISDN H0 and others), the central routing matrix has to guarantee constant throughput delay to maintain the sequence integrity between input and output channels. Figure 7 shows an example where the MT8985 device guarantees data integrity when data flows from the T1/E1 to the S/U interface links and vice-versa. Modern technologies available today such as Frame Relay network using dedicated fractional T1 are one of the key applications for the MT8985 device.

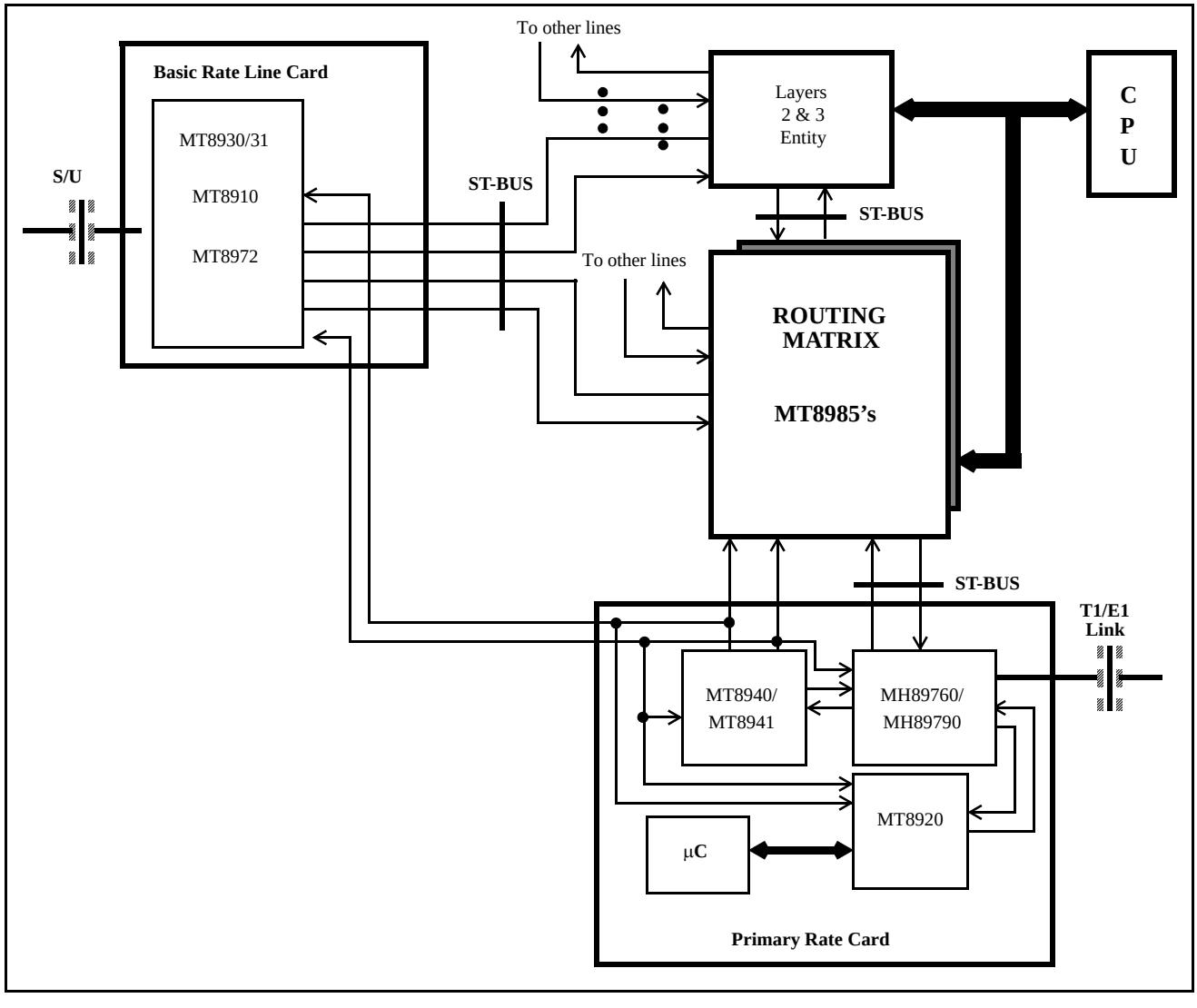


Figure 7 - Typical Exchange, PBX or Multiplexer Configuration

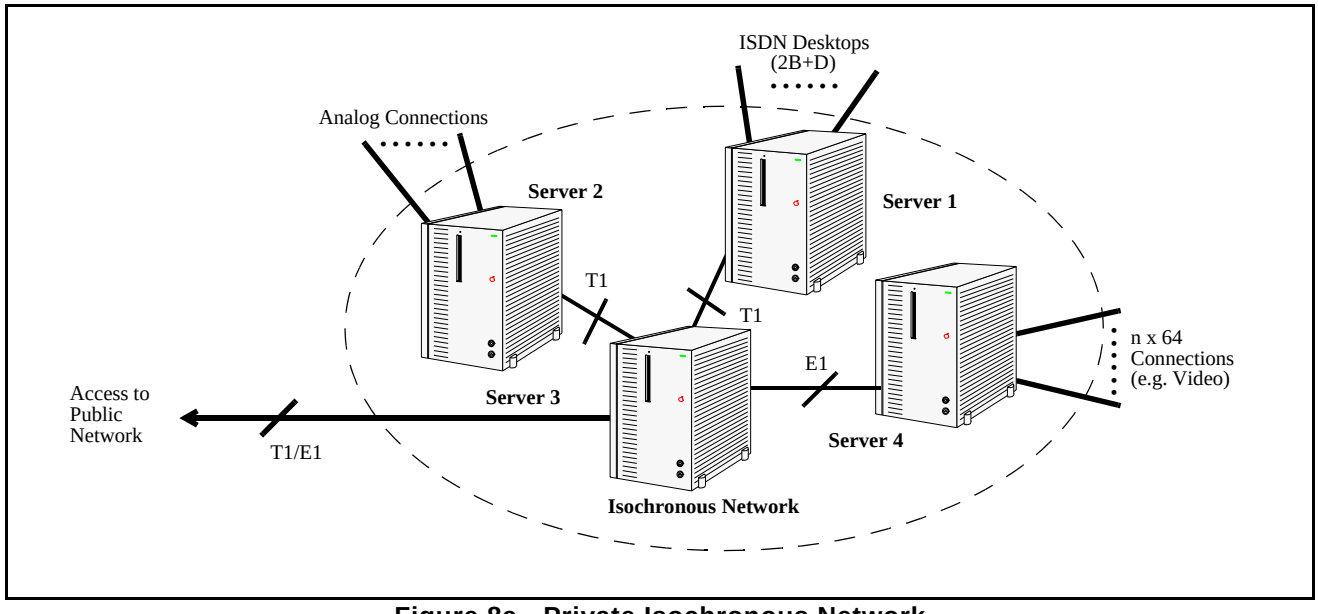


Figure 8a - Private Isochronous Network

Low Latency Isochronous Network

In today's local working group environment, there is an increasing demand for solutions on interconnection of desktop and telephone systems so that mixed voice, data and video services can be grouped together in a reliable network allowing the deployment of multimedia services. Existing multimedia applications require a network with predictable data transfer delays that can be implemented at a reasonable cost. The Low Latency Isochronous Network is one of the alternatives that system designers have chosen to accommodate this requirement (see Figure 8a). This network can be implemented using existing TDM transmission media devices such as ISDN Basic (S or U) and Primary rates trunks (T1 and CEPT) to transport mixed voice and data signals in grouped time slots; for example, 2B channels in case of ISDN S or U interfaces or up to 32 channels in case of a CEPT link.

Figure 8b shows a more detailed configuration whereby several PCs are connected to form an Isochronous network. Several services can be interconnected within a single PC chassis through the standardized Multi Vendor Integration Protocol (MVIP). Such an interface allows the distribution and interconnection of services like voice mail, integrated voice response, voice recognition, LAN gateways, key systems, fax servers, video cards, etc.

The information being exchanged between cards through the MVIP interface on every computer as well as between computers through T1 or CEPT links is, in general, of mixed type where 64Kb/s and N*64Kb/s channels are grouped together. When such a mixed type of data is transferred between cards within one chassis or from one computer to another, the sequence integrity of the concatenated channels has to be maintained. The MT8985 device suits this application and can be used to form a complete non-blocking switch matrix of 512 channels (see Figure 9). This allows 8 pairs of ST-BUS streams to be dedicated to the MVIP side whereas the remaining 8 pairs are used for local ancillary functions in typical dual T1/E1 interface applications (Figure 10).

Another application of the MT8985 in an MVIP environment is to build an ISDN S-interface card (Figure 11). In this card, 7 pairs of ST-BUS streams are connected to the MVIP interface while the remaining pair is reserved for the interconnection of Zarlink MT8930 (SNIC), MT8992 (H-PHONE) and the MVIP interface.

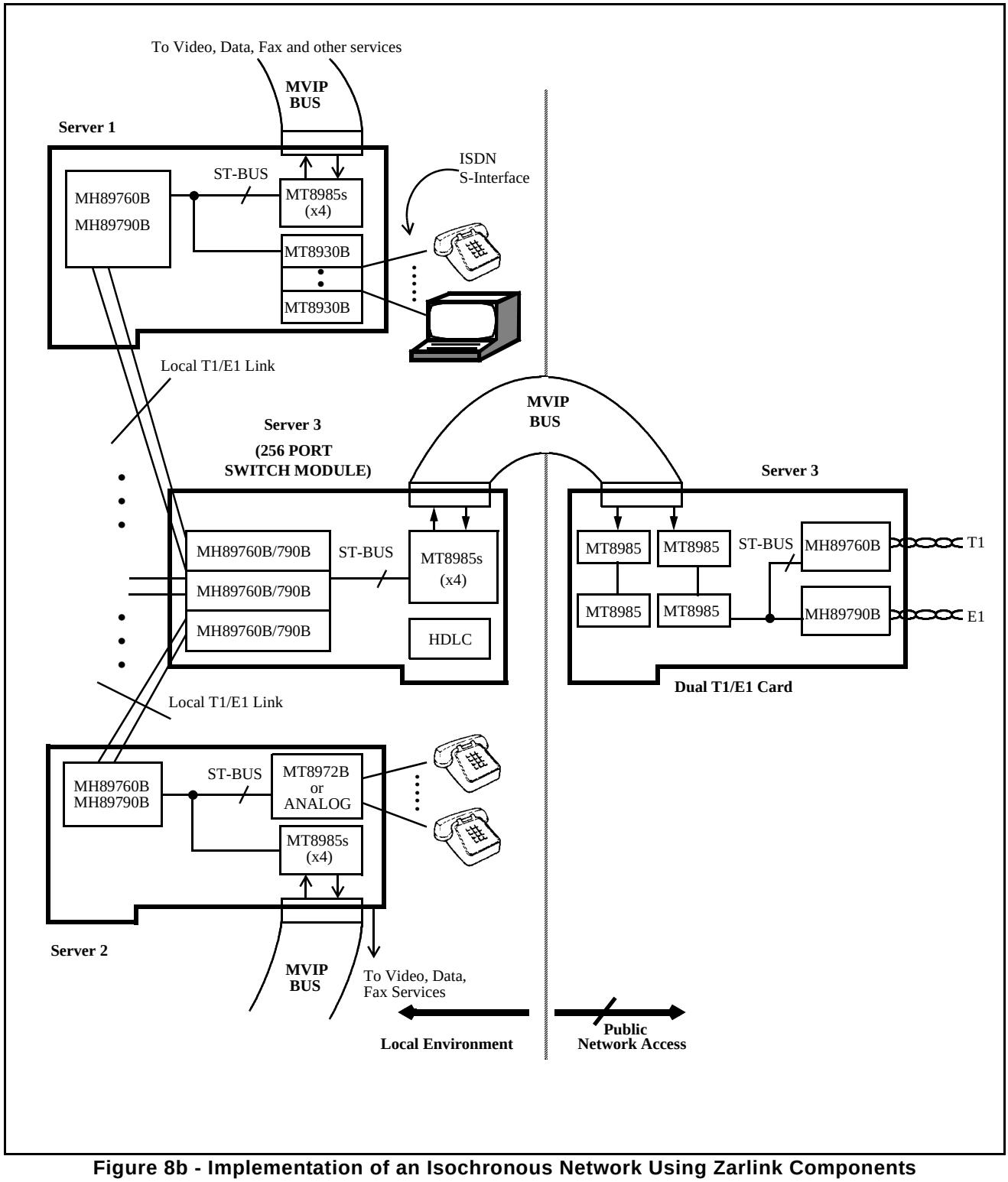


Figure 8b - Implementation of an Isochronous Network Using Zarlink Components

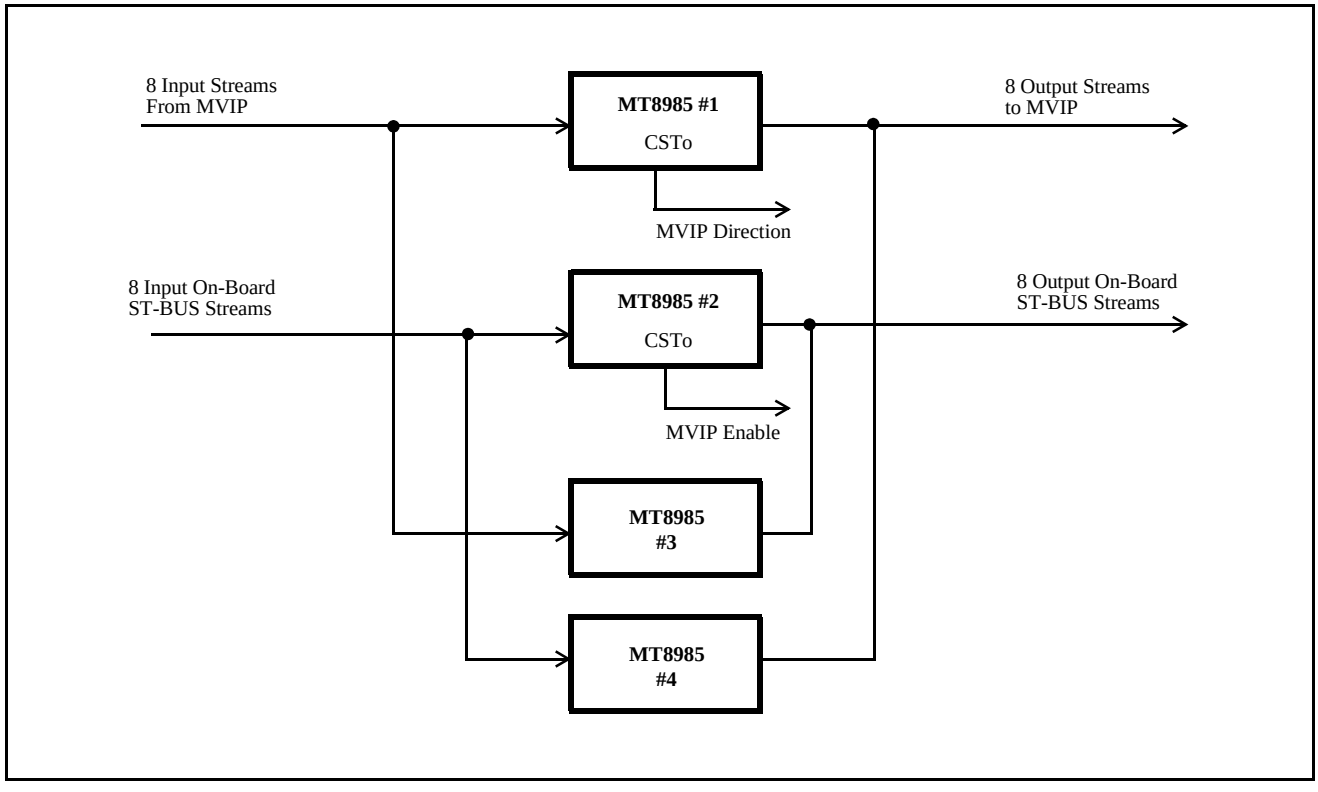


Figure 9 - 512-Channel Switch Array

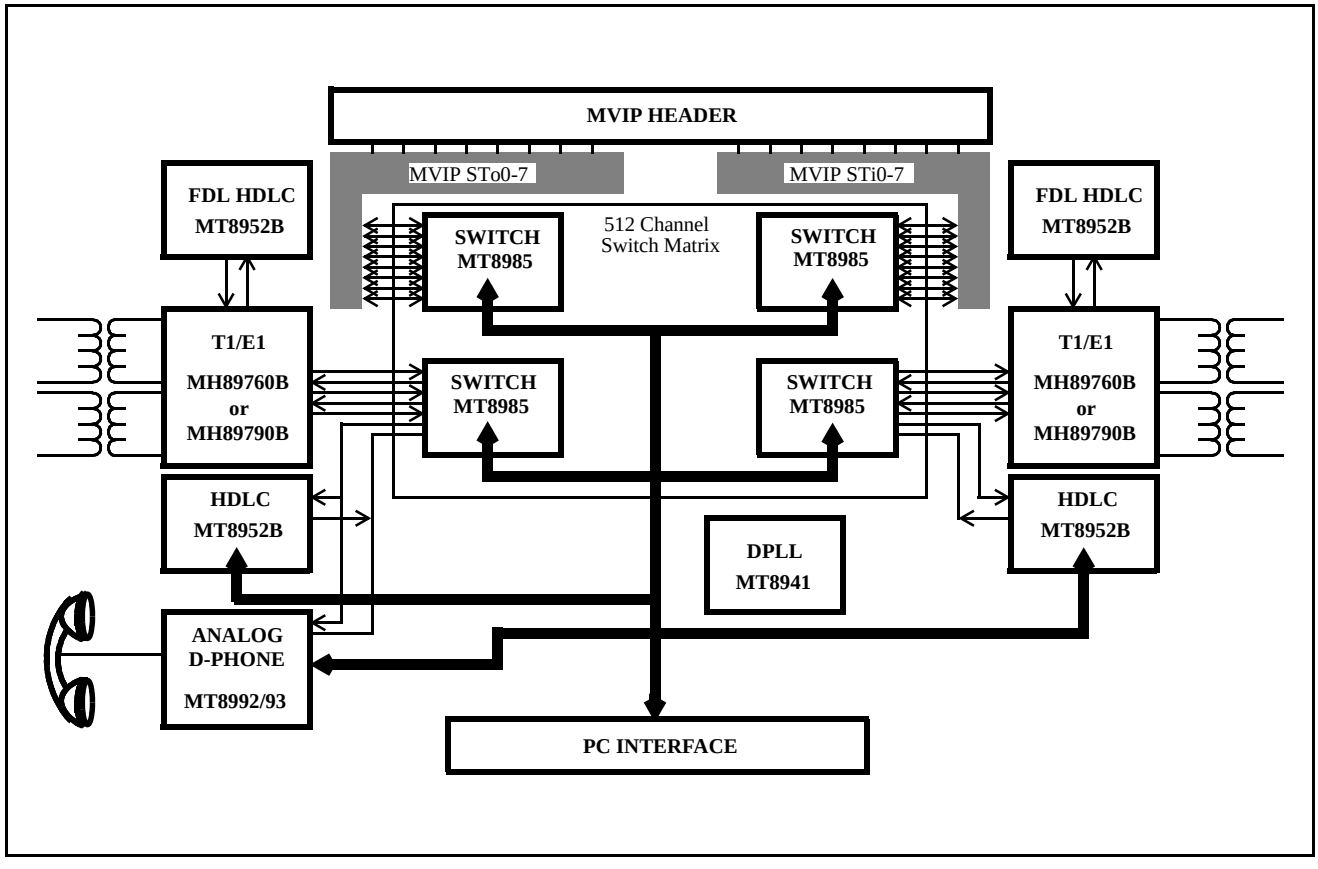


Figure 10 - Dual T1/E1 Card Functional Block Diagram

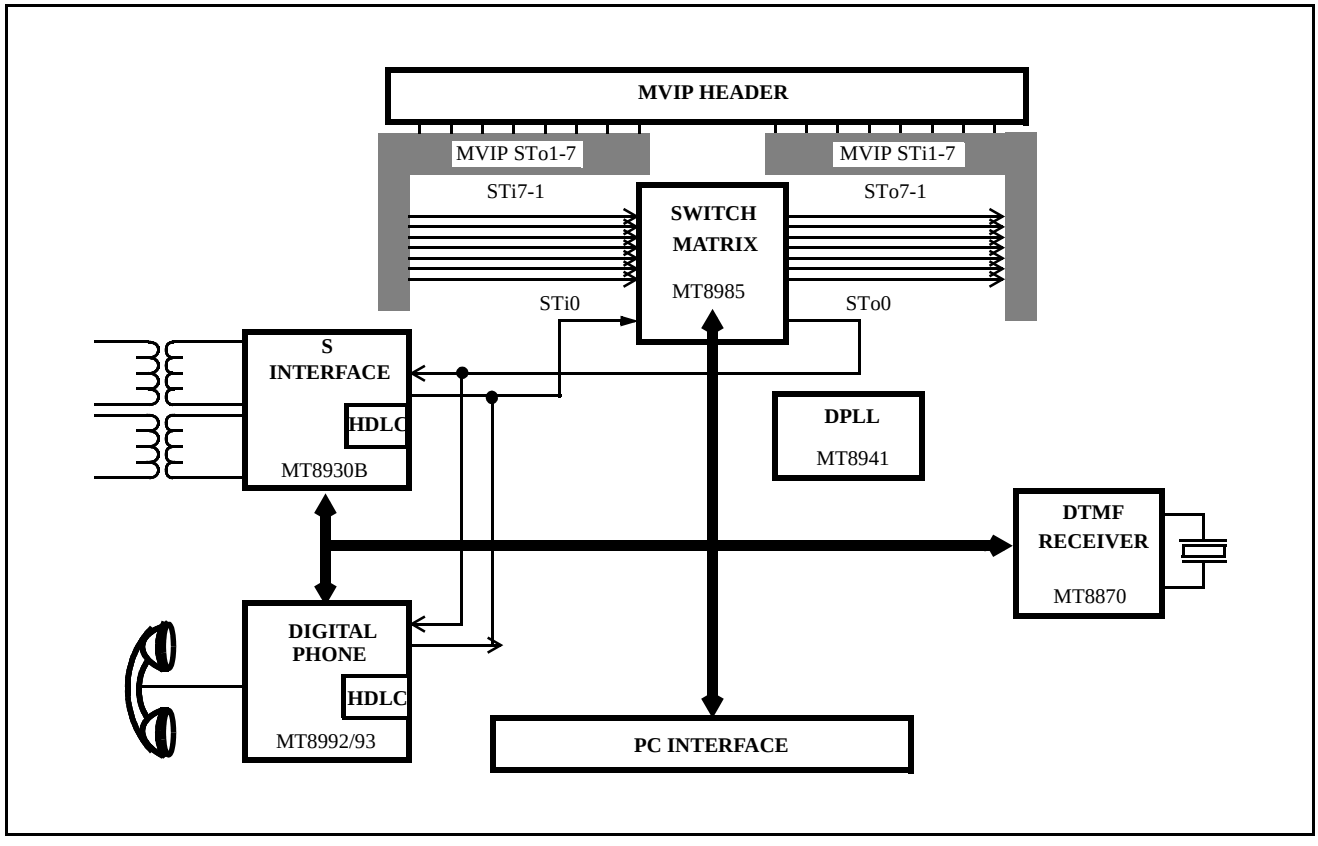


Figure 11 - S-Access Card Functional Block Diagram

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	V_{DD} - V_{SS}		-0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS}-0.3	V_{DD}+0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40	25	+85	°C	
2	Positive Supply	V_{DD}	4.75	5.0	5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Supply Current	I_{DD}		10	15	mA	Outputs unloaded
2		Input High Voltage	V_{IH}	2.0			V	
3		Input Low Voltage	V_{IL}			0.8	V	
4		Input Leakage (input pins) Input Leakage (I/O pins)	I_{IL}		 34	5 100	mA	V_I between V_{SS} and V_{DD}
5		Input Pin Capacitance	C_I		8		pF	
6	OUTPUTS	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10 mA
7		Output High Current	I_{OH}	10	15		mA	Sourcing. V_{OH}=2.4V
8		Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9		Output Low Current	I_{OL}	5	10		mA	Sinking. V_{OL} = 0.4V
10		High Impedance Leakage	I_{OZ}			5	mA	V_O between V_{SS} and V_{DD}
11		Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

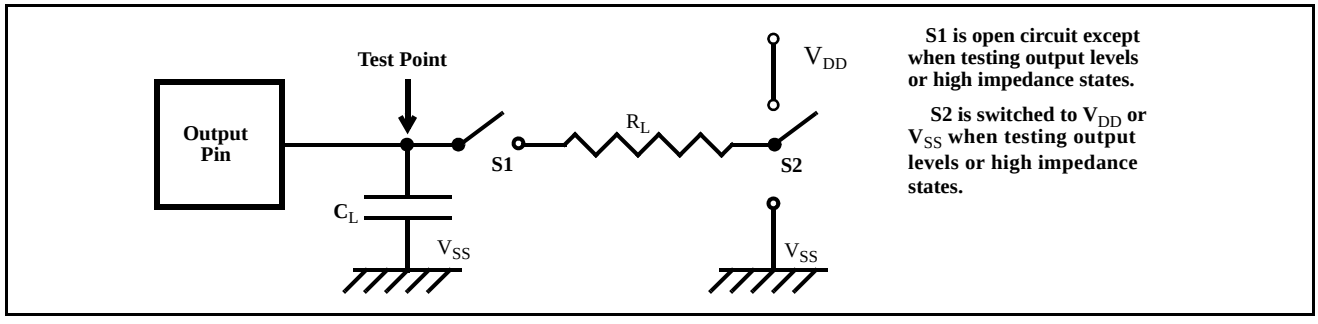


Figure 12 - Output Test Load

AC Electrical Characteristics† **- ST-BUS Timing -** Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Frame Pulse width	t_{F0iW}		244		ns	
2	Frame Pulse setup time	t_{F0iS}	10		190	ns	
3	Frame Pulse hold time	t_{F0iH}	20		190	ns	
4	STo delay Active to Active	t_{DAA}		45	100	ns	C_L=150 pF
5	STi setup time	t_{STiS}	20			ns	
6	STi hold time	t_{STiH}	20			ns	
7	Clock period	t_{C4i}	200	244	300	ns	
8	CK Input Low	t_{CL}	85	122	150	ns	
9	CK Input High	t_{CH}	85	122	150	ns	
10	Clock Rise/Fall Time	t_r, t_f			10	ns	

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

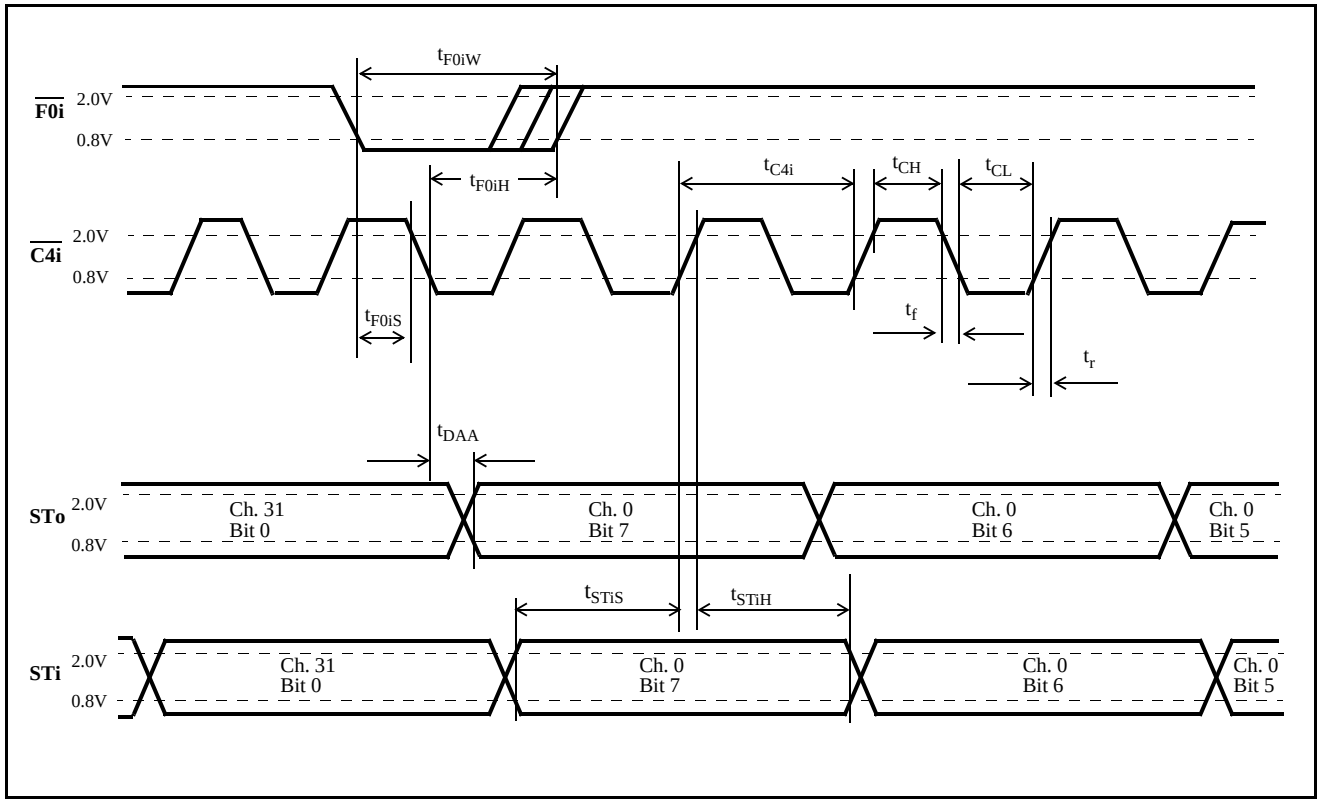


Figure 13 - ST-BUS Timing

AC Electrical Characteristics† - GCI Timing

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Clock Period	t_{C4i}	150	244	300	ns	
2	Pulse Width	t_{CL}, t_{CH}	73	122	150	ns	
3	Frame Width High	t_{WFH}		244		ns	
4	Frame Setup	t_{F0iS}	10		190	ns	
5	Frame Hold	t_{F0iH}	20		190	ns	
6	Data Delay/Clock Active to Active	t_{DAA}		45	100	ns	C_L=150 pF
7	Serial Input Setup	t_{STiS}	20			ns	
8	Serial Input Hold	t_{STiH}	20			ns	
9	Clock Rise/Fall Time	t_r,t_f			10	ns	

† Timing is over recommended temperature & power supply voltages (V_{DD}=5V±5%, V_{SS}=0V, T_A=–40 to 85°C).
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

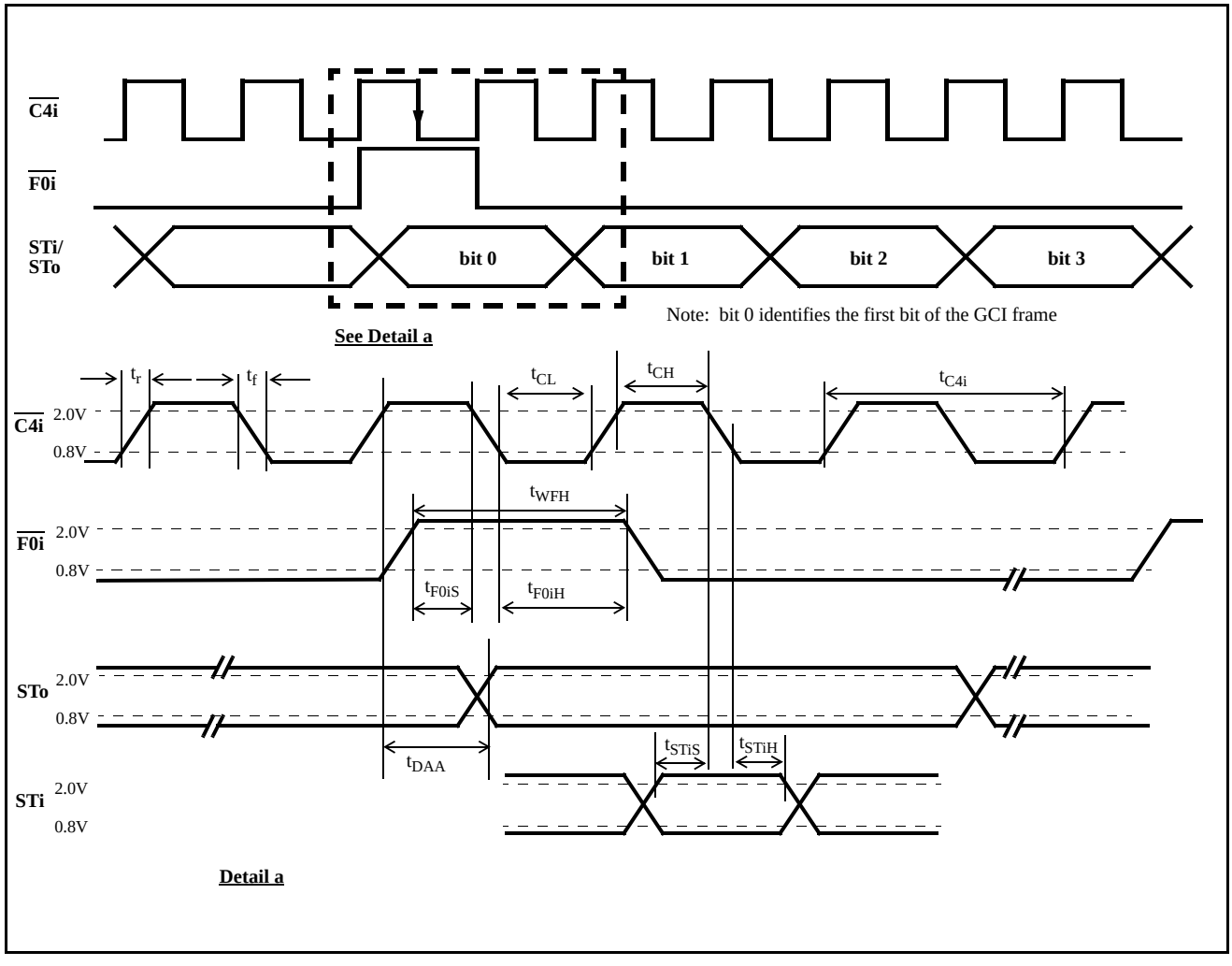


Figure 14 - GCI Timing

AC Electrical Characteristics† - Serial Streams for ST-BUS and GCI Backplanes

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	OUTPUTS	STo0/7 Delay - Active to High Z	t_{SAZ}			100	ns	R_L=1 KΩ*, C_L=150 pF
2		STo0/7 Delay - High Z to Active	t_{SZA}			100	ns	C_L=150 pF
3		Output Driver Enable Delay	t_{OED}			65	ns	R_L=1 KΩ*, C_L=150 pF
4		CSTo Output Delay	t_{XCD}	0		60	ns	C_L=150 pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

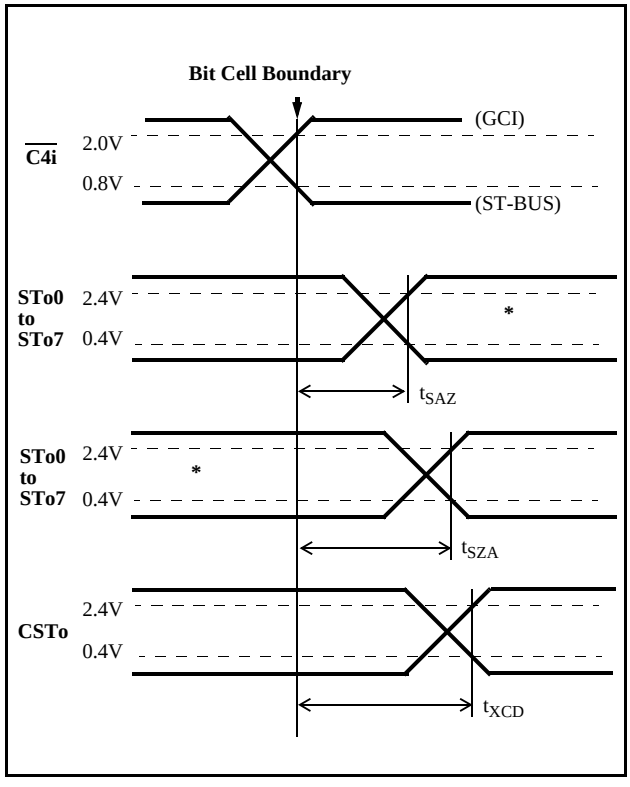


Figure 15 - Serial Outputs and External Control

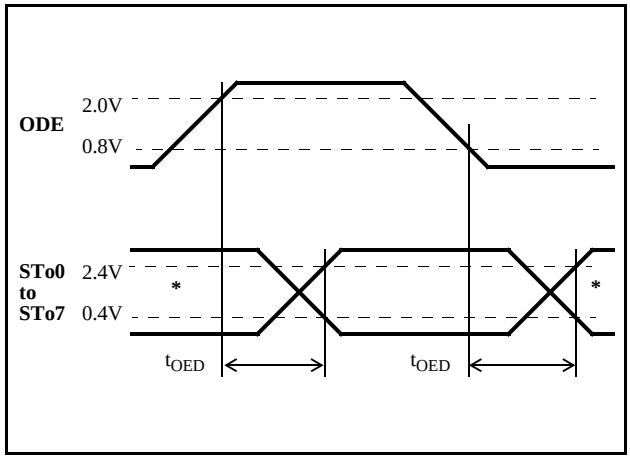


Figure 16 - Output Driver Enable

AC Electrical Characteristics† - Microprocessor Bus

Voltages are with respect to ground (VSS) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	$\overline{CS}$ Setup from DS rising	t_{CSS}	0			ns	
2	R/$\overline{W}$ Setup from DS rising	t_{RWS}	30			ns	
3	Add setup from DS rising	t_{ADS}	5			ns	
4	$\overline{CS}$ hold after DS falling	t_{CSH}	0			ns	
5	R/$\overline{W}$ hold after DS falling	t_{RWH}	5			ns	
6	Add hold after DS falling	t_{ADH}	5			ns	
7	Data setup from $\overline{DTA}$ Low on Read	t_{DDR}	10			ns	C_L=150 pF
8	Data hold on read	t_{DHR}	10	50	90	ns	R_L=1 KΩ*, C_L=150 pF
9	Data setup on write (fast write)	t_{DSW}	20			ns	
10	Valid Data Delay on write (slow write)	t_{SWD}			122	ns	
11	Data hold on write	t_{DHW}	8			ns	
12	Acknowledgement Delay: Reading Data Memory Reading/Writing Conn. Memory Writing to Control Register Reading Control Register	t_{AKD}		 560 300/370 47 70	 1220 730/800 95 155	 ns ns ns ns	C_L=150 pF
13	Acknowledgement Hold Time	t_{AKH}	10	60	110	ns	R_L=1 KΩ*, C_L=150 pF

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

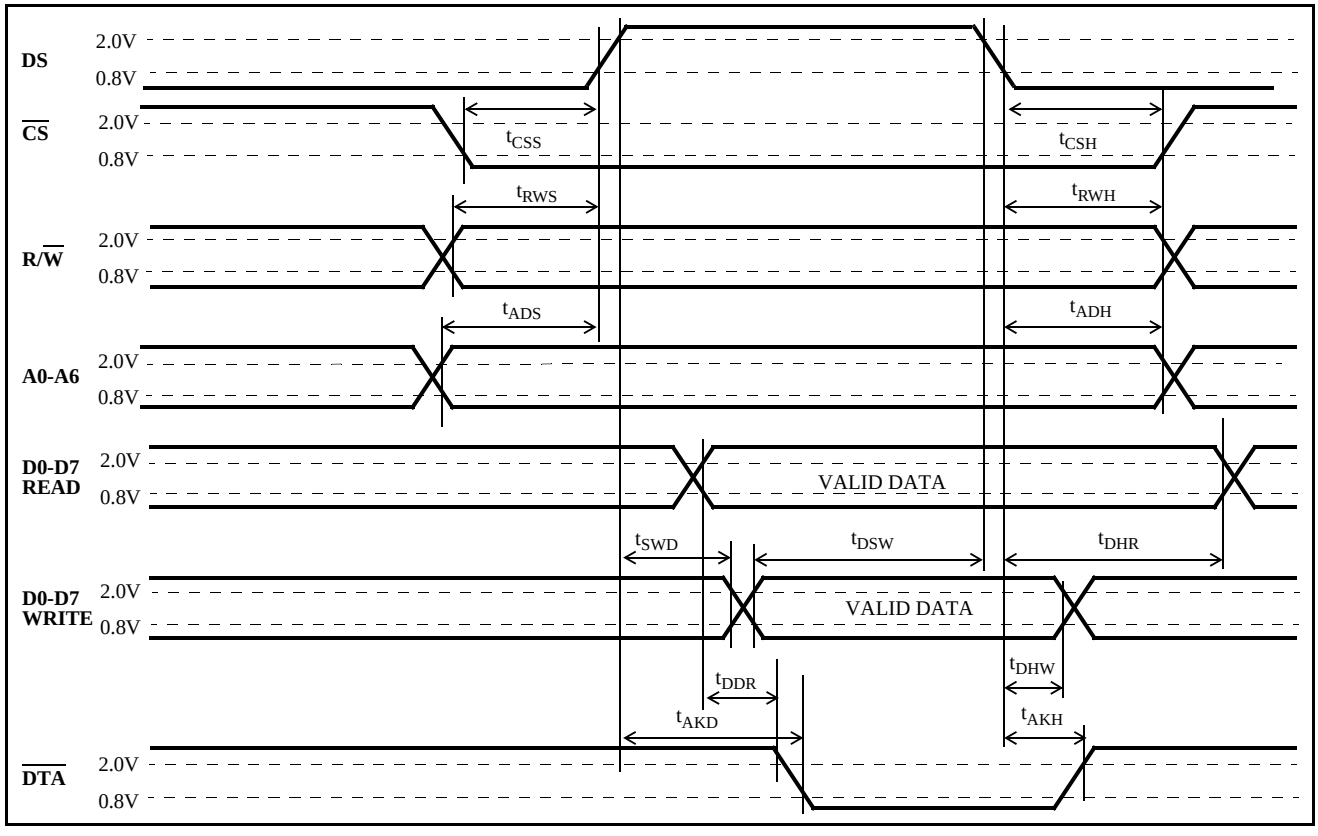
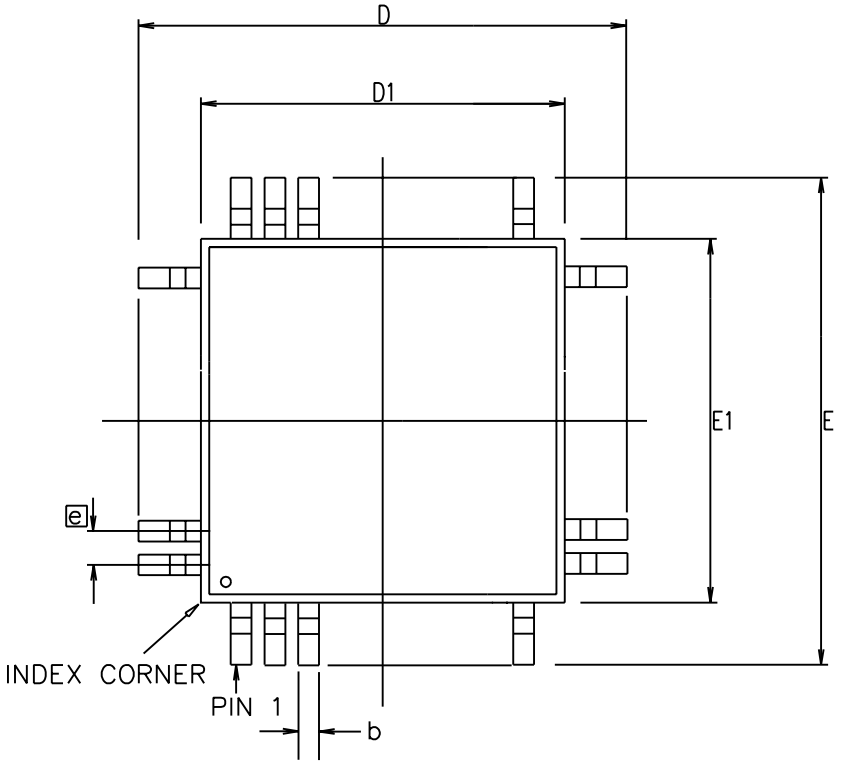
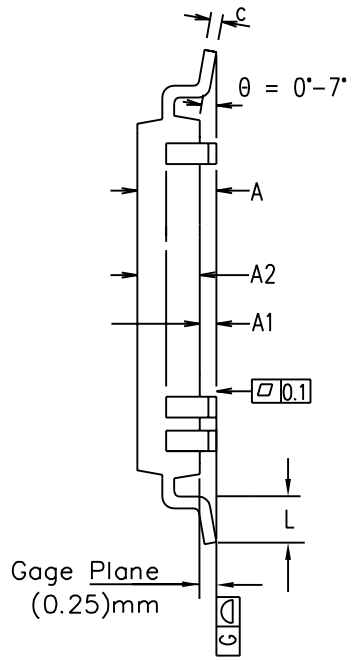


Figure 17 - Motorola Non-Multiplexed Bus Timing





Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	–	2.45		–	0.096
A1	0.25	–		0.010	–
A2	1.95	2.10		0.077	0.083
D	13.90 BSC			0.547 BSC	
D1	10.00 BSC			0.394 BSC	
E	13.90 BSC			0.547 BSC	
E1	10.00 BSC			0.394 BSC	
L	0.73	1.03		0.029	0.041
e	0.80 BSC.			0.031 BSC.	
b	0.30	0.45		0.012	0.018
c	0.11	0.23		0.004	0.009
	Pin features				
N	44				
ND	11				
NE	11				
NOTE	SQUARE				

Conforms to JEDEC MO–112 AA–1 Iss. B

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar prorusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/011 issue 15 (Swindon)

ISSUE	3	4	5	6
ACN	203205	204755	207046	212835
DATE	16Oct97	23Jun98	29Jun99	21May02
APPRD.				

ZARLINK SEMICONDUCTOR

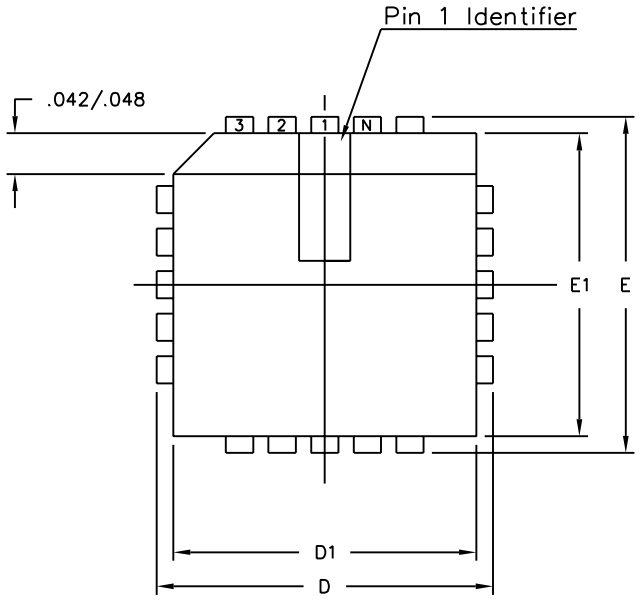
Previous package codes

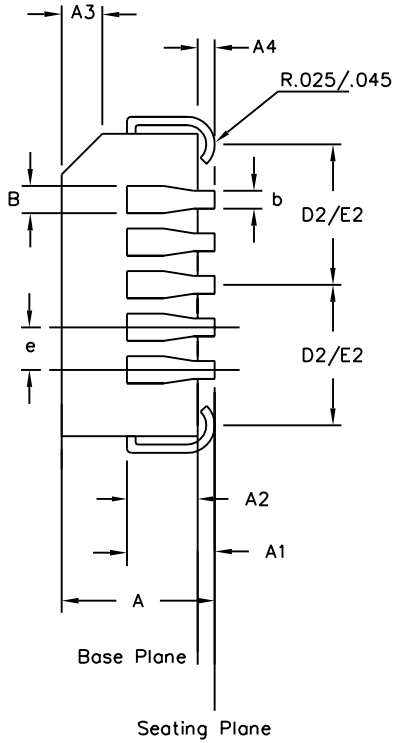
GP / L

Package Code QB

Package Outline for 44 lead MQFP (10 x 10 x 2.0mm) 3.9mm Footprint

GPD00234





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207470	213094	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

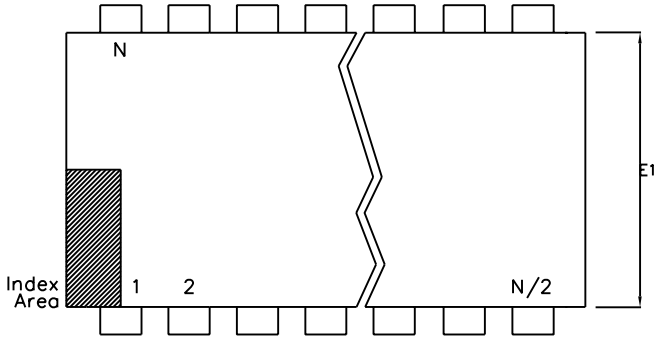
Previous package codes

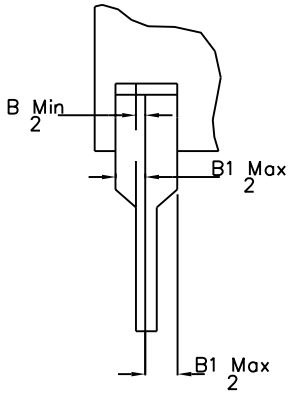
HP / P

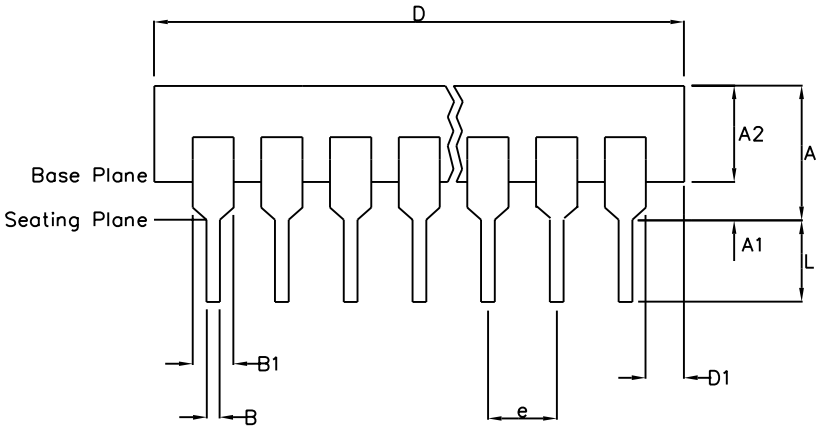
Package Code QA

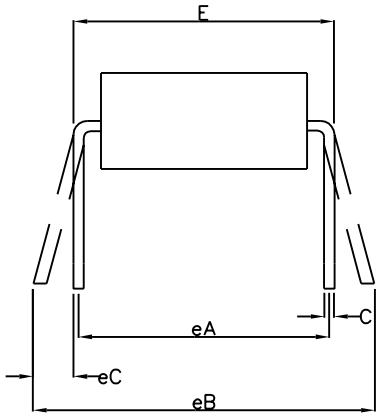
Package Outline for 44 lead PLCC

GPD00003









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jedec MS-011AC ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203533	213103	
DATE	20Apr95	25Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package Code DA

Package Outline for 40 lead PDIP

GPD00073

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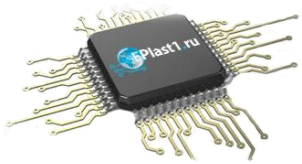
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.