Dual-Output, 3-A, Quiet Supply™ with Integrated DC-DC Converter and Low-Noise LDO

Check for Samples: TPS54122

FEATURES

- **Low-Noise Output: 17 μV_{RMS} at 10 Hz to 1 MHz**
- **Provides Two Configurable Supply Rails**
- **Wide Input Voltage Range: 2.95 V to 5.5 V**
- **Output Voltage Adjustable from 0.8 V to 3.6 V**
- **1% Overall Accuracy**
- **Excellent Load and Line Transient Response**
- **Sync to External Clock: 300 kHz to 2 MHz**
- **Small Package: 3,5-mm × 5,5-mm QFN-24**

APPLICATIONS

- **Telecom Infrastructure**
- **Pico and Femto Base Stations**
- **Powering Sensitive Clocking-Distribution Circuits**
- **Test and Measurement**
- **Powering RF Components: VCOs, Receivers, ADCs**
- **Professional Audio**

DESCRIPTION

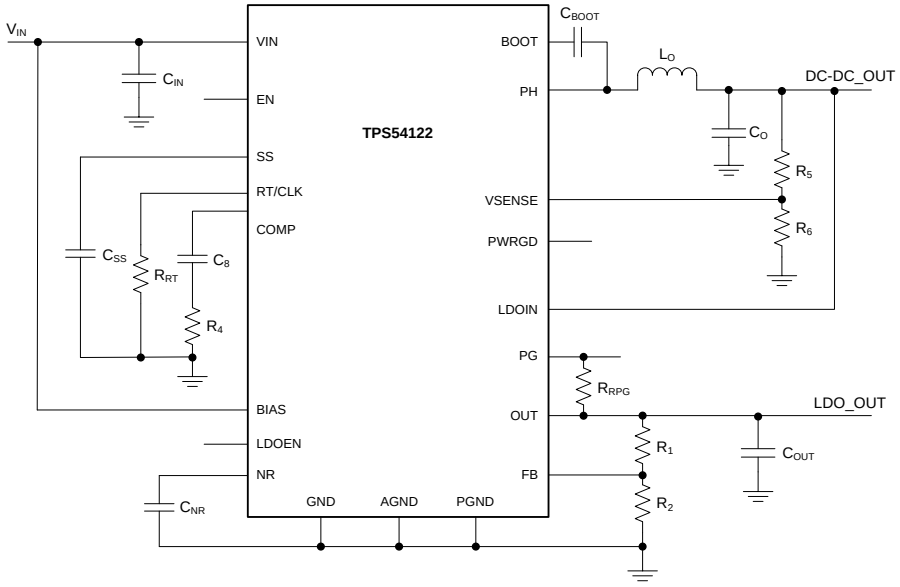
The TPS54122 combines the efficiency of a step-down switching (dc-dc) converter with a high power-supply rejection (PSR), low-noise, low-dropout regulator (LDO) to provide an ultralow-noise power supply that delivers Quiet Supply rails to noise-sensitive applications.

With a wide input range of 2.9 V to 5.5 V, the TPS54122 is ideally suited for systems with 5-V power busses, and supports a 3-A continuous output current. The output voltage can be set from 0.8 V to 3.6 V using external resistors. The TPS54122 can be used in a wide range of low-noise applications because the dc-dc converter and LDO are completely configurable. In addition, the TPS54122 includes features such as soft-start, switching frequency synchronization, and a power-good signal.

The TPS54122 can also be configured as a dual supply rail device, supplying a total of 3 A.

The TPS54122 is available in a space-saving, 3,5-mm × 5,5-mm QFN package, and is specified to operate over a –40°C to +125°C junction temperature range.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	VIN, EN, PWRGD	–0.3	7	V
	PH	–0.6	7	V
	PH (10ns transient)	–2	10	V
	BOOT	–0.3	PH + 7	V
	BOOT – PH	0	7	V
	LDOIN, LDOEN, BIAS, PG, NR, FB, RT/CLK	–0.3	6	V
	OUT	–0.3	V_{LDOIN} + 0.3	V
	VSENSE, COMP, SS	–0.3	3	V
Current	OUT	Internally limited		A
	RT/CLK, EN, SS	±100		µA
	PH	Internally limited		A
	PVIN	Internally limited		A
	COMP	±100		µA
	PWRGD (sinking)	–0.1	10	mA
Temperature	Operating junction, T_J	–40	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge ratings	Human body model (HBM)		1	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS54122 RHL (QFN) 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	34.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	39.0	
θ_{JB}	Junction-to-board thermal resistance	13.5	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	13.6	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	1.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_J = –40°C to +125°C, $V_{(BIAS)}$ = $V_{(VIN)}$ = 5 V, $V_{(LDOIN)}$ = DC-DC_OUT[1] = 2.1 V, $V_{(LDOEN)}$ = 1.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS54122 MIN	TPS54122 TYP	TPS54122 MAX	UNIT
POWER SUPPLY (VIN PIN)						
$V_{(VIN)}$	VIN pin input voltage range		2.95		6	V
	UVLO threshold			2.6	2.8	V
$I_{SD(VIN)}$	VIN pin shutdown current	$V_{(EN)}$ < 0.3 V		2		µA
$I_{(OP)}$	VIN pin operating current (no switching)	$V_{(VSENSE)}$ = 900 mV		360	575	µA
DC-DC BOOT (BOOT PIN)						
	(V_{BOOT} – V_{PH}) UVLO			2.2		V
	Boot charge resistance	$V_{(EN)}$ = 3 V		16		Ω
DC-DC CONVERTER ENABLE (EN PIN)						
$V_{IL(EN)}$	EN pin low-level input voltage	Falling		1.18		V
$V_{IH(EN)}$	EN pin high-level input voltage	Rising		1.25		V
$I_{(EN)}$	EN pin input current	$V_{(EN)}$ = 1.13 V		1.2		µA
		$V_{(EN)}$ = 1.3 V		4.6		µA
DC-DC CONVERTER VOLTAGE REFERENCE						
V_{ref}	Reference voltage	2.95 V ≤ $V_{(VIN)}$ ≤ 6 V	0.802	0.827	0.852	V
DC-DC MOSFET						
R_{HS}	High-side switch resistance	$V_{(BOOT)}$ – $V_{(PH)}$ = 5 V		45	81	mΩ
		$V_{(BOOT)}$ – $V_{(PH)}$ = 2.95 V		64	110	mΩ
R_{LS}	Low-side switch resistance	$V_{(VIN)}$ = 5 V		42	81	mΩ
		$V_{(VIN)}$ = 2.95 V		59	110	mΩ
DC-DC ERROR AMPLIFIER						
	Input current	$V_{(EN)}$ = 3 V		7		nA
g_M	Error amplifier transconductance	–2 µA ≤ $I_{(COMP)}$ ≤ 2 µA, $V_{(COMP)}$ = 1 V		245		µMho
	Error amplifier transconductance during slow-start operation	–2 µA ≤ $I_{(COMP)}$ ≤ 2 µA, $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		79		µMho
$I_{(COMP)}$	Error amplifier output current	$V_{(COMP)}$ = 1 V, 100-mV input overdrive		±20		µA
	COMP pin to I_{SWITCH} g_M			18		A/V
DC-DC CURRENT LIMIT						
	High-side current limit	$V_{(VIN)}$ = 3 V	4.2	6.6		A
DC-DC SOFT-START (SS PIN)						
	SS pin charge current	$V_{(SS)}$ = 0.4 V		2.2		µA
	SS pin to VSENSE pin matching	$V_{(SS)}$ = 0.4 V		35		mV
DC-DC POWER GOOD (PWRGD PIN)						
	VSENSE pin threshold	VSENSE falling (fault)		0.91V_{ref}		V
		VSENSE rising (good)		0.93V_{ref}		V
		VSENSE rising (fault)		1.07V_{ref}		V
		VSENSE falling (good)		1.05V_{ref}		V
	High-level output leakage current	$V_{(VSENSE)}$ = V_{ref}, $V_{(PWRGD)}$ = 5.5 V, $V_{(EN)}$ = 3 V		2		nA
	Low-level output voltage	$I_{(PWRGD)}$ = 3 mA		0.3	0.6	V
	Minimum VIN voltage for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		1.2	1.6	V

(1) DC-DC_OUT refers to the regulated output voltage of the switching regulator (see Figure 25).

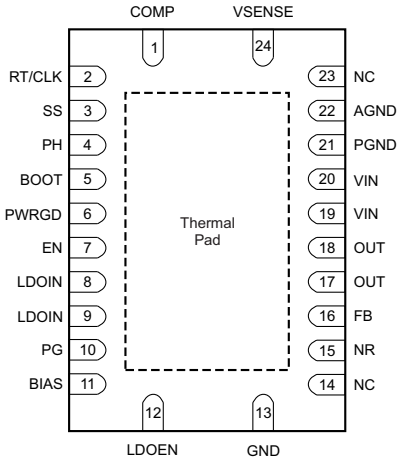
ELECTRICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, $V_{(BIAS)}$ = $V_{(VIN)}$ = 5 V, $V_{(LDOIN)}$ = DC-DC_OUT[1] = 2.1 V, $V_{(LDOEN)}$ = 1.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 10.0 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS54122			UNIT
			MIN	TYP	MAX	
LDO						
$V_{(LDOIN)}$	LDO input voltage range		$V_{(OUT)}$ + V_{DO}		5.5	V
$V_{(BIAS)}$	LDO bias input voltage range		2.375		5.5	V
$V_{(FB)}$	FB pin voltage	T_A = +25°C	0.796	0.8	0.804	V
$V_{(OUT)}$	OUT pin voltage range		$V_{(FB)}$		3.6	V
	OUT pin voltage accuracy	$V_{(OUT)}$ = $V_{(FB)}$, 50 mA ≤ $I_{(OUT)}$ < 3 A, 2.97 V ≤ $V_{(BIAS)}$ ≤ 5.25 V, $V_{(OUT\_nom)}$ + 0.3 V ≤ $V_{(LDOIN)}$, $V_{(OUT\_nom)}$ + 1.62 V ≤ $V_{(BIAS)}$,	–1.0%	±0.2%	1.0%	
$\Delta V_{O(\Delta IL)}$	Load regulation	0 mA ≤ $I_{(OUT)}$ ≤ 50 mA		0.013		%/mA
		50 mA ≤ $I_{(OUT)}$ ≤ 3 A		0.03		%/A
$\Delta V_{O(\Delta VI)}$	Line regulation	$V_{(OUT\_nom)}$ + 0.3 V ≤ $V_{(LDOIN)}$ ≤ 5.5 V		0.0005	0.06	%/V
$V_{DO(LDOIN)}$	$V_{(LDOIN)}$ dropout voltage	$I_{(OUT)}$ ≤ 3.0 A, $V_{(BIAS)}$ – $V_{(OUT\_nom)}$ ≥ 1.62 V		100	200	mV
$V_{DO(BIAS)}$	$V_{(BIAS)}$ dropout voltage	$I_{(OUT)}$ ≤ 3.0 A, $V_{(LDOIN)}$ = $V_{(BIAS)}$			1.62	V
I_{LIM}	Output current limit	$V_{(OUT)}$ = 0.8 × $V_{(OUT\_nom)}$	3.8		6.0	A
$I_{(BIAS)}$	BIAS pin current			2	4	mA
$I_{SD(LDO)}$	Shutdown current ($I_{(BIAS)}$)	$V_{(EN)}$ < 0.4 V		1	100	µA
$I_{(FB)}$	FB pin current		–250	95	250	nA
$I_{(LDOEN)}$	LDOEN pin input current	$V_{(EN)}$ = 5 V		0.1	1	µA
$V_{IL(LDOEN)}$	LDOEN pin low-level input voltage (disable)				0.4	V
$V_{IH(LDOEN)}$	LDOEN pin high-level input voltage (enable)		1.1			V
	PG pin trip threshold	$V_{(FB)}$ decreasing	0.86$V_{(FB)}$	0.90$V_{(FB)}$	0.94$V_{(FB)}$	V
	PG pin trip hysteresis			0.03$V_{(FB)}$		V
	High-level output leakage current	$V_{(PG)}$ = 5.25 V		0.03	1	µA
	Low-level output voltage	$I_{(PG)}$ = 1 mA			0.3	V
$I_{(NR)}$	NR pin charging current	$V_{(NR)}$ = 0.4 V	0.5	0.73	1	µA
DC-DC TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
	Switching frequency range (RT mode set point and PLL mode)		300		2000	kHz
	Switching frequency	$R_{(RT)}$ = 400 kΩ (1%)	400	500	600	kHz
	Switching frequency range in CLK mode		300		2000	kHz
	RT/CLK pin high threshold				2.2	V
	RT/CLK pin low threshold		0.4			V
	PLL lock-in time			14		µs
	RT/CLK pin falling edge to PH pin rising edge delay	Measure at 500 kHz with RT resistor in series		90		ns
PH PIN						
	Minimum on time	Measured at 50% points on PH, $I_{(OUT)}$ = 3 A		65		ns
		Measured at 50% points on PH, $I_{(OUT)}$ = 0 A		120		ns
	Minimum off time	Prior to skipping off pulses, $V_{(BOOT)}$ – $V_{(PH)}$ = 2.95 V, $I_{(OUT)}$ = 3 A		60		ns
	Rise time	$V_{(VIN)}$ = 5 V, $I_{(OUT)}$ = 3 A		2.5		V/ns
	Fall time	$V_{(VIN)}$ = 5 V, $I_{(OUT)}$ = 3 A		2		V/ns
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
NOISE						
V_n	Output noise voltage	BW = 10 Hz to 1 MHz, $C_{(NR)}$ = 10 µF, $C_{(FB)}$ = 0.1 µF, $I_{(OUT)}$ = 1 A , C_{OUT} = 100 µF		17		μV_{RMS}

PIN CONFIGURATION

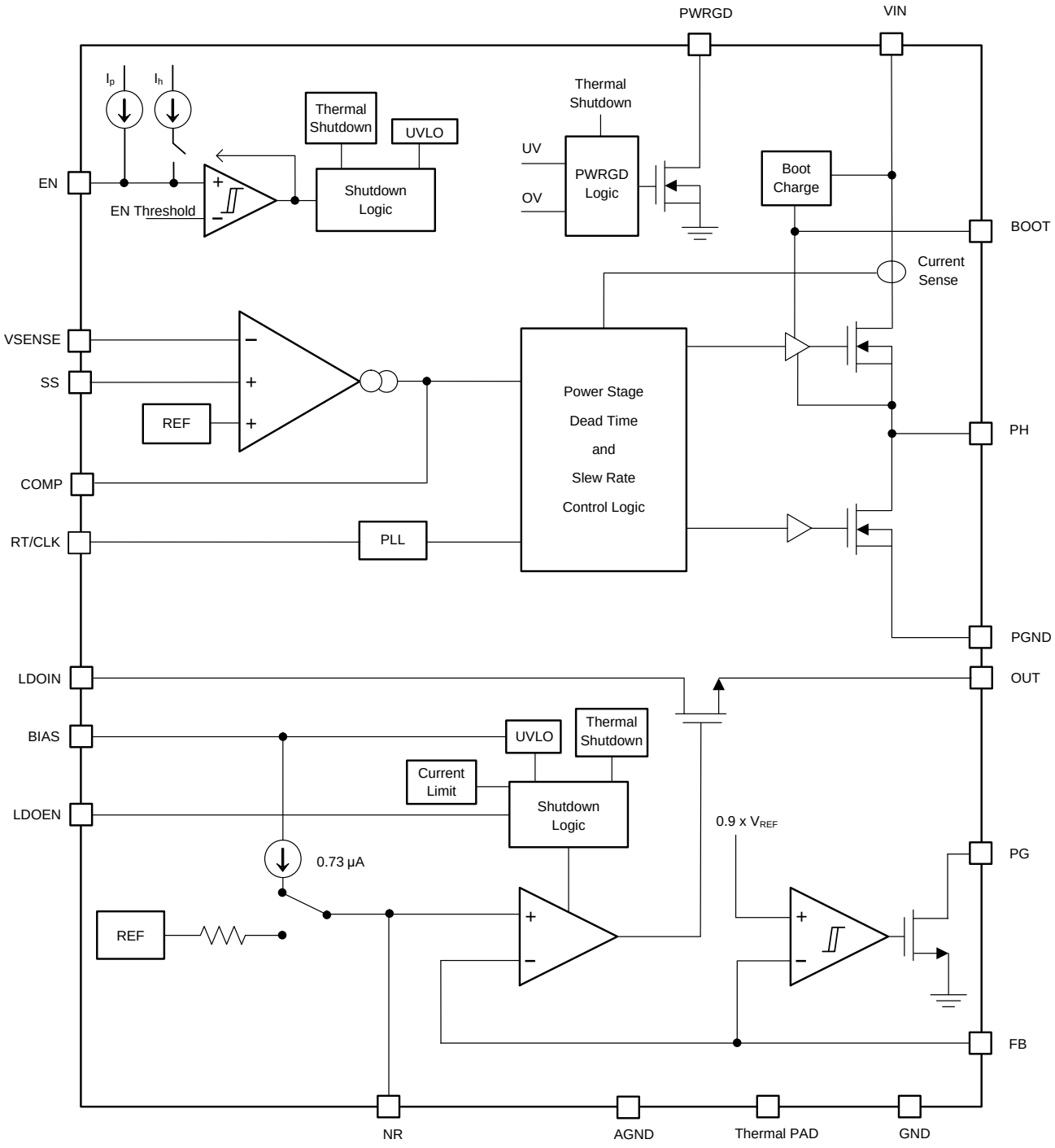
RHL PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
AGND	22	Ground return for dc-dc control circuitry of the dc-dc converter
BIAS	11	Bias input supply to the LDO control loop
BOOT	5	A bootstrap capacitor is required between the BOOT and PH pins. The voltage on this capacitor carries the gate drive voltage for the high-side MOSFET of the dc-dc converter.
COMP	1	DC-DC error amplifier output, and input to the output switch current comparator. Connect frequency compensation to this pin.
EN	7	Enable pin for dc-dc converter. Float this pin to enable. Adjust the input undervoltage lockout with two resistors.
FB	16	This pin is the input to the control-loop error amplifier of the LDO and is used to set its output voltage.
GND	13	LDO ground
LDOEN	12	Driving this pin high turns on the LDO. Driving this pin low shuts down the LDO. Note that the EN pin must not be left floating and can be connected to LDOIN if not used.
LDOIN	8, 9	LDO input
NC	14, 23	No internal connection
NR	15	LDO noise reduction pin. Connect an external capacitor between this pin and ground to reduce output noise to very low levels, and slow down the VOUT ramp (RC soft-start) of the LDO.
OUT	17, 18	LDO output. A 1-µF or larger capacitor is required for stability.
PG	10	Open-drain, power-good fault pin of the LDO. Asserts low as a result of thermal shutdown, undervoltage, EN shutdown, or during a slow start of the LDO.
PGND	21	Return for the dc-dc control circuitry and low-side power MOSFET of the dc-dc converter.
PH	4	DC-DC converter switch node
PWRGD	6	Open-drain, power-good fault pin of the dc-dc converter. Asserts low as a result of thermal shutdown, undervoltage, overvoltage, EN pin shutdown, or during a soft-start of the dc-dc converter.
RT/CLK	2	Automatically selects between RT mode and CLK mode. An external timing resistor adjusts the switching frequency of the device. In CLK mode, the device synchronizes to an external clock.
SS	3	Soft-start pin. Connect an external capacitor to this pin to set the internal reference voltage rise time. The voltage on this pin overrides the internal reference.
VIN	19, 20	Supplies the control circuitry of the dc-dc converter.
VSENSE	24	Inverting input of the g_M error amplifier of the dc-dc converter.
Thermal pad		GND; for best noise performance, connect the thermal pad to the LDO GND and to a large ground pad for thermal dissipation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At $V_{(VIN)}$ = $V_{(BIAS)}$= $V_{(LDOEN)}$= 5 V, $V_{(LDOIN)}$ = DC-DC_OUT = 2.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 25), unless otherwise noted.

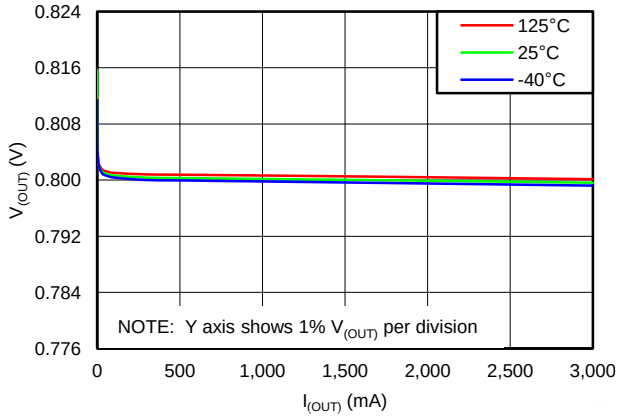


Figure 1. LOAD REGULATION

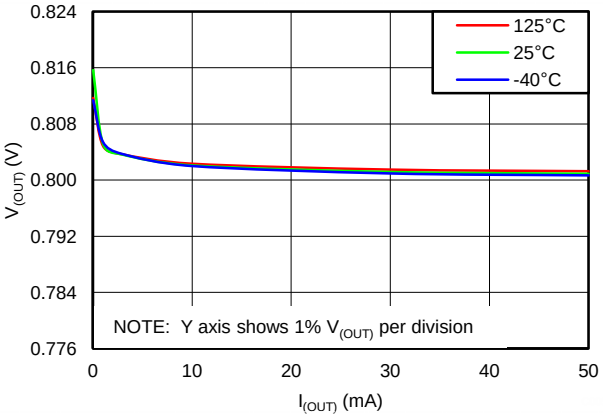


Figure 2. LOAD REGULATION UNDER LIGHT LOADS

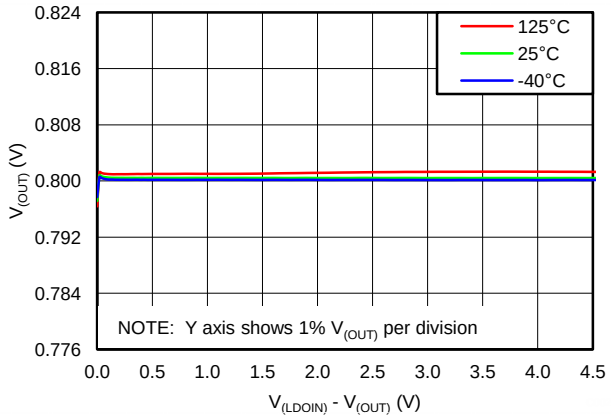


Figure 3. LDOIN LINE REGULATION

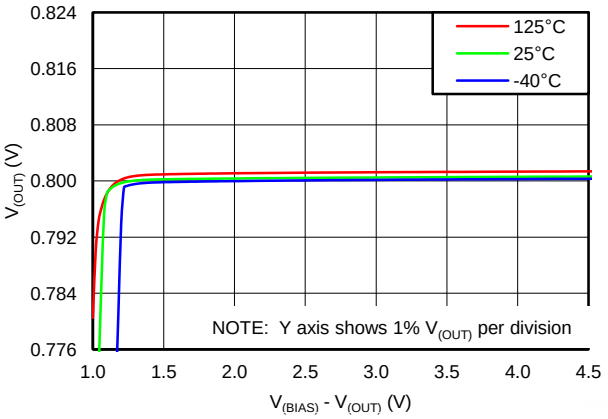


Figure 4. LDO BIAS LINE REGULATION

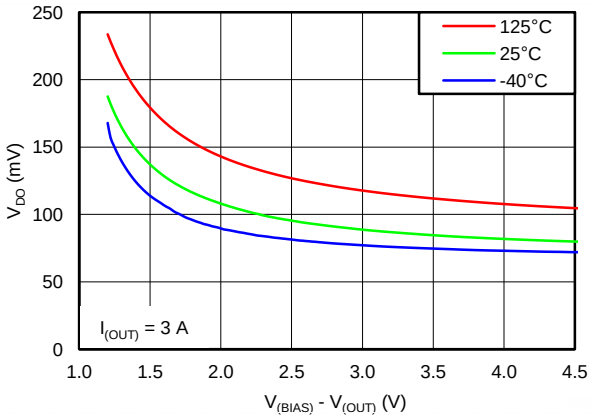


Figure 5. LDO DROPOUT VOLTAGE vs LDO BIAS VOLTAGE

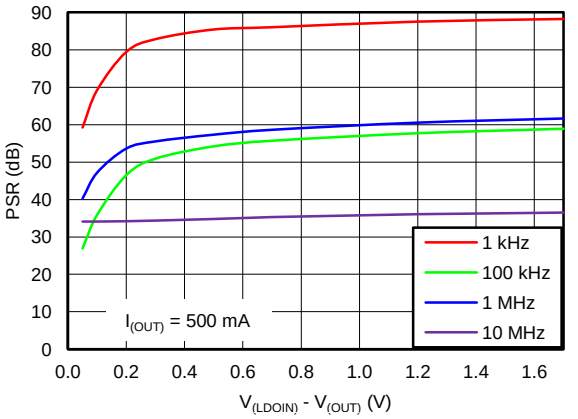


Figure 6. LDO POWER-SUPPLY RIPPLE REJECTION vs LDO DROPOUT VOLTAGE

TYPICAL CHARACTERISTICS (continued)

At $V_{(VIN)}$ = $V_{(BIAS)}$= $V_{(LDOEN)}$= 5 V, $V_{(LDOIN)}$ = DC-DC_OUT = 2.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 25), unless otherwise noted.

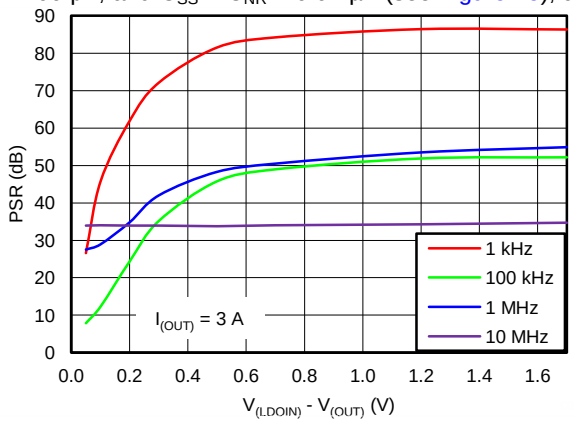


Figure 7. LDO POWER-SUPPLY RIPPLE REJECTION vs LDO DROPOUT VOLTAGE

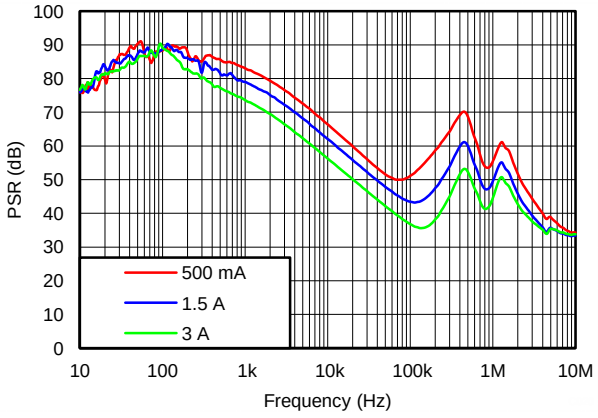


Figure 8. LDO POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

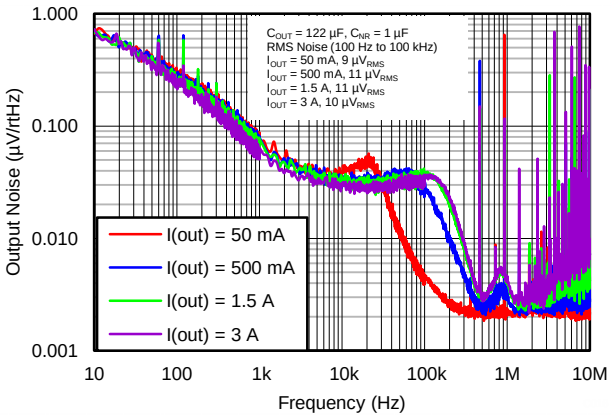


Figure 9. OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

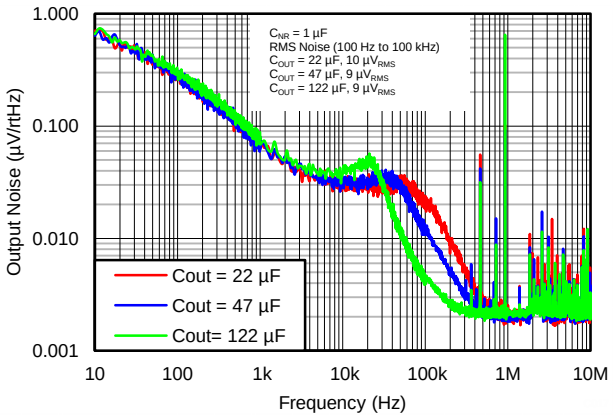


Figure 10. OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

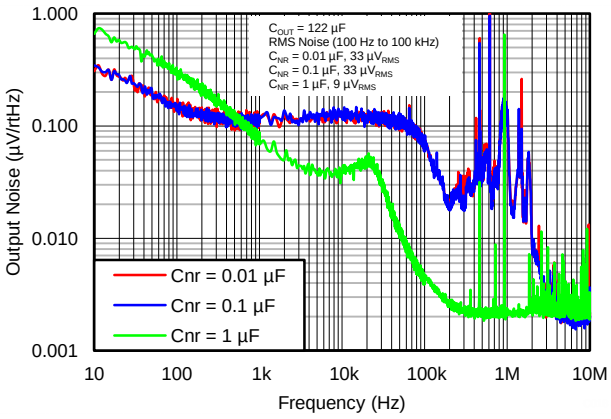


Figure 11. OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

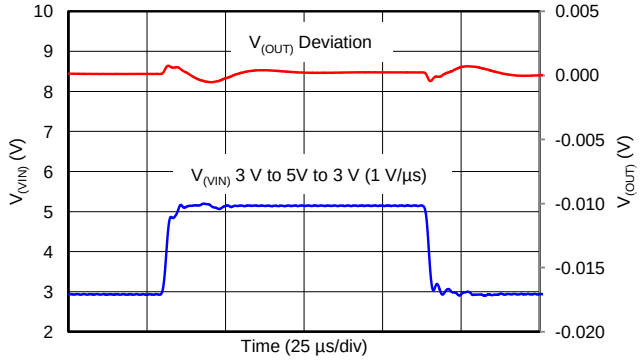


Figure 12. LINE TRANSIENT RESPONSE

TYPICAL CHARACTERISTICS (continued)

At $V_{(VIN)}$ = $V_{(BIAS)}$= $V_{(LDOEN)}$= 5 V, $V_{(LDOIN)}$ = DC-DC_OUT = 2.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 25), unless otherwise noted.

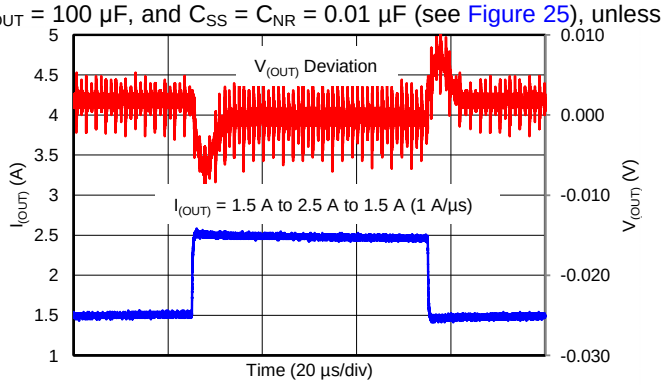


Figure 13. LOAD TRANSIENT RESPONSE

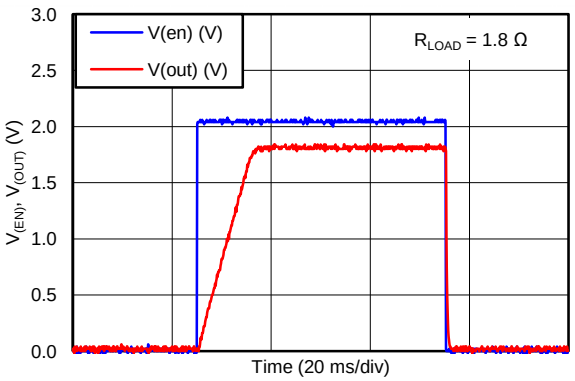


Figure 14. ENABLE PULSE RESPONSE

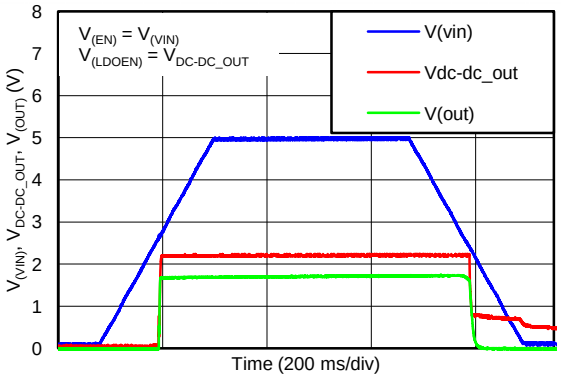


Figure 15. POWER-UP AND POWER DOWN RESPONSE

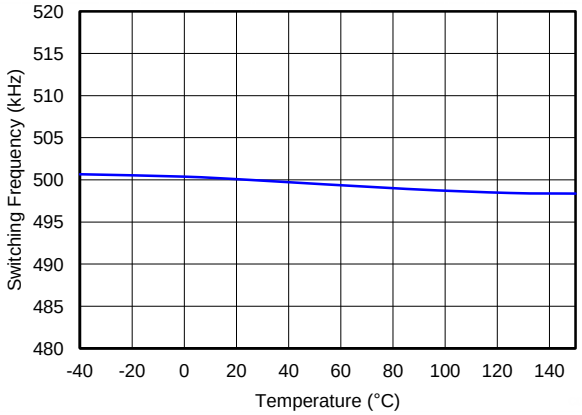


Figure 16. DC-DC SWITCHING FREQUENCY vs TEMPERATURE

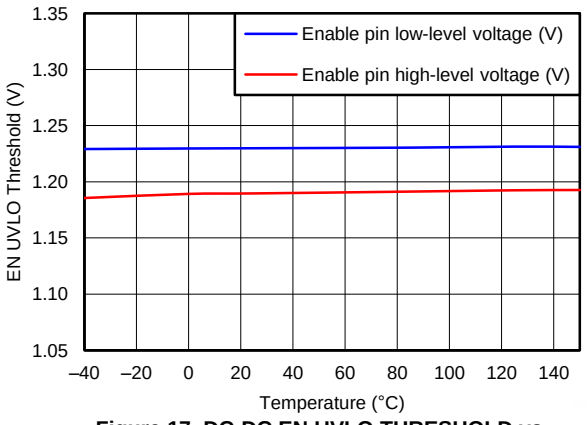


Figure 17. DC-DC EN UVLO THRESHOLD vs TEMPERATURE

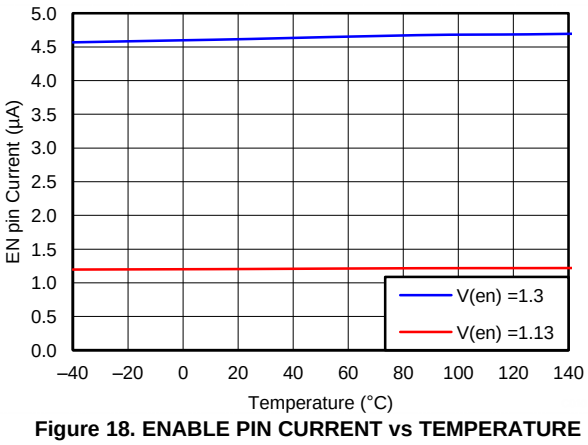


Figure 18. ENABLE PIN CURRENT vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

At $V_{(VIN)}$ = $V_{(BIAS)}$= $V_{(LDOEN)}$= 5 V, $V_{(LDOIN)}$ = DC-DC_OUT = 2.1 V, $V_{(OUT)}$ = 1.8 V, $I_{(OUT)}$ = 50 mA, $V_{(EN)}$ = floating, C_{OUT} = 100 µF, and C_{SS} = C_{NR} = 0.01 µF (see Figure 25), unless otherwise noted.

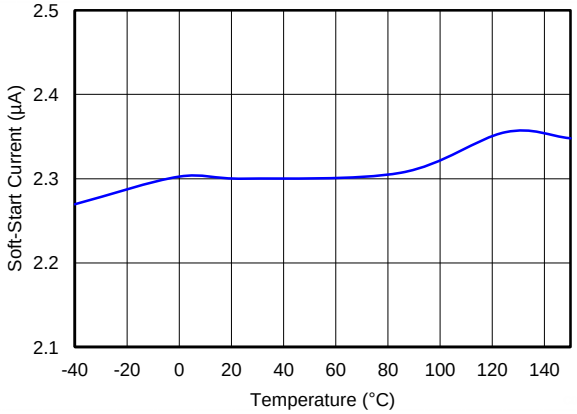


Figure 19. DC-DC SOFT-START CURRENT vs TEMPERATURE

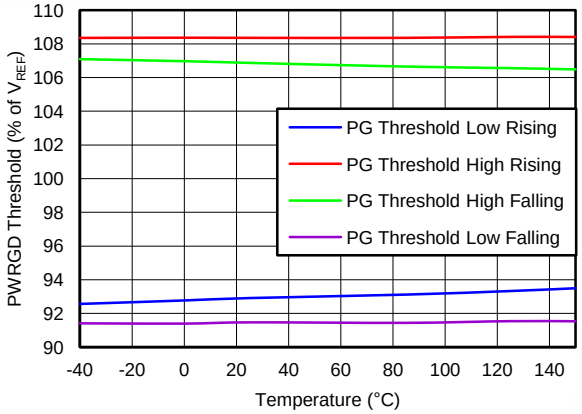


Figure 20. PG THRESHOLD vs TEMPERATURE

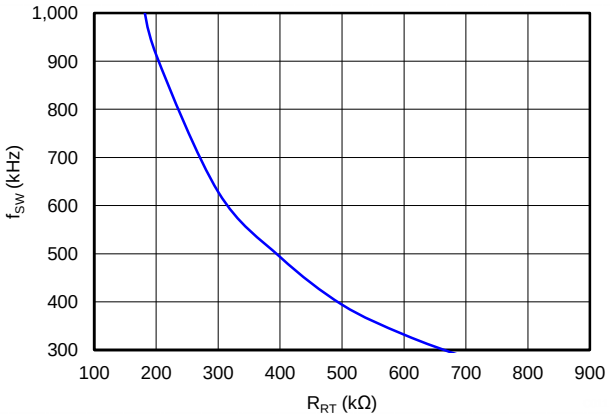


Figure 21. DC-DC SWITCHING FREQUENCY vs R_{RT}

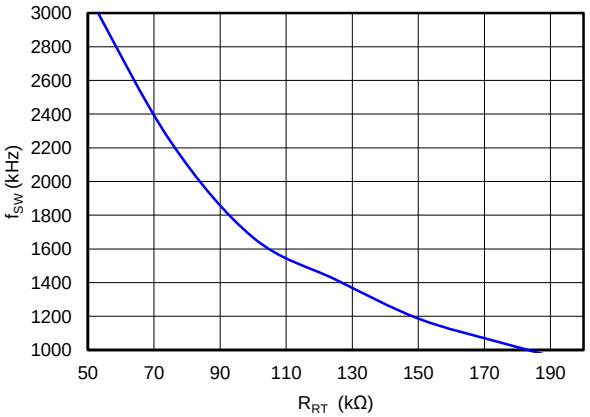


Figure 22. DC-DC SWITCHING FREQUENCY vs R_{RT}

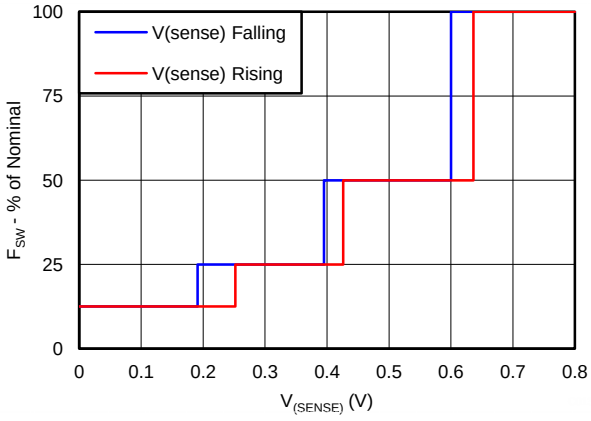


Figure 23. SWITCHING FREQUENCY vs VSENSE

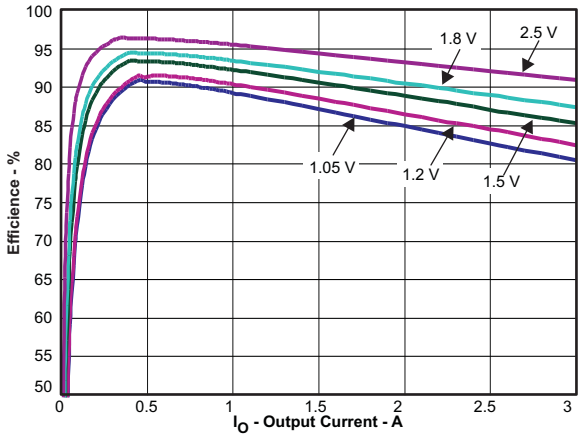


Figure 24. DC-DC Efficiency vs Output Current

DETAILED DESCRIPTION

OVERVIEW

The TPS54122 is a low-noise power supply that delivers a quiet power rail to noise-sensitive components. This device combines a current, mode-controlled, dc-dc, step-down (buck) regulator, and a low-noise, wide-bandwidth, low-dropout regulator (LDO) to create an efficient, stable, low-noise power supply. The TPS54122 is fully characterized for noise performance, thus allowing for easy creation of a quiet power supply. The device includes features such as soft-start, clock synchronization, and a power-good signal, making it well suited as a power supply for communication, test and measurement, and audio-equipment applications. Both the integrated switching regulator and LDO are fully configurable, allowing for complete design flexibility. In addition, a simplified design procedure enables quick development of a power supply custom suited to specific requirements; see the Simplified Design Methodology section for more details.

Figure 25 shows a typical application diagram for the TPS54122.

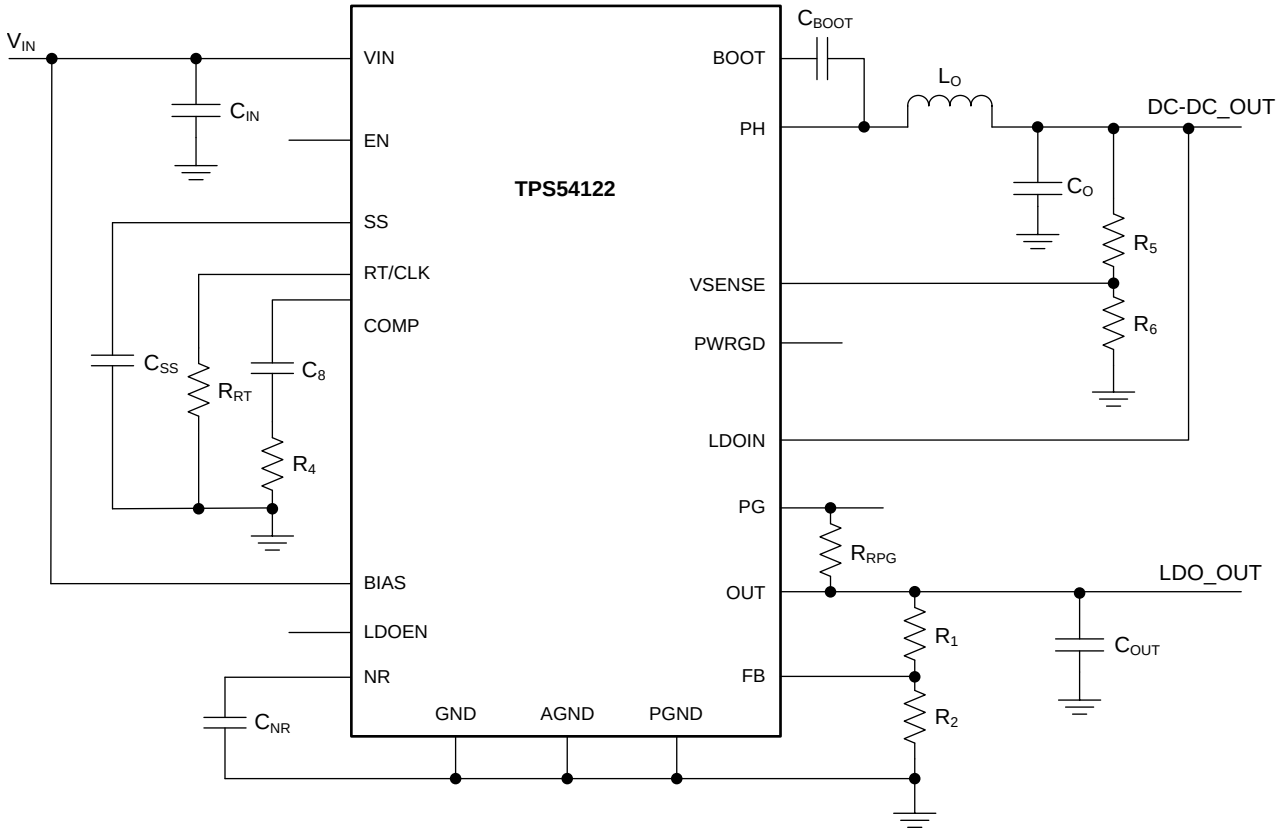


Figure 25. Typical Application

INPUT VOLTAGE RANGE

VIN

The TPS54122 VIN pin provides power to both the dc-dc control circuitry as well as the dc-dc power stage. Use a voltage divider connected from the VIN pin to the EN pin to set an undervoltage lockout (UVLO) for the dc-dc converter to provide consistent power-up behavior; refer to the *Device Enable and Undervoltage Lockout Adjustment* section for more information.

LDO Input Voltage (LDOIN)

The LDOIN pin provides power to the pass device of the LDO. The minimum input operating voltage that can be applied to the LDOIN pin of the TPS54122 is LDOVIN = (VOUT + VDO). The voltage into this pin must not exceed 6.0 V. This pin is designed to be connected to the output inductor of the integrated switcher; decouple this pin to the GND pin with a 1.0-µF ceramic capacitor.

LDO Bias Input Voltage (LDOBIAS)

The LDOBIAS pin provides power to the control circuitry of the LDO. The LDOBIAS voltage requires additional voltage headroom over the LDOIN voltage to allow the control circuitry to operate the N-channel pass device. The minimum input operating voltage that can be applied to the LDOBIAS pin is 2.375 V, or VOUT + 1.62 V. Therefore, for the case with OUT = 1.5 V, the LDOIN can be set to as low as 1.8 V, and the LDOBIAS can be set to 3.3 V, ±5%. In the majority of applications, the LDOBIAS pin can be connected to the VIN pin of the TPS54122.

ADJUSTING THE OUTPUT VOLTAGE

The output voltage of both the switcher and the LDO are adjustable. The output voltages are set with a resistor divider from the output voltage to the feedback sensing pins (VSENSE or FB). Use 1% tolerance or better divider resistors for best accuracy.

The values of the LDO feedback resistors can be calculated using Equation 1:

$$V_{(OUT)} = (R_1 + R_2)\, V_{ref} / R_2$$

Where:

V_{ref} = 0.8 V

R_1 = The resistor from the output to the FB pin of the LDO.

R_2 = The resistor from the FB pin to ground of the LDO. (1)

The values of the switching regulator feedback resistors can be calculated using Equation 2:

$$DC\text{-}DC\_OUT = (R_5 + R_6)\, V_{ref} / R_6$$

Where:

V_{ref} = 0.827 V

R_5 = The resistor from the switcher output at the inductor to the VSENSE pin of the switching regulator.

R_6 = The resistor from the VSENSE pin to ground switching regulator. (2)

To improve efficiency at light loads, consider using larger-value resistors. Larger-value resistors increase the noise sensitivity at the VSENSE and FB pins and error from the VSENSE and FB pin input currents. Using a value of 10 kΩ for R_2 and R_5 provides a good trade-off between these two issues.

POWER CONVERSION EFFICIENCY VERSUS OUTPUT NOISE

The configuration of the TPS54122 consists of a switching regulator followed by an LDO. The ability of the LDO to reject the noise created by the switching regulator and not pass it to the LDO output is determined by the power-supply rejection (PSR) of the LDO. The PSR of an LDO depends on the LDO input to LDO output voltage difference. The higher the voltage difference, the better the LDO ability to reject noise at its input. The LDO in the TPS54122 has been designed to provide high, wide-bandwidth PSR with a minimum of input to output voltage differential. At 3 A for the highest PSR performance, set the input-to-output voltage differential to 0.5 V or greater.

The LDO voltage differential is also a primary contributor to the overall power loss in the TPS54122. The LDO input and output voltage differentials contribution to the power loss is defined as the output current multiplied by the input-to-output voltage differential, as shown in Equation 3:

$$\text{Power Loss from the LDO} = I_{(OUT)} \times (V_{(LDOIN)} - V_{(OUT)}) \quad (3)$$

Therefore, for a 0.5-V drop at 1.5 A, this loss is 0.75 W. Reduce the impact of the power loss by lowering V_{DO}; note that a lower V_{DO} reduces the PSR of the LDO. In the Typical Characteristics section, Figure 6 and Figure 7 show the trade-off between PSR and V_{DO} for various output current levels and frequencies. For currents less than 1 A, a V_{DO} of 0.3 V does not have significant impact on PSR performance and provides a substantial improvement to the power loss from the V_{DO}.

BOOTSTRAP VOLTAGE AND LOW DROPOUT OPERATION

The TPS54122 has an integrated bootstrap-voltage regulator, and requires a small ceramic capacitor between the BOOT and PH pins to provide the gate drive for the high-side MOSFET. The boot capacitor is charged when the BOOT pin voltage is less than VIN and the (BOOT – PH) voltage is below regulation. Use a 0.1-µF ceramic capacitor with an X7R- or X5R-grade dielectric and a voltage rating of 10 V or higher because of the stable characteristics over temperature and voltage.

To improve dropout, the device is designed to operate at 100% duty cycle, as long as the BOOT to PH pin voltage is greater than 2.2 V. When the voltage between BOOT and PH drops below the 2.2-V UVLO threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on, allowing the boot capacitor to be recharged. The supply current source from the BOOT pin is very low; therefore, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor. Thus, the effective duty cycle of the switching regulator is nearly 100%.

DC-DC OUTPUT OVERVOLTAGE TRANSIENT PROTECTION (OVTP)

The TPS54122 has a overvoltage transient protection (OVTP) circuit on the dc-dc switcher output to minimize overshoots on the dc-dc switcher output. This circuit also protects the input of the LDO from experiencing overshoot above its rated values.

CAUTION

Any voltage above the absolute maximum rated input voltage into the LDOIN pin can damage the device.

The OVTP feature minimizes overshoot by comparing the VSENSE pin voltage to the OVTP threshold (107% of the dc-dc V_{ref}). If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops below the OVTP threshold, the high-side MOSFET is enabled at the next clock cycle.

OVERCURRENT PROTECTION

The TPS54122 provides multiple forms of overcurrent protection.

Switcher Overcurrent Protection

The integrated switcher of the TPS54122 is protected from overcurrent conditions by using a cycle-by-cycle current limit. During each switching cycle, the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current crosses the COMP pin voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current until the error amplifier output reaches the internally clamped voltage, which then functions as the switch current limit.

Frequency Division

In addition to a current limit on the high-side switch, the TPS54122 implements a switching-frequency division technique to allow the low-side MOSFET to be turned off long enough to reduce the current in the inductor to prevent current runaway. During an overcurrent condition, the frequency division reduces the frequency from 100% to 50%, to 25%, and then to 12.5%. The overcurrent condition is detected by decreases in voltage on the VSENSE pin. Figure 23 shows the reduction in frequency based on the VSENSE voltage reduction. During startup, the switching frequency increases correspondingly as the voltage on the VSENSE pin increases from 0 V to 0.827 V.

Reverse Overcurrent Protection

The TPS54122 implements low-side current protection by detecting the voltage drop across the low-side MOSFET. When the dc-dc converter sinks current through the low-side MOSFET, the control circuit turns off the low-side MOSFET if the reverse current is typically more than 2 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into prebiased outputs.

LDO Internal Current Limit

In addition to the switcher overcurrent protection, the TPS54122 has an internal current limit on the integrated LDO. The LDO internal current limit helps protect the LDO during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, do not operate the device in a current-limit state for extended periods of time. The NMOS pass element in the integrated LDO has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at LDOIN. This current is not limited, so if extended reverse-voltage operation is anticipated, external limiting may be required.

THERMAL INFORMATION

The internal thermal protection circuitry of the device has been designed to protect against overload conditions. However, this circuitry was not intended to replace proper heat sinking. Continuously running the device into thermal shutdown degrades device reliability. The TPS54122 has thermal protection for both the switcher and the LDO, and they operate independently of each other.

Thermal Protection of the Switcher

The internal thermal-shutdown circuitry of the switcher forces the device to stop switching if the junction temperature exceeds +165°C (typically). After the device junction temperature drops below +150°C (typically), the dc-dc converter reinitiates the power-up sequence by discharging the SS pin to less than 40 mV.

Thermal Protection of the LDO

Thermal protection of the integrated LDO disables the LDO output of the TPS54122 when the junction temperature rises to approximately +155°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal-protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

ADJUSTABLE SWITCHING FREQUENCY AND SYNCHRONIZATION (RT/CLK)

The RT/CLK pin can be used to set the switching frequency of the device in two modes: RT and CLK.

RT Mode

In RT mode, the $R_{(RT)}$ resistor is connected between the RT/CLK pin and GND. The switching frequency of the device is adjustable from 300 kHz to 2 MHz by using a maximum $R_{(RT)}$ value of 700 kΩ and minimum value of 85 kΩ, respectively. To determine the value of the RT resistor for a given switching frequency (f_{SW}), use Equation 4 or the curves in Figure 21 or Figure 22:

$$R_{(RT)}\ (k\Omega) = 311890\ f_{SW}^{-1.0793}\ (kHz) \quad (4)$$

CLK Mode

In CLK mode, an external clock is connected directly to the RT/CLK pin. The dc-dc converter is synchronized to the external clock frequency with an internal phase-locked loop (PLL) circuit. The dc-dc converter is able to automatically detect the required mode and switch from RT mode to CLK mode. CLK mode overrides RT mode. An internal PLL is implemented to allow synchronization between 300 kHz and 2 MHz, and to easily switch from RT mode to CLK mode. To implement the synchronization feature, connect a square-wave clock signal to the RT/CLK pin with a minimum on-time of at least 75 ns. The clock signal amplitude must transition to less than 0.6 V and to greater than 1.6 V. The rising edge of PH is synchronized to the falling edge of RT/CLK pin.

In applications where both RT mode and CLK mode are required, the device can be configured to have both an RT resistor and external clock connected at the same time to RT/CLK pin. If there is no external clock present, the device works in RT mode and the switching frequency is set by the $R_{(RT)}$ resistor. The first time the SYNC pin is pulled above the RT/CLK high threshold (1.6 V), the device switches from RT mode to CLK mode and the RT/CLK pin becomes high impedance as the PLL starts to lock on to the frequency of the external clock. After the clocking edges stop, the internal clocking circuitry is re-enabled, and the frequency returns to the one set by the $R_{(RT)}$ resistor.

START-UP TIME

The TPS54122 has start-up time control for both the LDO and the dc-dc converter.

Soft-Start of the Switcher

The rate at which the output voltage of the switcher rises up to the full operational level during the start-up phase is controlled through the SS pin. The C_{SS} capacitor is connected between the SS pin and ground. The size of the capacitor determines the soft-start ramp-up time (t_{ss}, 10% to 90%), as shown in Equation 5:

$$t_{SS}\ (ms) = C_{SS}\ (nF)\ V_{ref}\ (V) / I_{SS}\ (\mu A) \quad (5)$$

The device has an internal pull-up current source (I_{SS}) of 2.2 µA that charges the external soft-start capacitor, C_{SS}. The voltage reference, V_{ref}, for this device is 0.827 V. By sourcing a constant current onto the capacitor, the device linearly ramps up the voltage on the SS pin, which corresponds to the voltage on the FB pin, and thus, the output voltage of the switcher.

If the input UVLO is triggered, or the EN pin is pulled below 1.21 V, or a thermal shutdown event occurs, then the device stops switching and enters low-current operation. At the subsequent power-up, when the shutdown condition is removed, the dc-dc does not start switching until it has discharged the SS pin to ground, ensuring proper soft-start behavior.

NR Soft-Start Time and LDO Start-Up

The main purpose of the NR capacitor is to filter the noise from the LDO band gap, and thereby reduce the LDO output noise. However, the NR capacitor also affects the start-up time of the LDO. The TPS54122 has soft start circuit to charge C_{NR} at a controlled rate for a monotonic soft-start. The controlled voltage ramp of the output also reduces peak inrush current during start-up.

The soft-start ramp time depends on the soft-start charging current ($I_{(NR)}$), the external noise-reduction capacitor (C_{NR}), and the internal voltage reference of the LDO, and can be calculated as shown in Equation 6:

$$t_{SS}\ (s) = 1{,}095{,}890 \times C_{NR}\ (F) \quad (6)$$

POWER-GOOD INDICATORS

Switcher Power Good (PWRGD)

The PWRGD pin is an open-drain output. After the VSENSE pin rises above 93% or falls below 105% of the internal voltage reference, the PWRGD pin pull-down transistor is deasserted and the pin floats indicating a correct output voltage on the dc-dc converter. The PWRGD pin has a 2% hysteresis, so it does not pull down until the VSENSE pin falls below 91% or rises above 107% of the internal voltage reference, indicating an out-of-range output voltage. Use a 1-kΩ to 100-kΩ pull-up resistor to a voltage source that is less than or equal to 6 V. The PWRGD pin is in a defined state after the VIN input voltage exceeds 1.2 V.

The PWRGD pin is also pulled low if the input UVLO or thermal shutdown are asserted, or if the EN pin is pulled low.

LDO Power Good (PG)

The power-good (PG) pin of the LDO is an open-drain output and can be connected to any 5.5 V or lower voltage rail through an external pull-up resistor. This pin requires at least 1.1 V on the BIAS pin in order to have a valid output. At power-on, the PG output becomes high-impedance when VOUT is greater than 93% of the set output voltage. If VOUT falls below 90% of the set output voltage or if the BIAS pin voltage falls below 1.9 V, the open-drain turns on and pulls the PG output low. The PG pin also pulls low when the LDO is disabled. The recommended range for the PG pull-up resistor is 10 kΩ to 1 MΩ.

DEVICE ENABLE AND UNDERVOLTAGE LOCKOUT ADJUSTMENT

The TPS54122 provides enable undervoltage lockout adjustment for the dc-dc converter.

Switcher Enable and Undervoltage Lockout

Use the EN pin to turn the switcher on and off. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low I_Q state.

The EN pin has an internal pull-up current source; float the EN pin to enable the device. If an application requires control of the EN pin, use open-drain or open-collector output logic to interface with the pin.

The TPS54122 implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold (typically, 2.6 V). If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 26.

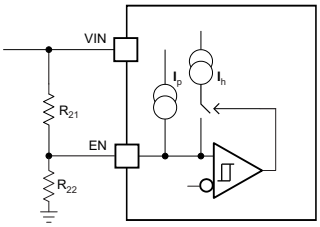


Figure 26. Adjustable VIN Undervoltage Lockout

The EN pin has a small pull-up current (I_p) that sets the state of the pin to enable (default) when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using Equation 7 and Equation 8.

$$R_{21} = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1-\frac{V_{ENFALLING}}{V_{ENRISING}}\right)+I_h}$$

$$R_{22} = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_p + I_h)} \quad (7)$$

Where:

V_{START} is the start up voltage for the dc-dc converter.
V_{STOP} is the shutdown voltage for the dc-dc converter.
$V_{ENFALLING}$ = 1.25 V
$V_{ENRISING}$ = 1.18 V
I_p = 1.2 µA
I_h = 4.6 µA (8)

LDO Enable (LDOEN) and Undervoltage Lockout

The TPS54122 LDO enable pin (LDOEN) is active high and compatible with standard digital-signaling levels. The LDOEN pin has hysteresis and deglitching (typically, 50 mV) that allows it to be use with relatively slow-ramping analog signals, such as an upstream power supply. Typical sequencing applications can be implemented using the TPS54122 dc-dc output or PG, or the output of another power supply. When shutdown capability is not required, EN can be connected to IN.

The LDO also has a fixed UVLO on the LDOBIAS pin to keep the output shut off until the LDO internal circuitry is working properly.

SEQUENCING

The TPS54122 is easy to use and suited for applications that require tracking and sequencing. It has a built-in power-good function to indicate the status of the device, a soft-start circuit to control the output voltage slope during start-up, noise reduction with start-up time for the LDO, and an enable function for independently controlling the start-up of both the LDO and the switcher. Each of these functions is useful for tracking and sequencing applications.

SWITCHER FIXED-FREQUENCY PWM CONTROL

The integrated switcher of the TPS54122 uses adjustable, fixed-frequency, peak-current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier that drives the COMP pin. An internal oscillator turns on the high-side power switch. The error amplifier output is converted into a current reference that is compared to the high-side power switch current. When the power-switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The device implements a current limit by clamping the COMP pin voltage to maximum level. A minimum level clamp is also implemented for improved transient-response performance.

SMALL-SIGNAL MODEL FOR LOOP RESPONSE

Figure 27 shows an equivalent model for the switcher control loop. This model can be run in a circuit simulation program to check frequency and transient responses. The error amplifier is a transconductance amplifier with a g_M of 245 µA/V, and can be modeled using an ideal voltage-controlled current source. Resistor R_O and capacitor C_O model the open-loop gain and frequency response of the error amplifier. The 1-mV, ac voltage source between nodes *a* and *b* effectively breaks the control loop for the frequency-response measurements. Plotting a / c shows the small-signal response of the frequency compensation. Plotting a / b shows the small-signal response of the overall loop. The transient response can be checked by replacing R_L with a current source using the appropriate load step, amplitude, and slew rate in a time-domain analysis.

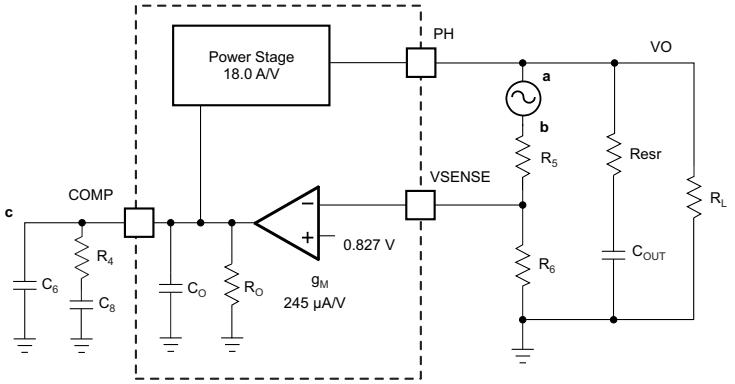


Figure 27. Small-Signal Model for Loop Response

Refer to Application Report SLVA352, *Designing Ultrafast Loop Response With Type-III Compensation for Current Mode Step-Down Converters*, for a more detailed treatment of the small-signal model and compensation for the TPS54122.

APPLICATION INFORMATION

DESIGN METHODOLOGY

The TPS54122 has a low-noise output voltage range from 0.8 V to 3.6 V with an output current of up to 3 A. To simplify design efforts using the TPS54122, see Table 1 for a list of typical designs for common applications according to the typical schematic diagram shown in Figure 28. For more details about designing with the TPS54122, refer to Application Report SLVA602, *Design Procedure for the TPS54122*.

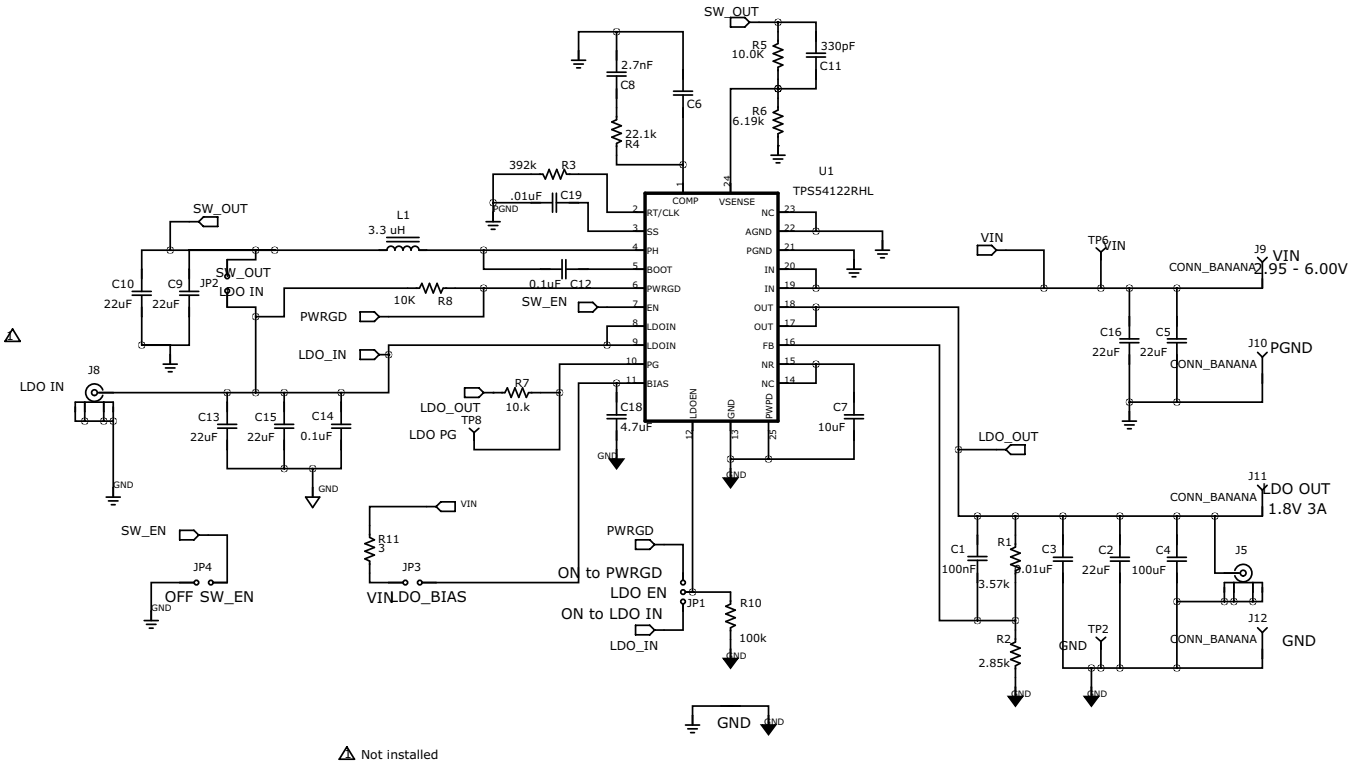


Figure 28. Application Circuit Schematic

The TPS54122 can also be configured to provide two separate power rails: one from the switching regulator and one from the LDO.

Figure 28 shows a typical application diagram for the TPS54122. The first step in the design process is to select the switching frequency for the regulator. Higher switching frequencies produce a smaller solution size using lower-valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, higher switching frequencies cause additional switching losses that negatively impact converter efficiency and thermal performance.

After a switching frequency is determined, the inductor and output capacitor values of the switcher are selected. These two component values are related to each other and depend on the input and output voltages of the switcher, as well as the current rating. Choosing a high inductor-ripple current also impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current.

The TPS54122 requires a high-quality ceramic (type X5R or X7R), input decoupling capacitor with a value of at least 4.7 µF on the input voltage rail. The voltage rating of the input capacitor must be greater than the maximum input voltage.

The internal LDO of the TPS54122 does not require an output capacitor to be stable. However, for best transient and noise performance, use standard ceramic output capacitors with values of 4.7 µF or larger. Higher values are recommended for better noise performance.

For proper operation, connect a 0.1-µF ceramic capacitor between the BOOT and PH pins. Use a ceramic capacitor with X5R or better grade dielectric, and a 10-V or higher voltage rating.

The output voltage of both the switcher and the LDO are adjustable using an external-resistor feedback network. Also, both the LDO and the switcher have a soft-start function that can be adjusted externally using the C_{SS} and C_{NR} capacitors, as shown in Figure 28.

There are several industry techniques used to compensate dc-dc regulators; refer to Application Report SLVA352, *Designing Ultrafast Loop Response With Type-III Compensation for Current Mode Step-Down Converters* for more details about different compensation networks for the TPS54120.

SIMPLIFIED DESIGN METHODOLOGY

The TPS54122 has a low-noise output voltage range of 0.8 V to 3.6 V with an output current of up to 3 A. To simplify design efforts using the TPS54122, the typical designs for common applications are listed in Table 1 based onFigure 28 above. For the designs shown below the values are the closest standard capacitor, inductor, and 1% resistor values. Also, $C_{DC\text{-}DC\_OUT} = C_9 + C_{10} + C_{13} + C_{14} + C_{15}$ and $C_{OUT} = C_2 + C_3 + C_4$. To execute a complete application design, refer to Application Report SLVA602, *Design Procedures for the TPS54122*.

Table 1. Simplified Design Table

$V_{(VIN)}$ (V)	DC-DC_ OUT (V)	$V_{(OUT)}$ (V)	$I_{(OUT)}$ (max) (A)	f_{SW} (kHz)	L_1 (µH)	$C_{DC\text{-}DC\_OUT}$ (µF)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)	R_4 (kΩ)	R_5 (kΩ)	R_6 (kΩ)	C_8 (nF)	C_2 (pF)	C_{OUT} (µF)	C_1 (nF)	C_{11} (pF)
5.0	3.7	3.3	3.0	500	3.3	88	3.57	1.15	392	28.7	10	2.87	4.7	N/A	122	100	1000
5.0	3.6	3.3	1.0	500	3.3	88	3.57	1.15	392	16.5	10	2.94	22	N/A	122	100	1500
5.0	3.6	2.5	2.0	500	3.3	88	3.57	1.69	392	23.2	10	2.94	6.8	N/A	122	100	1500
5.0	2.2	1.8	3.0	500	3.3	88	3.57	2.87	392	22.1	10	5.90	3.3	N/A	122	100	330
5.0	2.1	1.8	1.0	500	3.3	88	3.57	2.87	392	12.7	10	6.49	15	N/A	122	100	680
5.0	1.2	0.8	2.0	500	3.3	88	short	open	392	13.3	10	22.1	4.7	N/A	122	N/A	100
3.3	2.8	2.5	2.0	500	1.0	88	3.57	1.69	392	20.5	10	4.12	6.8	N/A	122	100	1000
3.3	2.2	1.8	3.0	500	2.0	88	3.57	2.87	392	22.1	10	5.90	3.3	N/A	122	100	470
3.3	2.1	1.8	1.0	1000	1.0	88	3.57	2.87	182	12.7	10	6.49	15	N/A	122	100	680
3.3	1.3	1.0	2.0	1000	1.0	88	1.13	4.52	182	14.0	10	17.4	4.7	N/A	122	100	220
3.3	1.1	0.8	2.0	1000	1.0	88	short	open	182	13.0	10	30.1	4.7	N/A	122	N/A	68

PCB LAYOUT GUIDELINES

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS54122 are attached to the end of this product datasheet, and are also available for download at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS FOR HIGH-PSR AND LOW-NOISE PERFORMANCE

Correct printed circuit board (PCB) layout is a critical portion of good power-supply design and is a particularly important for the high PSR and low-noise performance of the TPS54122. The following general guidelines are provided; for a more detailed description, refer to the TPS54122EVM-201 User Guide, SLVU829.

- Place the inductor, the boot capacitor, and the output cap of the dc-dc converter on layers of the board that help minimize the spread of the switching noise into the LDO area on the board, such as the bottom layer.
- Connect the boot cap and inductor L1 as close as possible to the PH pin to reduce parasitic inductance of long traces.
- To help shield the compensation components, the soft-start capacitors, CLK/RT resistor, and dc-dc feedback resistors from noise, ground these components to a power ground that is shielded from the high-current ground plane. To achieve this shielding, use a separate trace to the PGND pin.
- The RT/CLK pin is sensitive to noise, so place the RT resistor as close as possible to the device and routed with a short connection.
- Place the noise-reduction capacitor as close as possible to the device to avoid noise pickup into the LDO reference.
- Isolate the ground planes on the input and the output from each other and connected through a separate trace route that parallels the power-loop routing from the dc-dc output to the LDO input.
- Terminate the low-noise analog ground of the LDO circuits (such as the voltage set point divider, the LDO input, and output caps) to ground using a wide ground trace separate from the power ground plane.
- Place the LDO input and output capacitors as close to the device as possible.
- Bypass the VIN pin to ground using a low-ESR ceramic capacitor with X5R or X7R dielectric, and place as close as possible to the VIN and PGND pins.
- For operation at full-rated load, the top-side ground area together with the internal ground plane must provide adequate heat dissipation.
- Minimize PCB conductor planes to prevent excessive capacitive coupling.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2013) to Revision A	Page
• Added test condition to SS pin to VSENSE pin matching parameter	3
• Added test condition to FB pin voltage parameter	4
• Changed max value of switching frequency range parameter from 200 to 2000 (typo)	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54122RHLR	ACTIVE	VQFN	RHL	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PZFQ	Samples
TPS54122RHLT	ACTIVE	VQFN	RHL	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 150	PZFQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

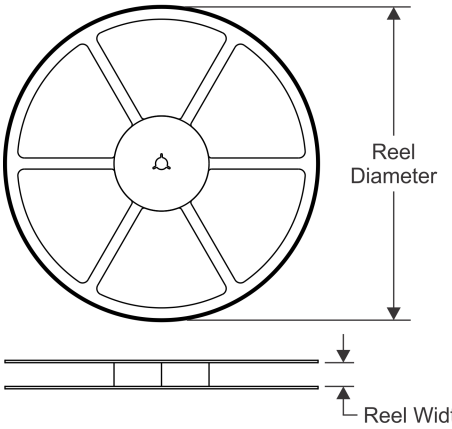
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

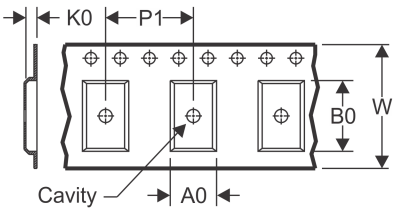
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

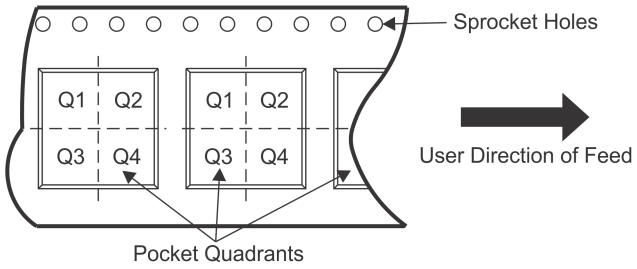


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

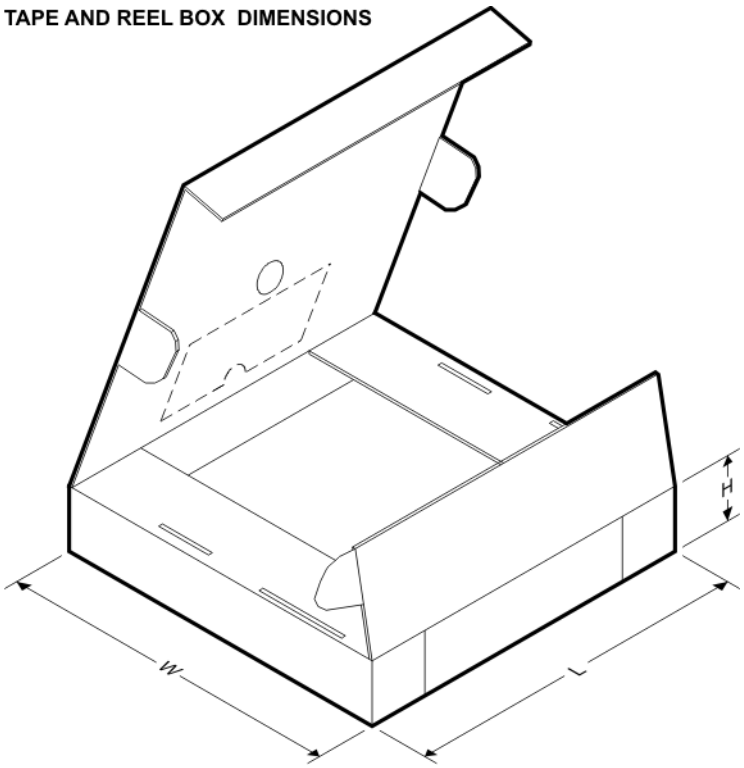
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54122RHLR	VQFN	RHL	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
TPS54122RHLT	VQFN	RHL	24	250	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

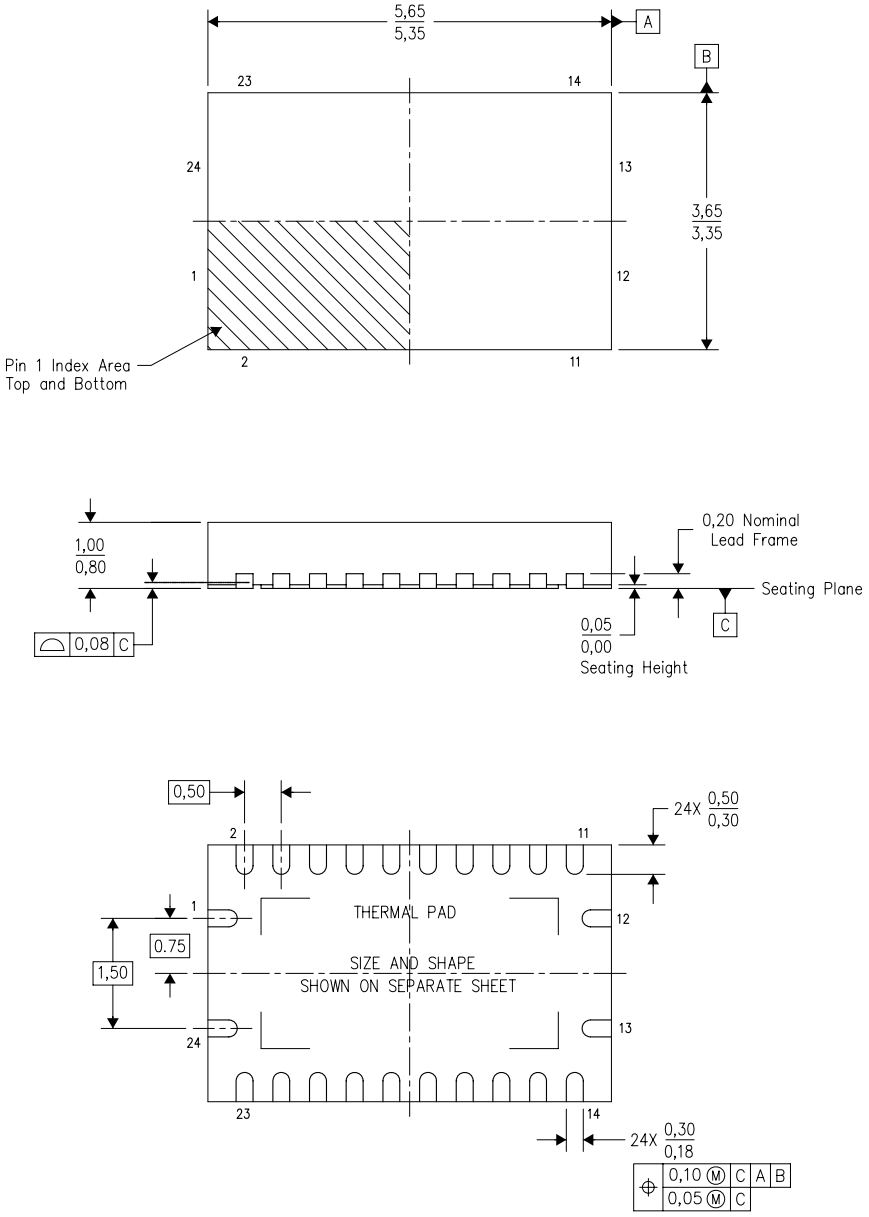
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54122RHLR	VQFN	RHL	24	3000	367.0	367.0	35.0
TPS54122RHLT	VQFN	RHL	24	250	210.0	185.0	35.0

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4205346–4/J 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. JEDEC MO–241 package registration pending.

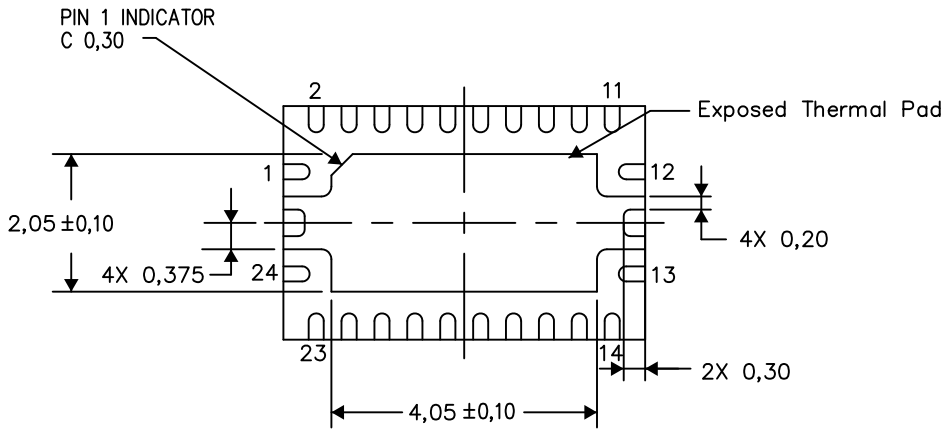
RHL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



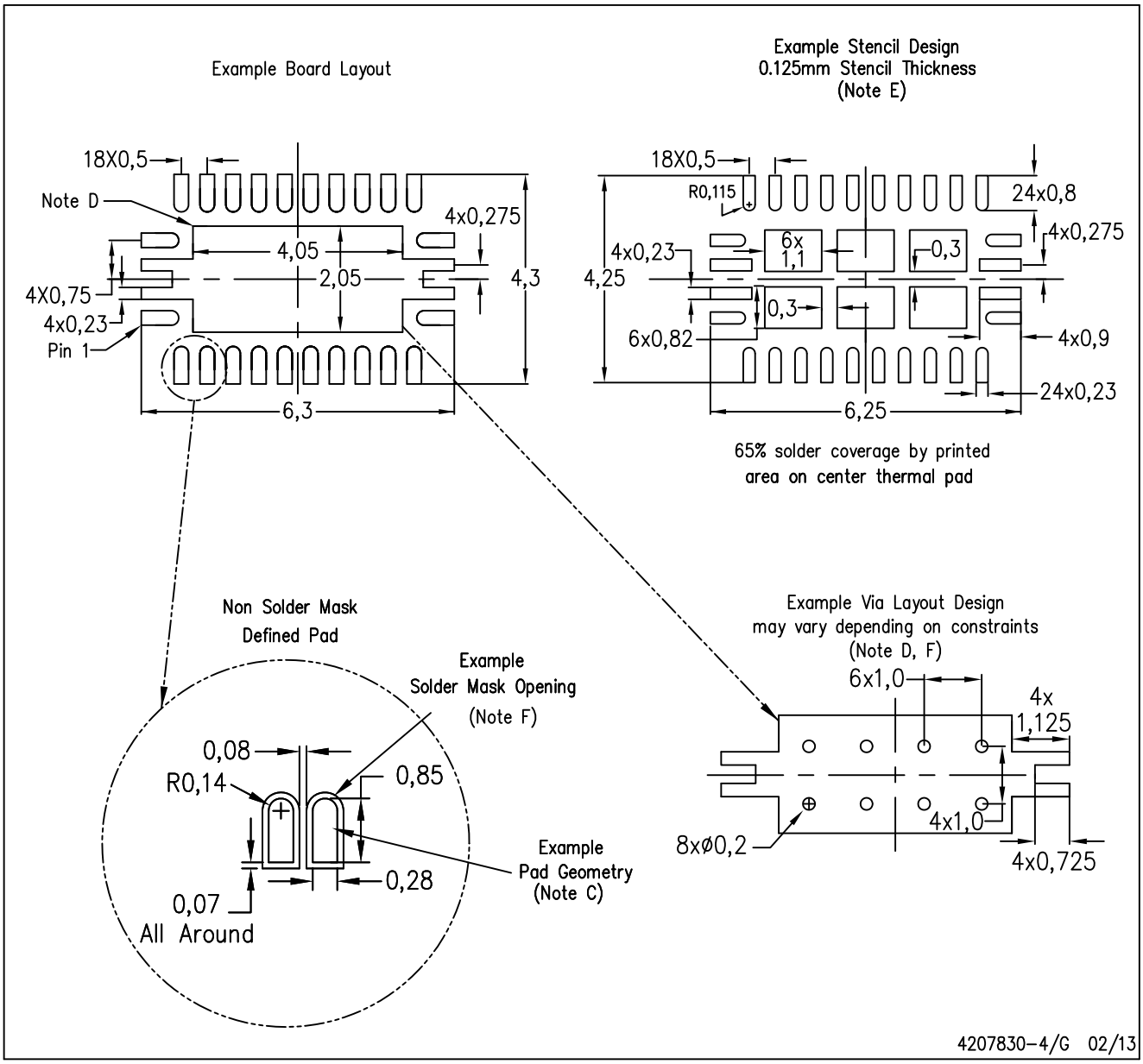
Bottom View

Exposed Thermal Pad Dimensions

4206363–4/M 08/12

NOTE: All linear dimensions are in millimeters

RHL (R–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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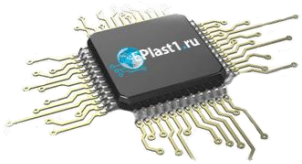

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