

Medium Power Thyristors (Stud Version), 10 A



TO-208AA (TO-48)

FEATURES

- Improved glass passivation for high reliability and exceptional stability at high temperature
- High di/dt and dV/dt capabilities
- Standard package
- Low thermal resistance
- Metric threads version available
- Types up to 1200 V V_{DRM}/V_{RRM}
- RoHS compliant
- Designed and qualified for industrial and consumer level



PRODUCT SUMMARY

$I_{T(AV)}$	50 A
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TYPICAL APPLICATIONS

- Medium power switching
- Phase control applications
- Can be supplied to meet stringent military, aerospace and other high reliability requirements

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		10	A
	T_C	85	°C
$I_{T(RMS)}$		25	A
I_{TSM}	50 Hz	225	A
	60 Hz	240	
I^2t	50 Hz	255	A ² s
	60 Hz	233	
V_{DRM}/V_{RRM}		100 to 1200	V
t_q	Typical	110	μs
T_J		- 65 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE ⁽¹⁾ V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE ⁽²⁾ V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
10RIA	10	100	150	20
	20	200	300	10
	40	400	500	
	60	600	700	
	80	800	900	
	100	1000	1100	
	120	1200	1300	

Notes

⁽¹⁾ Units may be broken over non-repetitively in the off-state direction without damage, if di/dt does not exceed 20 A/ μ s

⁽²⁾ For voltage pulses with $t_p \leq 5$ ms

ABSOLUTE MAXIMUM RATINGS							
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS	
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			10	A	
					85	°C	
Maximum RMS on-state current	I _{T(RMS)}				25	A	
Maximum peak, one-cycle non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T _J = T _J maximum	225	A	
		t = 8.3 ms			240		
		t = 10 ms	100 % V _{RRM} reapplied		190		
		t = 8.3 ms			200		
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplied			255	A ² s
		t = 8.3 ms				233	
		t = 10 ms	100 % V _{RRM} reapplied			180	
		t = 8.3 ms				165	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplied			2550	A ² √s	
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)}), T _J = T _J maximum			1.10	V	
High level value of threshold voltage	V _{T(TO)2}	(I > π × I _{T(AV)}), T _J = T _J maximum			1.39		
Low level value of on-state slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)}), T _J = T _J maximum			24.3	mΩ	
High level value of on-state slope resistance	r _{t2}	(I > π × I _{T(AV)}), T _J = T _J maximum			16.7		
Maximum on-state voltage	V _{TM}	I _{pk} = 32 A, T _J = 25 °C, t _p = 10 ms sine pulse			1.75	V	
Maximum holding current	I _H	T _J = 25 °C, anode supply 12 V resistive load			130	mA	
Typical latching current	I _L				200		



SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum rate of rise of turned-on current	$V_{DRM} \leq 600\text{ V}$	$T_J = T_J \text{ maximum, } V_{DM} = \text{Rated } V_{DRM}$ Gate pulse = 20 V, 15 Ω , $t_p = 6\text{ }\mu\text{s}$, $t_r = 0.1\text{ }\mu\text{s}$ maximum $I_{TM} = (2 \times \text{rated } di/dt)\text{ A}$	200	A/ μs
	$V_{DRM} \leq 800\text{ V}$		180	
	$V_{DRM} \leq 1000\text{ V}$		160	
	$V_{DRM} \leq 1600\text{ V}$		150	
Typical turn-on time	t_{gt}	$T_J = 25\text{ }^\circ\text{C}$, at rated V_{DRM}/V_{RRM} , $T_J = 125\text{ }^\circ\text{C}$	0.9	μs
Typical reverse recovery time	t_{rr}	$T_J = T_J \text{ maximum}$, $I_{TM} = I_{T(AV)}$, $t_p > 200\text{ }\mu\text{s}$, $di/dt = -10\text{ A}/\mu\text{s}$	4	
Typical turn-off time	t_q	$T_J = T_J \text{ maximum}$, $I_{TM} = I_{T(AV)}$, $t_p > 200\text{ }\mu\text{s}$, $V_R = 100\text{ V}$, $di/dt = -10\text{ A}/\mu\text{s}$, $dV/dt = 20\text{ V}/\mu\text{s}$ linear to 67 % V_{DRM} , gate bias 0 V to 100 W	110	

Note

- $t_q = 10\text{ }\mu\text{s}$ up to 600 V, $t_q = 30\text{ }\mu\text{s}$ up to 1600 V available on special request

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J \text{ maximum linear to } 100\text{ \% rated } V_{DRM}$	100	V/ μs
		$T_J = T_J \text{ maximum linear to } 67\text{ \% rated } V_{DRM}$	300 ⁽¹⁾	

Note

- ⁽¹⁾ Available with: $dV/dt = 1000\text{ V}/\mu\text{s}$, to complete code add S90 i.e. 10RIA120S90

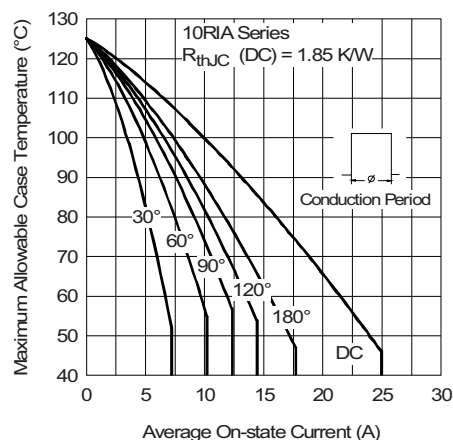
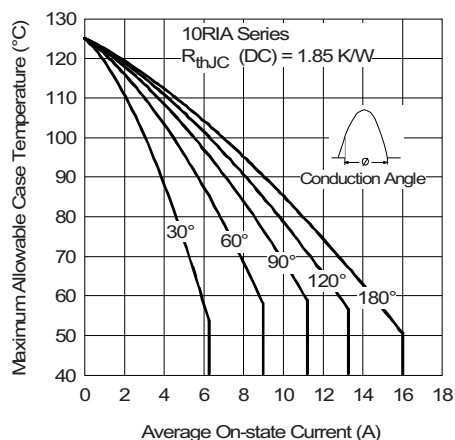
TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J \text{ maximum}$	8.0	W
Maximum average gate power	$P_{G(AV)}$		2.0	
Maximum peak positive gate current	I_{GM}	$T_J = T_J \text{ maximum}$	1.5	A
Maximum peak negative gate voltage	$-V_{GM}$	$T_J = T_J \text{ maximum}$	10	V
DC gate current required to trigger	I_{GT}	$T_J = -65\text{ }^\circ\text{C}$	90	mA
		$T_J = 25\text{ }^\circ\text{C}$	60	
		$T_J = 125\text{ }^\circ\text{C}$	35	
DC gate voltage required to trigger	V_{GT}	$T_J = -65\text{ }^\circ\text{C}$	3.0	V
		$T_J = 25\text{ }^\circ\text{C}$	2.0	
		$T_J = 125\text{ }^\circ\text{C}$	1.0	
DC gate current not to trigger	I_{GD}	$T_J = T_J \text{ maximum}$, $V_{DRM} = \text{Rated value}$	2.0	mA
DC gate voltage not to trigger	V_{GD}	$T_J = T_J \text{ maximum}$, $V_{DRM} = \text{Rated value}$	0.2	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction and storage temperature range	T_J, T_{Stg}		- 65 to 125	°C
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	1.85	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.35	
			TO NUT	TO DEVICE
Mounting torque		Lubricated threads (Non-lubricated threads)	20 (27.5)	25
			0.23 (0.32)	0.29
			2.3 (3.1)	2.8
Approximate weight			14	g
			0.49	oz.
Case style		See dimensions - link at the end of datasheet	TO-208AA (TO-48)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.44	0.32	$T_J = T_J$ maximum	K/W
120°	0.53	0.56		
90°	0.68	0.75		
60°	1.01	1.05		
30°	1.71	1.73		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC



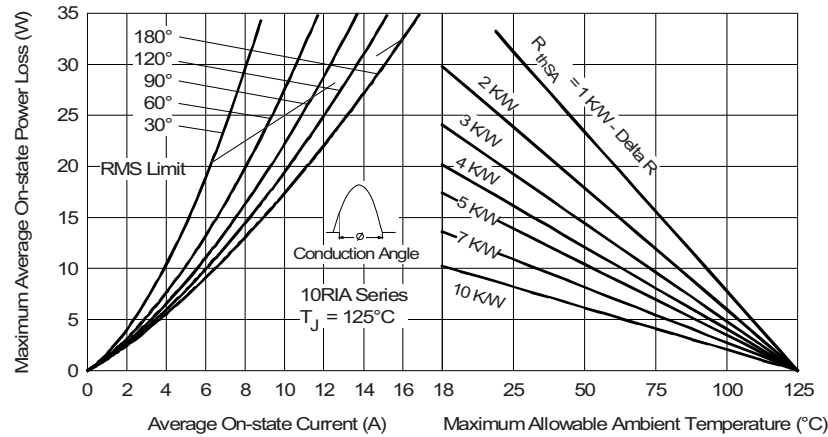


Fig. 3 - On-State Power Loss Characteristics

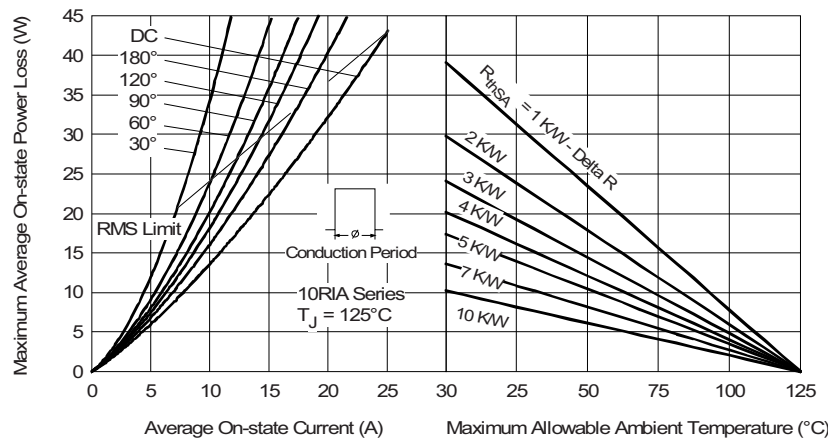


Fig. 4 - On-State Power Loss Characteristics

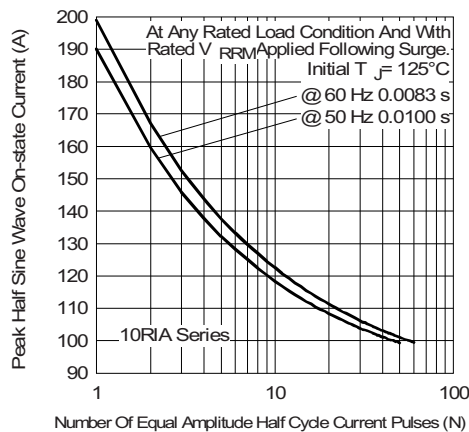


Fig. 5 - Maximum Non-Repetitive Surge Current

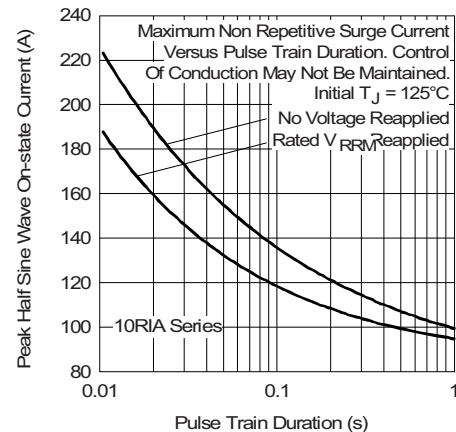


Fig. 6 - Maximum Non-Repetitive Surge Current

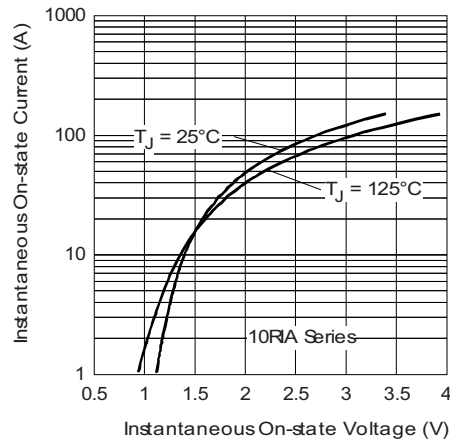


Fig. 7 - Forward Voltage Drop Characteristics

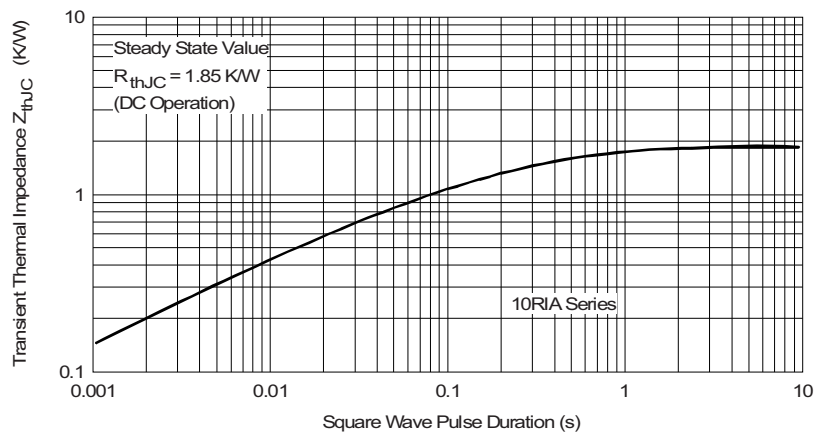


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

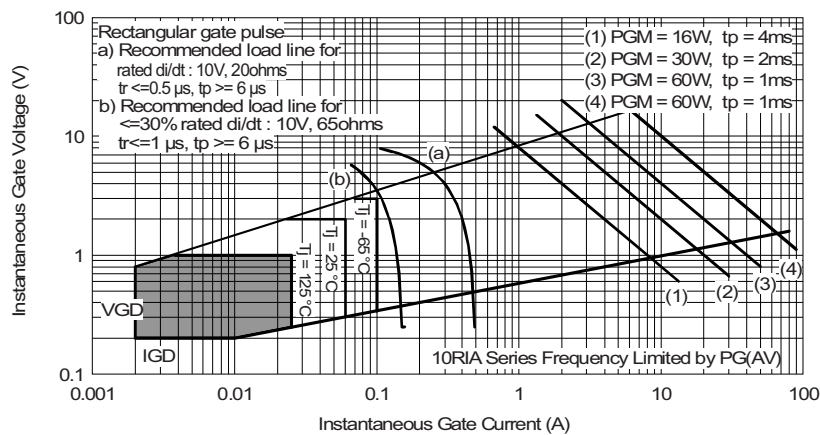


Fig. 9 - Gate Characteristics



ORDERING INFORMATION TABLE

Device code structure diagram:

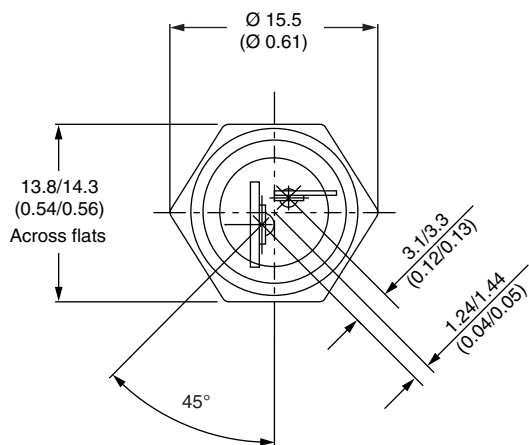
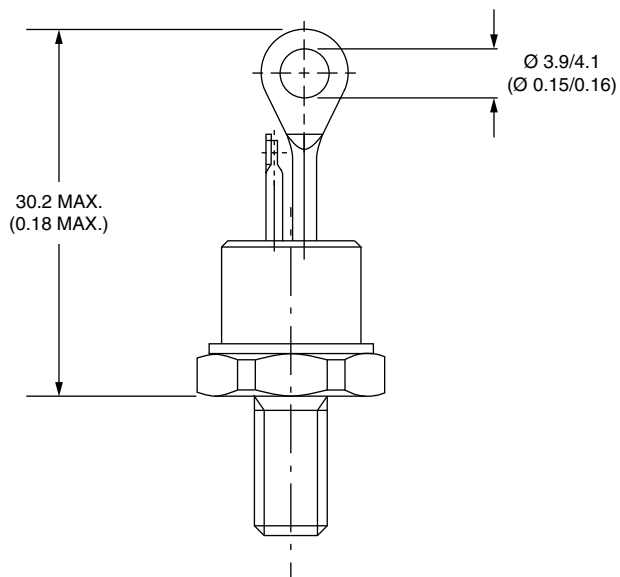
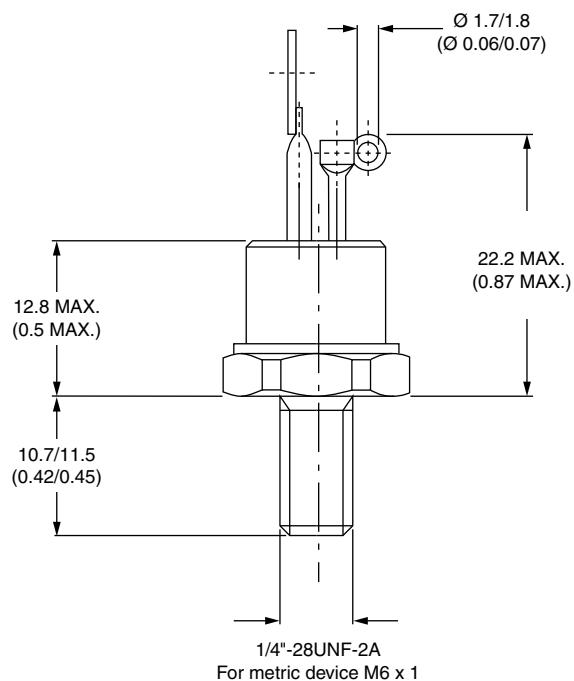
Segment	Value	Position
1	10	1
2	RIA	2
3	120	3
4	M	4
5	S90	5

- 1** - Current code
- 2** - Essential part number
- 3** - Voltage code x 10 = V_{RRM} (see Voltage Ratings table)
- 4** - None = Stud base TO-208AA (TO-48) 1/4" 28UNF-2A
M = Stud base TO-208AA (TO-48) M6 x 1
- 5** - Critical dV/dt:
None = 300 V/ μ s (standard value)
S90 = 1000 V/ μ s (special selection)

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95333

TO-208AA (TO-48)

DIMENSIONS in millimeters (inches)





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