# DATASHEET

# SIX CHANNEL HD AUDIO CODECS

## DUAL CAPLESS HEADPHONE AMPLIFIERS

# 92HD66C

## DESCRIPTION

The 92HD66C is a low power optimized, high fidelity, 6-channel audio codec compatible with Intel's High Definition (HD) Audio Interface.

The 92HD66C provides high quality, HD Audio capability to notebook and desktop PC applications.

## FEATURES

- **6 Channels (2 stereo ADCs) with 24-bit resolution**
- **Full HDA015-B and EuP low power support**
  - Audio inactivity transitions codec from D0 to D3 low power mode
  - Resume from D3 to D0 with audio activity in < 10 msec
  - D3 to D0 transition with < -65dB pop/click
  - Port presence detect in D3 with or without bit clock
  - PC beep wake up in D3
  - Additional vendor specific modes for even lower power
- **Microsoft WLP premium logo compliant**
- **4 or 5 analog ports with port presence detect***
- **3 integrated headphone amplifiers**
- **2 Capless headphone amplifiers**
- **3 or 4 ports support adjustable microphone bias***
- **Dual SPDIF outputs for WLP compliant support of simultaneous HDMI and SPDIF output**
- **SPDIF Input**
- **Two digital microphone inputs (mono, stereo or quad)**
- **High performance analog mixer**
- **Support for 1.5V and 3.3V HDA signaling**
- **Integrated AVDD LDO for improved PSRR**
- **+5 V or +3.3V analog power supply**
- **Digital and Analog PC Beep to all outputs**
- **48-pin or 40-pin QFN RoHS packages**

## SOFTWARE SUPPORT

- **Intuitive TSI HD Sound graphical user interface that allows configurability and preference settings**
- **12 band fully parametric equalizer**
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode "presets" tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- **Dynamics Processing**
  - Enables improved voice articulation
  - Compressor/limiter allows higher average volume level without resonances or damage to speakers.
- **TSI Vista APO wrapper**
  - Enables multiple APOs to be used with the TSI Driver
- **Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression**
- **Dynamic Stream Switching**
  - Improved multi-streaming user experience with less support calls
- **Broad 3rd party branded software including Creative, Dolby, DTS, and SRS**

## DEVICE OPTIONS

- **6 Channel, 48-pin QFN package**
- **6 Channel, 40-pin QFN package**

  - ***40-pin package removes**
    - Port E and related VREF_Out
    - Mono Out
    - GPIO 4


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# 1. DESCRIPTION

## 1.1. Overview

The 92HD66C provide stereo 24- bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. SPDIF outputs support sample rates of 192kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. SPDIF input supports 96KHz, 88.2KHz, 48KHz, and 44.1KHz sample rates. Additional sample rates are supported by the driver software.

The 92HD66C supports a wide range of desktop and laptop 6-channel configurations. The 2 independent SPDIF output interfaces provides connectivity to consumer electronic equipment or to a home entertainment system. Simultaneous HDMI and SPDIF output is possible. All inputs can be programmed with 0-30 dB gain in 10 dB steps allowing for line or microphone use of any input.

Port presence detect capabilities allow the CODEC to detect when audio devices are connected to the CODEC. The fully parametric TSI SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The 92HD66C operates with a 3.3V digital supply and a 5V analog supply. It allows for 1.5V and 3.3V HDA signaling; the correct signalling level is selected based on the power supply voltage on the DVDD-IO pin.

The 92HD66C is offered in a 48 or 40 pin QFN Environmental (ROHS) package.

## 1.2. Orderable Part Numbers

| | |
|---|---|
| 92HD66C1X5NDGXyyX | 6ch, 40QFN, 1.5V HDA Signaling, 5V AVDD |
| 92HD66C1X3NDGXyyX | 6ch, 40QFN, 1.5V HDA Signaling, 3.3V AVDD |
| 92HD66C2X5NDGXyyX | 6ch, 40QFN, 3.3V HDA Signaling, 5V AVDD |
| 92HD66C2X3NDGXyyX | 6ch, 40QFN, 3.3V HDA Signaling, 3.3V AVDD |
| 92HD66C3X5NLGXyyX | 6ch, 48QFN, switchable 1.5V or 3.3V HDA Signaling, 5V AVDD |

yy = silicon stepping/revision, contact sales for current data.
Add an “8” to the end for tape and reel delivery.


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# 2. DETAILED DESCRIPTION

## 2.1. Port Functionality

**Table 1. Port Functionality**

| Pins (40-pin) | Pins (48-pin) | Port | Input | Output | Head phone | Mic Bias (Vref pin) | Input boost amp |
|---|---|---|---|---|---|---|---|
| 22/23/32/33 | 29/30/39/40 | A | Yes | Yes | Yes | Yes[1] | Yes |
| 24/25/35/36 | 31/32/42/43 | B | Yes | Yes | Yes | Yes[1] | Yes |
| 14/15 | 19/20 | C | Yes | Yes | | Yes | Yes |
| - | - | D | | | | | |
| - | 15/16 | E | Yes | Yes | | Yes | Yes |
| 12/13 | 17/18 | F | Yes | Yes | Yes | | Yes |
| 40 | 48 | SPDIF_OUT0 | Yes[2] | Yes | | | Yes[3] |
| 38 | 46 | SPDIF_OUT1 | Yes[2] | Yes | | | Yes[3] |
| 37 | 45 | SPDIF_IN | Yes | | | | |
| 3 (CLK=2) | 4 (CLK=2) | DMIC0 | Yes | | | | Yes |

1. Ports A and B provide internal microphone bias on the headphone out pins. No external VrefOut pin is needed.
2. DMIC1
3. Boost amp is only available for DMIC input and is not associated with the pin widget

## 2.2. Port Characteristics

Universal (Bi-directional) jacks are supported on ports A, B, C, E, and F. Ports A, B, and F are designed to drive 32 ohm (nominal) headphones or a 10K (nominal) load. Line Level outputs are intended to drive an external 10K load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 2.8K ohms and above when implementing ports capable of operating as microphone inputs or line outputs. Input ports are 75K (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are greater than 1V rms at 5V (+5%/ -10%) to meet WLP requirements. Line output ports and Headphone output ports on the codec may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports implement anti-pop circuits to prevent pops/clicks associated with turning power on/off or charging and discharging output coupling capacitors (except for cap-less headphone ports). Unused ports should be left unconnected. When updating existing designs to use the codec, ensure that there are no conflicts between the output ports on the codec and existing circuitry.

| AFG Power State | Input Enable | Output Enable | Used as output for DAC/Mixer | Used as output for analog PC_Beep | Used as input for ADC, mixer | Port Behavior |
|---|---|---|---|---|---|---|
| D0-D2 | 1 | 1 | Don't care | Don't care | Yes | Not allowed. Port is active as Input. |
| | 1 | 1 | Don't care | Don't care | No | Not allowed. Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 1 | 0 | NA | NA | Yes | Active - Port enabled as input |


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| AFG Power State | Input Enable | Output Enable | Used as output for DAC/Mixer | Used as output for analog PC_Beep | Used as input for ADC, mixer | Port Behavior |
|---|---|---|---|---|---|---|
| | 1 | 0 | NA | NA | No | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 0 | 1 | currently used by DAC, mixer, beep, or is traditional line or headphone output | | NA | Active - Port enabled as output |
| | 0 | 1 | not currently used by DAC, mixer, beep, and is cap-less headphone output | | NA | Inactive (Power Down) |
| | 0 | 0 | NA | NA | | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D3 | 1 | 1 | NA | NA | Don't care | Not allowed. Port is active as Input. |
| | 1 | 0 | NA | NA | Don't care | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| | 0 | 1 | currently used by DAC, mixer, beep, or is traditional line or headphone output | | Don't care | Low power state. If enabled, Beep will output from the port |
| | 0 | 1 | not currently used by DAC, mixer, beep, and is cap-less headphone output | | Don't care | Inactive (Power Down) |
| | 0 | 0 | NA | NA | Don't care | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D3cold | - | - | | | | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D4 | - | - | | | | Inactive (Power Down) - Port keeps output coupling caps charged if port uses caps. |
| D5 | - | - | | | | Off - Charge on coupling caps (if used) will not be maintained. |

## 2.3. Vref_Out

Ports A, B, C, & E (48-pin package only) support Vref_Out pins for biasing electret cartridge microphones. Settings of 80% AVDD, 50% AVDD, GND, and Hi-Z are supported. Attempting to program a pin widget control with a reserved or unsupported value will cause the associated Vref_Out pin to assume a Hi-Z state and the pin widget control Vref_En field will return a value of '000' (Hi-Z) when read.

## 2.4. Jack Detect

Plugs inserted to a jack are detected using SENSE inputs as described in the tables below. Per ECR15-B, the detection circuit operates when the CODEC is in D0 - D3 and can also operate if both the CODEC and Controller are in D3 (no bus clock.) Jack detection requires that all supplies (analog and digital) are active and stable. When AVDD is not present, the value reported in the pin widget is invalid.

When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in port connectivity is sensed and then


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generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per ECR015-B, this will take less than 10mS.

The following table summarizes the proper resistor tolerances for different analog supply voltages.

.

| AVdd Nominal Voltage (+/- 5%) | Resistor Tolerance Pull-Up | Resistor Tolerance SENSE_A/B |
|---|---|---|
| 4.75V or 5.0V | 1% | 1% |

| Resistor | SENSE_A | SENSE_B |
|---|---|---|
| 39.2K | PORT A | PORT E |
| 20.0K | PORT B | Mono |
| 10.0K | PORT C | SPDIF0/DMIC1 |
| 5.11K | PORT F | SPDIF1/DMIC1 |
| 2.49K | Pull-up to Avreg (X5)<br>Pull-up to AVDD (X3) | Pull-up to Avreg (X5)<br>Pull-up to AVDD (X3) |

.

| Resistor | SENSE_A |
|---|---|
| 39.2K | PORT A |
| 20.0K | PORT B |
| 10.0K | PORT C |
| 5.11K | PORT F |
| 2.49K | Pull-up to Avreg (X5)<br>Pull-up to AVDD (X3) |

See reference design for more information on Jack Detect implementation.

## 2.5. SPDIF Output

Both SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

Note: Peak to peak jitter is currently limited to less than 4.5nS (half of the internal master clock cycle) which does not meet the IEC-60958-3 0.05UI requirement at 192KHz.

The two SPDIF output converters can not be aligned in phase with the DACs. Even when attached to the same stream, the two SPDIF output converters may be misaligned with respect to their frame boundaries.

Per HDA015-B, the SPDIF outputs support the ability to provide clocking information even when no stream is selected for the converter, or when in a low power state. Also, as stated in the DCN, the SPDIF output ports support port presence detect.


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SPDIF Outputs are outlined in tables below. .

| AFG Power State | RESET# | GPIO0 Enable | Input Enable | Output Enable | Keep Alive En | Converter Dig En | Stream ID | Pin Mode | Pin Behavior |
|---|---|---|---|---|---|---|---|---|---|
| D0-D4 | Asserted (Low) | - | - | - | - | - | - | | Hi-Z immediately after power on, otherwise the previous state is retained. |
| D0-D4 | De-Asserted (High) | 0 | 0 | 0 | - | - | - | | Hi-Z |
| D0-D4 | De-Asserted (High) | 1 | - | - | - | - | - | GPIO | Active - Pin reflects GPIO0 configuration (internal pull-down enabled) |
| D0-D4 | De-Asserted (High) | 0 | 1 | 0 | - | - | - | SPDIF IN or DMIC IN | Pin functions as SPDIF input or DMIC input |
| D0 | De-Asserted (High) | 0 | 0 | 1 | 0 | 0 | - | SPDIF OUT | Active - Pin drives 0 |
| | | | | | | 1 | 0 | | Active - Pin drives SPDIF-format, but data is zeroes |
| | | | | | | | 1-15 | | Active - Pin drives SPDIFOut1 data |
| | | | | | 1 | 0 | - | | Active - Pin drives SPDIF-format, but data is zeroes |
| | | | | | | 1 | 0 | | Active - Pin drives SPDIF-format, but data is zeroes |
| | | | | | | | 1-15 | | Active - Pin drives SPDIFOut1 data |
| D1-D2 | De-Asserted (High) | 0 | 0 | 1 | 0 | 0 | - | | Active - Pin drives 0 |
| | | | | | 0 | 1 | - | | Active - Pin drives 0 |
| | | | | | 1 | 0 | - | | Active - Pin drives SPDIF-format, but data is zeroes |
| | | | | | 1 | 1 | - | | Active - Pin drives SPDIF-format, but data is zeroes |
| D3 | De-Asserted (High) | 0 | 0 | 1 | 0 | 0 | - | | Hi-Z |
| | | | | | 0 | 1 | - | | Hi-Z |
| | | | | | 1 | 0 | - | | Active - Pin drives SPDIF-format, but data is zeroes |
| | | | | | 1 | 1 | - | | Active - Pin drives SPDIF-format, but data is zeroes |
| D3cold | De-Asserted (High) | 0 | 0 | 1 | - | - | - | | Hi-Z |
| D4 | De-Asserted (High) | 0 | 0 | 1 | - | - | - | | Hi-Z |
| D5 | - | - | - | - | - | - | - | | Hi-Z |

## 2.6. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz, or 96 KHz, and implements internal Jack Sensing (Port presence Detect).


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A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs.

Status flags from the input stream are updated only after the entire valid block has been received (or at least when all bits of a particular status flag have been received) to ensure that software does not read an invalid mixture of old and new data.

In general, the SPDIF input block does not alter the data received. However, it is sometimes necessary to alter the data when the converter widget settings do not match the stream format. The following table outlines a few cases and the expected behavior.

Port presence detect for SPDIF_IN operates differently from other ports. Once the PLL has locked and valid framing (no errors) has been detected, then the port presence detect bit is set. In D3, and D3 without a clock, it is not possible to check for proper framing. Monitoring of activity (rising and falling edges) is sufficient to verify a change in connectivity in D3. If no clock is present, then the internal oscillator is used until a clock is restored. When the HD Audio bus is in a low power state (reset asserted and clock stopped) the CODEC will generate a Power State Change Request when a change in SPDIF_IN port connectivity is sensed and then generate an unsolicited response after the HD Audio link has been brought out of a low power state and the device has been enumerated. Per HDA015-B, this will take less than 10mS.

**Table 2. SPDIF Behavior**

| Conflict | Behavior | Resolution |
|---|---|---|
| Converter widget rate does not equal the stream rate | Although the SPDIF input block is designed to handle inputs slightly above or below the programmed rate, samples may be lost if the input rate is much higher than the rate programmed into the converter widget. | Program the converter widget with the same rate as indicated by the input stream. |
| Converter widget programmed for a word length less than the word length provided by the input stream | If the input stream indicates non PCM data, the data will be truncated to the requested word length. If LPCM data is indicated in the input stream, the CODEC will round the received data to the requested length.[1] | Program the converter widget with the word length indicated in the input stream. |
| Converter widget programmed with a word length greater than the word length provided by the input stream. | Regardless of content, 24 bits per channel of data will be transferred from the SPDIF input stream to the HD Audio bus interface. Truncation or rounding to the requested word length will be handled as described as above. Any non-zero data in the incoming stream will cause problems. | Program the converter widget with the word length indicated in the input stream. Although not recommended, application or driver software may program the converter widget with a word length of 24 bits, truncate the input to the word length indicated by the input stream, then right extend the data using 0s to the desired word length. |

1. Rounding may be disabled by setting the disable bit (AFG vendor specific verb -see widget list) or setting the SPDIF_IN converter widget Frmt StrmType field to 1 (non-PCM)

## 2.7. Mono Output

The Mono Out port source selection, power state, and mute characteristics are all independently controlled by the mono output port controls. **The mono output pin is not available on the 40-pin package options.**


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The following sources are available for the Mono Out pin:

- DAC0 Output: When selected (by using the port connection list), the DAC0 left and right outputs are summed together.
- DAC1 Output: When selected (by using the port connection list), the DAC1 left and right outputs are summed together.
- DAC2 Output: When selected (by using the port connection list), the DAC2 left and right outputs are summed together.
- Mixer Output: When selected (by using the port connection list), the mixer left and right outputs are summed together.

The stereo inputs are scaled by -6dB and then summed to provide an output that is the average of the two inputs. The full scale output at mono out is designed to be about 0dBV. Like the stereo line and headphone outputs, it is not possible to adjust to a +3dBV output level using a vendor defined verb.

## 2.8. Analog Mixer

The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input. The following inputs are available: The output of the mixer may be sent to the ADC where the ADC record gain can adjust the volume. If the output of the mixer is sent to an analog port, then a separate volume control is provided to adjust the output volume. This mixer output volume control supports a gain range of -46.5dB to 0dB in 1.5dB steps. (Selecting -46.5dB will automatically mute the output.)

- Port A
- Port B
- Port C
- Port E (not available on 40-pin option)
- Port F
- DAC0
- DAC1
- DAC2

## 2.9. ADC Multiplexers

The codec implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (-16 to +30dB gain in 1dB steps) as an output amp and allow a preselection of one of these possible inputs:

- Port A
- Port B
- Port C
- Port E (not available on 40-pin option)
- Port F
- Mixer Output
- DMIC 0
- DMIC 1


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## 2.10. Power Management

The HD Audio specification defines power states, power state widgets, and power state verbs. Power management is implemented at several levels. The Audio Function Group (AFG) , all converter widgets, and all pin complexes support the power state verb F05/705. Converter widgets are active in D0 and inactive in D1-D3.

The following table describes what functionality is active in each power state.

| Function | D0 | D1[1] | D2 | D3 | D3cold | Vendor Specific D4[2] | Vendor SpecificD5[2] |
|---|---|---|---|---|---|---|---|
| SPDIF Outputs | On | On | On (idle) | On (idle)[6] | Off | Off | Off |
| SPDIF Input | On | Off | Off | Off | Off | Off | Off |
| Digital Microphone inputs | On | Off | Off | Off | Off | Off | Off |
| DAC | On | Off | Off | Off | Off | Off | Off |
| D2S | On | Off | Off | Off | Off | Off | Off |
| ADC | On | Off | Off | Off | Off | Off | Off |
| ADC Volume Control | On | Off | Off | Off | Off | Off | Off |
| Ref ADC | On | Off | Off | Off | Off | Off | Off |
| Analog Clocks | On | Off | Off | Off | Off | Off | Off |
| GPIO pins | On | On | On | On[6] | On | On | Off |
| VrefOut Pins | On | On | Off | Off | Off | Off | Off |
| Input Boost | On | On | Off | Off | Off | Off | Off |
| Analog mixer | On | On | Off | Off | Off | Off | Off |
| Mixer Volumes | On | On | Off | Off | Off | Off | Off |
| Analog PC_Beep | On | On | On | On | Off | Off | Off |
| Digital PC_Beep | On | On | On | On[6] | Off | Off | Off |
| Lo/HP Amps | On | On | On | Low Drive[3] | Low Drive[3] | Low Drive[3] | Off |
| VAG amp | On | On | On | Low Drive[4] | Low Drive | Low Drive | Off |
| Port Sense | On | On | On | On[5] | Off | Off | Off |
| Reference Bias generator | On | On | On | On | On | On | Off |
| Reference Bandgap core | On | On | On | On | On | On | Off |
| HD Audio-Link | On | On | On | On[6] | Limited[7] | Off | Off |
| PLL | On | On | On | Off[8] | Off[9] | Off | Off |

**Table 3. Power Management**

1. No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2. D4 and D5 power states are entered only when D3cold is requested. D4 and D5 may be viewed as D3cold behavioral options.
3. VAG is kept active when ports are disabled or in D3/D3cold/D4. PC_Beep is supported in D3 but may be attenuated and distorted depending on load impedance.
4. VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
5. Both AVDD and DVDD must be available for Port Sense to operate.
6. Not active if BITCLK is not running (Controller in D3), but can signal power state change request (PME)
7. Only double function group reset verbs and link reset supported per ECR15b


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8. PLL remains on if SPDIF_Out Keep Alive is enabled. PLL disabled only after DAC fading is complete and SDM has settled.
9. PLL disabled only after DAC fading is complete and SDM has settled.

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under TSI Device Driver control for further power reduction. The analog mixer, line and headphone amps, port presence detect, and internal references may be disabled using vendor specific verbs. Use of these vendor specific verbs will cause pops.

The default power state for the Audio Function Group after reset is D3.

## 2.11. AFG D0

The AFG D0 state is the active state for the device. All functions are active if their power state (if they support power management at their node level) has been set to D0.

## 2.12. AFG D1

D1 is a lower power mode where all converter widgets are disabled. Analog mixer and port functions are active. The part will resume from theD1 to theD0 state within 1 mS.

## 2.13. AFG D2

The D2 state further reduces power by disabling the mixer and port functions. The port amplifiers and internal references remain active to keep port coupling caps charged and the system ready for a quick resume to either the D1 or D0 state. The part will resume from the D2 state to the D0 state within 2mS.

## 2.14. AFG D3

The D3-default state is available for HD Audio compliance. All converters are shut down. Port amplifiers and references are active but in a low power state to prevent pops. Resume times may be longer than those from D2, but still less than 10mS to meet Intel low power goals. The default power state for the Audio Function Group after power is applied is D3.

While in AFG D3, the HD Audio controller may be in a D0 state (HD Audio bus active) or in a D3 state (HD Audio bus held in reset with no Bit_Clk, SData_Out, or Sync activity.) The expected behavior is as follows (see the HDA015-B section for more information):

| Function | HDA Bus active | HDA Bus stopped |
|---|---|---|
| Port Presence Detect state change | Unsolicited Response | Wake Event followed by an unsolicited response |
| GPIO state change | Unsolicited Response | Wake Event followed by an unsolicited response |

### *2.14.1. AFG D3cold*

The D3cold power state is the lowest power state available that does not use vendor specific verbs. While in D3cold, the CODEC will still respond to bus requests to revert to a higher power state (double AFG reset, link reset). However, audio processing, port presence detect, and other functions are disabled. Per the HD Audio bus HDA015-B, the D3cold state is intended to be used just prior to removing power to the CODEC. Typically, power will be removed within 200mS. However, the codec may exit from the D3cold state by generating 2, back-to-back, AFG reset events. Resume time from D3cold is less than 200mS.


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## 2.15. Vendor Specific Function Group Power States D4/D5

The codec introduces vendor specific power states. A vendor defined verb is added to the Audio Function Group that combines multiple vendor specific power control bits into logical power states for use by the audio driver. The 2 states defined offer lower power than the 5 existing states defined in the HD Audio specification and HDA015-B. The Vendor Specific D4 state provides lower digital power consumption relative to D3cold by disabling HD Audio link responses. Vendor specific D5 further reduces power consumption on the digital supply by turning off GPIO drivers, and reduces analog power consumption by turning off all analog circuitry except for reset circuits.

States D4/D5 are not entered until D3cold has been requested so are actually D3cold options rather than true, independent, power states. Software can pre-program the D4 or D5 state as a re-definition of how the part will behave when the D3cold power state is requested or software may enter D3cold, then set the D4 or D5 before performing the power state get command. The preferred method is to request D3cold, then select D4 or D5 as desired.This will reduce the severity of pops encountered when entering D4 or D5.

Both power states require a link reset or removal of DVDD to exit.

The CODEC may pop when using these verbs and transition times to an active state (D1 or D0 for example) may take several seconds.

## 2.16. Vendor Specific Function Group Power State “D5 Kill”

Vendor specific “D5 Kill” places the device in a low power, non responsive, state that is intended to disable the CODEC when, for security reasons, it is desired that no audio playback or recording take place.

State “D5 Kill” is not entered until D3cold has been requested. Software pre-programs both the D4 and D5 state request bits (D4 and D5 = 1) then request D3cold. After responding to the Function Group Power State Get verb (needed to enter D3cold), the CODEC will no longer respond to any link activity. The only way to exit this state is to remove power (Power on reset will set the power state to D3.)

“D5 Kill” is identical to vendor specific D5 with the exception that the CODEC will only exit this state when power is removed.

## 2.17. Low-voltage HDA Signaling

The codec is compatible with either 1.5V or 3.3V HDA bus signaling; in the 48-QFN package the voltage selection is done dynamically based on the input voltage of DVDD_IO.

DVDD_IO is currently not a logic configuration pin, but rather provides the digital power supply to be used for the HDA bus signals.

When in 1.5V mode, the codec can correctly decode BITCLK, SYNC, RESET# and SDO as they operate at 1.5V; additionally it will drive SDI and SDO at 1.5V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

## 2.18. Multi-channel capture

The capability to assign multiple ADC Converters to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are


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still supported this is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) may be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

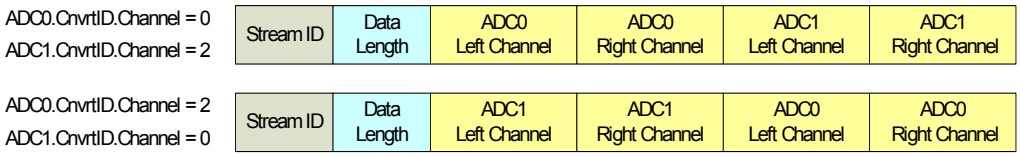
The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

| | | |
|---|---|---|
| **ADC1 CnvtrID** | **(NID = 0x08)** | |
| | [3:0] | Ch = 2 |
| **ADC0 CnvtrID** | **(NID = 0x07)** | |
| | [3:0] | Ch=0 |

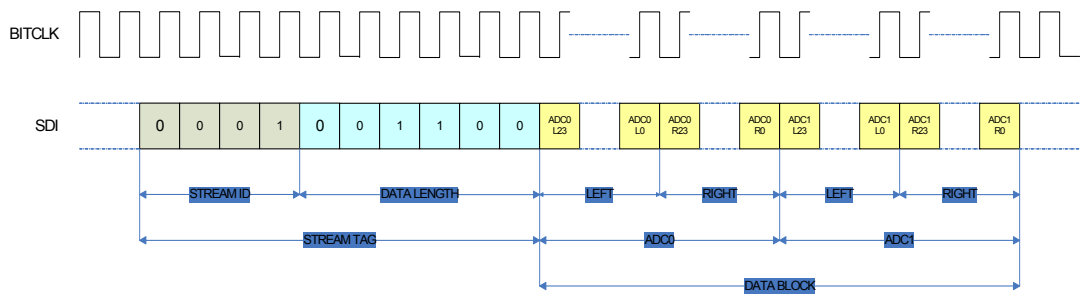
**Table 4. Example channel mapping**

**Figure 1. Multi-channel capture**




The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

**Figure 2. Multi-channel timing diagram**





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| ADC[1:0] Cnvtr | Bit Number | Sub Field Name | Description |
|---|---|---|---|
| | [15] | StrmType | Stream Type (TYPE):<br>0: PCM<br>1: Non-PCM (not supported) |
| | [14] | FrmtSmplRate | Sample Base Rate<br>0= 48kHz<br>1=44.1KHz |
| | [13:11] | SmplRateMultp | Sample Base Rate Multiple<br>000=48kHz/44.1kHz or less<br>001= x2<br>010= x3 (not supported)<br>011= x4 192kHz only, 176.4 not supported<br>100-111= Reserved |
| | [10:8] | SmplRateDiv | Sample Base Rate Divisor<br>000= Divide by 1<br>001= Divide by 2 (not supported)<br>010= Divide by 3 (not supported)<br>011= Divide by 4 (not supported)<br>100= Divide by 5 (not supported)<br>101= Divide by 6 (not supported)<br>110= Divide by 7 (not supported)<br>111= Divide by 8 (not supported) |
| | [6:4] | BitsPerSmpl | Bits per Sample<br>000= 8 bits (not supported)<br>001= 16 bits<br>010= 20 bits<br>011= 24 bits<br>100-111= Reserved |
| | [3:0] | NmbrChan | Number of Channels<br>Number of channels for this stream in each “sample block” of the “packets” in each “frame” on the link.<br>0000=1 channel (not supported)<br>0001 = 2 channels<br>…<br>1111= 16 channels. |
| | [7:4] | Strm | Software-programmable integer representing link stream ID used by the converter widget. By convention stream 0 is reserved as unused. |
| | [3:0] | Ch | Integer representing lowest channel used by converter.<br>0 and 2 are valid Entries<br>If assigned to the same stream, one ADC must be assigned a value of 0 and the other ADC assigned a value of 2. |

**Table 5: Multi-channel**

## 2.19. EAPD

The EAPD pin (pin 47) is a dedicated, bi-directional control pin. Although named External Amplifier Power Down (EAPD) by the HD Audio specification, this pin operates as an external amplifier power up signal. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up (equivalent to D0), and a 0 causes it to power down (equivalent to D3.) When the EAPD value =


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1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value (in the register) may remain 1. The pin defaults to an open-drain configuration (an external pull-up is recommended.)

Per the HD Audio specification and HDA015-B, multiple ports may control EAPD. The EAPD pin assumes the highest power state of all the EAPD bits in all of the pin complexes. The default value of EAPD is 1 (powered on), but the FG power state will override and the pin will be low.

Vendor specific verbs are available to configure this pin. These verbs retain their values across link and single function group resets but are set to their default values by power on reset:

| MODE1 | MODE0 | EAPD Pin Function | Description |
|---|---|---|---|
| 0 | 0 | Open Drain I/O | Value at pin is wired-AND of EAPD bit and external signal.(default) |
| 0 | 1 | CMOS Output | Value of EAPD bit in pin widget is forced at pin |
| 1 | 0 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |
| 1 | 1 | CMOS Input | External signal controls internal amps. EAPD bit in pin widget ignored |

**Table 6. EAPD Pin Mode Select**

| Control Flag | Description |
|---|---|
| EAPD PIN MODE 1:0 | Defines if EAPD pin is used as input, output, or bi-directional port (Open Drain) |
| HP SD | 0 = Amp controlled by EAPD pin only (default) / 1 = Amp controlled by power state (pin and FG) only |
| HP SD MODE | 0 = Amp will mute when disabled (default) / 1 = Amp will shut down (enter a low power state) when disabled |
| HP SD INV | 0 = AMP will power down (or mute) when EAPD pin is low (default) / 1 = Amp will power down (or mute) when EAPD pin is high. |

**Table 7. Control bit descriptions for BTL amplifier and Headphone amplifier enable configurations**

| HP SD | HP SD MODE | HP SD INV | EAPD Pin State | Headphone Amp State |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Amplifier is mute (default[1]) |
| 0 | 0 | 0 | 1 | Amplifier is active |
| 0 | 0 | 1 | 0 | Amplifier is active |
| 0 | 0 | 1 | 1 | Amplifier is mute |
| 0 | 1 | 0 | 0 | Amplifier is in a low power state |
| 0 | 1 | 0 | 1 | Amplifier is active |
| 0 | 1 | 1 | 0 | Amplifier is active |
| 0 | 1 | 1 | 1 | Amplifier is in a low power state |
| 1 | 0 | NA | NA | Amplifier follows pin/function group power state and will mute when disabled |
| 1 | 1 | NA | NA | Amplifier follows pin/function group power state and will enter a low power state when disabled |

**Table 8. BTL Amp Enable Configuration**

1. EAPD bit is set to one by default but the EAPD state is 0 after power-on reset because the function group is not in D0. The state after a single or double function group reset will be compliant with HDA015-B.

***Each Headphone port has its own configuration bits for SD, SD MODE, and SD INV.***


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| Analog BEEP enabled | EAPD Pin value[1] | Description |
|---|---|---|
| 0 | Forced to low when in D2 or D3 | Follows description in HD Audio spec. External amplifier is shut down when pin or function group power state is D2 or D3 independent of value in EAPD bit. |
| 1 | Forced low in D2 or D3 unless port is enabled as output | Power state is ignored if port is enabled as output and port EAPD=1 to allow PC_Beep support in D2 and D3 |

**Table 9. EAPD Analog PC_Beep behavior**

1. When pin is enabled as Open Drain or CMOS output.

| AFG Power State | RESET# | Analog PC_BEEP | Port Power State | Pin Behavior |
|---|---|---|---|---|
| D0-D3 | Asserted (Low) | Enabled[1] | - | Active high immediately after power on, otherwise the previous state is retained across FG and link reset events |
| D0-D3 | Asserted (Low) | Disabled | - | The previous state is retained across FG and link reset events |
| D0 | De-Asserted (High) | - | - | Active - Pin reflects EAPD bit unless held low by external source. |
| D1 | De-Asserted (High) | - | D0-D1 | Active - Pin reflects EAPD bit unless held low by external source. |
| D2 | De-Asserted (High) | Disabled | D0-D2 | Pin forced low to disable external amp |
| D2 | De-Asserted (High) | Enabled | D0-D2 | Active - EAPD Pin high if any port EAPD bit =1 and that port also enabled as output. |
| D3 | De-Asserted (High) | Disabled | D0-D3 | Pin forced low to disable external amp |
| D3 | De-Asserted (High) | Enabled | D0-D3 | Active - EAPD Pin high if any port EAPD bit=1 and that port also enabled as output. |
| D3cold | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D4 | De-Asserted (High) | - | - | Pin forced low to disable external amp |
| D5 | De-Asserted (High) | - | - | Pin Hi-Z (off) |

**Table 10. EAPD Behavior**

1. PC_Beep is automatically routed to ports A, B, D, and F after power-on reset while link reset is active and EAPD will be high to enable an external amplifier. This may be disabled using a vendor specific verb. If the automatic beep path is disabled, beep will still be supported with EAPD active in link reset if Analog Beep is manually enabled and at least one port is configured as an output before entering link reset. If the automatic Beep routing is disabled and Analog Beep has not been manually configured before entering link reset, then the EAPD pin will retain its current state.


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HP AUDIO CONTROL BLOCK DIAGRAM

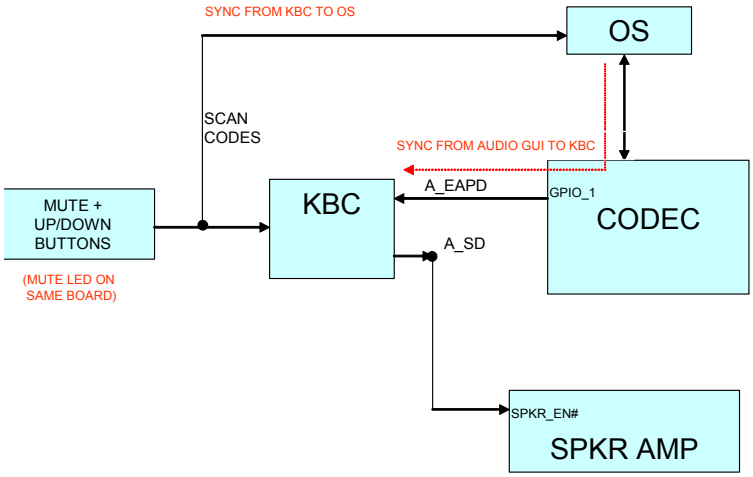


**Figure 3. EAPD System level Example**

## 2.20. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital microphone data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels. This mode is selected using a vendor specific verb and the left time slot is copied to the ADC left and right inputs.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the internal master clock. The default frequency is 2.352Mhz.

The two DMIC data inputs are reported as two stereo input pin widgets that incorporate a boost amplifier. The pin widgets are shown connected to the ADCs through the same multiplexors as the analog ports. Although the internal implementation is different between the analog ports and the digital microphones, the functionality is the same. In most cases, the default values for the DMIC clock rate and data sample phase will be appropriate and an audio driver will be able to configure and use the digital microphones exactly like an analog microphone.

To conserve power, the analog portion of the ADC will be turned off if the D-mic input is selected. When switching from the digital microphone to an analog input to the ADC, the analog portion of the ADC will be brought back to a full power state and allowed to stabilize before switching from the digital microphone to the analog input. This should take less than 10mS.

The DMIC capable pin widgets (NID 1Fh and NID 20h) support port presence detect using SENSE-B input on 2/3 DAC parts in a 48-pin package but not in a 40-pin package. However, the DMIC0 pin widget (NID 11h) does not support presence detect.


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| Digital Mics | Data Sample | ADC Conn. | Notes |
|---|---|---|---|
| 0 | N/A | N/A | No Digital Microphones |
| 1 | Single Edge | 0, or 1 | Available on either DMIC_0 or DMIC_1<br>When using a microphone that supports multiplexed operation (2-mics can share a common data line), configure the microphone for “Left” and select mono operation using the vendor specific verb.<br>“Left” D-mic data is used for ADC left and right channels. |
| 2 | Double Edge on either DMIC_0 or 1 | 0, or 1 | Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability. |
| 3 | Double Edge on one DMIC pin and Single Edge on the second DMIC pin. | 0, or 1 | Requires both DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge (multiplexed output) capability. Two ADC units are required to support this configuration |
| 4 | Double Edge | 0, or 1 | Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don’t support alternative clock edge capability. Two ADC units are required to support this configuration |

**Table 11. Valid Digital Mic Configurations**

| Power State | DMIC Widget Enabled? | DMIC_CLK Output | DMIC_0,1 | Notes |
|---|---|---|---|---|
| D0 | Yes | Clock Capable | Input Capable | DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low |
| D1-D3 | Yes | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D0-D3 | No | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D4 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |
| D5 | - | Clock Disabled | Input Disabled | DMIC_CLK is HIGH-Z with Weak Pull-down |

**Table 12. DMIC_CLK and DMIC_0,1 Operation During Power States**


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**Figure 4. Single Digital Microphone (data is ported to both left and right channels**

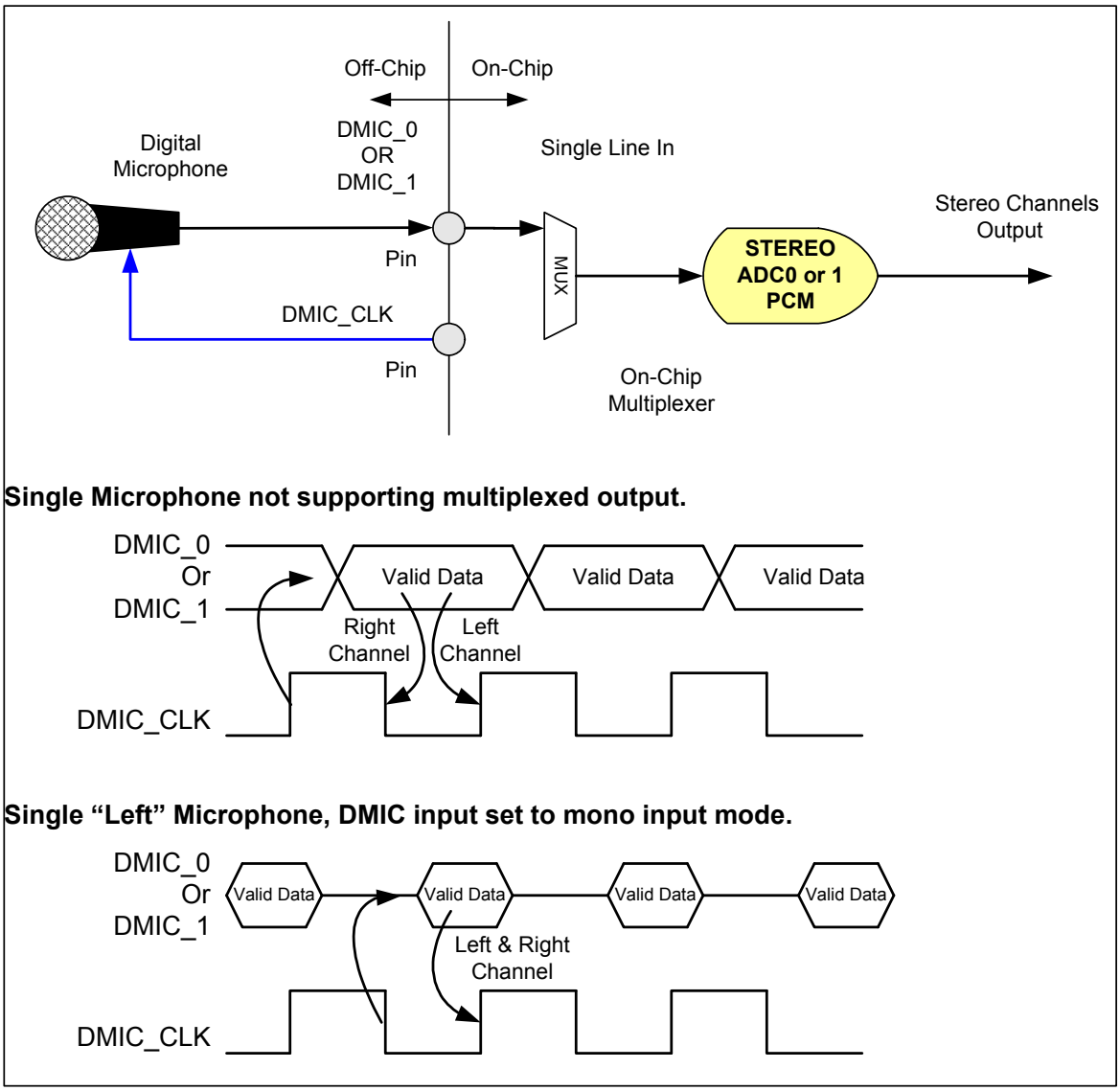



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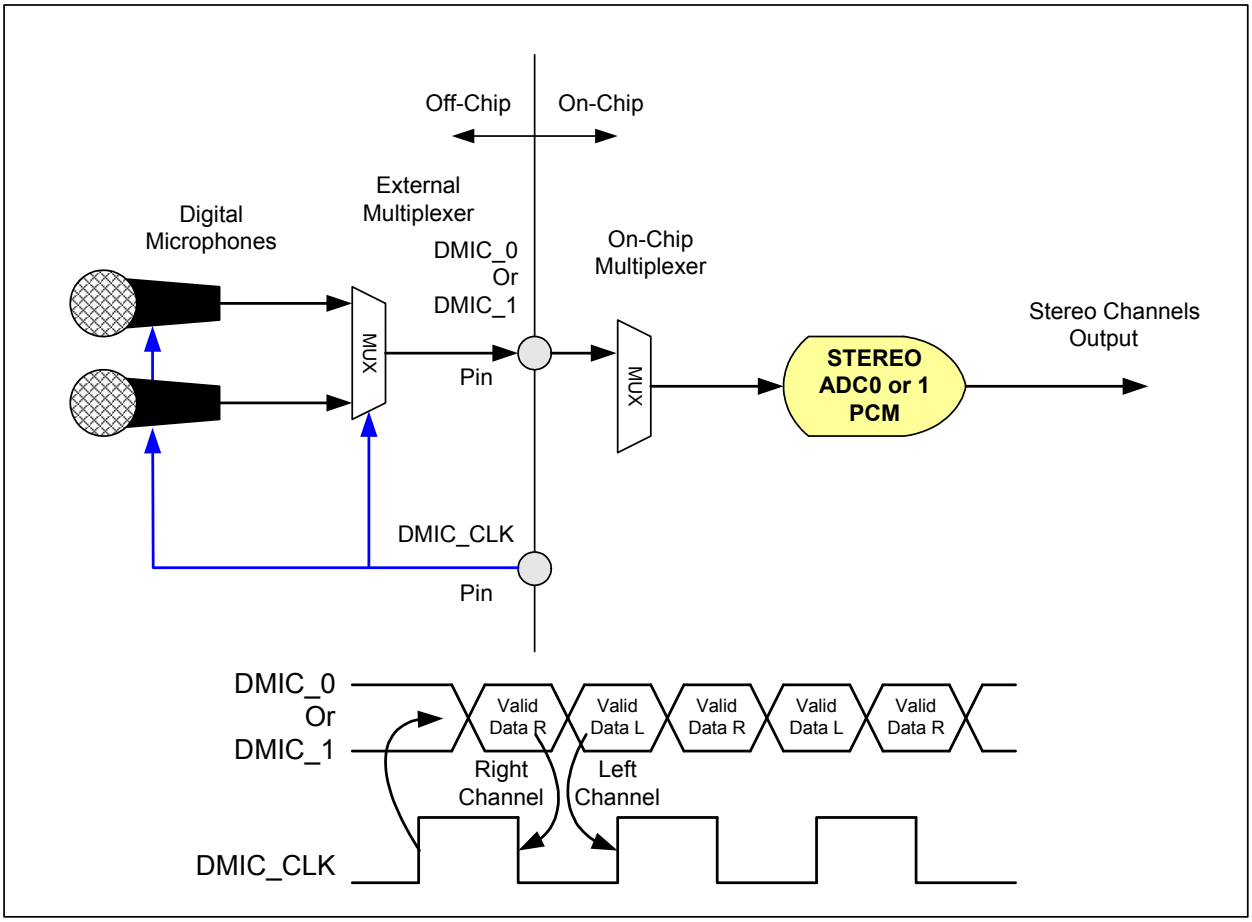
**Figure 5. Stereo Digital Microphone Configuration**




*Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.*


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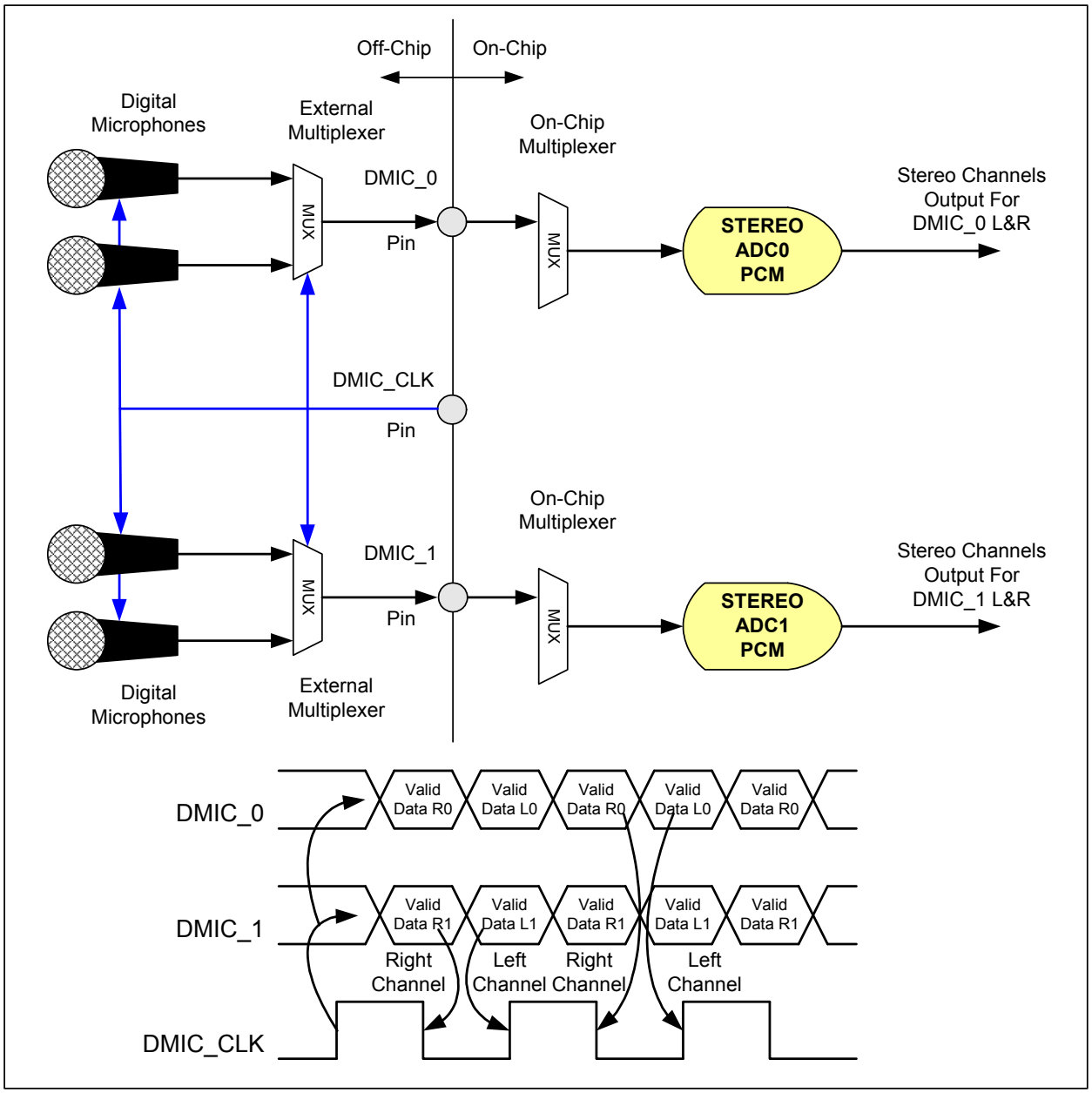
**Figure 6. Quad Digital Microphone Configuration**




*Note: Some Digital Microphone Implementations support data on either edge, in this case the external multiplexer is not required.*

## 2.21. Analog PC-Beep

The codec supports automatic routing of the PC_Beep pin to several outputs when the HD-Link is in reset. The codec will route PC_Beep to ports A, B, and F by default when reset is applied. To prevent pops, beep is not enabled immediately when power is applied. 92HD66B will mute outputs and wait until references and amplifiers have stabilized before enabling beep pass thru after power on reset. To prevent pops when removing power, automatic routing of PC_Beep is not supported in D3cold, D4, or D5.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Analog PC-Beep may also be supported during HD-Link Reset if analog PC_Beep is manually enabled before entering reset. Analog PC_Beep is mixed at the port and only ports enabled as outputs will pass PC_Beep. Analog PC_Beep (or a digital equivalent) must not prevent passing WLP when analog PC_Beep is enabled. Analog PC_Beep, when enabled, must not prevent other audio sources from playing (we must mix not mux.) Beeps from ICH (from Beep.sys) can have a frequency of about 37Hz to about 32KHz. Beep duration is programmable from 1mS to about 32 seconds. A typical beep under Windows XP is 500Hz or 2KHz and lasts 75ms or 150mS. Due to external XOR gates used as mixers, the idle state may be logic 0 or logic 1.

PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced.

Analog PC_Beep is not supported in D3 Cold, or the vendor specific states D4/D5.

Analog PC_Beep is typically used during POST to route error beep codes to internal speakers for diagnostic purposes. When using a legacy OS such as DOS, analog PC_Beep routes “Bell” and “Alarm” tones from the south bridge to internal speakers or headphones. Keyboard controller “Key-click” sounds are also routed to internal speakers using the analog beep function in both Windows and legacy operating systems.

### *2.21.1. PC_Beep Activity Monitor*

An activity monitor will allow the cap-less headphone amplifiers to remain in shutdown when the function group is in D3 until the beep pin is active and then quickly change to an active state (within 10mS) to pass the beep tone.

Beep activity monitoring is only required when the analog beep path is enabled and the CODEC or amplifier is in a low power state (D3).

#### *2.21.1.1. Input Characteristics:*

- There is no correlation between frequency of the tone and duration of the tone.
- There will always be at least one complete cycle
- A minimum input level of -23dBV (200mVpp) is required for proper detection. (Inputs are typically driven by 3.3V CMOS logic followed by 12-20dB attenuation and filtering)
- Beeps from ICH (from Beep.sys) can have a frequency of about 37Hz to about 32KHz and are 1-bit (PFM)
- Beeps from the Keyboard or system management controller are typically PWM (rate unknown but typically 48KHz or less.)
- Beep duration may be from 1mS to ~32 seconds if provided by ICH under OS control.
- A typical beep under Windows XP is 500Hz or 2KHz and lasts 75ms or 150mS
- Due to external XOR gates used as mixers, the idle state may be logic 0 or logic 1

#### *2.21.1.2. Firmware/Software Requirements:*

The reconfiguration outlined in this chapter must be enabled by default (without the help of firmware or OS driver.)

This autonomous mode must not interfere with normal operation.


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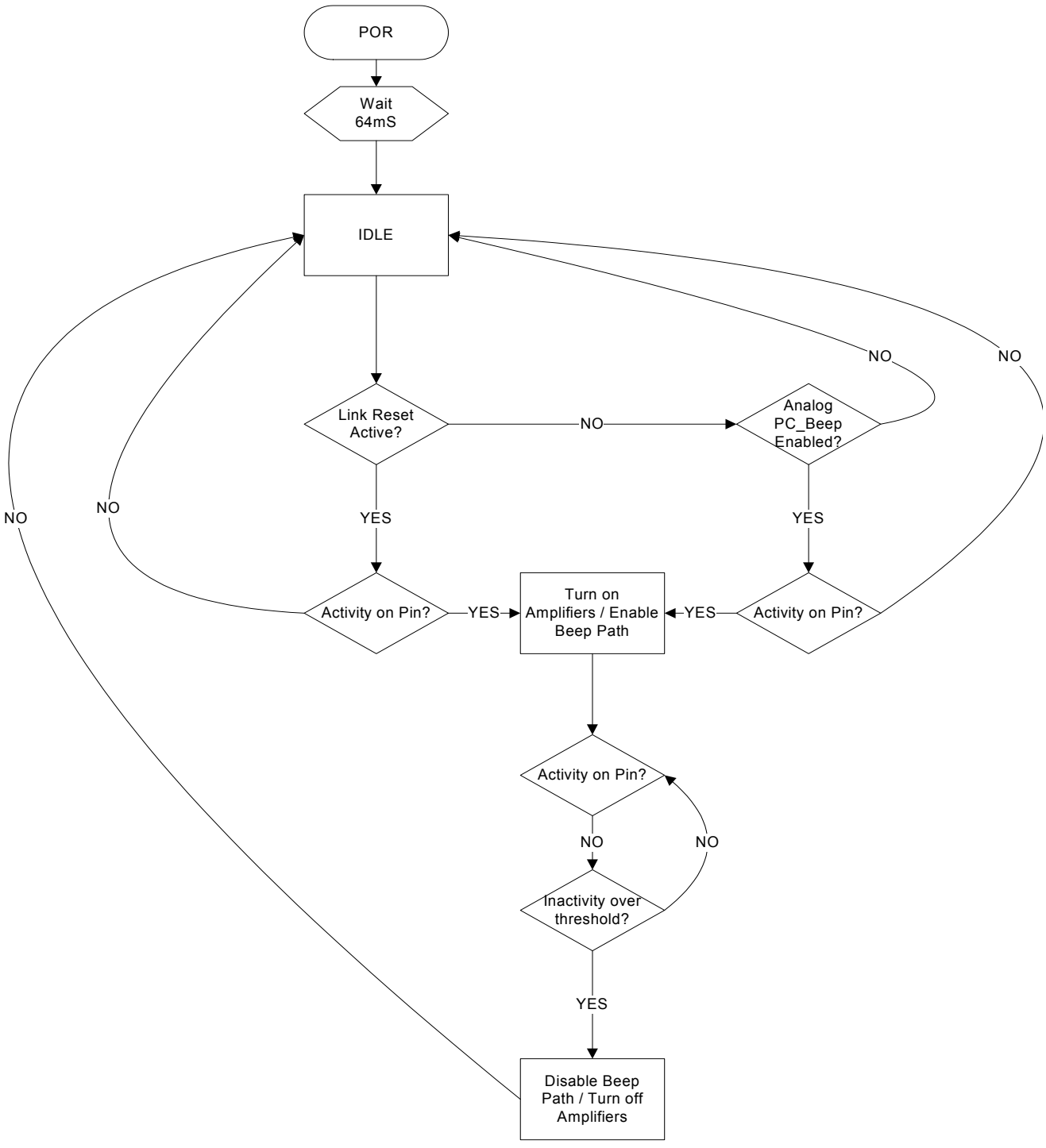
**Figure 7. Analog PCBeep Flow Chart**




Digital detector will detect the “BEEP_SENSE” following the state machine in Figure above and output a signal called “BEEP_PRESENCE”. BEEP_PRESENCE is 1 when the state is Beep _Presence. Otherwise, it is 0.

In the 1ms window, the signal will be sampled and counted in first 500us of 1ms window. The counter will be reset during the second 500us of 1ms window. So the actual sample period is 500us. The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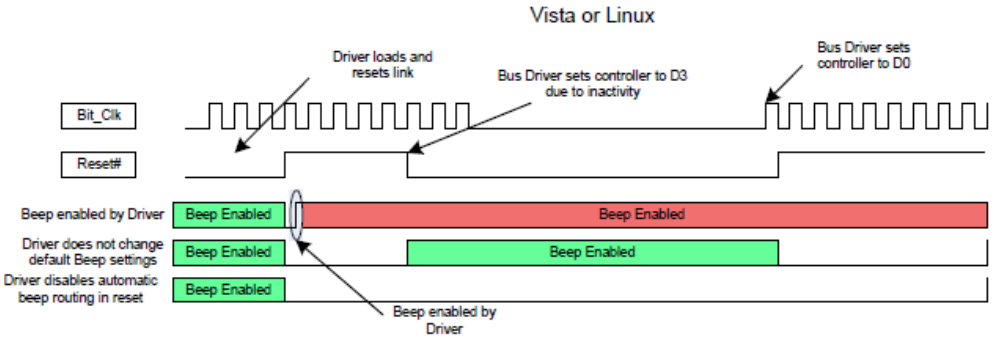
main clock is typically 810KHZ. The threshold_high is 150 cycles (~37%) and the threshold_low is 30 cycles (~7.5%).

If BEEP_PRESENCE=1, it will be cleared until counter is lower than threshold in 1ms window and it repeat for N times. N(1 is for 1ms) can be programmable to one among 64ms, 64ms*2, 64ms*4 and 64ms*8.

#### *2.21.1.3. Logic control*




- **Phase 1:** analog beep auto-routing phase in the period after digital POR, before the first rising edge of link reset.
  - Once Analog PCbeep is detected(BEEP_PRESENCE=1) after 64ms delays (after POR), the Amplifier will be turned on(port_pwd=0, port_output_en=1, there is a timing between these two signals) and analog_beep_en=1. If BEEP_PRESENCE=0 for longer than the threshold time, the amplifiers will be turned off to save power and prevent unwanted system noise from being heard.
- **Phase 2:** When not in phase 1
  - If analog beep function is disabled by driver. Analog beep auto-detect will also be disabled.
  - If analog beep function is enabled by driver.

Once analog PCbeep is detected(BEEP_PRESENCE=1), analog pc_beep will be enabled

If in D0-D2, enabled simply means muting or un-muting beep to avoid hearing system noise on the beep input pin but it is acceptable to turn off port amplifiers if not currently used by DACs, mixer, or beep to save power.

If in D3, enabled means that the necessary amplifiers are turned on so that the beep signal may be heard on all ports configured as outputs (see analog pc-beep description section above)

All needed amplifiers are enabled until BEEP_PRESENCE=0 for longer than the idle threshold

## 2.22. Digital PC-Beep

This block uses an 8-bit divider value to generate the PC beep from the 48kHz HD Audio Sync pulse. The digital PC_Beep block generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). Other audio sources are disabled when digital PC_Beep is active.

It should be noted that digital PC Beep is disabled if the divider = 00h.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PC-Beep may be attenuated and distorted when the CODEC is in D3 depending on the load impedance seen by the output amplifier since all ports are in a low power state while in D3. Load impedances of 10K or larger can support full scale outputs but lower impedance loads will distort unless the output amplitude is reduced. Digital PC_Beep requires a clock to operate and the CODEC will prevent the system from stopping the bus clock while in D3 by setting the Clock_Stop_OK bit to 0 to indicate that the part requires a clock.

## 2.23. Headphone Drivers

The codec implements headphone capable outputs on some ports. The Microsoft Windows Logo Program allows up to the equivalent of 100ohms in series. However, an output level of +3dBV at the pin is required to support 300mV at the jack with a 32ohm load and 1V with a 320 ohm load. Microsoft allows device and system manufactures to limit output voltages to address EU safety requirements. (WLP 3.09 - please refer to the latest Windows Logo Program requirements from Microsoft.) The 92HD66B codec does not implement power limiting. Power limiting may be implemented through the use of an external series resistance.

Although 3 Headphone amplifiers are present, only two may be used simultaneously. Headphone performance will degrade if more than one port is driving a 32 ohm load.

## 2.24. GPIO

### *2.24.1. GPIO Pin mapping and shared functions*

| GPIO # | 48 pin package | 40 pin package | Supply | SPDIF In | SPDIF Out | EAPD | GPI/O | VrefOut | DMIC | Pull Up | Pull Down |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 46 | 38 | DVDD | | YES | | YES | | IN | | 50K |
| 1 | 2 | 2 | DVDD | | | | YES | | CLK | | 50K |
| 2 | 4 | 3 | DVDD | | | | YES | | IN | | 50K |
| 3 | 48 | 40 | DVDD | | YES | | YES | | IN | | 50K |
| 4 | 44 | | DVDD | | | | YES | | | | 50K |

### *2.24.2. Digital Microphone/GPIO Selection*

2 functions are available on the DMIC_CLK/GPIO1 and the DMIC_0/GPIO2 pins. To determine which function is enabled, the order of precedence is followed:

1. If GPIOs are not enabled through the AFG, then at reset, the pins are pulled low by an internal pull-down resistor.
2. If the GPIO 1 is enabled, the 2 DMIC pins become mute (unless programmed for GPIO or SPDIF use) and pin2 becomes GPIO with an internal pull-down.
3. If GPIO2 is enabled through the AFG, pin 4 (3 on 40-pin package) becomes a GPIO and is pulled low by an internal pull-down resistor.
4. If the port is enabled as an input, the digital microphone will be used.
5. If the port is not enabled as an input or if the pin is configured as a GPIO, the digital microphone path will be mute.


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### 2.24.3. SPDIF_OUT/GPIO/DMIC Selection

3 functions are available on the SPDF0/GPIO3/DMIC1 and SPDF1/GPIO0/DMIC1 pins. To determine which function is enabled, the order of precedence is followed:

1. Default at power-on is SPDIF_OUT/DMIC1 for pin 48 (40) and SPDIF_OUT/DMIC1 for pin 46(38)
2. If GPIO is enabled for that pin, it overrides the SPDIF_OUT and DMIC functions for that pin.
3. If the GPIO function is not enabled for that pin, then the DMIC or SPDIF_OUT function may be enabled by setting the pin input or output enable to 1, respectively. (Setting input and output enable to 1 at the same time will only enable DMIC)

*Note: If the pin selected for DMIC1 input is configured as an output or GPIO, the DMIC block will behave as if silence is present at the input.*

| GPIO3 Enable | Dig0Pin Input Enable | Dig0Pin Output Enable | Selected by DMIC1Vol (NID 0x12) | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | NA | Unused (input) |
| | 0 | 1 | NA | SPDIF0 output |
| | 1 | NA | No | Unused (input) |
| | | | Yes | DMIC1 input |
| 1 | NA | NA | NA | GPIO3 |

**Table 13. Dig0Pin (Pin 48/40) Function Selection**

| GPIO0 Enable | Dig1Pin Input Enable | Dig1Pin Output Enable | Selected by DMIC1Vol (NID 0x12) | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | NA | Unused (input) |
| | 0 | 1 | NA | SPDIF1 output |
| | 1 | NA | No | Unused (input) |
| | | | Yes | DMIC1 input |
| 1 | NA | NA | NA | GPIO0 |

**Table 14. Dig1Pin (Pin 46/38) Function Selection**

## 2.25. HD Audio ECR 15b support

The codec implements complete support for the HDA015-B specification building on the support already present in previous products. HDA015-B features supported are:

1. Persistence of many configuration options through bus and function group reset.
2. The ability to support port presence detect in D3 even when the HD Audio bus is in a low power state (no clock.)
3. Fast resume times from low power states: 1ms D1 to D0, 2ms D2 to D0, 10mS D3 to D0.
4. Notification if persistent register settings have been unexpectedly reset.
5. SPDIF Out active in D3 (required)
6. The ability to notify the driver that a clock is necessary so entering D3 with the clock stopped is not permissible


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## 2.26. Digital Core Voltage Regulator

The digital core operates from 1.8V (+/- 10%). Many systems require that the CODEC use a single 3.3V digital supply, so an integrated regulator is included on die. The regulator uses pin 9, DVDD, as its voltage source. The output of the LDO is connected to pin 1 and the digital core. A 10uF capacitor must be placed on pin 1 for proper load regulation and regulator stability.

The digital core voltage regulator is only dependent on DVDD. DVDDIO may be either 3.3 or 1.5V and may precede or follow DVDD in sequence. The CODEC digital logic and I/O (unless referenced to AVDD) will operate in the absence of AVDD. DVDD and AVDD supply sequencing for the application of power and the removal of power is neither defined nor guaranteed. It is common for desktop systems to supply AVDD from the system standby supply and the CODEC will tolerate, indefinitely, the condition where AVDD is active but DVDD and DVDDIO are inactive.

## 2.27. Analog Core Voltage Regulator

Many systems provide only a noisy 5 volt supply that is inappropriate for analog audio so an integrated regulator is included on die to generate the core analog supply of 4.5V. The regulator uses AVDD1 as its voltage source. A 10uF capacitor must be placed on the LDO output pin for proper load regulation and regulator stability. 92HD66C may be ordered with the analog core LDO enabled (5V operation) or bypassed (3.3V operation).

## 2.28. Combo Jack

The codec implements a sophisticated microphone detection algorithm to differentiate between headphones and headsets when implementing 4-conductor “combo” jacks. A programmable sense window (2s to ∞) provides flexibility in managing problematic slow plug insertions and partial insertions. Programmable de-bounce, anti-pop delay, and headphone-microphone unsolicited response delay controls help ensure a robust, pleasing, experience for the end user. Support for a lanyard (“turbo”) switch using TSI’s driver further enhances combo-jack implementations by supporting many common cellular headsets.


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# 3. CHARACTERISTICS

## 3.1. Audio Fidelity

- 5V
  - DAC SNR: >95dB, A-Weighted 4.75V - 5.25V
  - ADC SNR: >90dB, A-Weighted 4.75V - 5.25V
- 3.3V
  - DAC SNR: >90dB, A-Weighted 3.3V
  - ADC SNR: >85dB, A-Weighted 3.3V

## 3.2. Electrical Specifications

### *3.2.1. Absolute Maximum Ratings*

Stresses above the ratings listed below can cause permanent damage to the 92HD66C. These ratings, which are standard values for TSI commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Pin | Maximum Rating |
|---|---|---|
| Analog maximum supply voltage | AVdd | 6 Volts |
| Digital maximum supply voltage | DVdd | 5.5 Volts |
| | PVdd | 6 Volts |
| VREFOUT output current | | 5 mA |
| Voltage on any pin relative to ground | | Vss - 0.3V to Vdd + 0.3V |
| Operating temperature | | 0 $^{o}$C to +70 $^{o}$C |
| Storage temperature | | -55 $^{o}$C to +125 $^{o}$C |
| Soldering temperature | | Soldering temperature information for all available in the package section. |

**Table 15. Electrical Specification: Maximum Ratings**

### *3.2.2. Recommended Operating Conditions*

| Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power Supplies | DVDD_Core | 1.6 | 1.8 | 1.98 | V |
| | DVDD_IO (3.3V signaling) | 3.135 | 3.3 | 3.465 | V |
| | DVDD_IO (1.5V signaling) | 1.418 | 1.5 | 1.583 | V |
| Power Supply Voltage | + 3.3V Digital | 3.135 | 3.3 | 3.465 | V |
| | + 4.75V Analog | 4.500 | 4.750 | 5.000 | V |
| | + 5.0V Analog | 4.750 | 5.000 | 5.250 | |
| | + 3.3V Analog | 3.135 | 3.3 | 03.465 | V |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Case Temperature | $T_{case}$ | | | +90 | °C |

**Table 16. Recommended Operating Conditions**


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***ESD:*** The 92HD66C is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the 92HD66C implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

## 3.3. 92HD66C Analog Performance Characteristics

- 5V AVDD

($T_{ambient}$ = 25 ºC, AVdd = 4.75V (4.5-5.25V), DVdd = 3.3V ± 5% or 1.8V± 10%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0dB FS = 1Vrms for AVdd = 4.75V, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

- 3.3V AVDD

($T_{ambient}$ = 25 ºC, AVdd = 3.3V, DVdd = 3.3V ± 5% or 1.8V ± 10%, AVss=DVss=0V; 20Hz to 20KHz swept sinusoidal input; Sample Frequency = 48 kHz; 0dB FS = 0.707Vrms for AVdd = 3.3V, 10KΩ//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Digital to Analog Converters** | | | | | | |
| Resolution | | All | | 24 | | Bits |
| Dynamic Range[1]: PCM to All Analog Outputs | -60dB FS signal level | 5V<br>3.3V | | 95<br>93 | | dB |
| SNR[2] - DAC to All Mono/Line-Out Ports | Analog Mixer Disabled, PCM data | 5V<br>3.3V | | 98<br>95 | | dB |
| THD+N[3] - DAC to All Mono/Line-Out Ports | Analog Mixer Disabled, -3 dB FS Signal, PCM data | 5V<br>3.3V | | 88<br>83 | | dB |
| SNR[2] - DAC to All Headphone Ports | Analog Mixer Disabled, 10KΩ load, PCM data | 5V<br>3.3V | | 98<br>95 | | dB |
| THD+N[3] - DAC to All Headphone Ports | Analog Mixer Disabled, -3 dB FS Signal, 10Kv load, PCM data | 5V<br>3.3V | | 88<br>83 | | dB |
| SNR2 - DAC to All Headphone Ports | Analog Mixer Disabled, 32Ω load, PCM data | 5V<br>3.3V | | 98<br>95 | | dB |
| THD+N[3] - DAC to All Headphone Ports | Analog Mixer Disabled, -3 dB FS Signal, 32Ω load, PCM data | 5V<br>3.3V | | 71<br>70 | | dB |
| Any Analog Input (ADC) to DAC Crosstalk | 10KHz Signal Frequency | All | -65 | | | dB |
| Any Analog Input (ADC) to DAC Crosstalk | 1KHz Signal Frequency | All | -65 | | | dB |
| DAC L/R crosstalk | DAC to LO or HP 20-15KHz into 10KΩ load | All | -65 | 70 | | dB |
| DAC L/R crosstalk | DAC to HP 20-15KHz into 32Ω load | All | -65 | 75 | | dB |
| Gain Error | Analog Mixer Disabled | All | | | 0.5 | dB |
| Interchannel Gain Mismatch | Analog Mixer Disabled | All | | | 0.5 | dB |
| D/A Digital Filter Pass Band[4] | | All | 20 | | 21,000 | Hz |
| D/A Digital Filter Pass Band Ripple[5] | | All | | | 0.1 | +/- dB |

**Table 17. Analog Performance**


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| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| D/A Digital Filter Transition Band | | All | 21,000 | | 31,000 | Hz |
| D/A Digital Filter Stop Band | | All | 31,000 | | | Hz |
| D/A Digital Filter Stop Band Rejection[6] | | All | -100 | | | dB |
| D/A Out-of-Band Rejection[7] | | All | -55 | | | dB |
| Group Delay (48KHz sample rate) | | All | | | 1 | ms |
| Attenuation, Gain Step Size DIGITAL | | All | | 0.75 | | dB |
| DAC Offset Voltage | | All | | 10 | 20 | mV |
| Deviation from Linear Phase | | All | | 1 | 10 | deg. |
| **Analog Outputs** | | | | | | |
| Full Scale All Mono/Line-Outs | DAC PCM Data | 5V<br>3.3V | 1.00<br>0.707 | | | Vrms |
| Full Scale All Mono/Line-Outs | DAC PCM Data | 5V<br>3.3V | 2.83<br>2.00 | | | Vp-p |
| All Headphone Capable Outputs | 32Ω load | 5V<br>3.3V | 40<br>31 | 60<br>42 | | mW (peak) |
| Amplifier output impedance | Mono/Line Outputs<br>Headphone Outputs | All | | 150<br>0.1 | | Ohms |
| External load Capacitance | Mono/Line Outputs<br>Headphone Outputs | All | | | 220 | pF |
| **Analog Inputs** | | | | | | |
| Full Scale Input Voltage | 0dB Boost @4.75V<br>(input voltage required for 0dB FS output) | 5V<br>3.3V | 1.05<br>0.71 | | | Vrms |
| All Analog Inputs with boost | 10dB Boost | 5V<br>3.3V | 0.320<br>0.225 | | | Vrms |
| All Analog Inputs with boost | 20dB Boost | 5V<br>3.3V | 0.105<br>0.071 | | | Vrms |
| All Analog Inputs with boost | 30dB Boost | 5V<br>3.3V | 0.032<br>0.023 | | | Vrms |
| Boost Gain Accuracy[8] | | All | -2 | | 2 | dB |
| Input Impedance | | All | | 50 | | KΩ |
| Input Capacitance | | All | | 15 | | pF |

**Table 17. Analog Performance**


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| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Analog Mixer** | | | | | | |
| Dynamic Range: PCM to All Analog Outputs | -60dB FS signal level Analog Beep enabled all other mixer inputs mute | 5V<br>3.3V | 90<br>87 | | | dB |
| SNR[2] - All Line-In to all Line-Outs | All inputs unmuted, but only one driven with test signal. | 5V<br>3.3V | 85<br>80 | | | dB |
| THD+N[3] - All Line-In to all Line-Out | 0dBFS Input on one input. All others silent. | 5V<br>3.3V | 65<br>60 | | | dB |
| SNR[2] - DAC to All Line-Out Ports | Analog Beep Enabled, PCM data. all other inputs mute | 5V<br>3.3V | 93<br>93 | | | dB |
| SNR[2] - DAC to All Ports | Analog Mixer Enabled, PCM data all other inputs unmuted/silent | 5V<br>3.3V | 85<br>80 | | | dB |
| THD+N[3] - DAC to All Ports | Analog Mixer Enabled, 0dB FS Signal, PCM data. all other inputs unmuted/silent | 5V<br>3.3V | 72<br>72 | | | dB |
| Attenuation, Gain Step Size ANALOG | | All | - | 1.5 | | dB |
| **Analog to Digital Converter** | | | | | | |
| Resolution | | All | | 24 | | Bits |
| Full Scale Input Voltage | 0dB Boost<br>(input voltage required to generate 0dBFS per AES 17) | 5V<br>3.3V | 1.05<br>0.71 | | | Vrms |
| Dynamic Range[1], All Analog Inputs to A/D | High Pass Filter Enabled, -60dB FS, No boost | 5V<br>3.3V | | 93<br>87 | | dB |
| Full Scale Input Voltage | 20dB Boost<br>(input voltage required to generate 0dBFS per AES 17) | 5V<br>3.3V | 0.105<br>0.071 | | | Vrms |
| Dynamic Range[1], All Analog Inputs to A/D | 20dB Boost<br>High Pass Filter Enabled, -60dB FS | 5V<br>3.3V | | 87<br>83 | | dB |
| THD+N All Analog Inputs to A/D | High Pass Filter enabled, -1/-3 dB FS signal level | 5V<br>3.3V | | 83<br>75 | | dB |
| THD+N All Analog Inputs to A/D | 20dB Boost, High Pass Filter enabled, -1/-3 dB FS signal level | 5V<br>3.3V | | 80<br>75 | | dB |
| Analog Frequency Response[9] | | All | 10 | | 30,000 | Hz |
| A/D Digital Filter Pass Band[4] | | All | 20 | | 21,000 | Hz |
| A/D Digital Filter Pass Band Ripple[5] | | All | | | 0.1 | +/- dB |
| A/D Digital Filter Transition Band | | All | 21,000 | | 31,000 | Hz |
| A/D Digital Filter Stop Band | | All | 31,000 | | | Hz |
| A/D Digital Filter Stop Band Rejection[6] | | All | -100 | | | dB |
| Group Delay | 48 KHz sample rate | All | | | 1 | ms |

**Table 17. Analog Performance**


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| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Any unselected analog Input to ADC Crosstalk | 10KHz Signal Frequency | All | -65 | | | dB |
| Any unselected analog Input to ADC Crosstalk | 1KHz Signal Frequency | All | -65 | | | dB |
| ADC L/R crosstalk | Any selected input to ADC 20-15Khz | All | -65 | | | dB |
| DAC to ADC crosstalk | Any DAC output to ADC 20-15Khz | All | -65 | | | dB |
| Spurious Tone Rejection[10] | | All | | -100 | | dB |
| Attenuation, Gain Step Size (analog) | | All | | 1.5 | | dB |
| Interchannel Gain Mismatch ADC | | All | | | 0.5 | dB |
| **Power Supply** | | | | | | |
| Digital Vreg Core Input Voltage | | | 2.8 | 3.3 | 3.8 | V |
| Digital Vreg Core Output Voltage | | | 1.65 | 1.8 | 1.95 | V |
| Digital Core Vreg Output Current | | | 35 | 50 | | mA |
| Power Supply Rejection Ratio | 10kHz | All | | -60 | | dB |
| Power Supply Rejection Ratio | 1kHz | All | | -70 | | dB |
| D0 Didd[11] | 3.3V, 1.8V | | | 25 | | mA |
| D0 Aidd[11] | 5V, 3.3V | | | 60 | | mA |
| D0 Didd[12] | 3.3V, 1.8V | | | 20 | | mA |
| D0 Aidd[12] | 5V, 3.3V | | | 34 | | mA |
| D1 Didd[13] | 3.3V, 1.8V | | | 7 | | mA |
| D1 Aidd[13] | 5V, 3.3V | | | 30 | | mA |
| D2 Didd | 3.3V, 1.8V | | | 7 | | mA |
| D2 Aidd | 5V, 3.3V | | | 15 | | mA |
| D3 (Beep enabled) Didd[14] | 3.3V, 1.8V | | | 2 | | mA |
| D3 (Beep enabled) Aidd[13] | 5V, 3.3V | | | 7 | | mA |
| D3 Didd[13] | 3.3V, 1.8V | | | 2 | | mA |
| D3 Aidd[13] | 5V, 3.3V | | | 5 | | mA |
| D3cold Didd[13] | 3.3V, 1.8V | | | 1 | | mA |
| D3cold Aidd[13] | 5V, 3.3V | | | 5 | | mA |
| Vendor D4 Didd | 3.3V, 1.8V | | | 0.4 | | mA |
| Vendor D4 Aidd | 5V, 3.3V | | | 5 | | mA |
| Vendor D5 Didd | 3.3V, 1.8V | | | 0.4 | | mA |
| Vendor D5 Aidd | 5V, 3.3V | | | 0.6 | | mA |
| One Stereo ADC Didd | 3.3V, 1.8V | | | 4 | | mA |
| One Stereo ADC Aidd | 5V, 3.3V | | | 8 | | mA |

**Table 17. Analog Performance**


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| Parameter | Conditions | AVdd | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| One Stereo DAC Didd | 3.3V, 1.8V | | | 4 | | mA |
| One Stereo DAC Aidd | 5V, 3.3V | | | 6 | | mA |
| **Voltage Reference Outputs** | | | | | | |
| VREFOut[15] | | All | - | 0.5 X AVdd | | V |
| VREFOut Drive[16] | | All | | 1.6 | | mA |
| VREFILT (VAG) | | All | | 0.45 X AVdd | | V |
| **Phased Locked Loop** | | | | | | |
| PLL lock time | | All | | 96 | 200 | usec |
| PLL (or Azalia Bit CLK) 24MHz clock jitter | | All | | 150 | 500 | psec |
| **ESD / Latchup** | | | | | | |
| IEC1000-4-2 | | All | 1 | | | Level |
| JESD22-A114-B | | All | 2 | | | Class |
| JESD22-C101 | | All | 4 | | | Class |

**Table 17. Analog Performance**

1.Dynamic Range is the ratio of the full scale signal to the noise output with a -60dBFS signal as defined in AES17 as SNR in the presence of signal and outlined in AES6id, measured “A weighted” over 20 Hz to 20 kHz bandwidth.
2.Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3.THD+N ratio as defined in AES17 and outlined in AES6id,non-weighted, swept over 20 Hz to 20 kHz bandwidth as required by WLP 3.09. Results at the jack are dependent on external components and will likely be 1 - 2dB worse.
4.48 kHz or 44.1 kHz Sample Frequency. -1dB upper band limit. -3dB lower band limit.
5.Peak-to-Peak Ripple over Passband meets ± 0.125dB limits, 48 kHz or 44.1 kHz Sample Frequency. 1dB limit.
6.Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7.The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8.Boost gain may be within +/-2dB of target, but actual gain will always ensure that the WLP FSIV requirement will be met and that the boost implementation will not interfere with the +/-0.5dB gain accuracy for the ADC record gain as exposed in the ADC mux widget.
9.± 1dB limits for Line Output & 0 dB gain, at -20dBV
10.Spurious tone rejection is tested with ADC dither enabled and compared to ADC performance without dither.
11.All functions/converters active, pin complexes enabled, two FDX streams, line (10Kohm) loads. Add 24mA analog current per stereo 32 ohm headphone.
12.One stereo DAC and corresponding pin widgets enabled (playback mode)
13.Mixer enabled
14.Idle measurement D3 set for minimum clicks/pops (biases and min. amps. on)
15.Can be set to 50% or 80% of AVdd.
16.Designed to mimic 80% and 50% of 3.3V. 80% setting is nominal 2.6V, 50% setting is nominal 1.6V


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## 3.4. Capless Headphone Supply Characteristics

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| LDO idle current | | 1 | 2 | mA |
| Capless Headphone Amp idle current | | 2 | 3 | |
| Charge Pump idle current | | 4 | 6 | mA |
| Charge Pump shutdown time | | 1 | | mS |
| Charge Pump start-up time | | 10 | | mS |
| Frequency | | 384 | | KHz |
| C1/C2 cap value | | 2.2 | | uF |

**Table 18. Capless Headphone Supply**

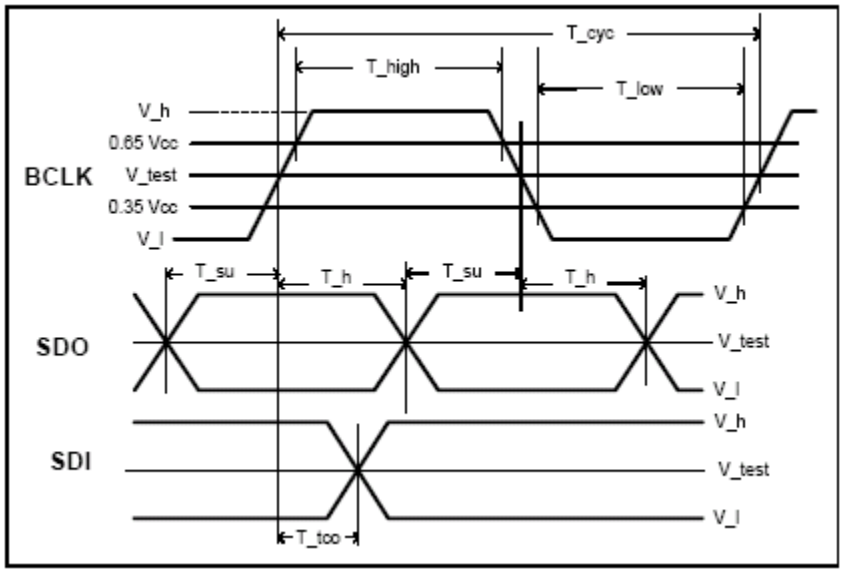
## 3.5. AC Timing Specs

### *3.5.1. HD Audio Bus Timing*

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| BCLK Frequency | Average BCLK frequency | | 23.9976 | 24.0 | 24.0024 | Mhz |
| BCLK Period | Period of BCLK including jitter | Tcyc | 41.163 | 41.67 | 42.171 | ns |
| BCLK High Phase | High phase of BCLK | T_high | 17.5 | | 24.16 | ns |
| BCLK Low Phase | Low phase of BCLK | T_low | 17.5 | | 24.16 | ns |
| BCLK jitter | BCLK jitter | | | 150 | 500 | ps |
| SDI delay | Time after rising edge of BCLK that SDI becomes valid | T_tco | 3 | | 11 | ns |
| SDO setup | Setup for SDO at both rising and falling edges of BCLK | T_su | 5 | | | ns |
| SDO hold | Hold for SDO at both rising and falling edges of BCLK | T_h | 5 | | | ns |

**Table 19. HD Audio Bus Timing**

**Figure 8. HD Audio Bus Timing**





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### 3.5.2. SPDIF Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| SPDIF_OUT Frequency | highest rate of encoded signal<br>64 times the sample rate | | 2.8224 | 3.072 | 12.288 | MHz |
| SPDIF_OUT unit interval | 1/(128 times the sample rate) | UI | 177.15 | 162.76 | 40.69 | ns |
| SPDIF_OUT jitter | SPDIF_OUT jitter | | | | 4.43 | ns |
| SPDIF_OUT rise time | | T_rise | | | 15 | ns |
| SPDIF_OUT fall time | | T_fall | | | 15 | ns |

**Table 20. SPDIF Timing**

### 3.5.3. Digital Microphone Timing

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| DMIC_CLK Frequency | Average DMIC_CLK frequency | | 1.176 | 2.352 | 4.704 | MHz |
| DMIC_CLK Period | Period of DMIC_CLK | Tdmic_cyc | 850.34 | 425.17 | 212.59 | ns |
| DMIC_CLK jitter | DMIC_CLK jitter | | | | 5000 | ps |
| DMIC Data setup | Setup for the microphone data at both rising and falling edges of DMIC_CLK | Tdmic_su | 5 | | | ns |
| DMIC Data hold | Hold for the microphone data at both rising and falling edges of DMIC_CLK | Tdmic_h | 5 | | | ns |

**Table 21. Digital Mic timing**

### 3.5.4. GPIO Characteristics

| Parameter | Definition | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input High Voltage | input level at or above which a 1 is reliably recorded | Vih | 0.6 x VDD | | | V |
| Input Low Voltage | input level at or below which a 0 is reliably recorded<br>VDD may be DVDD or AVDD | Vil | | | 0.35 x VDD | V |
| Output High Voltage | iout = 4mA<br>VDD may be DVDD or AVDD depending on pin | Voh | 0.9 x VDD | | | V |
| Output Low Voltage | iout = -4mA<br>VDD may be DVDD or AVDD depending on pin | Vol | | | 0.1 x VDD | V |
| Input rise/fall time | transition time between 10% and 90% of supply | T_rise/T_fall | | | 10 | ns |
| Input/Tristate High Leakage Current | Vin = VDD<br>VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present) | | | 0.5 | | uA |
| Input/Tristate Low Leakage Current | Vin = 0<br>VDD may be DVDD or AVDD depending on pin (does not include pull-up or pull-down resistor if present) | | | -50 | | uA |

**Table 22. GPIO Characteristics**


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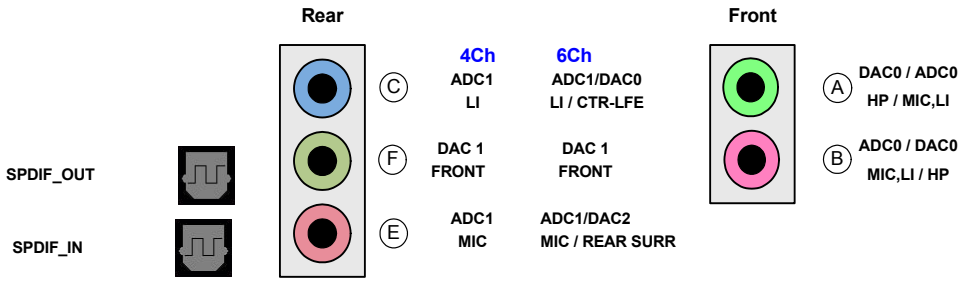
# 4. COMMON PORT CONFIGURATIONS

## Consumer Desktop (default configuration)

### Stereo + RTC + Rear Line/Mic or 5.1




## Mobile 6 Ch

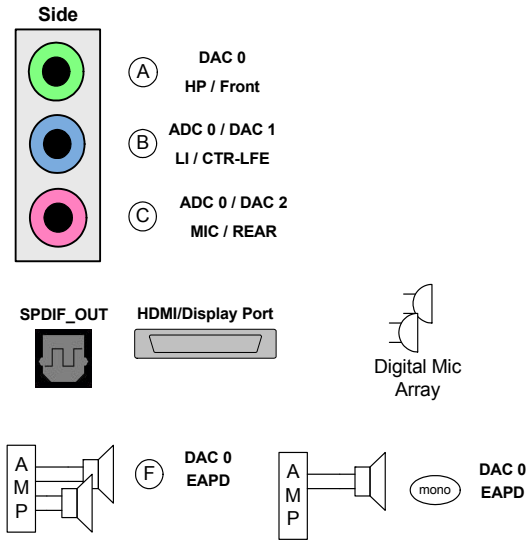



**Figure 9. Common Port Configurations**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# 5. FUNCTIONAL DIAGRAMS

## 5.1. 48-Pin Package

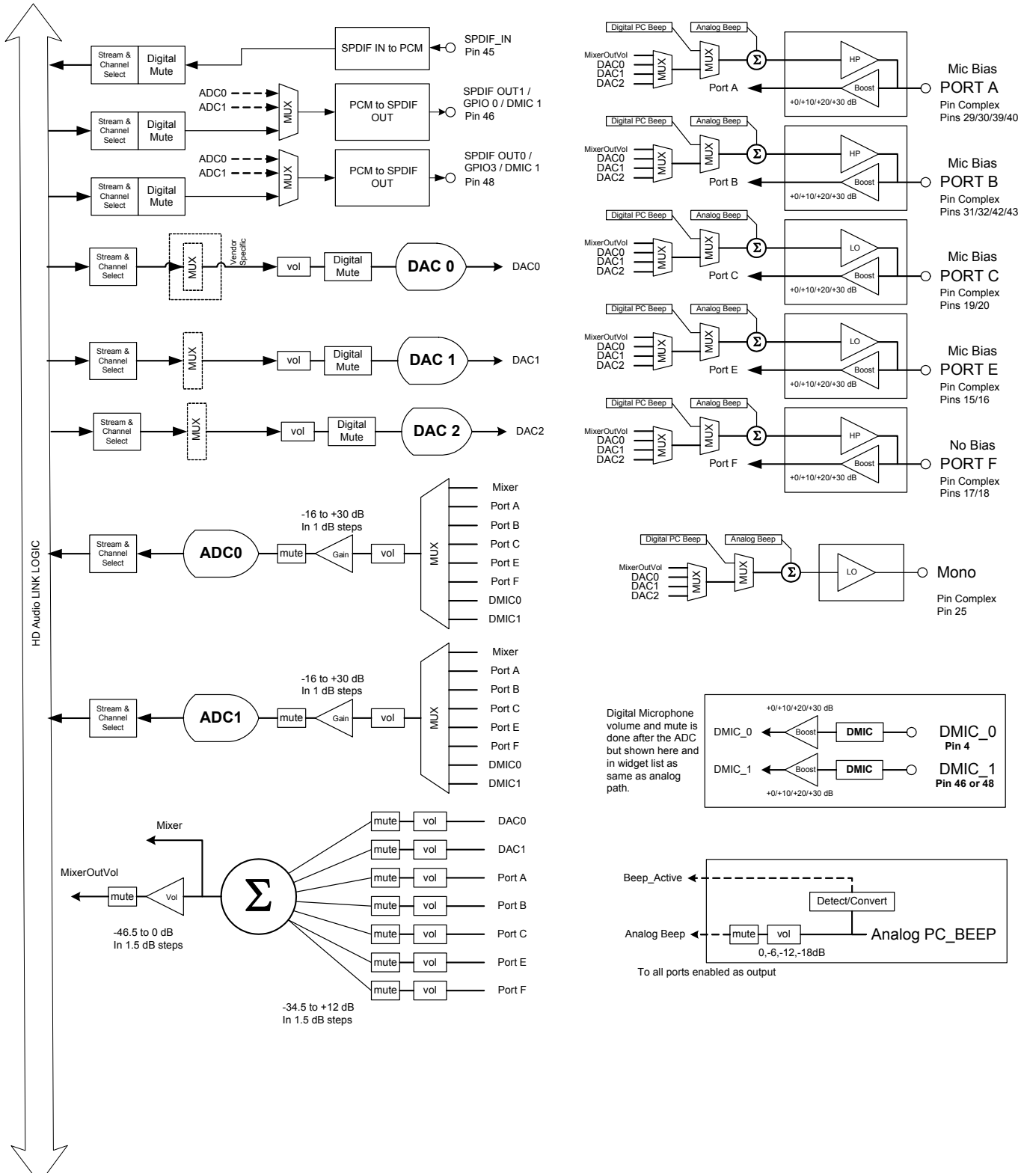


**Figure 10. 48-pin Package Functional Diagram**


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## 5.2. 40-Pin Package

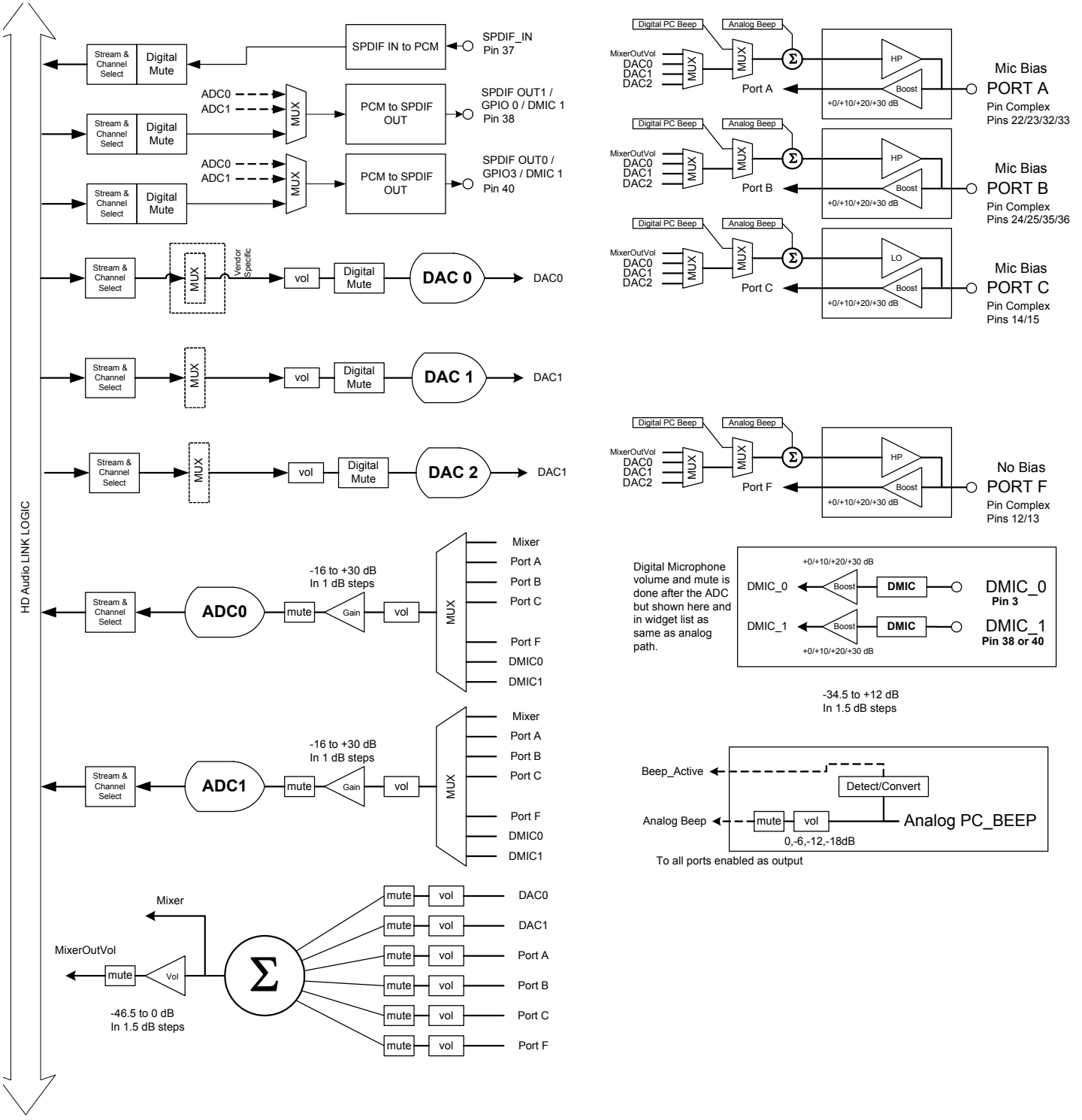


**Figure 11. 40-pin Package Functional Diagram**


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## 5.3. 48-Pin Package Widget Diagram

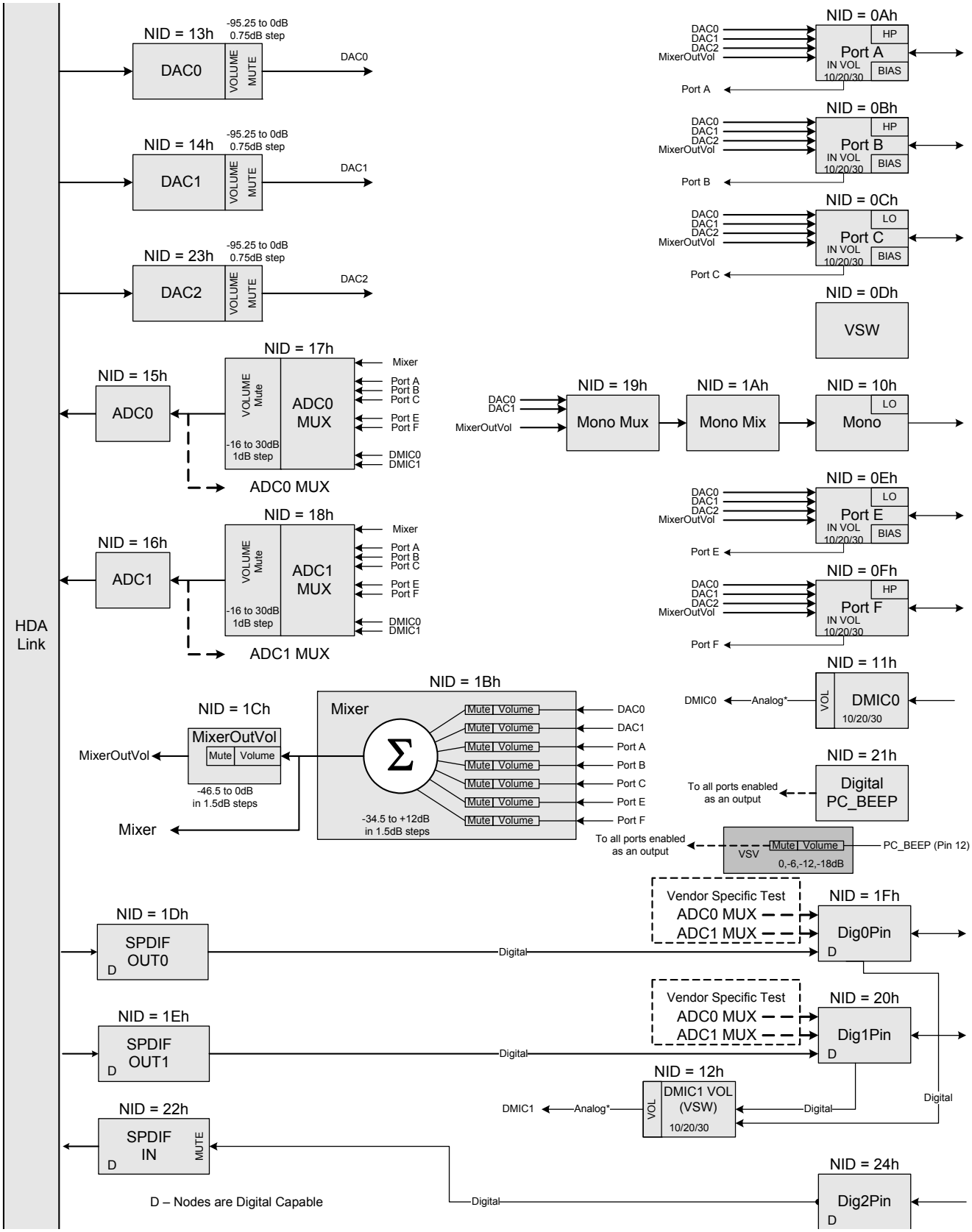


**Figure 12. 48-pin Package Widget Diagram**


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## 5.4. 40-Pin Package Widget Diagram

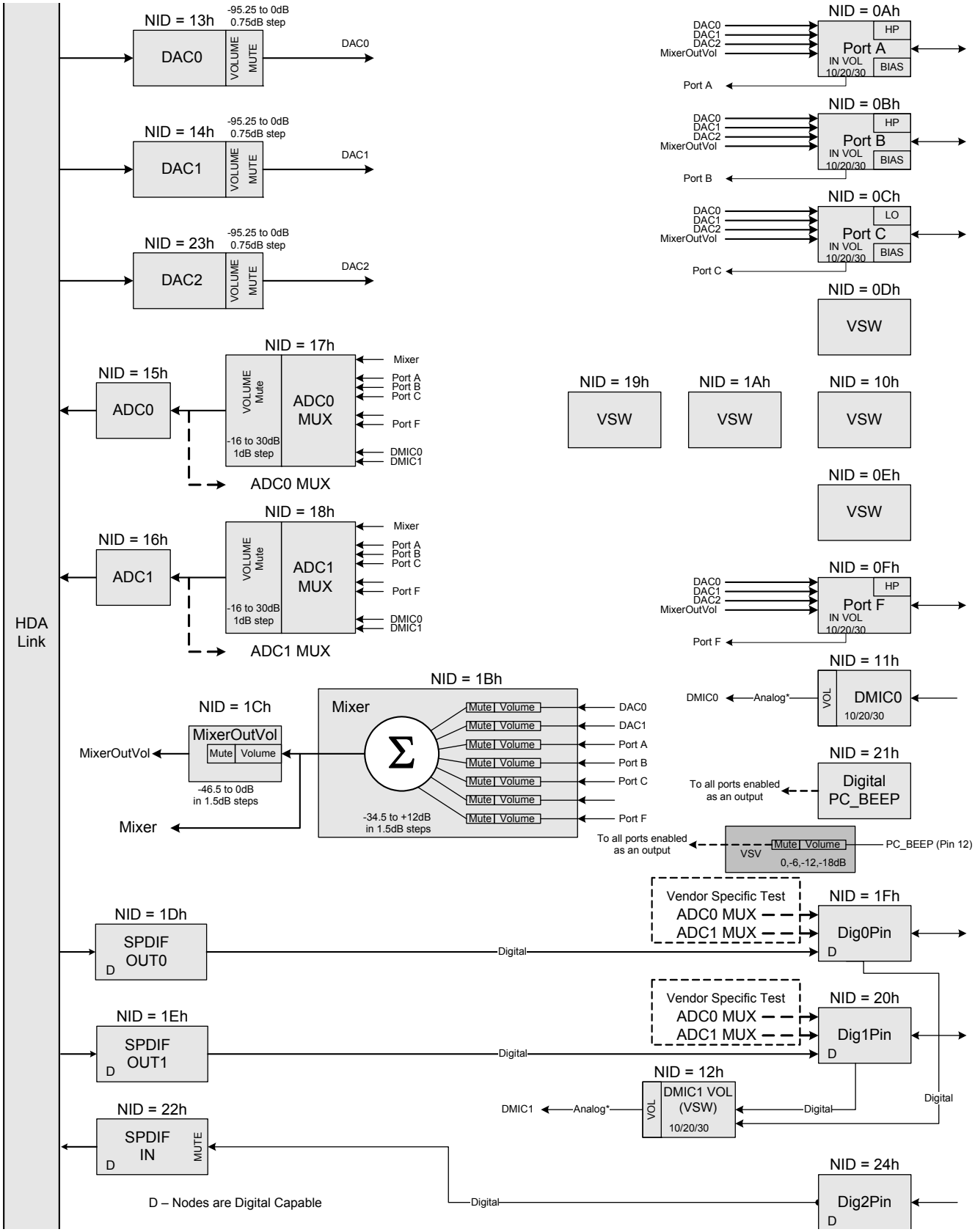


**Figure 13. 40-pin Package Widget Diagram**


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## 5.5. 48-Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Consumer Desktop 5-jack implementation with 2 jacks in front and 3 jacks in rear. The front panel headphone and mic are dedicated to RTC as suggested by Microsoft. SPDIF_OUT is implemented as an SPDIF optical out jack. SPDIF_In is implemented as an optical input. Digital Microphones are listed as part of the muxed capture device.

| Pin Name | Port | Location | Device | Connection | Color | Misc | Assoc. | Seq |
|---|---|---|---|---|---|---|---|---|
| PortAPin | Jack<br>00b | Main Front<br>2h | HP Out<br>2h | 1/8 inch Jack<br>1h | Green<br>4h | Jack Detect Override=0 | 1h | 0h |
| PortBPin | Jack<br>00b | Main Front<br>2h | Mic In<br>Ah | 1/8 inch Jack<br>1h | Pink<br>9h | Jack Detect Override=0 | 2h | 0h |
| PortCPin | Jack<br>00b | Main Rear<br>1h | Line In<br>8h | 1/8 inch Jack<br>1h | Blue<br>3h | Jack Detect Override=0 | 4h | Eh |
| PortEPin | Jack<br>00b | Main Rear<br>1h | Mic In<br>Ah | 1/8 inch Jack<br>1h | Pink<br>9h | Jack Detect Override=0 | 4h | 0h |
| PortFPin | Jack<br>00b | Main Rear<br>1h | Line Out<br>0h | 1/8 inch Jack<br>1h | Green<br>4h | Jack Detect Override=0 | 3h | 0h |
| MonoOutPin | No Connect<br>01b | NA<br>000000b | Other<br>Fh | Unknown<br>0h | Unknown<br>0h | Jack Detect Override=0 | Fh | 0h |
| DMIC0Pin | Internal<br>10b | Internal<br>010000b | Mic In<br>Ah | ATAPI<br>3h | Unknown<br>0h | Jack Detect Override=1 | 4h | 1h |
| Dig0Pin | Jack<br>00b | Main Rear<br>000001b | SPDIF Out<br>4h | optical<br>5h | Black<br>1h | Jack Detect Override=1 | 5h | 0h |
| Dig1Pin | Jack<br>10b | Internal<br>011000b | Digital Other Out<br>5h | Other Digital<br>6h | Unknown<br>0h | Jack Detect Override=1 | 6h | 0h |
| Dig2Pin | Jack<br>00b | Main Rear<br>000001b | SPDIF IN<br>Ch | optical<br>5h | Gray<br>2h | Jack Detect Override=0 | 7h | 0h |


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## 5.6. 40-Pin Configuration Default Register Settings

The following table shows the Pin Widget Configuration Default settings. Common Desktop 4-jack implementation with 2 jacks in front and 2 jacks in rear. The front panel headphone and mic are dedicated to RTC as suggested by Microsoft. SPDIF_OUT is implemented as an SPDIF optical out jack. SPDIF_In is implemented as an optical input. Digital Microphones are listed as part of the muxed capture device.

| Pin Name | Port | Location | Device | Connection | Color | Misc | Assoc. | Seq |
|---|---|---|---|---|---|---|---|---|
| PortAPin | Jack<br>00b | Main Front<br>2h | HP Out<br>2h | 1/8 inch Jack<br>1h | Green<br>4h | Jack Detect Override=0 | 1h | 0h |
| PortBPin | Jack<br>00b | Main Front<br>2h | Mic In<br>Ah | 1/8 inch Jack<br>1h | Pink<br>9h | Jack Detect Override=0 | 2h | 0h |
| PortCPin | Jack<br>00b | Main Rear<br>1h | Line In<br>8h | 1/8 inch Jack<br>1h | Blue<br>3h | Jack Detect Override=0 | 4h | Eh |
| PortFPin | Jack<br>00b | Main Rear<br>1h | Line Out<br>0h | 1/8 inch Jack<br>1h | Green<br>4h | Jack Detect Override=0 | 3h | 0h |
| DMIC0Pin | Internal<br>10b | Internal<br>010000b | Mic In<br>Ah | ATAPI<br>3h | Unknown<br>0h | Jack Detect Override=1 | 4h | 1h |
| Dig0Pin | Jack<br>00b | Main Rear<br>000001b | SPDIF Out<br>4h | optical<br>5h | Black<br>1h | Jack Detect Override=1 | 5h | 0h |
| Dig1Pin | Jack<br>10b | Internal<br>011000b | Digital Other Out<br>5h | Other Digital<br>6h | Unknown<br>0h | Jack Detect Override=1 | 6h | 0h |
| Dig2Pin | Jack<br>00b | Main Rear<br>000001b | SPDIF IN Ch | optical<br>5h | Gray<br>2h | Jack Detect Override=0 | 7h | 0h |


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# 6. WIDGET INFORMATION

## 6.1. Widget List

| Node ID | 48-Pin Package | 40-Pin Package |
|---|---|---|
| 00h | Root | Root |
| 01h | AFG | AFG |
| 0Ah | Port A | Port A |
| 0Bh | Port B | Port B |
| 0Ch | Port C | Port C |
| 0Dh | VSW | VSW |
| 0Eh | Port E | VSW |
| 0Fh | Port F | Port F |
| 10h | Mono Out | VSW |
| 11h | DMIC0 | DMIC0 |
| 12h | VSW (DMIC1 VOL) | VSW (DMIC1 VOL) |
| 13h | DAC0 | DAC0 |
| 14h | DAC1 | DAC1 |
| 15h | ADC0 | ADC0 |
| 16h | ADC1 | ADC1 |
| 17h | ADC0Mux | ADC0Mux |
| 18h | ADC1Mux | ADC1Mux |
| 19h | MonoMux | VSW |
| 1Ah | MonoMix | VSW |
| 1Bh | Mixer | Mixer |
| 1Ch | MixerOutVol | MixerOutVol |
| 1Dh | SPDIFOut0 | SPDIFOut0 |
| 1Eh | SPDIFOut1 | SPDIFOut1 |
| 1Fh | Dig0Pin | Dig0Pin |
| 20h | Dig1Pin | Dig1Pin |
| 21h | DigBeep | DigBeep |
| 22h | SPDIFIN | SPDIFIN |
| 23h | DAC2 | DAC2 |
| 24h | Dig2Pin | Dig2Pin |

**Table 23. High Definition Audio Widget**


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## 6.2. Widget Descriptions

| Widget Name | Description |
|---|---|
| Root | Root Node |
| AFG | Audio Function Group |
| Port X | Port X (A, B, Etc.) Pin Widget |
| Port MonoOut | Port MonoOut Pin Widget (output only) |
| DigMic N | Digital Microphone Pin Widget (N represents the instance) |
| DACN | Stereo Output Converter to DAC (N represents the instance) |
| ADCN | Stereo Input Converter to ADC (N represents the instance) |
| ADCNMux | ADC N Mux with volume and mute |
| Mono Mux | Mono output source select |
| Mono Mix | Stereo to mono conversion |
| Mixer | Input/Output Mixer (Input Ports, DACs) |
| MixerOutVol | Volume control for analog mixer |
| SPDIFOutN | Digital Output Converter for SPDIF_Out (N represents the instance) |
| DigNPin | Digital I/O Pin for SPDIF In/Out (N represents the instance) |
| PCBeep | Digital PC Beep Widget |
| InPortNMux | Input port pre-select for mixer (N represents the instance) |
| VSWN | Vendor Specific Widget (N represents the instance) |

**Table 24. Widget Descriptions**


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## 6.3. Reset Key

| Abbreviation | Description |
|---|---|
| POR | Power On Reset. |
| SAFG | Single AFG Reset - One single write to the Reset Verb in the AFG Node. |
| DAFG | Double AFG Reset - Two consecutive Single AFG Resets with only idle frames (if any) and no Link Resets between. |
| S&DAFG | Single And Double AFG Reset - Either one will cause reset. |
| LR | Link Reset - Level sensitive reset anytime the HDA Reset is set low. |
| ELR | Exiting Link Reset - Edge sensitive reset any time the HDA Reset transitions from low to high. |
| ULR | Unexpected Link Reset - Level sensitive reset anytime the HDA Reset is set low when the ClkStopOK indicator is currently set to 0. |
| PS | Power State Change - Reset anytime the Actual Power State changes for the Widget in question. |

## 6.4. Root (NID = 00h): VendorID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Vendor | 31:16 | R | 111Dh | N/A |
| | Vendor ID. | | | |
| DeviceFix | 15:8 | R | see below | N/A |
| | Device ID. | | | |
| DeviceProg | 7:0 | R | see below | N/A |
| | Device ID. | | | |

| Device | 92HD66C1X5 | 92HD66C2X5 | 92HD66C3X5 | 92HD66C1X3 | 92HD66C2X3 |
|---|---|---|---|---|---|
| Device ID | 76EBh | 76ECh | 76EDh | 76F1h | 76F2h |


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### 6.4.1. Root (NID = 00h): RevID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Major | 23:20 | R | 1h | N/A (Hard-coded) |
| | Major rev number of compliant HD Audio spec. | | | |
| Minor | 19:16 | R | 0h | N/A (Hard-coded) |
| | Minor rev number of compliant HD Audio spec. | | | |
| RevisionFix | 15:12 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| RevisionProg | 11:8 | R | xh | N/A (Hard-coded) |
| | Vendor's rev number for this device. | | | |
| SteppingFix | 7:4 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |
| SteppingProg | 3:0 | R | xh | N/A (Hard-coded) |
| | Vendor stepping number within the Vendor RevID. | | | |

### 6.4.2. Root (NID = 00h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| StartNID | 23:16 | R | 01h | N/A (Hard-coded) |
| | Starting node number (NID) of first function group | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 01h | N/A (Hard-coded) |
| | Total number of nodes | | | |

## 6.5. AFG (NID = 01h): NodeInfo

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StartNID | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Starting node number for function group subordinate nodes. | | | |
| Rsvd1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| TotalNodes | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Total number of nodes. | | | |

### *6.5.1. AFG (NID = 01h): FGType*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0005h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:9 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| UnSol | 8 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response supported: 1 = yes, 0 = no. | | | |
| NodeType | 7:0 | R | 1h | N/A (Hard-coded) |
| | Function group type:<br>00h = Reserved<br>01h = Audio Function Group<br>02h = Vendor Defined Modem Function Group<br>03h-7Fh = Reserved<br>80h-FFh = Vendor Defined Function Group | | | |

### *6.5.2. AFG (NID = 01h): AFGCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0008h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 31:17 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| BeepGen | 16 | R | 1h | N/A (Hard-coded) |
| | Beep generator present: 1 = yes, 0 = no. | | | |
| Rsvd2 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| InputDelay | 11:8 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link. | | | |
| Rsvd1 | 7:4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| OutputDelay | 3:0 | R | Dh | N/A (Hard-coded) |
| | Typical latency in frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin. | | | |

### *6.5.3. AFG (NID = 01h): PCMCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

### *6.5.4. AFG (NID = 01h): StreamCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Bh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 0h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

### *6.5.5. AFG (NID = 01h): InAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 0h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 27h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.5.6. AFG (NID = 01h): PwrStateCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Fh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| EPSS | 31 | R | 1h | N/A (Hard-coded) |
| | Extended power states support: 1 = yes, 0 = no. | | | |
| ClkStop | 30 | R | 1h | N/A (Hard-coded) |
| | D3 clock stop support: 1 = yes, 0 = no. | | | |
| LPD3Sup | 29 | R | 1h | N/A (Hard-coded) |
| | Codec state intended during system S3 state: 1 = D3Hot, 0 = D3Cold. | | | |
| Rsvd | 28:5 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| D3ColdSup | 4 | R | 1h | N/A (Hard-coded) |
| | D3Cold power state support: 1 = yes, 0 = no. | | | |
| D3Sup | 3 | R | 1h | N/A (Hard-coded) |
| | D3 power state support: 1 = yes, 0 = no. | | | |
| D2Sup | 2 | R | 1h | N/A (Hard-coded) |
| | D2 power state support: 1 = yes, 0 = no. | | | |
| D1Sup | 1 | R | 1h | N/A (Hard-coded) |
| | D1 power state support: 1 = yes, 0 = no. | | | |
| D0Sup | 0 | R | 1h | N/A (Hard-coded) |
| | D0 power state support: 1 = yes, 0 = no. | | | |


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### 6.5.7. AFG (NID = 01h): GPIOCnt

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0011h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| GPIWake | 31 | R | 1h | N/A (Hard-coded) |
| | Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIO's configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin. | | | |
| GPIUnsol | 30 | R | 1h | N/A (Hard-coded) |
| | GPIO unsolicited response support: 1 = yes, 0 = no. | | | |
| Rsvd | 29:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumGPIs | 23:16 | R | 00h | N/A (Hard-coded) |
| | Number of GPI pins supported by function group. | | | |
| NumGPOs | 15:8 | R | 00h | N/A (Hard-coded) |
| | Number of GPO pins supported by function group. | | | |
| NumGPIOs | 7:0 | R | 05h | N/A (Hard-coded) |
| | Number of GPIO pins supported by function group. | | | |

### 6.5.8. AFG (NID = 01h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 02h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 7Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 7Fh | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.5.9. AFG (NID = 01h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Function Group have been reset. Cleared by PwrState 'Get' to this Widget. | | | |
| ClkStopOK | 9 | R | 1h | POR - DAFG - ULR |
| | Bit clock can currently be removed: 1 = yes, 0 = no. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 6:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 2:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.5.10. AFG (NID = 01h): UnsolResp*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### *6.5.11. AFG (NID = 01h): GPIO*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 715h |
| Get | F1500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Data4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 (Available only on 48-pin versions) | | | |
| Data3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |
| Data0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing "0". For details of read back value, refer to HD Audio spec. section 7.3.3.22 | | | |

### *6.5.12. AFG (NID = 01h): GPIOEn*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 716h |
| Get | F1600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mask4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control (Available only on 48-pin versions) | | | |
| Mask3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control | | | |

### *6.5.13. AFG (NID = 01h): GPIODir*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 717h |
| Get | F1700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Control4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO4: 0 = GPIO is configured as input; 1 = GPIO is configured as output (Available only on 48-pin versions) | | | |
| Control3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO3: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Control2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO2: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO1: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |
| Control0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Direction control for GPIO0: 0 = GPIO is configured as input; 1 = GPIO is configured as output | | | |

### *6.5.14. AFG (NID = 01h): GPIOWakeEn*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 718h |
| Get | F1800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| W4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. (Available only on 48-pin versions) | | | |
| W3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| W1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |
| W0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = When HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link. | | | |

### *6.5.15. AFG (NID = 01h): GPIOUnsol*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 719h |
| Get | F1900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EnMask4 | 4 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO4. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. (Available only on 48-pin versions) | | | |
| EnMask3 | 3 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO2 is configured as input and changes state. | | | |
| EnMask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO1 is configured as input and changes state. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| EnMask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state. | | | |

### 6.5.16. AFG (NID = 01h): GPIOSticky

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 71Ah |
| Get | F1A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mask4 | 4 | RW | 0h | POR - DAFG - ULR |
| | GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). (Available only on 48-pin versions) | | | |
| Mask3 | 3 | RW | 0h | POR - DAFG - ULR |
| | GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |
| Mask2 | 2 | RW | 0h | POR - DAFG - ULR |
| | GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |
| Mask1 | 1 | RW | 0h | POR - DAFG - ULR |
| | GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |
| Mask0 | 0 | RW | 0h | POR - DAFG - ULR |
| | GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). | | | |

### 6.5.17. AFG (NID = 01h): SubID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 723h | 722h | 721h | 720h |


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### 6.5.17. AFG (NID = 01h): SubID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Get | F2300h / F2200h / F2100h / F2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Subsys3 | 31:24 | RW | 00h | POR |
| | Subsystem ID (byte 3) | | | |
| Subsys2 | 23:16 | RW | 00h | POR |
| | Subsystem ID (byte 2) | | | |
| Subsys1 | 15:8 | RW | 01h | POR |
| | Subsystem ID (byte 1) | | | |
| Assembly | 7:0 | RW | 00h | POR |
| | Assembly ID (Not applicable to codec vendors). | | | |

### 6.5.18. AFG (NID = 01h): GPIOPIrty

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 770h |
| Get | F7000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| GP4 | 4 | RW | 1h | POR - DAFG - ULR |
| | GPIO4 Polarity:<br>If configured as output or non-sticky input:<br>0 = inverting<br>1 = non-inverting<br><br>If configured as sticky input:<br>0 = falling edges will be detected<br>1 = rising edges will be detected<br>(Available only on 48-pin versions) | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| GP3 | 3 | RW | 1h | POR - DAFG - ULR |
| | GPIO3 Polarity:<br>If configured as output or non-sticky input:<br>0 = inverting<br>1 = non-inverting<br><br>If configured as sticky input:<br>0 = falling edges will be detected<br>1 = rising edges will be detected | | | |
| GP2 | 2 | RW | 1h | POR - DAFG - ULR |
| | GPIO2 Polarity:<br>If configured as output or non-sticky input:<br>0 = inverting<br>1 = non-inverting<br><br>If configured as sticky input:<br>0 = falling edges will be detected<br>1 = rising edges will be detected | | | |
| GP1 | 1 | RW | 1h | POR - DAFG - ULR |
| | GPIO1 Polarity:<br>If configured as output or non-sticky input:<br>0 = inverting<br>1 = non-inverting<br><br>If configured as sticky input:<br>0 = falling edges will be detected<br>1 = rising edges will be detected | | | |
| GP0 | 0 | RW | 1h | POR - DAFG - ULR |
| | GPIO0 Polarity:<br>If configured as output or non-sticky input:<br>0 = inverting<br>1 = non-inverting<br><br>If configured as sticky input:<br>0 = falling edges will be detected<br>1 = rising edges will be detected | | | |

### *6.5.19. AFG (NID = 01h): GPIODrive*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 771h |
| Get | F7100h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:5 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OD4 | 4 | RW | 0h | POR - DAFG - ULR |
| | GPIO4 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). (Available only on 48-pin versions) | | | |
| OD3 | 3 | RW | 0h | POR - DAFG - ULR |
| | GPIO3 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD2 | 2 | RW | 0h | POR - DAFG - ULR |
| | GPIO2 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD1 | 1 | RW | 0h | POR - DAFG - ULR |
| | GPIO1 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open drain (drive 0, float for 1). | | | |
| OD0 | 0 | RW | 0h | POR - DAFG - ULR |
| | GPIO0 Drive Mode: 0 = push-pull (drive 0 and 1); 1 = open-drain (drive 0, float for 1). | | | |

### *6.5.20. AFG (NID = 01h): DMic*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 778h |
| Get | F7800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mono1 | 5 | RW | 0h | POR |
| | DMic1 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel). | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mono0 | 4 | RW | 0h | POR |
| | DMic0 mono select: 0 = stereo operation, 1 = mono operation (left channel duplicated to the right channel). | | | |
| PhAdj | 3:2 | RW | 0h | POR |
| | Selects what phase of the DMic clock the data should be latched:<br>0h = left data rising edge/right data falling edge<br>1h = left data center of high/right data center of low<br>2h = left data falling edge/right data rising edge<br>3h = left data center of low/right data center of high | | | |
| Rate | 1:0 | RW | 2h | POR |
| | Selects the DMic clock rate:<br>0h = 4.704MHz<br>1h = 3.528MHz<br>2h = 2.352MHz<br>3h = 1.176MHz. | | | |

### *6.5.21. AFG (NID = 01h): DACMode*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 780h |
| Get | F8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SDMSettleDisable | 7 | RW | 0h | POR |
| | SDM wait-to-settle disable:<br>1 = at mute, the SDM switches to the mute pattern immediately<br>0 = at mute, the SDM switches to the mute pattern after settling (can take up to ~45ms) | | | |
| SDMCoeffSel | 6 | RW | 0h | POR |
| | DAC SDM coefficient select (stages 1, 2, 3):<br>1 = 1/16, 1/2, 1/4<br>0 = 1/16, 1/4, 1/2 | | | |
| SDMLFHalf | 5 | RW | 0h | POR |
| | DAC SDM local feedback coefficient select: 1 = 1/4096, 0 = 1/2048. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SDMLFDisable | 4 | RW | 0h | POR |
| | DAC SDM local feedback disable: 1 = local feedback disabled, 0 = local feedback enabled. | | | |
| InvertValid | 3 | RW | 0h | POR |
| | DAC Valid Invert: 1 = 7.056MHz valid strobe is inverted, 0 = 7.056MHz valid strobe is not inverted. | | | |
| InvertData | 2 | RW | 0h | POR |
| | DAC Data Invert: 1 = 1-bit outputs are inverted, 0 = 1-bit outputs are not inverted. | | | |
| Atten6dBDisable | 1 | RW | 1h | POR |
| | Disable built-in -6dB digital attenuation: 1 = -6dB disabled, 0 = -6dB enabled. | | | |
| Fade | 0 | RW | 1h | POR |
| | DAC Gain Fade Enable:<br>1 = gain will be slowly faded from old value to new value (~10ms)<br>0 = gain will jump immediately to new value. | | | |

### *6.5.22. AFG (NID = 01h): ADCMode*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 784h |
| Get | F8400h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:4 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| InvertValid | 3 | RW | 0h | POR |
| | ADC Valid Invert: 1 = 14.112MHz valid strobe is inverted, 0 = 14.112MHz valid strobe is not inverted. | | | |
| InvertData | 2 | RW | 0h | POR |
| | ADC Data Invert: 1 = 1-bit inputs are inverted, 0 = 1-bit inputs are not inverted. | | | |
| ADCClkDelay | 1 | RW | 0h | POR |
| | Delay ADC clock. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| DACClkDelay | 0 | RW | 0h | POR |
| | Delay DAC clock. | | | |

### *6.5.23. AFG (NID = 01h): PortUse*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7C0h |
| Get | FC000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mono | 6 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortF | 5 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortE | 4 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable (Available only on 48-pin versions) | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| PortC | 2 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortB | 1 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable | | | |
| PortA | 0 | RW | 1h | POR |
| | 1=power down port if not input or output enabled, 0=do not force power down based on input or output enable. | | | |


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### 6.5.24. AFG (NID = 01h): ComJack

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 7C7h | 7C6h |
| Get | FC700h/FC600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 31:14 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| ComJackSupport | 11 | RW | 1h | POR |
| | Combo Jack support enable, 0 = disable; 1 = enable | | | |
| RbCon | 10:8 | RW | 4h | POR |
| | Combo jack detection reference voltage<br><br>000 = 0.18*AVDD<br>001 = 0.16*AVDD<br>010 = 0.14*AVDD<br>011 = 0.12*AVDD<br>100 = 0.10*AVDD<br>101 = 0.08*AVDD<br>110 = 0.06*AVDD<br>111 = 0.04*AVDD | | | |
| MasterPort | 7:5 | RW | 0h | POR |
| | Port tied to the jack presence detection switch<br><br>000 = Port A<br>001 = Port B<br>010 = Port C<br>011 = Port D<br>100 = Port E<br>101 = Port F | | | |
| Rsvd1 | 4 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SlavePort | 3:1 | RW | 0h | POR |
| | Port used as microphone input<br><br>When combo jack detection is enabled, Port presence detection as shown in the pin complex is not sensed directly by the sense input but is inferred by the load placed on the Vref_Output associated with the port<br><br>010 = Port C;100 = Port E (Available only on 48-pin versions)<br>others revserved. | | | |
| Det_en | 0 | R | 0h | POR |
| | 0h = disable combo jact detection 1h = enable combo jact detection | | | |

### *6.5.25. AFG (NID = 01h): ComJackTime*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 7CAh | 7C9h |
| Get | FCA00h / FC900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 31:16 | R | 00000h | N/A (Hard-coded) |
| | Reserved. | | | |
| bouncetimer_bypass | 15 | RW | 0h | POR |
| | 0 = all the combjack debounce time in normal; 1= all the comjack debounce time in simulation mode(debounce time is short). | | | |
| t_delay_slave_port_usr | 14:12 | RW | 3h | POR |
| | 000 = 2frame<br>001 =4frame<br>010 =8frame<br>011 =16frame<br>100 = 32frame<br>101 =64frame<br>110 = 128frame<br>111 = 256frame | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| t_stable | 11:8 | RW | 7h | POR |
| | 0000 = 0.1ms<br>0001 =0.5ms<br>0010 =1ms<br>0011 =2ms<br>0100 = 4ms<br>0101 =8ms<br>0110 = 16ms<br>0111 = 32ms<br>1000 = 64ms<br>1001 =128ms;1010 =256ms;1011 =512ms<br>1100 = 1024ms<br>1101 =1024ms<br>1110 = 1024ms<br>1111 = 1024ms | | | |
| Rsvd2 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| t_long_realtime_detect | 6:4 | RW | 5h | POR |
| | 000 = 2s<br>001 =4s<br>010 =8s<br>011 =16s<br>100 = 32s<br>101 =64s<br>110 = 128s<br>111 = infinite | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| t_delay_verfout | 2:0 | RW | 3h | POR |
| | 000 = 0.1ms<br>001 =50ms<br>010 = 125ms<br>011 =250ms<br>100 = 500ms<br>101 = 1s<br>110 = 2s<br>111 = 4s | | | |


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### 6.5.26. AFG (NID = 01h): VSPwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7D8h |
| Get | FD800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| D5 | 1 | RW | 0h | POR - ELR |
| | Vendor specific D5 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If set, this bit overrides the D4 bit (bit 0). Includes the power savings of D4, but additionally powers down GPIO pins, the VAG amp, and the HP amps. Exits this power state via POR or rising edge of Link Reset. | | | |
| D4 | 0 | RW | 0h | POR - ELR |
| | Vendor specific D4 power state, only entered once the part is already in D3cold (this bit must be set before the command to enter D3cold). If the D5 bit (bit 1) is set, this bit is overridden. Includes the power savings of D3cold, but additionally powers down the HDA interface (no responses). Exit this power state via POR or rising edge of Link Reset. | | | |

### 6.5.27. AFG (NID = 01h): AnaPort

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 7EDh | 7ECh |
| Get | FED00h / FEC00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| MonoPwd | 6 | RW | 0h | POR |
| | Power down Mono Output. (Available only on 48-pin versions) | | | |
| FPwd | 5 | RW | 0h | POR |
| | Power down Port F | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| EPwd | 4 | RW | 0h | POR |
| | Power down Port E (Available only on 48-pin versions) | | | |
| Rsvd1 | 3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| CPwd | 2 | RW | 0h | POR |
| | Power down Port C. | | | |
| BPwd | 1 | RW | 0h | POR |
| | Power down Port B. | | | |
| APwd | 0 | RW | 0h | POR |
| | Power down Port A. | | | |


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### 6.5.28. AFG (NID = 01h): AnaBeep

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7EEh |
| Get | FEE00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:9 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Detect | 8 | R | 0h | POR - DAFG - ULR |
| | 0: no beep present; 1: beep present | | | |
| ConvertEn | 7 | RW | 1h | POR |
| | analog pc beep quantization enable (enabled only when both d2a_ana_pc_beep_det_en and d2a_ana_pc_beep_convert_en are 1) | | | |
| DetectEn | 6 | RW | 1h | POR |
| | Analog pc beep detection enable 0h = disable 1h = enable | | | |
| Gain | 5:4 | RW | 3h | POR |
| | Analog PC Beep Gain: 0h = -24dB, 1h = -18dB, 2h = -12dB, 3h = -6dB. | | | |
| CntSel | 3:2 | RW | 0h | POR |
| | Select counter delay.0h=64ms,1h = 128ms, 2h = 256ms, 3h = 512ms. | | | |
| Mode | 1:0 | RW | 2h | POR |
| | Analog PC Beep Mode:<br>00b = Always disabled<br>01b = Always enabled<br>1Xb = Enabled during HDA Link Reset only | | | |

### 6.5.29. AFG (NID = 01h): AnaCapless

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 7FBh | 7FAh | 7F9h | 7F8h |
| Get | FFB00h / FFA00h / FF900h / FF800h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:30 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRegSCDet | 29 | R | 0h | POR |
| | Capless regulator short circuit detect indicator. | | | |
| ChargePumpSCDet | 28 | R | 0h | POR |
| | Capless charge pump short circuit detect indicator. | | | |
| VRegSel | 27:24 | RW | ZA=5h<br>ZB=6h | POR |
| | Capless regulator output voltage multiply ratio<br>Bits [3..2] Reserved<br><br>Bits [1..0]:<br>00b = 2*Vbg<br>01b = 2.1*Vbg<br>10b = 2.2*Vbg<br>11b = 2.3*Vbg | | | |
| VRegSCRstB | 23 | RW | 0h | POR |
| | Capless regulator short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| VRegGndShort | 22 | RW | 0h | POR |
| | Ground the capless regulator output. | | | |
| VRegPwd | 21 | RW | 0h | POR |
| | Capless regulator powerdown. | | | |
| ChargePumpSCRstB | 20 | RW | 0h | POR |
| | Capless charge pump short circuit detect reset: 0 = short circuit detect disabled, 1 = short circuit detect enabled. | | | |
| ChargePumpHiZ | 19 | RW | 0h | POR |
| | Hi-Z the capless charge pump outputs. | | | |
| ChargePumpPwd | 18 | RW | 0h | POR |
| | Capless charge pump powerdown. | | | |
| ChargePumpSplyDetOverride | 17 | RW | 0h | POR |
| | Capless charge pump supply detect override. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ChargePumpFreqBypass | 16 | RW | 1h | POR |
| | Capless charge pump frequency reg bypass. | | | |
| ChargePumpClkRate | 15:12 | RW | 8h | POR |
| | Capless charge pump clock rate:<br>0000b = 800.0kHz (24MHz/30)<br>0001b = 750.0kHz (24MHz/32)<br>0010b = 706.9kHz (24MHz/34)<br>0011b = 666.7kHz (24MHz/36)<br>0100b = 631.6kHz (24MHz/38)<br>0101b = 600.0kHz (24MHz/40)<br>0110b = 571.4kHz (24MHz/42)<br>0111b = 545.5kHz (24MHz/44)<br>1000b = 800.0kHz (24MHz/30)<br>1001b = 857.1kHz (24MHz/28)<br>1010b = 923.1kHz (24MHz/26)<br>1011b = 1.000MHz (24MHz/24)<br>1100b = 1.091MHz (24MHz/22)<br>1101b = 1.200MHz (24MHz/20)<br>1110b = 1.333MHz (24MHz/18)<br>1111b = 1.500MHz (24MHz/16) | | | |
| ChargePumpClkDiv | 11:9 | RW | 2h | POR |
| | Capless charge pump analog clock divider:<br>001b = No divide<br>010b = Divide by 2, 50% duty cycle<br>100b = Divide by 4, 50% duty cycle<br>110b = Divide by 2, 75% duty cycle<br>011b = Divide by 4, 75% duty cycle<br>111b = Divide by 4, 87.5% duty cycle<br>Other values undefined | | | |
| ChargePumpClkSel | 8 | RW | 0h | POR |
| | Capless charge pump clock select: 0 = ring oscillator, 1 = charge pump clock defined by AFGCaplessChargePumpClkRate[3:0] field below. | | | |
| PortBPadGnd | 7 | RW | 0h | POR |
| | Ground the output pad of the capless amplifiers. | | | |
| PortBInputGnd | 6 | RW | 0h | POR |
| | Ground the input to the capless output amplifiers. | | | |
| Rsvd3 | 5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortBAntiPopBypass | 4 | RW | 0h | POR |
| | 0 = Enable anti-pop on the capless headphone; 1 = bypass anti-pop on the capless headphone. | | | |
| PortAPadGnd | 3 | RW | 0h | NA |
| | Ground the output pad of the capless amplifiers. | | | |
| PortAInputGnd | 2 | RW | 0h | POR |
| | Ground the input to the capless output amplifiers. | | | |
| Rsvd1 | 1 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| PortAAntiPopBypass | 0 | RW | 0h | POR |
| | 0 = Enable anti-pop on the capless headphone; 1 = bypass anti-pop on the capless headphone. | | | |

### *6.5.30. AFG (NID = 01h): Reset*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7FFh |
| Get | FFF00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Execute | 7:0 | W | 00h | N/A (Hard-coded) |
| | Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The codec should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response. | | | |


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## 6.6. PortA (NID = 0Ah): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.6.1. PortA (NID = 0Ah): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.6.2. PortA (NID = 0Ah): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### 6.6.3. PortA (NID = 0Ah): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x23) on 92HD66C. 92HD66B this is reserved. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### 6.6.4. PortA (NID = 0Ah): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.6.5. PortA (NID = 0Ah): InAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.6.6. PortA (NID = 0Ah): ConSelectCtrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |


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### 6.6.7. PortA (NID = 0Ah): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.6.8. PortA (NID = 0Ah): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections):<br>000b= HI-Z<br>001b= 50%<br>010b= GND<br>011b= Reserved<br>100b= 80%<br>101b= 100%<br>110b= Reserved<br>111b= Reserved | | | |

### *6.6.9. PortA (NID = 0Ah): UnsolResp*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.6.10. PortA (NID = 0Ah): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.6.11. PortA (NID = 0Ah): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.6.12. PortA (NID = 0Ah): ConfigDefault*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 02h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Device | 23:20 | RW | 2h | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Color | 15:12 | RW | 4h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 1h | POR |
| | Default assocation. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

## 6.7. PortB (NID = 0Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.7.1. PortB (NID = 0Bh): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.7.2. PortB (NID = 0Bh): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |


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### 6.7.3. PortB (NID = 0Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x23) on 92HD66C. 92HD66B this is reserved. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### 6.7.4. PortB (NID = 0Bh): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget. | | | |


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### 6.7.5. PortB (NID = 0Bh): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget. | | | |

### 6.7.6. PortB (NID = 0Bh): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

### 6.7.7. PortB (NID = 0Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.7.8. PortB (NID = 0Bh): PinWCntrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections):<br>000b= HI-Z<br>001b= 50%<br>010b= GND<br>011b= Reserved<br>100b= 80%<br>101b= 100%<br>110b= Reserved<br>111b= Reserved | | | |

### *6.7.9. PortB (NID = 0Bh): UnsolResp*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |


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### 6.7.10. PortB (NID = 0Bh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.7.11. PortB (NID = 0Bh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.7.12. PortB (NID = 0Bh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 02h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | Ah | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |
| Color | 15:12 | RW | 9h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 2h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |


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## 6.8. PortC (NID = 0Ch): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.8.1. PortC (NID = 0Ch): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.8.2. PortC (NID = 0Ch): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.8.3. PortC (NID = 0Ch): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 converter widget (0x23) on 92HD66C. 92HD66B this is reserved. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### *6.8.4. PortC (NID = 0Ch): InAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.8.5. PortC (NID = 0Ch): InAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.8.6. PortC (NID = 0Ch): ConSelectCtrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |


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### 6.8.7. PortC (NID = 0Ch): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.8.8. PortC (NID = 0Ch): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections):<br>000b= HI-Z<br>001b= 50%<br>010b= GND<br>011b= Reserved<br>100b= 80%<br>101b= 100%<br>110b= Reserved<br>111b= Reserved | | | |

### *6.8.9. PortC (NID = 0Ch): UnsolResp*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.8.10. PortC (NID = 0Ch): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.8.11. PortC (NID = 0Ch): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.8.12. PortC (NID = 0Ch): ConfigDefault*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 01h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Device | 23:20 | RW | 8h | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Color | 15:12 | RW | 3h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 4h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | Eh | POR |
| | Sequence. | | | |

## 6.9. NID = 0Dh Reserved

## 6.10. PortE (NID = 0Eh): WCap (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.10.1. PortE (NID = 0Eh): PinCap* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VrefCntrl | 15:8 | R | 17h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.10.2. PortE (NID = 0Eh): ConLst* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |


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### *6.10.3. PortE (NID = 0Eh): ConLstEntry0* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x23) on 92HD66C. 92HD66B this is reserved. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### *6.10.4. PortE (NID = 0Eh): InAmpLeft* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.10.5. PortE (NID = 0Eh): InAmpRight* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |


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### 6.10.5. *PortE (NID = 0Eh): InAmpRight* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.10.6. *PortE (NID = 0Eh): ConSelectCtrl* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

### 6.10.7. *PortE (NID = 0Eh): PwrState* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.10.8. PortE (NID = 0Eh): PinWCntrl* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | N/A (Hard-coded) |
| | Input enable: 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 4:3 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| VRefEn | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Vref selection (See VrefCntrl field of PinCap parameter for supported selections):<br>000b= HI-Z<br>001b= 50%<br>010b= GND<br>011b= Reserved<br>100b= 80%<br>101b= 100%<br>110b= Reserved<br>111b= Reserved. | | | |

### *6.10.9. PortE (NID = 0Eh): UnsolResp* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### *6.10.10. PortE (NID = 0Eh): ChSense* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |


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### *6.10.10. PortE (NID = 0Eh): ChSense* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.10.11. PortE (NID = 0Eh): EAPDBTLLR* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.10.12. PortE (NID = 0Eh): ConfigDefault* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 01h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | Ah | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |
| Color | 15:12 | RW | 9h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 4h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |


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## 6.11. PortF (NID = 0Fh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.11.1. PortF (NID = 0Fh): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 1h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 1h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.11.2. PortF (NID = 0Fh): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.11.3. PortF (NID = 0Fh): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x23) on 92HD66C. 92HD66B this is reserved. | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### *6.11.4. PortF (NID = 0Fh): InAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.11.5. PortF (NID = 0Fh): InAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.11.6. PortF (NID = 0Fh): ConSelectCtrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |


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### 6.11.7. PortF (NID = 0Fh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.11.8. PortF (NID = 0Fh): PinWCntrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPhnEn | 7 | RW | 0h | POR - DAFG - ULR |
| | Headphone amp enable: 1 = enabled, 0 = disabled. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.11.9. PortF (NID = 0Fh): UnsolResp*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |


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### 6.11.10. PortF (NID = 0Fh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.11.11. PortF (NID = 0Fh): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EAPD | 1 | RW | 1h | POR - DAFG - ULR |
| | EAPD control: 1 = set EAPD pin to 1 (powered) up if this pin is powered up, 0 = set EAPD pin to 0. | | | |
| Rsvd1 | 0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.11.12. PortF (NID = 0Fh): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 01h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | 0h | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnectionType | 19:16 | RW | 1h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |
| Color | 15:12 | RW | 4h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 3h | POR |
| | Default association. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |


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## 6.12. MonoOut (NID = 10h): WCap (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 0h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.12.1. MonoOut (NID = 10h): PinCap* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 0h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.12.2. MonoOut (NID = 10h): ConLst* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### 6.12.3. *MonoOut (NID = 10h): ConLstEntry0* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Ah | N/A (Hard-coded) |
| | MonoMix Summing widget (0x1A) | | | |

### 6.12.4. *MonoOut (NID = 10h): PwrState* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.12.5. MonoOut (NID = 10h): PinWCntrl* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 5:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.12.6. *MonoOut (NID = 10h): UnsolResp* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.12.7. *MonoOut (NID = 10h): ChSense* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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### *6.12.8. MonoOut (NID = 10h): ConfigDefault* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 1h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 00h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Device | 23:20 | RW | Fh | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |
| ConnectionType | 19:16 | RW | 0h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Color | 15:12 | RW | 0h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | Fh | POR |
| | Default assocation. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

## 6.13. DMic0 (NID = 11h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.13.1. DMic0 (NID = 11h): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VRefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 0h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HPhnDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 0h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.13.2. DMic0 (NID = 11h): InAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.13.3. DMic0 (NID = 11h): InAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |


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### 6.13.3. DMic0 (NID = 11h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.13.4. DMic0 (NID = 11h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.13.5. DMic0 (NID = 11h): PinWCntrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:6 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.13.6. DMic0 (NID = 11h): ConfigDefault*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 2h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 10h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | Ah | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnectionType | 19:16 | RW | 3h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |
| Color | 15:12 | RW | 0h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 4h | POR |
| | Default assocation. | | | |
| Sequence | 3:0 | RW | 1h | POR |
| | Sequence. | | | |


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## 6.14. DMic1Vol (NID = 12h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | Fh | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.14.1. DMic1Vol (NID = 12h): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 02h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |


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### 6.14.2. DMic1Vol (NID = 12h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 20h | N/A (Hard-coded) |
| | Dig1Pin Pin widget (0x20) | | | |
| ConL0 | 7:0 | R | 1Fh | N/A (Hard-coded) |
| | Dig1Pin Pin widget (0x1F) | | | |

### 6.14.3. DMic1Vol (NID = 12h): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.14.4. DMic1Vol (NID = 12h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 31:2 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.14.5. DMic1Vol (NID = 12h): ConSelectCtrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:1 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

### *6.14.6. DMic1Vol (NID = 12h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

## 6.15. DAC0 (NID = 13h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |


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### *6.15.1. DAC0 (NID = 13h): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.15.2. DAC0 (NID = 13h): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.15.3. DAC0 (NID = 13h): OutAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.15.4. DAC0 (NID = 13h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.15.5. DAC0 (NID = 13h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

### 6.15.6. DAC0 (NID = 13h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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## 6.16. DAC1 (NID = 14h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.16.1. DAC1 (NID = 14h): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.16.2. DAC1 (NID = 14h): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.16.3. DAC1 (NID = 14h): OutAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.16.4. DAC1 (NID = 14h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.16.5. DAC1 (NID = 14h): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |


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### 6.16.6. DAC1 (NID = 14h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

## 6.17. ADC0 (NID = 15h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |


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### 6.17.1. ADC0 (NID = 15h): ConLst

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### 6.17.2. ADC0 (NID = 15h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 17h | N/A (Hard-coded) |
| | ADC0Mux Selector widget (0x17) | | | |


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### 6.17.3. ADC0 (NID = 15h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.17.4. ADC0 (NID = 15h): ProcState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

### *6.17.5. ADC0 (NID = 15h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.17.6. ADC0 (NID = 15h): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

## 6.18. ADC1 (NID = 1Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 1h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.18.1. ADC1 (NID = 1Bh): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.18.2. ADC1 (NID = 1Bh): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 18h | N/A (Hard-coded) |
| | ADC1Mux widget (0x18) | | | |

### *6.18.3. ADC1 (NID = 1Bh): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |


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### 6.18.4. ADC1 (NID = 1Bh): ProcState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 703h |
| Get | F0300h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| HPFOCDIS | 7 | RW | 0h | POR - DAFG - ULR |
| | HPF offset calculation disable. 1 = calculation disabled; 0 = calculation enabled. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| ADCHPFByp | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Processing State: 00b= bypass the ADC HPF ("off"), 01b-11b= ADC HPF is enabled ("on" or "benign"). | | | |

### 6.18.5. ADC1 (NID = 1Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.18.6. ADC1 (NID = 1Bh): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

## 6.19. ADC0Mux (NID = 17h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.19.1. ADC0Mux (NID = 17h): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 08h | N/A (Hard-coded) |
| | Number of NID entries in connection list | | | |

### *6.19.2. ADC0Mux (NID = 17h): ConLstEntry4*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0204h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL7 | 31:24 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E) (Available only on 48-pin versions) | | | |
| ConL6 | 23:16 | R | 12h | N/A (Hard-coded) |
| | Port DMIC1 widget (0x12) | | | |
| ConL5 | 15:8 | R | 11h | N/A (Hard-coded) |
| | Port DMIC0 widget (0x11) | | | |
| ConL4 | 7:0 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) | | | |

### *6.19.3. ADC0Mux (NID = 17h): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C) | | | |
| ConL2 | 23:16 | R | 0Bh | N/A (Hard-coded) |
| | Port B Pin widget (0x0B | | | |
| ConL1 | 15:8 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

### *6.19.4. ADC0Mux (NID = 17h): OutAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 03h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 2Eh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 10h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.19.5. ADC0Mux (NID = 17h): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### 6.19.6. ADC0Mux (NID = 17h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### 6.19.7. ADC0Mux (NID = 17h): ConSelectCtrl

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |


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### 6.19.8. ADC0Mux (NID = 17h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.19.9. ADC0Mux (NID = 17h): EAPDBTLLR

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

## 6.20. ADC1Mux (NID = 18h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| DigitalStrm | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnsolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParamOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.20.1. ADC1Mux (NID = 18h): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 08h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.20.2. ADC1Mux (NID = 18h): ConLstEntry4*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL7 | 31:24 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E) (Available only on 48-pin versions). | | | |
| ConL6 | 23:16 | R | 12h | N/A (Hard-coded) |
| | Port DMIC1 widget (0x12). | | | |
| ConL5 | 15:8 | R | 11h | N/A (Hard-coded) |
| | Port DMIC0 widget (0x11) | | | |
| ConL4 | 7:0 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F) | | | |

### *6.20.3. ADC1Mux (NID = 18h): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C) | | | |
| ConL2 | 23:16 | R | 0Bh | N/A (Hard-coded) |
| | Port B Pin widget (0x0B) | | | |
| ConL1 | 15:8 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A) | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

### *6.20.4. ADC1Mux (NID = 18h): OutAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 03h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 2Eh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Offset | 6:0 | R | 10h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### 6.20.5. ADC1Mux (NID = 18h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### 6.20.6. ADC1Mux (NID = 18h): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 5:0 | RW | 10h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.20.7. ADC1Mux (NID = 18h): ConSelectCtrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 2:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

### *6.20.8. ADC1Mux (NID = 18h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.20.9. ADC1Mux (NID = 18h): EAPDBTLLR*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

## 6.21. MonoMux (NID = 19h): WCap (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.21.1. MonoMux (NID = 19h): ConLst* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 04h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.21.2. MonoMux (NID = 19h): ConLstEntry0* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 Converter widget (0x23) on 92HD66C. 92HD66B this is reserved | | | |
| ConL2 | 23:16 | R | 1Ch | N/A (Hard-coded) |
| | MixerOutVol Selector widget (0x1C) | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 Converter widget (0x14) | | | |
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 Converter widget (0x13) | | | |

### *6.21.3. MonoMux (NID = 19h): ConSelectCtrl* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 701h |
| Get | F0100h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Index | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Connection select control index. | | | |

### *6.21.4. MonoMux (NID = 19h): PwrState* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

## 6.22. MonoMix (NID = 1Ah): WCap (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 2h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 0h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.22.1. MonoMix (NID = 1Ah): ConLst* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.22.2. MonoMix (NID = 1Ah): ConLstEntry0* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 19h | N/A (Hard-coded) |
| | MonoMux Selector widget (0x19) | | | |

### *6.22.3. MonoMix (NID = 1Ah): PwrState* (Available only on 48-pin versions)

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

## 6.23. Mixer (NID = 1Bh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 2h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.23.1. Mixer (NID = 1Bh): InAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Dh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 17h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.23.2. Mixer (NID = 1Bh): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 08h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |


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### 6.23.3. Mixer (NID = 1Bh): ConLstEntry4

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0204h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL7 | 31:24 | R | 23h | N/A (Hard-coded) |
| | DAC2 widget (0x23) on 92HD66C. 92HD66B this is reserved. Uses InAmpLeft7/InAmpRight7 controls | | | |
| ConL6 | 23:16 | R | 0Eh | N/A (Hard-coded) |
| | Port E Pin widget (0x0E). Uses InAmpLeft6/InAmpRight6 controls (Available only on 48-pin versions) | | | |
| ConL5 | 15:8 | R | 0Fh | N/A (Hard-coded) |
| | Port F Pin widget (0x0F). Uses InAmpLeft5/InAmpRight5 controls | | | |
| ConL4 | 7:0 | R | 0Ch | N/A (Hard-coded) |
| | Port C Pin widget (0x0C). Uses InAmpLeft4/InAmpRight4 controls | | | |

### 6.23.4. Mixer (NID = 1Bh): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 0Bh | N/A (Hard-coded) |
| | Port B Pin widget (0x0B). Uses InAmpLeft3/InAmpRight3 controls. | | | |
| ConL2 | 23:16 | R | 0Ah | N/A (Hard-coded) |
| | Port A Pin widget (0x0A). Uses InAmpLeft2/InAmpRight2 controls. | | | |
| ConL1 | 15:8 | R | 14h | N/A (Hard-coded) |
| | DAC1 widget (0x14). Uses InAmpLeft1/InAmpRight1 controls. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL0 | 7:0 | R | 13h | N/A (Hard-coded) |
| | DAC0 widget (0x13). Uses InAmpLeft0/InAmpRight0 controls. | | | |

### 6.23.5. Mixer (NID = 1Bh): InAmpLeft0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.23.6. Mixer (NID = 1Bh): InAmpRight0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.7. Mixer (NID = 1Bh): InAmpLeft1*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 361h |
| Get | B2001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.8. Mixer (NID = 1Bh): InAmpRight1*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 351h |
| Get | B0001h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.9. Mixer (NID = 1Bh): InAmpLeft2*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 362h |
| Get | B2002h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.10. Mixer (NID = 1Bh): InAmpRight2*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 352h |
| Get | B0002h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.11. Mixer (NID = 1Bh): InAmpLeft3*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 363h |
| Get | B2003h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.12. Mixer (NID = 1Bh): InAmpRight3*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 353h |
| Get | B0003h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.13. Mixer (NID = 1Bh): InAmpLeft4*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 364h |
| Get | B2004h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.14. Mixer (NID = 1Bh): InAmpRight4*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 354h |
| Get | B0004h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.15. Mixer (NID = 1Bh): InAmpLeft5*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 365h |
| Get | B2005h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.16. Mixer (NID = 1Bh): InAmpRight5*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 355h |
| Get | B0005h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### *6.23.17. Mixer (NID = 1Bh): InAmpLeft6*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 366h |
| Get | B2006h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |


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### 6.23.18. Mixer (NID = 1Bh): InAmpRight6

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 356h |
| Get | B0006h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.23.19. Mixer (NID = 1Bh): InAmpLeft7

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 367h |
| Get | B2007h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |


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### 6.23.20. Mixer (NID = 1Bh): InAmpRight7

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 357h |
| Get | B0007h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 17h | POR - DAFG - ULR |
| | Amp gain step number (see InAmpCap parameter pertaining to this widget). | | | |

### 6.23.21. Mixer (NID = 1Bh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

## 6.24. MixerOutVol (NID = 1Ch): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 3h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.24.1. MixerOutVol (NID = 1Ch): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.24.2. MixerOutVol (NID = 1Ch): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Bh | N/A (Hard-coded) |
| | Mixer Summing widget (0x1B) | | | |

### *6.24.3. MixerOutVol (NID = 1Ch): OutAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 05h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 1Fh | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 1Fh | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.24.4. MixerOutVol (NID = 1Ch): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### 6.24.5. MixerOutVol (NID = 1Ch): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 4:0 | RW | 1Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### 6.24.6. MixerOutVol (NID = 1Ch): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

## 6.25. SPDIFOut0 (NID = 1Dh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 4h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 1h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.25.1. SPDIFOut0 (NID = 1Dh): PCMCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |


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### 6.25.2. SPDIFOut0 (NID = 1Dh): StreamCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 1h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

### 6.25.3. SPDIFOut0 (NID = 1Dh): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 00h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| NumSteps | 14:8 | R | 00h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.25.4. SPDIFOut0 (NID = 1Dh): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| FrmtNonPCM | 15 | RW | 0h | POR - DAFG - ULR |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.25.5. SPDIFOut0 (NID = 1Dh): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.25.6. SPDIFOut0 (NID = 1Dh): OutAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.25.7. SPDIFOut0 (NID = 1Dh): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.25.8. SPDIFOut0 (NID = 1Dh): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

### *6.25.9. SPDIFOut0 (NID = 1Dh): DigCnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 73Fh | 73Eh | 70Eh | 70Dh |
| Get | F0E00h / F0D00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| KeepAlive | 23 | RW | 0h | POR - DAFG - ULR |
| | Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3. | | | |
| Rsvd1 | 22:15 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| CC | 14:8 | RW | 00h | POR - DAFG - ULR |
| | CC: Category Code. | | | |
| L | 7 | RW | 0h | POR - DAFG - ULR |
| | L: Generation Level. | | | |
| PRO | 6 | RW | 0h | POR - DAFG - ULR |
| | PRO: Professional. | | | |
| AUDIO | 5 | RW | 0h | POR - DAFG - ULR |
| | /AUDIO: Non-Audio. | | | |
| COPY | 4 | RW | 0h | POR - DAFG - ULR |
| | COPY: Copyright. | | | |
| PRE | 3 | RW | 0h | POR - DAFG - ULR |
| | PRE: Preemphasis. | | | |
| VCFG | 2 | RW | 0h | POR - DAFG - ULR |
| | VCFG: Validity Config. | | | |
| V | 1 | RW | 0h | POR - DAFG - ULR |
| | V: Validity. | | | |
| DigEn | 0 | RW | 0h | POR - DAFG - ULR |
| | Digital enable: 1 = converter enabled, 0 = converter disable. | | | |

## 6.26. SPDIFOut1 (NID = 1Eh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |


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## 6.26. SPDIFOut1 (NID = 1Eh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 4h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 1h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.26.1. SPDIFOut1 (NID = 1Eh): PCMCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 1h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

### *6.26.2. SPDIFOut1 (NID = 1Eh): StreamCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 1h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

### *6.26.3. SPDIFOut1 (NID = 1Eh): OutAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 00h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 00h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### *6.26.4. SPDIFOut1 (NID = 1Eh): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| FrmtNonPCM | 15 | RW | 0h | POR - DAFG - ULR |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.26.5. SPDIFOut1 (NID = 1Eh): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.26.6. SPDIFOut1 (NID = 1Eh): OutAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.26.7. SPDIFOut1 (NID = 1Eh): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.26.8. SPDIFOut1 (NID = 1Eh): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |


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### *6.26.9. SPDIFOut1 (NID = 1Eh): DigCnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 73Fh | 73Eh | 70Eh | 70Dh |
| Get | F0E00h / F0D00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| KeepAlive | 23 | RW | 0h | POR - DAFG - ULR |
| | Keep Alive Enable: 1 = clocking information maintained during D3, 0 = clock information not required during D3. | | | |
| Rsvd1 | 22:15 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| CC | 14:8 | RW | 00h | POR - DAFG - ULR |
| | CC: Category Code. | | | |
| L | 7 | RW | 0h | POR - DAFG - ULR |
| | L: Generation Level. | | | |
| PRO | 6 | RW | 0h | POR - DAFG - ULR |
| | PRO: Professional. | | | |
| AUDIO | 5 | RW | 0h | POR - DAFG - ULR |
| | /AUDIO: Non-Audio. | | | |
| COPY | 4 | RW | 0h | POR - DAFG - ULR |
| | COPY: Copyright. | | | |
| PRE | 3 | RW | 0h | POR - DAFG - ULR |
| | PRE: Preemphasis. | | | |
| VCFG | 2 | RW | 0h | POR - DAFG - ULR |
| | VCFG: Validity Config. | | | |
| V | 1 | RW | 0h | POR - DAFG - ULR |
| | V: Validity. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| DigEn | 0 | RW | 0h | POR - DAFG - ULR |
| | Digital enable: 1 = converter enabled, 0 = converter disable. | | | |

## 6.27. Dig0Pin (NID = 1Fh): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.27.1. Dig0Pin (NID = 1Fh): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.27.2. Dig0Pin (NID = 1Fh): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.27.3. Dig0Pin (NID = 1Fh): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Dh | N/A (Hard-coded) |
| | SPDIFOut0 Converter widget (0x1D) | | | |

### *6.27.4. Dig0Pin (NID = 1Fh): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.27.5. Dig0Pin (NID = 1Fh): PinWCntrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable; 1 = enabled, 0 = disabled | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.27.6. Dig0Pin (NID = 1Fh): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.27.7. Dig0Pin (NID = 1Fh): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.27.8. Dig0Pin (NID = 1Fh): ConfigDefault*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 01h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Device | 23:20 | RW | 4h | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |
| ConnectionType | 19:16 | RW | 5h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Color | 15:12 | RW | 1h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 5h | POR |
| | Default assocation. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |

## 6.28. Dig1Pin (NID = 20h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 4h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.28.1. Dig1Pin (NID = 20h): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 0h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |
| VrefCntrl | 15:8 | R | 00h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no. | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no. | | | |
| OutCap | 4 | R | 1h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no. | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no. | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no. | | | |

### *6.28.2. Dig1Pin (NID = 20h): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |


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### 6.28.3. Dig1Pin (NID = 20h): ConLstEntry0

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 1Eh | N/A (Hard-coded) |
| | SPDIFOut1 Converter widget (0x1E) | | | |

### 6.28.4. Dig1Pin (NID = 20h): PwrState

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.28.5. Dig1Pin (NID = 20h): PinWCntrl*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 0000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | RW | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 4:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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### 6.28.6. Dig1Pin (NID = 20h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.28.7. Dig1Pin (NID = 20h): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.28.8. Dig1Pin (NID = 20h): ConfigDefault

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 2h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 18h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |
| Device | 23:20 | RW | 5h | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConnectionType | 19:16 | RW | 6h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8" stereo/mono<br>2h = 1/4" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |
| Color | 15:12 | RW | 0h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 1h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 6h | POR |
| | Default assocation. | | | |
| Sequence | 3:0 | RW | 0h | POR |
| | Sequence. | | | |


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## 6.29. DigBeep (NID = 21h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 7h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Rsvd3 | 19:11 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no." | | | |
| Rsvd2 | 9:4 | R | 00h | N/A (Hard-coded) |
| | Reserved | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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### 6.29.1. DigBeep (NID = 21h): OutAmpCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0012h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 17h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 03h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 03h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### 6.29.2. DigBeep (NID = 21h): OutAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:2 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Gain | 1:0 | RW | 1h | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.29.3. DigBeep (NID = 21h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Set | 1:0 | RW | 0h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### 6.29.4. DigBeep (NID = 21h): Gen

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ah |
| Get | F0A00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Divider | 7:0 | RW | 00h | POR - DAFG - LR |
| | Enable internal PC-Beep generation. Divider == 00h disables internal PC Beep generation and enables normal operation of the codec. Divider != 00h generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that the beep tone frequency = (48kHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 kHz (logarithmic scale). | | | |

### 6.29.5. SPDIFIn (NID = 22h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Type | 23:20 | R | 1h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 4h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 0h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 1h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 1h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 1h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 1h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |


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## 6.30. SPDIFIn (NID = 22h): Cnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| FrmtNonPCM | 15 | RW | 0h | POR - DAFG - ULR |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter: 0000b-1111b= 1-16 channels. | | | |

### *6.30.1. SPDIFIn (NID = 22h): PCMCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ah | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:21 | R | 000h | N/A (Hard-coded) |
| | Reserved. | | | |
| B32 | 20 | R | 0h | N/A (Hard-coded) |
| | 32 bit audio format support: 1 = yes, 0 = no. | | | |
| B24 | 19 | R | 1h | N/A (Hard-coded) |
| | 24 bit audio format support: 1 = yes, 0 = no. | | | |
| B20 | 18 | R | 1h | N/A (Hard-coded) |
| | 20 bit audio format support: 1 = yes, 0 = no. | | | |
| B16 | 17 | R | 1h | N/A (Hard-coded) |
| | 16 bit audio format support: 1 = yes, 0 = no. | | | |
| B8 | 16 | R | 0h | N/A (Hard-coded) |
| | 8 bit audio format support: 1 = yes, 0 = no. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| R12 | 11 | R | 0h | N/A (Hard-coded) |
| | 384kHz rate support: 1 = yes, 0 = no. | | | |
| R11 | 10 | R | 1h | N/A (Hard-coded) |
| | 192kHz rate support: 1 = yes, 0 = no. | | | |
| R10 | 9 | R | 0h | N/A (Hard-coded) |
| | 176.4kHz rate support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| R9 | 8 | R | 1h | N/A (Hard-coded) |
| | 96kHz rate support: 1 = yes, 0 = no. | | | |
| R8 | 7 | R | 0h | N/A (Hard-coded) |
| | 88.2kHz rate support: 1 = yes, 0 = no. | | | |
| R7 | 6 | R | 1h | N/A (Hard-coded) |
| | 48kHz rate support: 1 = yes, 0 = no. | | | |
| R6 | 5 | R | 1h | N/A (Hard-coded) |
| | 44.1kHz rate support: 1 = yes, 0 = no. | | | |
| R5 | 4 | R | 0h | N/A (Hard-coded) |
| | 32kHz rate support: 1 = yes, 0 = no. | | | |
| R4 | 3 | R | 0h | N/A (Hard-coded) |
| | 22.05kHz rate support: 1 = yes, 0 = no. | | | |
| R3 | 2 | R | 0h | N/A (Hard-coded) |
| | 16kHz rate support: 1 = yes, 0 = no. | | | |
| R2 | 1 | R | 0h | N/A (Hard-coded) |
| | 11.025kHz rate support: 1 = yes, 0 = no. | | | |
| R1 | 0 | R | 0h | N/A (Hard-coded) |
| | 8kHz rate support: 1 = yes, 0 = no. | | | |

### *6.30.2. SPDIFIn (NID = 22h): StreamCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Bh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| AC3 | 2 | R | 1h | N/A (Hard-coded) |
| | AC-3 formatted data support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Float32 | 1 | R | 0h | N/A (Hard-coded) |
| | Float32 formatted data support: 1 = yes, 0 = no. | | | |
| PCM | 0 | R | 1h | N/A (Hard-coded) |
| | PCM-formatted data support: 1 = yes, 0 = no. | | | |

### *6.30.3. SPDIFIn (NID = 22h): ConLst*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Eh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| LForm | 7 | R | 0h | N/A (Hard-coded) |
| | Connection list format: 1 = long-form (15-bit) NID entries, 0 = short-form (7-bit) NID entries. | | | |
| ConL | 6:0 | R | 01h | N/A (Hard-coded) |
| | Number of NID entries in connection list. | | | |

### *6.30.4. SPDIFIn (NID = 22h): ConLstEntry0*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0200h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL3 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL2 | 23:16 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ConL1 | 15:8 | R | 00h | N/A (Hard-coded) |
| | Unused list entry. | | | |
| ConL0 | 7:0 | R | 24h | N/A (Hard-coded) |
| | Dig2Pin pin widget (0x24) | | | |

### *6.30.5. SPDIFIn (NID = 22h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |


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### 6.30.6. SPDIFIn (NID = 22h): CnvtrID

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |

### 6.30.7. SPDIFIn (NID = 22h): DigCnvtr

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 73Fh | 73Eh | 70Eh | 70Dh |
| Get | F0E00h / F0D00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Rsvd1 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| CC | 14:8 | R | 00h | POR - DAFG - ULR |
| | CC: Category Code. | | | |
| L | 7 | R | 0h | POR - DAFG - ULR |
| | L: Generation Level. | | | |
| PRO | 6 | R | 0h | POR - DAFG - ULR |
| | PRO: Professional. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| AUDIO | 5 | R | 0h | POR - DAFG - ULR |
| | /AUDIO: Non-Audio. | | | |
| COPY | 4 | R | 0h | POR - DAFG - ULR |
| | COPY: Copyright. | | | |
| PRE | 3 | R | 0h | POR - DAFG - ULR |
| | PRE: Preemphasis. | | | |
| VCFG | 2 | R | 0h | POR - DAFG - ULR |
| | VCFG: Validity Config. | | | |
| V | 1 | R | 0h | POR - DAFG - ULR |
| | V: Validity. | | | |
| DigEn | 0 | RW | 0h | POR - DAFG - ULR |
| | Digital enable: 1 = converter enabled, 0 = converter disable. | | | |

### *6.30.8. SPDIFIn (NID = 22h): InAmpCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Dh | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Mute | 31 | R | 1h | N/A (Hard-coded) |
| | Mute support: 1 = yes, 0 = no. | | | |
| Rsvd3 | 30:23 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| StepSize | 22:16 | R | 00h | N/A (Hard-coded) |
| | Size of each step in the gain range: 0 to 127 = .25dB to 32dB, in .25dB steps. | | | |
| Rsvd2 | 15 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| NumSteps | 14:8 | R | 00h | N/A (Hard-coded) |
| | Number of gains steps (number of possible settings - 1). | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Offset | 6:0 | R | 00h | N/A (Hard-coded) |
| | Indicates which step is 0dB | | | |

### 6.30.9. SPDIFIn (NID = 22h): InAmpLeft

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 360h |
| Get | B2000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.30.10. SPDIFIn (NID = 22h): InAmpRight

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 350h |
| Get | B0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:2 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 0h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Rsvd1 | 6:0 | RW | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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### 6.30.11. SPDIFIn (NID = 22h): VS

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7E0h |
| Get | FE000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:2 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| RoundDis | 1 | RW | 0h | POR - DAFG - ULR |
| | SPDIF Input rounding disable: 0 = rounding is enabled, 1 = rounding is disabled. | | | |
| LoLvSel | 0 | RW | 0h | POR - DAFG - ULR |
| | SPDIF Input level select: 0 = standard level, 1 = low level (input buffer enabled. | | | |

### 6.30.12. SPDIFIn (NID = 22h): Status

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 7E8h |
| Get | FE800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| RcvSmplRate | 31:29 | R | 7h | POR - DAFG - ULR |
| | Received Sample Rate:<br>000b = 44.1kHz<br>001b = 48kHz<br>010b = 88.2kHz<br>011b = 96kHz<br>100b = 176.4kHz<br>101b = 192kHz<br>11Xb = Invalid Rate | | | |
| Rsvd2 | 28.26 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| OrigFS | 25:22 | R | 0h | POR - DAFG - ULR |
| | Original Sample Rate (per IEC60958-3 spec):<br>0000b = Original sampling frequency not indicated<br>0001b = 192kHz<br>0010b = 12kHz<br>0011b = 176.4kHz<br>0100b = Reserved<br>0101b = 96kHz<br>0110b = 8kHz<br>0111b = 88.2kHz<br>1000b = 16kHz<br>1001b = 24kHz<br>1010b = 11.025kHz<br>1011b = 22.05kHz<br>1100b = 32kHz<br>1101b = 48khz<br>1110b = Reserved<br>1111b = 44.1kHz | | | |
| CA | 21:20 | R | 0h | POR - DAFG - ULR |
| | Clock Accuracy (per IEC60958-3 spec):<br>00b = Level II<br>01b = Level I<br>10b = Level III<br>11b = Reserved | | | |
| FS | 19:16 | R | 0h | POR - DAFG - ULR |
| | Sample Rate (per IEC60958-3 spec):<br>0000b = 44.1kHz<br>0001b = Original sampling frequency not indicated<br>0010b = 48kHz<br>0011b = 32kHz<br>0100b = 22.05kHz<br>0101b = Reserved<br>0110b = 24kHz<br>0111b = Reserved<br>1000b = 88.2kHz<br>1001b = Reserved<br>1010b = 96kHz<br>1011b = Reserved<br>1100b = 176.4kHz<br>1101b = Reserved<br>1110b = 192kHz<br>1111b = Reserved | | | |
| CN | 15:12 | R | 0h | POR - DAFG - ULR |
| | Channel Number (per IEC60958-3 spec):<br>0000b = Do not take into account<br>0001b = Channel 1 (Left channel for stereo channel format)<br>0010b = Channel 2 (Right channel for stereo channel format)<br>0011b-1111b = Channel 3-15 | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SmplWrdL | 11:9 | R | 0h | POR - DAFG - ULR |
| | Sample Word Length (per IEC60958-3 spec):<br>000b = Word length not indicated<br>001b = Max length - 4<br>010b = Max length - 2<br>011b = Reserved<br>100b = Max length - 1<br>101b = Max length - 0<br>110b = Max length - 3<br>111b = Reserved | | | |
| MaxWrdL | 8 | R | 0h | POR - DAFG - ULR |
| | Max Word Length (per IEC60958-3 spec): 0 = 20 bits, 1 = 24 bits. | | | |
| NoBlkChk | 7 | RW | 0h | POR - DAFG - ULR |
| | Disable Sample Block Checking. | | | |
| Rsvd | 6:5 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| ParityLimit | 4:3 | RW | 0h | POR - DAFG - ULR |
| | SPDIFIn Parity Limit (DPLL loses lock when the set number of parity errors per block is detected):<br>00b = 4 Parity errors<br>01b = 3 Parity errors<br>10b = 2 Parity errors<br>11b = 1 Parity error | | | |
| SPRun | 2 | R | 0h | POR - DAFG - ULR |
| | SPDIFIn Running 0 = no signal on SPDIFIn Pin, 1 = Signal on SPDIFIn pin. | | | |
| SiPerr | 1 | RW | 0h | POR - DAFG - ULR |
| | SPDIFIn Parity Error: 0 = No error detected, 1 = Error detected (write 0 to clear). Not affected by ParityLimit. | | | |
| CopyInv | 0 | RW | 0h | POR - DAFG - ULR |
| | Copyright Invert: 0 = Do not invert COPY bit, 1 = Invert COPY bit. | | | |


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## 6.31. DAC2 (NID = 23h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | Dh | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 0h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 0h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 1h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.31.1. DAC2 (NID = 23h): Cnvtr*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | 2h | |
| Get | A0000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:16 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| StrmType | 15 | R | 0h | N/A (Hard-coded) |
| | Stream type: 1 = Non-PCM, 0 = PCM. | | | |
| FrmtSmplRate | 14 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate: 1 = 44.1kHz, 0 = 48kHz. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SmplRateMultp | 13:11 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate multiple:<br>000b= x1 (48kHz/44.1kHz or less)<br>001b= x2 (96kHz/88.2kHz/32kHz)<br>010b= x3 (144kHz)<br>011b= x4 (192kHz/176.4kHz)<br>100b-111b Reserved | | | |
| SmplRateDiv | 10:8 | RW | 0h | POR - DAFG - ULR |
| | Sample base rate divider:<br>000b= Divide by 1 (48kHz/44.1kHz)<br>001b= Divide by 2 (24kHz/20.05kHz)<br>010b= Divide by 3 (16kHz/32kHz)<br>011b= Divide by 4 (11.025kHz)<br>100b= Divide by 5 (9.6kHz)<br>101b= Divide by 6 (8kHz)<br>110b= Divide by 7<br>111b= Divide by 8 (6kHz) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BitsPerSmpl | 6:4 | RW | 3h | POR - DAFG - ULR |
| | Bits per sample:<br>000b= 8 bits<br>001b= 16 bits<br>010b= 20 bits<br>011b= 24 bits<br>100b= 32 bits<br>101b-111b= Reserved | | | |
| NmbrChan | 3:0 | RW | 1h | POR - DAFG - ULR |
| | Total number of channels in the stream assigned to this converter:<br>0000b-1111b= 1-16 channels. | | | |

### *6.31.2. DAC2 (NID = 23h): OutAmpLeft*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 3A0h |
| Get | BA000h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.31.3. DAC2 (NID = 23h): OutAmpRight*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 390h |
| Get | B8000h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Mute | 7 | RW | 1h | POR - DAFG - ULR |
| | Amp mute: 1 = muted, 0 = not muted. | | | |
| Gain | 6:0 | RW | 7Fh | POR - DAFG - ULR |
| | Amp gain step number (see OutAmpCap parameter pertaining to this widget). | | | |

### *6.31.4. DAC2 (NID = 23h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - LR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 3h | POR - DAFG - LR |
| | Current power state setting for this widget. | | | |

### *6.31.5. DAC2 (NID = 23h): CnvtrID*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 706h |
| Get | F0600h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| Strm | 7:4 | RW | 0h | POR - S&DAFG - LR - PS |
| | Stream ID: 0h = Converter "off", 1h-Fh = valid ID's. | | | |
| Ch | 3:0 | RW | 0h | POR - S&DAFG - LR - PS |
| | Channel assignment ("Ch" and "Ch+1" assigned as a pair, for a stereo converter). | | | |


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### *6.31.6. DAC2 (NID = 23h): EAPDBTLLR*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 70Ch |
| Get | F0C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:3 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapEn | 2 | RW | 0h | POR - DAFG - ULR |
| | Swap enable: 1 = L/R swap enabled, 0 = L/R swap disabled. | | | |
| Rsvd1 | 1:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |


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## 6.32. Dig2Pin (NID = 24h): WCap

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F0009h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:24 | R | 00h | N/A (Hard-coded) |
| | Reserved. | | | |
| Type | 23:20 | R | 0h | N/A (Hard-coded) |
| | Widget type:<br>0h = Out Converter<br>1h = In Converter<br>2h = Summing (Mixer)<br>3h = Selector (Mux)<br>4h = Pin Complex<br>5h = Power<br>6h = Volume Knob<br>7h = Beep Generator<br>8h-Eh = Reserved<br>Fh = Vendor Defined | | | |
| Delay | 19:16 | R | 0h | N/A (Hard-coded) |
| | Number of sample delays through widget. | | | |
| Rsvd1 | 15:12 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| SwapCap | 11 | R | 1h | N/A (Hard-coded) |
| | Left/right swap support: 1 = yes, 0 = no. | | | |
| PwrCntrl | 10 | R | 1h | N/A (Hard-coded) |
| | Power state support: 1 = yes, 0 = no. | | | |
| Dig | 9 | R | 1h | N/A (Hard-coded) |
| | Digital stream support: 1 = yes (digital), 0 = no (analog). | | | |
| ConnList | 8 | R | 0h | N/A (Hard-coded) |
| | Connection list present: 1 = yes, 0 = no. | | | |
| UnSolCap | 7 | R | 1h | N/A (Hard-coded) |
| | Unsolicited response support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| ProcWidget | 6 | R | 0h | N/A (Hard-coded) |
| | Processing state support: 1 = yes, 0 = no. | | | |
| Stripe | 5 | R | 0h | N/A (Hard-coded) |
| | Striping support: 1 = yes, 0 = no. | | | |
| FormatOvrd | 4 | R | 0h | N/A (Hard-coded) |
| | Stream format override: 1 = yes, 0 = no. | | | |
| AmpParOvrd | 3 | R | 0h | N/A (Hard-coded) |
| | Amplifier capabilities override: 1 = yes, no. | | | |
| OutAmpPrsnt | 2 | R | 0h | N/A (Hard-coded) |
| | Output amp present: 1 = yes, 0 = no. | | | |
| InAmpPrsnt | 1 | R | 0h | N/A (Hard-coded) |
| | Input amp present: 1 = yes, 0 = no. | | | |
| Stereo | 0 | R | 1h | N/A (Hard-coded) |
| | Stereo stream support: 1 = yes (stereo), 0 = no (mono). | | | |

### *6.32.1. Dig2Pin (NID = 24h): PinCap*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | |
| Get | F000Ch | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:17 | R | 0000h | N/A (Hard-coded) |
| | Reserved. | | | |
| EapdCap | 16 | R | 00h | N/A (Hard-coded) |
| | EAPD support: 1 = yes, 0 = no. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| VrefCntrl | 15:8 | RW | 0h | N/A (Hard-coded) |
| | Vref support:<br>bit 7 = Reserved<br>bit 6 = Reserved<br>bit 5 = 100% support (1 = yes, 0 = no)<br>bit 4 = 80% support (1 = yes, 0 = no)<br>bit 3 = Reserved<br>bit 2 = GND support (1 = yes, 0 = no)<br>bit 1 = 50% support (1 = yes, 0 = no)<br>bit 0 = Hi-Z support (1 = yes, 0 = no) | | | |
| Rsvd1 | 7 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| BalancedIO | 6 | R | 0h | N/A (Hard-coded) |
| | Balanced I/O support: 1 = yes, 0 = no | | | |
| InCap | 5 | R | 1h | N/A (Hard-coded) |
| | Input support: 1 = yes, 0 = no | | | |
| OutCap | 4 | R | 0h | N/A (Hard-coded) |
| | Output support: 1 = yes, 0 = no. | | | |
| HdphDrvCap | 3 | R | 0h | N/A (Hard-coded) |
| | Headphone amp present: 1 = yes, 0 = no | | | |
| PresDtctCap | 2 | R | 1h | N/A (Hard-coded) |
| | Presence detection support: 1 = yes, 0 = no. | | | |
| TrigRqd | 1 | R | 0h | N/A (Hard-coded) |
| | Trigger required for impedance sense: 1 = yes, 0 = no | | | |
| ImpSenseCap | 0 | R | 0h | N/A (Hard-coded) |
| | Impedance sense support: 1 = yes, 0 = no | | | |

### *6.32.2. Dig2Pin (NID = 24h): PwrState*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 705h |
| Get | F0500h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd4 | 31:11 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| SettingsReset | 10 | R | 1h | POR - DAFG - ULR |
| | Indicates if any persistent settings in this Widget have been reset. Cleared by PwrState 'Get', or a 'Set' to any Verb in this Widget. | | | |
| Rsvd3 | 9 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Error | 8 | R | 0h | POR - DAFG - ULR |
| | Error indicator: 1 = cannot enter requested power state, 0 = no problem with requested power state. | | | |
| Rsvd2 | 7:6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Act | 5:4 | R | 3h | POR - DAFG - ULR |
| | Actual power state of this widget. | | | |
| Rsvd1 | 3:2 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Set | 1:0 | RW | 0h | POR - DAFG - ULR |
| | Current power state setting for this widget. | | | |

***Dig2Pin (NID = 24h): PinWCntrl***

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 707h |
| Get | F0700h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:7 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| OutEn | 6 | R | 0h | POR - DAFG - ULR |
| | Output enable: 1 = enabled, 0 = disabled. | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| InEn | 5 | RW | 0h | POR - DAFG - ULR |
| | Input enable: 1 = enabled, 0 = disabled | | | |
| Rsvd1 | 4:0 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |

### 6.32.3. Dig2Pin (NID = 24h): UnsolResp

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 708h |
| Get | F0800h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Rsvd2 | 31:8 | R | 000000h | N/A (Hard-coded) |
| | Reserved. | | | |
| En | 7 | RW | 0h | POR - DAFG - ULR |
| | Unsolicited response enable (also enables Wake events for this Widget): 1 = enabled, 0 = disabled. | | | |
| Rsvd1 | 6 | R | 0h | N/A (Hard-coded) |
| | Reserved. | | | |
| Tag | 5:0 | RW | 00h | POR - DAFG - ULR |
| | Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node. | | | |

### 6.32.4. Dig2Pin (NID = 24h): ChSense

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | | | | 709h |
| Get | F0900h | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PresDtct | 31 | R | 0h | POR |
| | Presence detection indicator: 1 = presence detected; 0 = presence not detected. | | | |
| Rsvd | 30:0 | R | 00000000h | N/A (Hard-coded) |
| | Reserved. | | | |

### *6.32.5. Dig2Pin (NID = 24h): ConfigDefault*

| Reg | Byte 4 (Bits 31:24) | Byte 3 (Bits 23:16) | Byte 2 (Bits 15:8) | Byte 1 (Bits 7:0) |
|---|---|---|---|---|
| Set | 71Fh | 71Eh | 71Dh | 71Ch |
| Get | F1F00h / F1E00h / F1D00h / F1C00h | | | |

| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| PortConnectivity | 31:30 | RW | 0h | POR |
| | Port connectivity:<br>0h = Port complex is connected to a jack<br>1h = No physical connection for port<br>2h = Fixed function device is attached<br>3h = Both jack and internal device attached (info in all other fields refers to integrated device, any presence detection refers to jack) | | | |
| Location | 29:24 | RW | 01h | POR |
| | Location<br><br>Bits [5..4]:<br>0h = External on primary chassis<br>1h = Internal<br>2h = Separate chassis<br>3h = Other<br><br>Bits [3..0]:<br>0h = N/A<br>1h = Rear<br>2h = Front<br>3h = Left<br>4h = Right<br>5h = Top<br>6h = Bottom<br>7h-9h = Special<br>Ah-Fh = Reserved | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Device | 23:20 | RW | Ch | POR |
| | Default device:<br>0h = Line out<br>1h = Speaker<br>2h = HP out<br>3h = CD<br>4h = SPDIF Out<br>5h = Digital other out<br>6h = Modem line side<br>7h = Modem handset side<br>8h = Line in<br>9h = Aux<br>Ah = Mic in<br>Bh = Telephony<br>Ch = SPDIF In<br>Dh = Digital other in<br>Eh = Reserved<br>Fh = Other | | | |
| ConnectionType | 19:16 | RW | 5h | POR |
| | Connection type:<br>0h = Unknown<br>1h = 1/8"" stereo/mono<br>2h = 1/4"" stereo/mono<br>3h = ATAPI internal<br>4h = RCA<br>5h = Optical<br>6h = Other digital<br>7h = Other analog<br>8h = Multichannel analog (DIN)<br>9h = XLR/Professional<br>Ah = RJ-11 (modem)<br>Bh = Combination<br>Ch-Eh = Reserved<br>Fh = Other | | | |


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| Field Name | Bits | R/W | Default | Reset |
|---|---|---|---|---|
| Color | 15:12 | RW | 2h | POR |
| | Color:<br>0h = Unknown<br>1h = Black<br>2h = Grey<br>3h = Blue<br>4h = Green<br>5h = Red<br>6h = Orange<br>7h = Yellow<br>8h = Purple<br>9h = Pink<br>Ah-Dh = Reserved<br>Eh = White<br>Fh = Other | | | |
| Misc | 11:8 | RW | 0h | POR |
| | Miscellaneous:<br>Bits [3..1] = Reserved<br>Bit 0 = Jack detect override | | | |
| Association | 7:4 | RW | 7h | POR |
| | Default assocation. | | | |
| Sequence | 7:4 | RW | 0h | POR |
| | Sequence. | | | |


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# 7. PINOUTS AND PACKAGE INFORMATION

## 7.1. 48-Pin Pinout

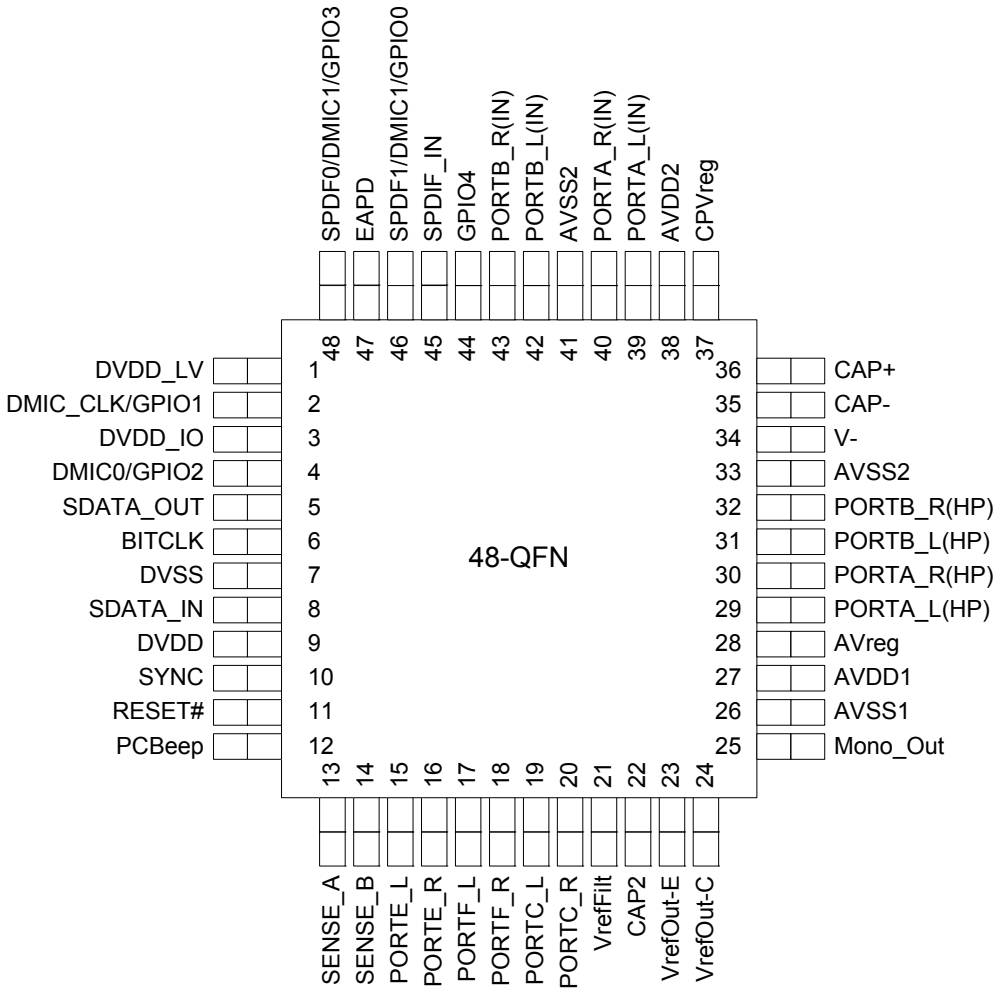


**Figure 14. 48-Pin Pinout**


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## 7.2. 40-Pin Pinout

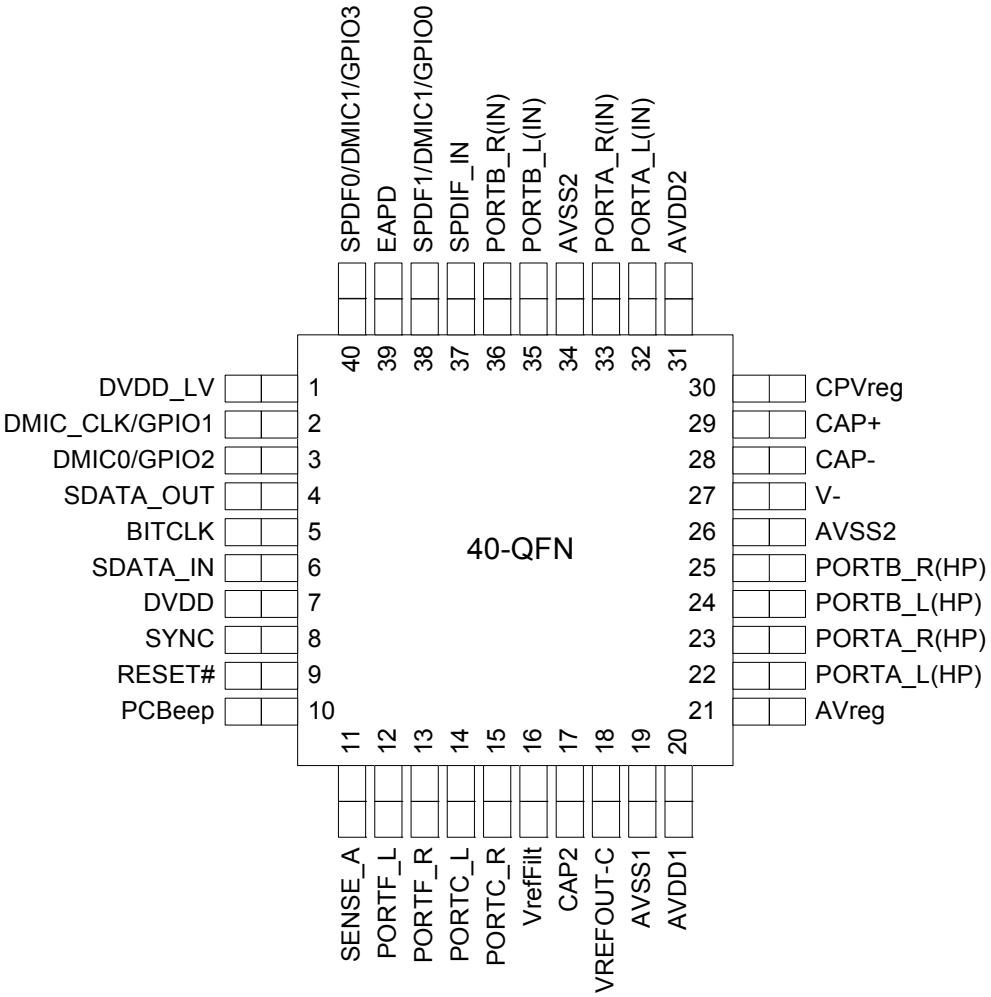


**Figure 15. 40-Pin Pinout**


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## 7.3. Pin Table for 48-Pin

| Pin Name | Pin Function | I/O | Internal Pull-up Pull-down | QFN location |
|---|---|---|---|---|
| DVDD_LV | 1.5V Digital Core Regulator Filter Cap | O(Power) | None | 1 |
| DMIC_CLK/GPIO1 | Digital Mic Clock Output/GPIO1 | I/O(Digital) | 60K Pull-down | 2 |
| DVDD_IO | Reference Voltage (1.5V or 3.3V) | I(Power) | None | 3 |
| DMIC0/GPIO2 | Digital Mic 01 Input/GPIO2 | I/O(Digital) | 60K Pull-down | 4 |
| SDATA_OUT | HD Audio Serial Data output from controller | I(Digital) | None | 5 |
| BITCLK | HD Audio Bit Clock | I(Digital) | None | 6 |
| DVSS | Digital Ground | I(Digital) | None | 7 |
| SDATA_IN | HD Audio Serial Data Input to controller | I/O(Digital) | None | 8 |
| DVDD | Digital Vdd= 3.3V | I(Power) | None | 9 |
| SYNC | HD Audio Frame Sync | I(Digital) | None | 10 |
| RESET# | HD Audio Reset | I(Digital) | None | 11 |
| PCBeep | PC Beep Input | I(Analog) | None | 12 |
| SENSE_A | Jack insertion detection | I(Analog) | None | 13 |
| SENSE_B | Jack insertion detection | I(Analog) | None | 14 |
| PORTE_L | Port E Left | I/O(Analog) | None | 15 |
| PORTE_R | Port E Right | I/O(Analog) | None | 16 |
| PORTF_L | Port F Left | I/O(Analog) | None | 17 |
| PORTF_R | Port F Right | I/O(Analog) | None | 18 |
| PORTC_L | Port C Left | I/O(Analog) | None | 19 |
| PORTC_R | Port C Right | I/O(Analog) | None | 20 |
| VREFFILT | Analog Virtual Ground | O(Analog) | None | 21 |
| CAP 2 | ADC reference bypass capacitor | O(Analog) | None | 22 |
| VREFOUT-E | Reference Voltage out (for mic bias) | O(Analog) | None | 23 |
| VREFOUT-C | Reference Voltage out (for mic bias) | O(Analog) | None | 24 |
| Mono_Out | Mono output port | O(Analog) | None | 25 |
| AVSS1 | Analog Ground | I(Analog) | None | 26 |
| AVDD1 | Analog Vdd=5.0V | I(Analog) | None | 27 |
| AVreg | Analog Core LDO decoupling cap | O(Analog) | None | 28 |
| PORTA_L (HP) | Port A Output Left | O(Analog) | None | 29 |
| PORTA_R (HP) | Port A Output Right | O(Analog) | None | 30 |
| PORTB_L (HP) | Port B Output Left | O(Analog) | None | 31 |
| PORTB_R (HP) | Port B Output Right | O(Analog) | None | 32 |
| AVSS2 | Analog Ground | I(Analog) | None | 33 |
| V- | Charge-pump negative output | O(Analog) | None | 34 |
| CAP- | Charge-pump flying cap - | I(Analog) | None | 35 |
| CAP+ | Charge-pump flying cap + | O(Analog) | None | 36 |

**Table 25. 48-PinTable**


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| Pin Name | Pin Function | I/O | Internal Pull-up Pull-down | QFN location |
|---|---|---|---|---|
| CPVreg | Charge-pump LDO decoupling cap | O(Analog) | None | 37 |
| AVDD2 | Analog Supply for VREG | I(Power) | None | 38 |
| PORTA_L (IN) | Port A Left Input | I(Analog) | None | 39 |
| PORTA_R (IN) | Port A Right Input | I(Analog) | None | 40 |
| AVSS2 | Analog Ground | I(Power) | None | 41 |
| PORTB_L(IN) | Port B Left Input | I(Analog) | None | 42 |
| PORTB_R(IN) | Port B Right Input | I(Analog) | None | 43 |
| GPIO 4 | General purpose I/O | I/O (Digital) | 60K Pull-Down | 44 |
| SPDIFIN | SPDIF Input | I(Digital) | 60K Pull-Down | 45 |
| SPDF1/GPIO0/ DMIC1 | SPDIF 0utput, GPIO0, Digital microphone input | I/O(Digital) | 60K Pull-Down | 46 |
| EAPD | External Amplifier Power Down (active low) | I/O(Digital) | 60K Pull-Up | 47 |
| SPDF0/GPIO3/ DMIC1 | SPDIF 0utput, GPIO3, Digital microphone input | I/O(Digital) | 60K Pull-Down | 48 |

**Table 25. 48-PinTable**

## 7.4. Pin Table for 40-Pin

| Pin Name | Pin Function | I/O | Internal Pull-up Pull-down | QFN location |
|---|---|---|---|---|
| DVDD_LV | 1.5V Digital Core Regulator Filter Cap | O(Power) | None | 1 |
| DMIC_CLK/GPIO1 | Digital Microphone clock output or GPIO 1 | I/O(Digital) | 60K Pull-Down | 2 |
| DMIC0/GPIO2 | Digital Microphone data input or GPIO 2 | I/O(Digital) | 60K Pull-Down | 3 |
| SDATA_OUT | HD Audio Serial Data output from controller | I(Digital) | None | 4 |
| BITCLK | HD Audio Bit Clock | I(Digital) | None | 5 |
| SDATA_IN | HD Audio Serial Data Input to controller | I/O(Digital) | None | 6 |
| DVDD | Digital Vdd= 3.3V | I(Power) | None | 7 |
| SYNC | HD Audio Frame Sync | I(Digital) | None | 8 |
| RESET# | HD Audio Reset | I(Digital) | None | 9 |
| PCBeep | PC Beep input | I(Analog) | None | 10 |
| SENSE_A | Jack insertion detection | I(Analog) | None | 11 |
| PORTF_L | Port F Left | I/O(Analog) | None | 12 |
| PORTF_R | Port F Right | I/O(Analog) | None | 13 |
| PORTC_L | Port C Left | I/O(Analog) | None | 14 |
| PORTC_R | Port C Right | I/O(Analog) | None | 15 |
| VREFFILT | Analog Virtual Ground | O(Analog) | None | 16 |
| CAP 2 | ADC reference bypass capacitor | O(Analog) | None | 17 |

**Table 26. 40-Pin Table**


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| Pin Name | Pin Function | I/O | Internal Pull-up Pull-down | QFN location |
|---|---|---|---|---|
| VREFOUT-C | Reference Voltage out drive (intended for mic bias) | O(Analog) | None | 18 |
| AVSS1 | Analog Ground | I(Power) | None | 19 |
| AVDD1 | Analog Vdd=5.0V or 3.3V | I(Analog) | None | 20 |
| AVreg | Analog Core LDO decoupling cap | O(Analog) | None | 21 |
| PORTA_L (HP) | Port A Output Left | O(Analog) | None | 22 |
| PORTA_R (HP) | Port A Output Right | O(Analog) | None | 23 |
| PORTB_L (HP) | Port B Output Left | O(Analog) | None | 24 |
| PORTB_R (HP) | Port B Output Right | O(Analog) | None | 25 |
| AVSS2 | Analog Ground | I(Power) | None | 26 |
| V- | Charge-pump negative output | O(Analog) | None | 27 |
| CAP- | Charge-pump flying cap - | I(Analog) | None | 28 |
| CAP+ | Charge-pump flying cap + | O(Analog) | None | 29 |
| CPVreg | Charge-pump LDO decoupling cap | I(Analog) | None | 30 |
| AVDD2 | Analog Supply for VREG | I(Power) | None | 31 |
| PORTA_L(IN) | Port A Left Input | I(Analog) | None | 32 |
| PORTA_R(IN) | Port ARight Input | I(Analog) | None | 33 |
| AVSS2 | Analog Ground | I(Power) | None | 34 |
| PORTB_L(IN) | Port B Left Input | I(Analog) | None | 35 |
| PORTB_R(IN) | Port B Right Input | I(Analog) | None | 36 |
| SPDIFIN | SPDIF Input | I (Digital) | 60K Pull-Down | 37 |
| SPDF1/GPIO0/ DMIC1 | SPDIF output, GPIO0, or digital microphone input | I/O(Digital) | 60K Pull-Down | 38 |
| EAPD | External Amplifier Power-Down (active low) | I/O(Digital) | 60K Pull-Up | 39 |
| SPDF0/GPIO3/ DMIC1 | SPDIF output, GPIO3, or digital microphone input | I/O(Digital) | 60K Pull-Down | 40 |

**Table 26. 40-Pin Table**


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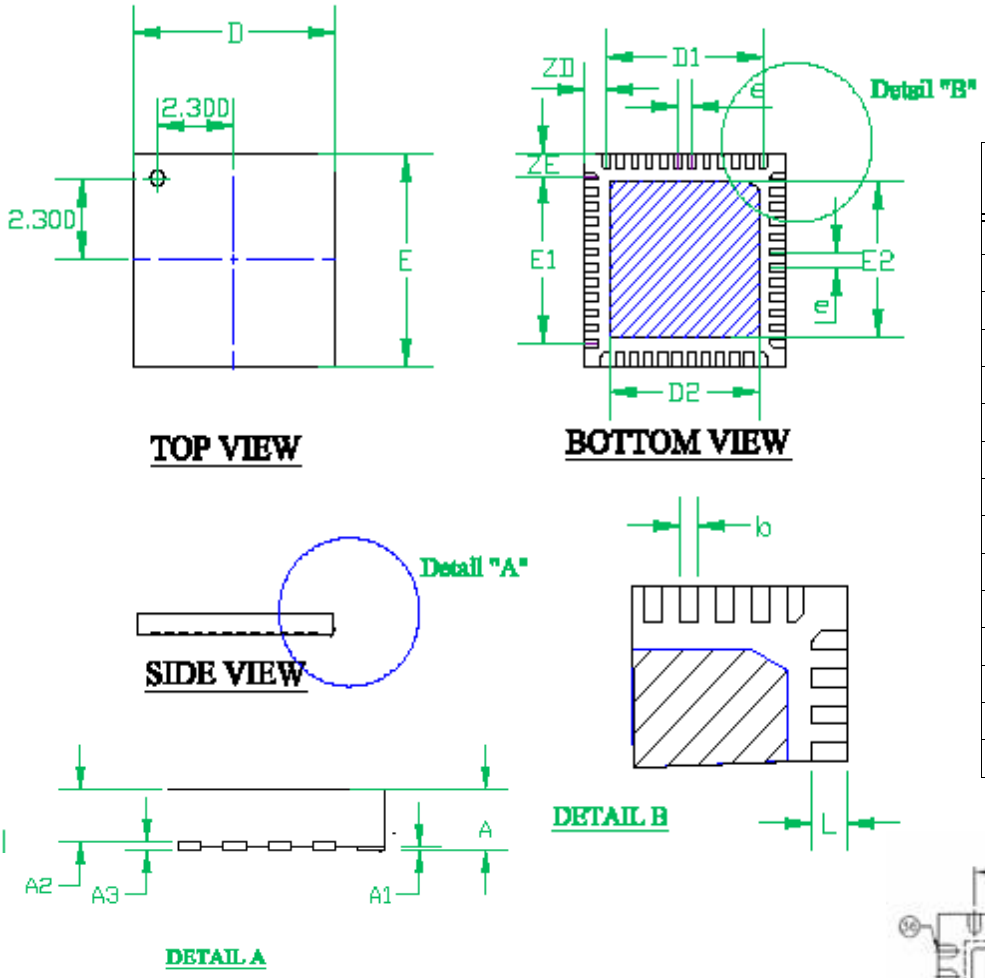
## 7.5. 48QFN Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95




| Key | QFN Dimensions in mm | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.80 | 0.90 | 1.0 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| D | | 7.00 BSC | |
| D1 | | 5.50 BSC | |
| E | | 7.00 BSC | |
| E1 | | 5.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| e | | 0.50 BSC | |
| R | | 0.20-0.25 | |
| b | 0.18 | 0.25 | 0.30 |
| D2 | 5.50 | 5.65 | 5.80 |
| E2 | 5.50 | 5.65 | 5.80 |
| ZD | | 0.75 BSC | |
| ZE | | 0.75 BSC | |

Additional Approved Option

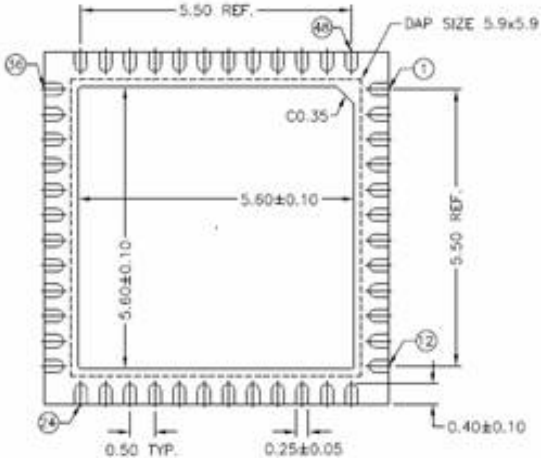



**Figure 16. 48QFN Package Diagram**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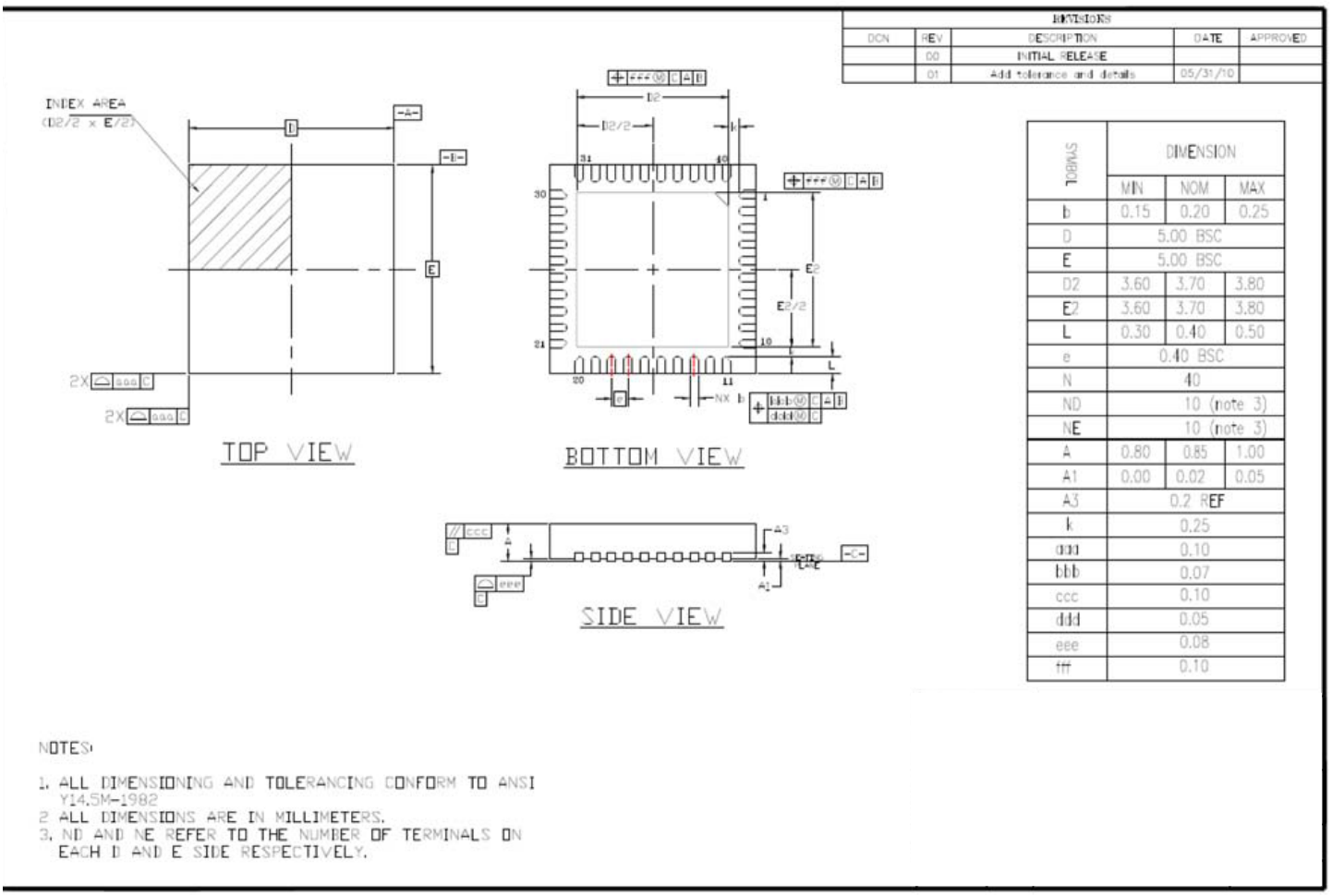
## 7.6. 40QFN Package Outline and Package Dimensions

Package dimensions are kept current with JEDEC Publication No. 95




| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| b | 0.15 | 0.20 | 0.25 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| D2 | 3.60 | 3.70 | 3.80 |
| E2 | 3.60 | 3.70 | 3.80 |
| L | 0.30 | 0.40 | 0.50 |
| e | | 0.40 BSC | |
| N | | 40 | |
| ND | | 10 (note 3) | |
| NE | | 10 (note 3) | |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.2 REF | |
| k | | 0.25 | |
| aaa | | 0.10 | |
| bbb | | 0.07 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

**Figure 17. 40QFN Package Diagram**

## 7.7. Pb Free Process- Package Classification Reflow Temperatures

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350 - 2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6mm | 260 + 0 °C* | 260 + 0 °C* | 260 + 0 °C* |
| 1.6mm - 2.5mm | 260 + 0 °C* | 250 + 0 °C* | 245 + 0 °C* |
| > or = 2.5mm | 250 + 0 °C* | 245 + 0 °C* | 245 + 0 °C* |
| *Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0 °C. For example 260 °C+0 °C) at the rated MSL level. | | | |

**Table 27. Reflow**

Note: TSI's package thicknesses are <2.5mm and <350 $mm^3$, so 260 applies in every case.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# 9. DOCUMENT REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| 0.5 | November 2010 | Initial release |
| 0.6 | March 2011 | Pin out and package changes |
| 0.7 | April 2011 | Added 3.3V AVDD options, part numbers, device ID and electrical/performance characteristics. Pin defaults and combo jack description added. Corrected MonoMux and Mono/Mix in 40QFN package to VSW in widget list. |
| 0.8 | July 2011 | Corrected pin numbers for ports A&D in table 1 port functionality. Clarified Mono Output and digital mic description text. Corrected Jack detect sense resistor. |
| 0.85 | August 2011 | Updated minimum values with typical performance values on analog performance. |
| 0.90 | October 2011 | Added widget details |
| 0.91 | October 2011 | ZB silicon default value changed from 5h to 6h in the AFG: AnaCapless VRegSel (bits 27:24). Added PVdd max value to electrical characteristics section. Removed 92HD66C3X3 part number option, it will not be offered. Corrected WLCSP column in pinout tables, there is no WLCSP option for this device. |
| 1.0 | February 2012 | Removed Preliminary status. |
| 1.1 | May 2012 | Correct functional block diagram for SPDIF I/O data and pin numbers, correct Port Pin numbers |
| 1.2 | September 2014 | Released in TSI Format |

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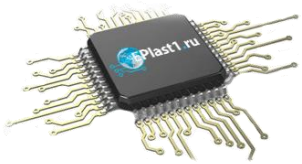


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