

# NCV8405A, NCV8405B

## Self-Protected Low Side Driver with Temperature and Current Limit

NCV8405A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device is suitable for harsh automotive environments.

### Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

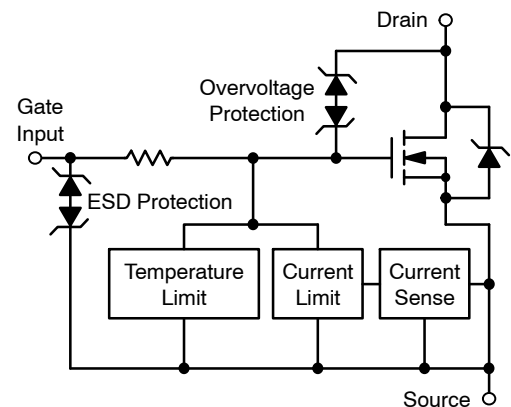


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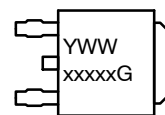
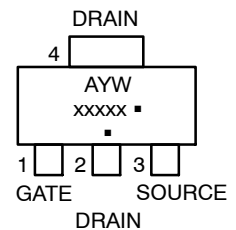
[www.onsemi.com](http://www.onsemi.com)

| $V_{(BR)DSS}$<br>(Clamped) | $R_{DS(ON)}$ TYP | $I_D$ MAX |
|----------------------------|------------------|-----------|
| 42 V                       | 90 mΩ @ 10 V     | 6.0 A*    |

\*Max current limit value is dependent on input condition.



### MARKING DIAGRAM



A = Assembly Location

Y = Year

W, WW = Work Week

xxxxx = 8405A or 8405B

G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

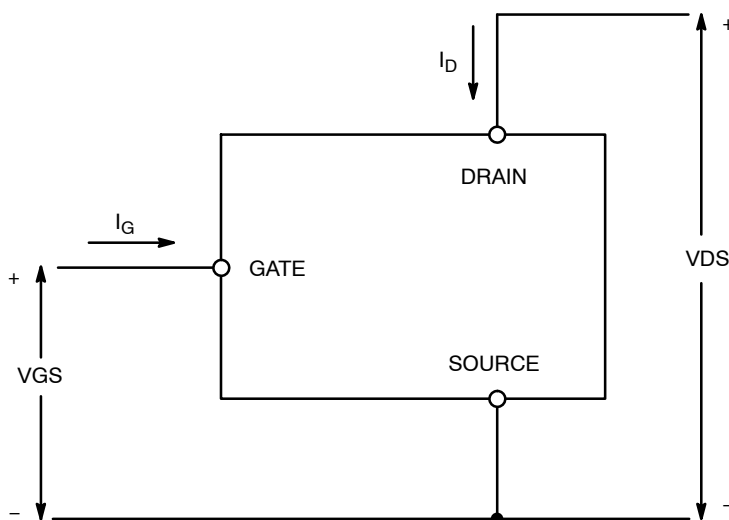
# NCV8405A, NCV8405B

## MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

| Rating   | Symbol   | Value              | Unit |
|--|--|--------------------|------|
| Drain-to-Source Voltage Internally Clamped   | V <sub>DSS</sub>   | 42                 | V    |
| Drain-to-Gate Voltage Internally Clamped (R <sub>G</sub> = 1.0 MΩ)   | V <sub>DGR</sub>   | 42                 | V    |
| Gate-to-Source Voltage   | V <sub>GS</sub>  | ± 14               | V    |
| Continuous Drain Current   | I <sub>D</sub>   | Internally Limited |      |
| Power Dissipation – SOT-223 Version<br>@ T <sub>A</sub> = 25°C (Note 1)<br>@ T <sub>A</sub> = 25°C (Note 2)<br>@ T <sub>S</sub> = 25°C   | P <sub>D</sub>   | 1.0                | W    |
| Power Dissipation – DPAK Version<br>@ T <sub>A</sub> = 25°C (Note 1)<br>@ T <sub>A</sub> = 25°C (Note 2)<br>@ T <sub>S</sub> = 25°C  |  | 2.0<br>2.5<br>40   |      |
| Thermal Resistance – SOT-223 Version<br>Junction-to-Ambient Steady State (Note 1)<br>Junction-to-Ambient Steady State (Note 2)<br>Junction-to-Soldering Point Steady State               | R <sub>θJA</sub><br>R <sub>θJA</sub><br>R <sub>θJS</sub> | 130<br>72<br>11    | °C/W |
| Thermal Resistance – DPAK Version<br>Junction-to-Ambient Steady State (Note 1)<br>Junction-to-Ambient Steady State (Note 2)<br>Junction-to-Soldering Point Steady State                  | R <sub>θJA</sub><br>R <sub>θJA</sub><br>R <sub>θJS</sub> | 60<br>50<br>3.0    |      |
| Single Pulse Drain-to-Source Avalanche Energy<br>(V <sub>DD</sub> = 40 V, V <sub>G</sub> = 5.0 V, I <sub>PK</sub> = 2.8 A, L = 80 mH, R <sub>G(ext)</sub> = 25 Ω, T <sub>J</sub> = 25°C) | E <sub>AS</sub>  | 275                | mJ   |
| Load Dump Voltage V <sub>LD</sub> = V <sub>A</sub> + V <sub>S</sub> (V <sub>GS</sub> = 0 and 10 V, R <sub>I</sub> = 2.0 Ω, R <sub>L</sub> = 6.0 Ω, t <sub>d</sub> = 400 ms)              | V <sub>LD</sub>  | 53                 | V    |
| Operating Junction Temperature   | T <sub>J</sub>   | -40 to 150         | °C   |
| Storage Temperature  | T <sub>stg</sub>   | -55 to 150         | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted onto min pad FR4 PCB, (2 oz. Cu, 0.06" thick).
- Surface-mounted onto 2" sq. FR4 board (1" sq., 1 oz. Cu, 0.06" thick).



**Figure 1. Voltage and Current Convention**

# NCV8405A, NCV8405B

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

| Parameter                                  | Test Condition   | Symbol               | Min | Typ | Max | Unit |
|--|--|----------------------|-----|-----|-----|------|
| <b>OFF CHARACTERISTICS</b>                 |  |                      |     |     |     |      |
| Drain-to-Source Breakdown Voltage (Note 3) | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 25°C           | V <sub>(BR)DSS</sub> | 42  | 46  | 51  | V    |
|  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C (Note 5) |                      | 42  | 45  | 51  |      |
| Zero Gate Voltage Drain Current            | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 25°C           | I <sub>DSS</sub>     |     | 0.5 | 2.0 | μA   |
|  | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V, T <sub>J</sub> = 150°C (Note 5) |                      |     | 2.0 | 10  |      |
| Gate Input Current                         | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 5.0 V                                 | I <sub>GSSF</sub>    |     | 50  | 100 | μA   |

## ON CHARACTERISTICS (Note 3)

|  |  |                                     |     |      |     |        |
|--|--|-------------------------------------|-----|------|-----|--------|
| Gate Threshold Voltage                 | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 150 μA                      | V <sub>GS(th)</sub>                 | 1.0 | 1.6  | 2.0 | V      |
| Gate Threshold Temperature Coefficient |  | V <sub>GS(th)</sub> /T <sub>J</sub> |     | 4.0  |     | -mV/°C |
| Static Drain-to-Source On-Resistance   | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 25°C            | R <sub>DS(on)</sub>                 |     | 90   | 100 | mΩ     |
|  | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 150°C (Note 5)  |                                     |     | 165  | 190 |        |
|  | V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 25°C           |                                     |     | 105  | 120 |        |
|  | V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 1.4 A, T <sub>J</sub> = 150°C (Note 5) |                                     |     | 185  | 210 |        |
|  | V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 25°C           |                                     |     | 105  | 120 |        |
|  | V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 0.5 A, T <sub>J</sub> = 150°C (Note 5) |                                     |     | 185  | 210 |        |
| Source-Drain Forward On Voltage        | V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7.0 A                                    | V <sub>SD</sub>                     |     | 1.05 |     | V      |

## SWITCHING CHARACTERISTICS (Note 5)

|   |  |                                     |  |     |  |      |
|---|--|-------------------------------------|--|-----|--|------|
| Turn-ON Time (10% V <sub>IN</sub> to 90% I <sub>D</sub> )   | V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V<br>I <sub>D</sub> = 2.5 A, R <sub>L</sub> = 4.7 Ω | t <sub>ON</sub>                     |  | 20  |  | μs   |
| Turn-OFF Time (90% V <sub>IN</sub> to 10% I <sub>D</sub> )  |  | t <sub>OFF</sub>                    |  | 110 |  |      |
| Slew-Rate ON (70% V <sub>DS</sub> to 50% V <sub>DS</sub> )  | V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V,<br>R <sub>L</sub> = 4.7 Ω                        | -dV <sub>DS</sub> /dt <sub>ON</sub> |  | 1.0 |  | V/μs |
| Slew-Rate OFF (50% V <sub>DS</sub> to 70% V <sub>DS</sub> ) |  | dV <sub>DS</sub> /dt <sub>OFF</sub> |  | 0.4 |  |      |

## SELF PROTECTION CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (Note 4)

|                              |  |                       |     |      |     |    |
|------------------------------|--|-----------------------|-----|------|-----|----|
| Current Limit                | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 25°C           | I <sub>LIM</sub>      | 6.0 | 9.0  | 11  | A  |
|                              | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5.0 V, T <sub>J</sub> = 150°C (Note 5) |                       | 3.0 | 5.0  | 8.0 |    |
|                              | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 25°C            |                       | 7.0 | 10.5 | 13  |    |
|                              | V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 10 V, T <sub>J</sub> = 150°C (Note 5)  |                       | 4.0 | 7.5  | 10  |    |
| Temperature Limit (Turn-off) | V <sub>GS</sub> = 5.0 V (Note 5)   | T <sub>LIM(off)</sub> | 150 | 180  | 200 | °C |
| Thermal Hysteresis           | V <sub>GS</sub> = 5.0 V  | ΔT <sub>LIM(on)</sub> |     | 15   |     |    |
| Temperature Limit (Turn-off) | V <sub>GS</sub> = 10 V (Note 5)  | T <sub>LIM(off)</sub> | 150 | 165  | 185 |    |
| Thermal Hysteresis           | V <sub>GS</sub> = 10 V   | ΔT <sub>LIM(on)</sub> |     | 15   |     |    |

## GATE INPUT CHARACTERISTICS (Note 5)

|  |  |                  |  |      |  |    |
|--|--|------------------|--|------|--|----|
| Device ON Gate Input Current           | V <sub>GS</sub> = 5 V, I <sub>D</sub> = 1.0 A  | I <sub>GON</sub> |  | 50   |  | μA |
|  | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A |                  |  | 400  |  |    |
| Current Limit Gate Input Current       | V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V  | I <sub>GCL</sub> |  | 0.05 |  | mA |
|  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V |                  |  | 0.4  |  |    |
| Thermal Limit Fault Gate Input Current | V <sub>GS</sub> = 5 V, V <sub>DS</sub> = 10 V  | I <sub>GTL</sub> |  | 0.22 |  | mA |
|  | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 10 V |                  |  | 1.0  |  |    |

## ESD ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted) (Note 5)

|                                     |                        |     |      |  |  |   |
|-------------------------------------|------------------------|-----|------|--|--|---|
| Electro-Static Discharge Capability | Human Body Model (HBM) | ESD | 4000 |  |  | V |
|                                     | Machine Model (MM)     |     | 400  |  |  |   |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

TYPICAL PERFORMANCE CURVES

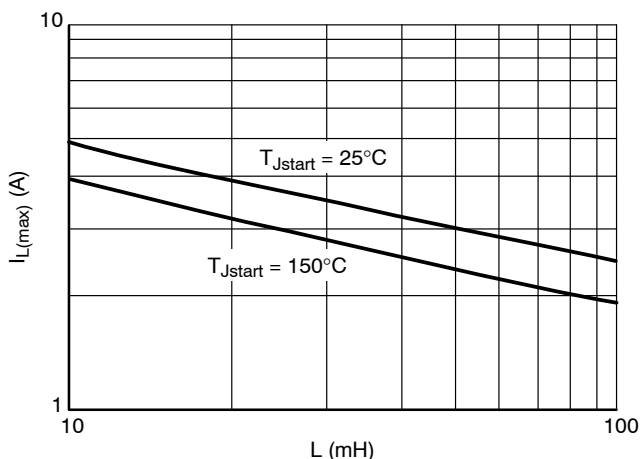


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

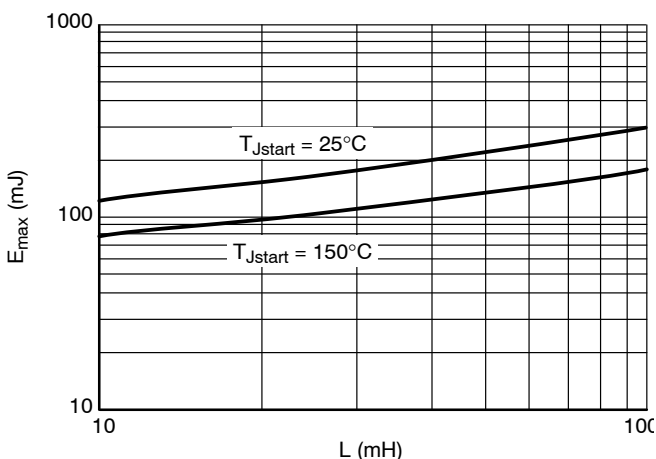


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

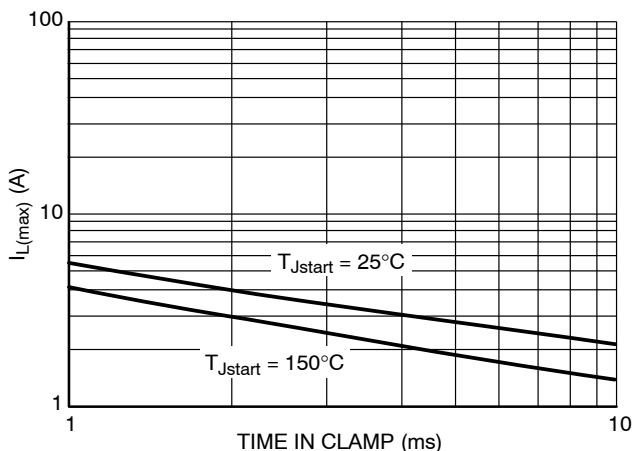


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

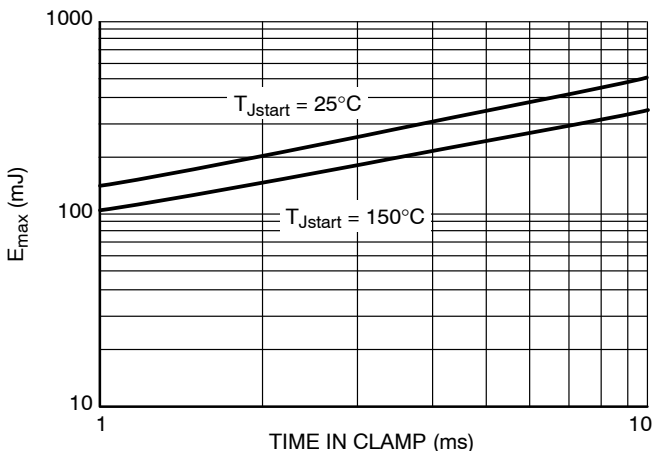


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

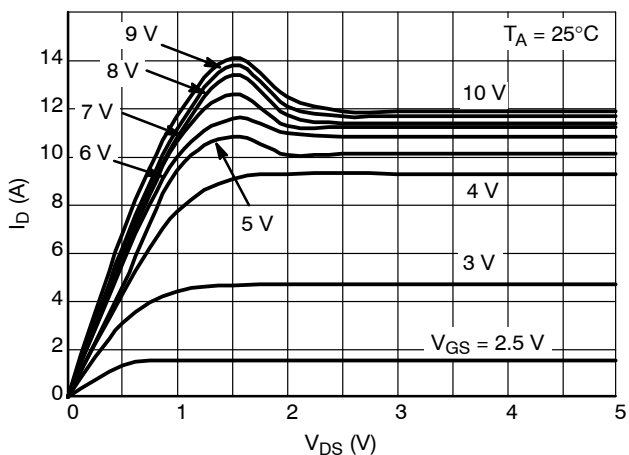


Figure 6. Output Characteristics

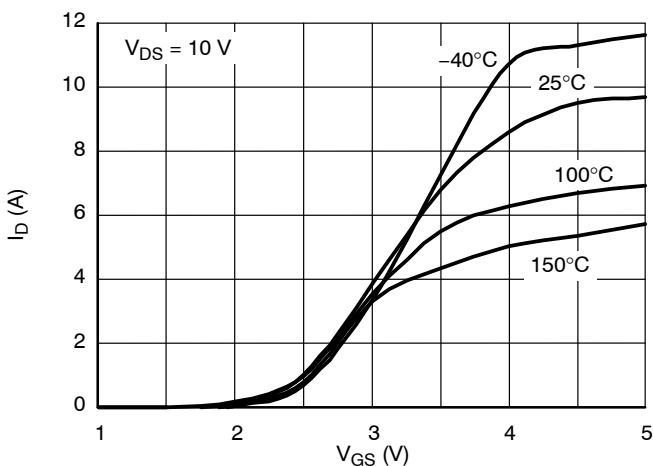


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

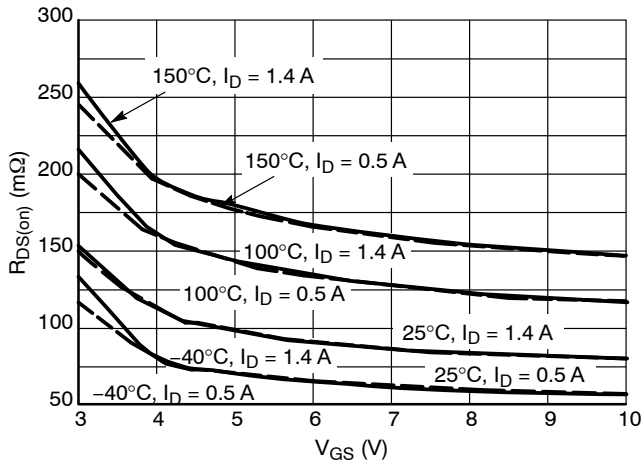


Figure 8.  $R_{DS(on)}$  vs. Gate-Source Voltage

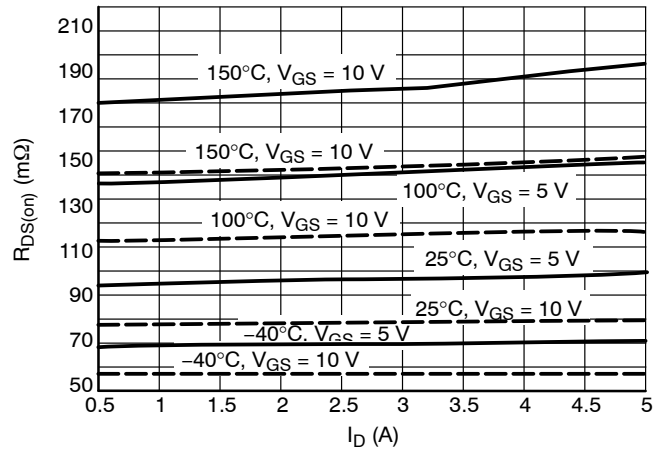


Figure 9.  $R_{DS(on)}$  vs. Drain Current

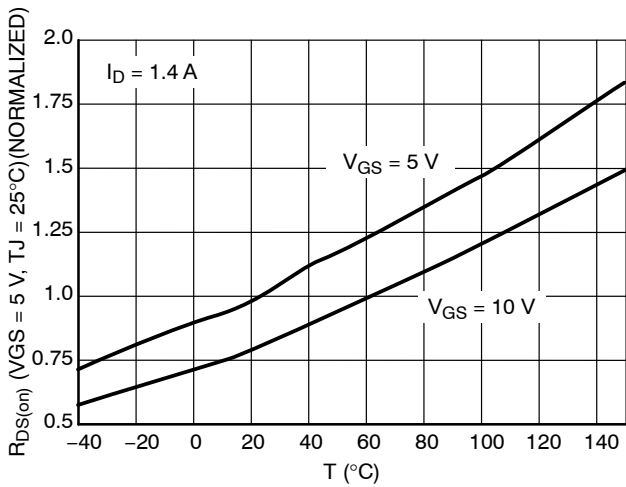


Figure 10. Normalized  $R_{DS(on)}$  vs. Temperature

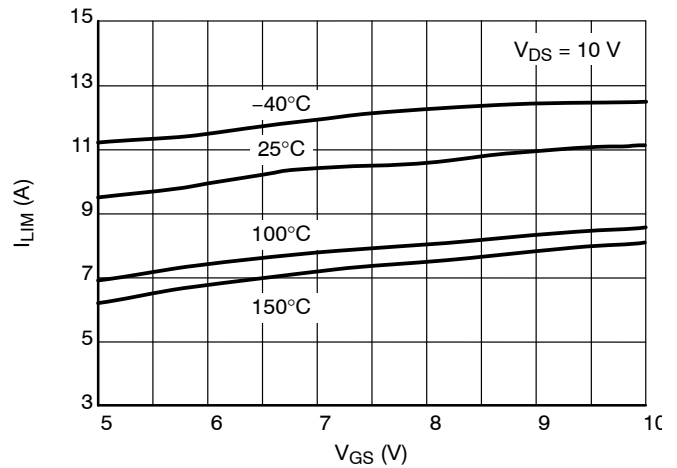


Figure 11. Current Limit vs. Gate-Source Voltage

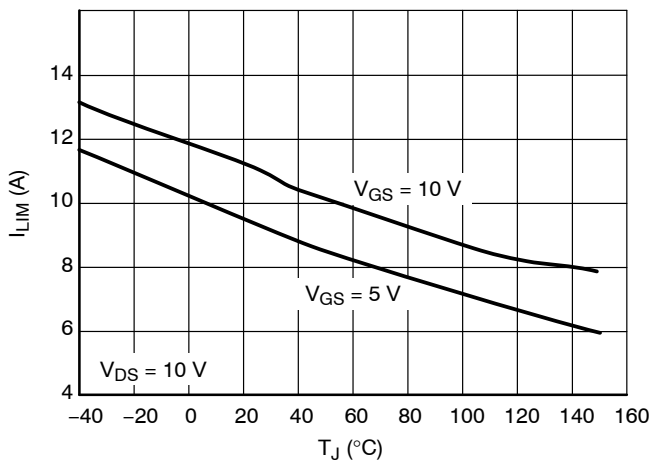


Figure 12. Current Limit vs. Junction Temperature

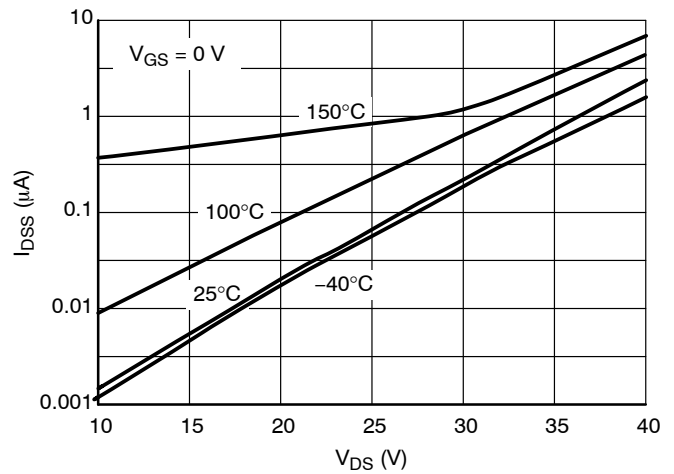


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

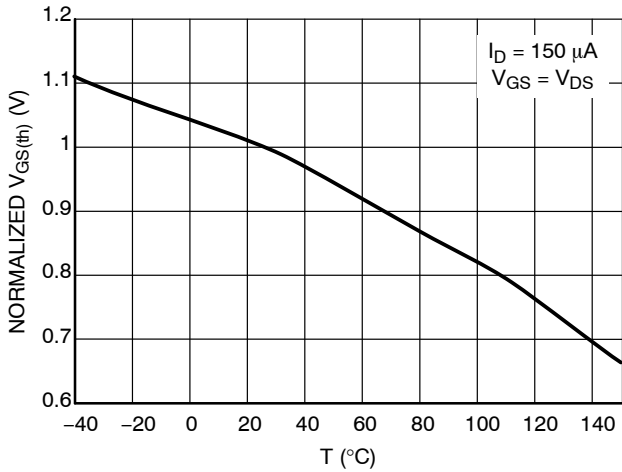


Figure 14. Normalized Threshold Voltage vs. Temperature

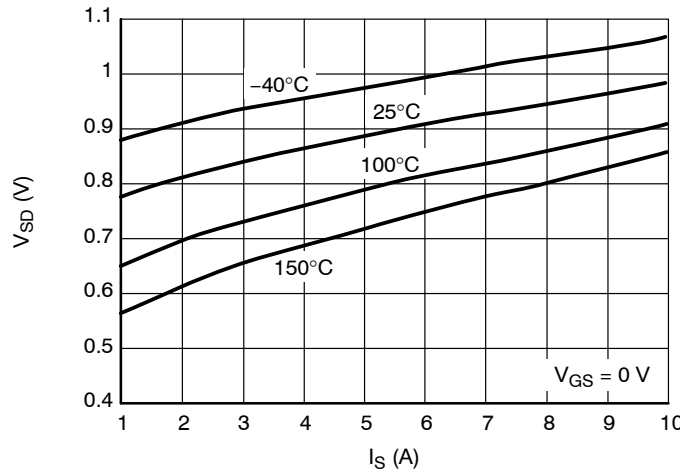


Figure 15. Body-Diode Forward Characteristics

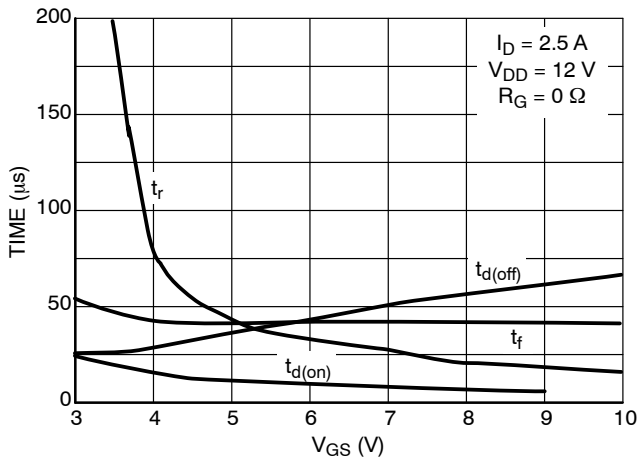


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

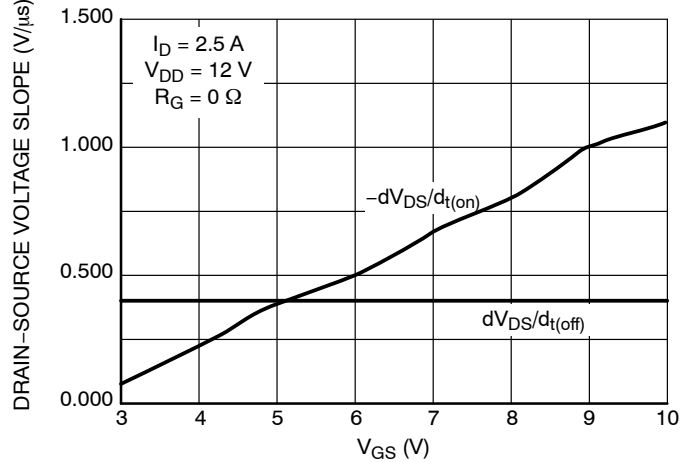


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

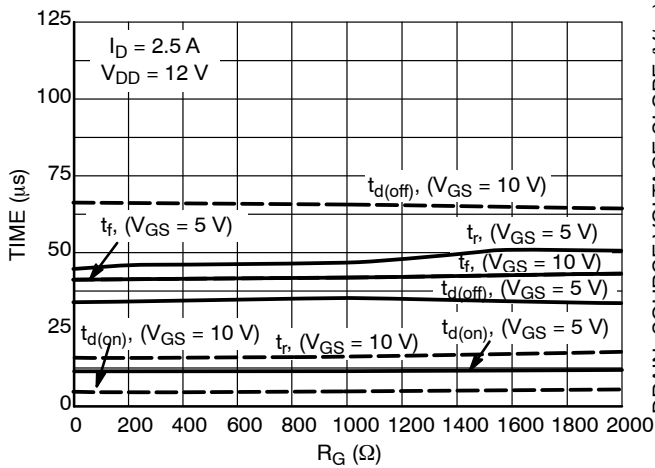


Figure 18. Resistive Load Switching Time vs. Gate Resistance

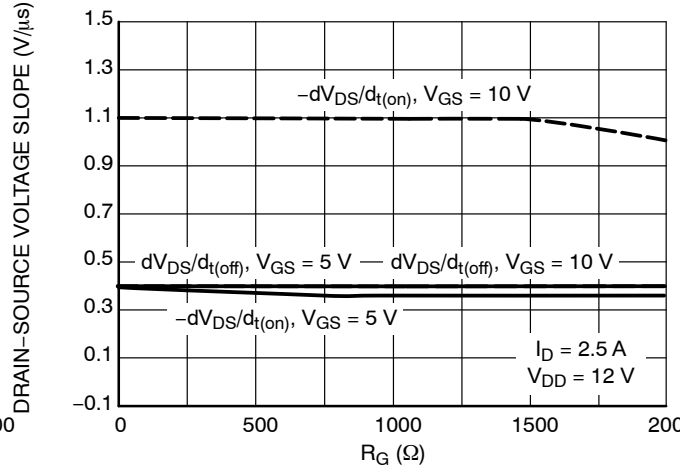


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

# NCV8405A, NCV8405B

## TYPICAL PERFORMANCE CURVES

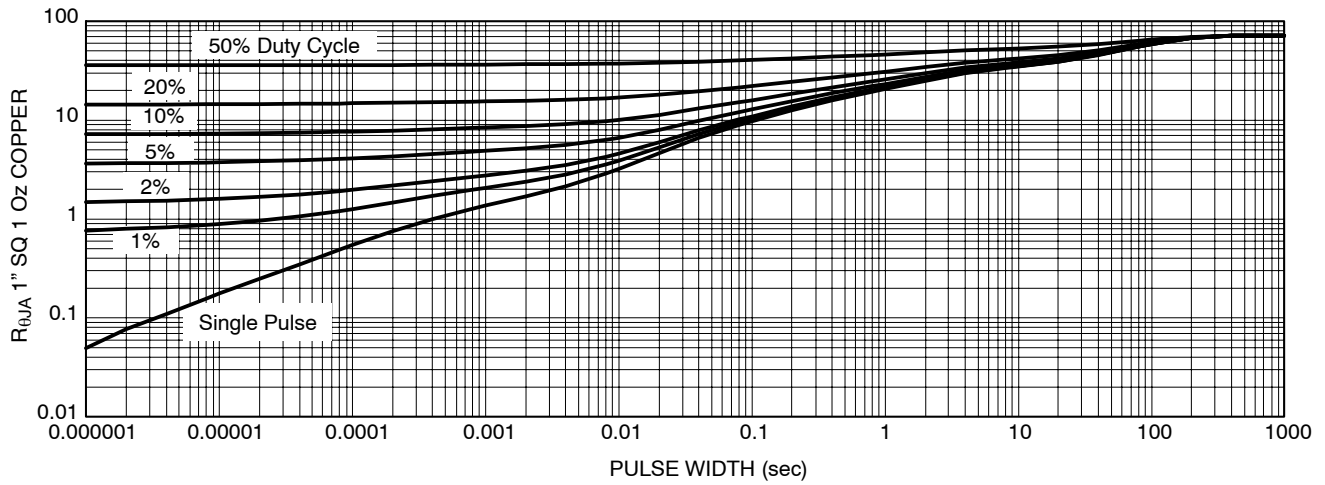


Figure 20. Transient Thermal Resistance

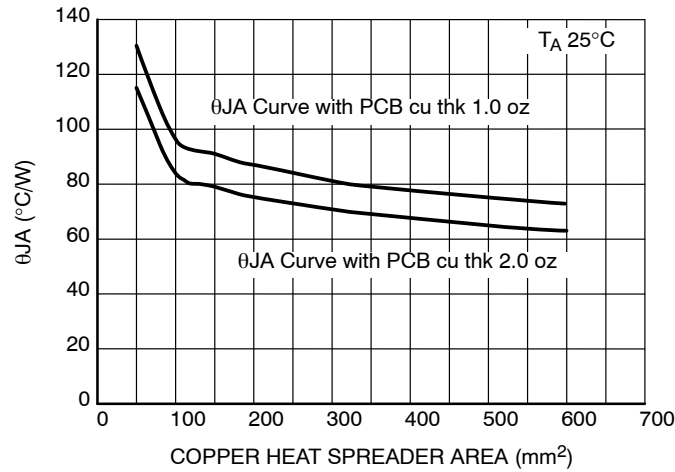


Figure 21.  $\theta_{JA}$  vs. Copper

# NCV8405A, NCV8405B

## TEST CIRCUITS AND WAVEFORMS



Figure 22. Resistive Load Switching Test Circuit

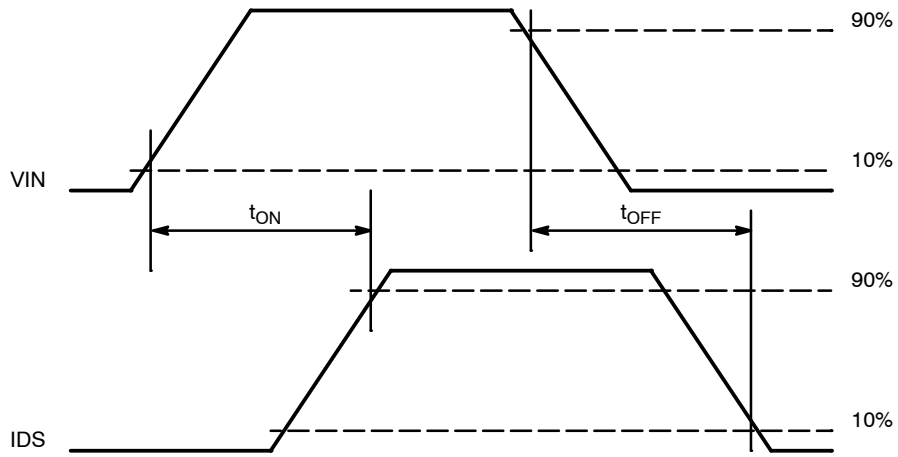


Figure 23. Resistive Load Switching Waveforms



# NCV8405A, NCV8405B

## TEST CIRCUITS AND WAVEFORMS

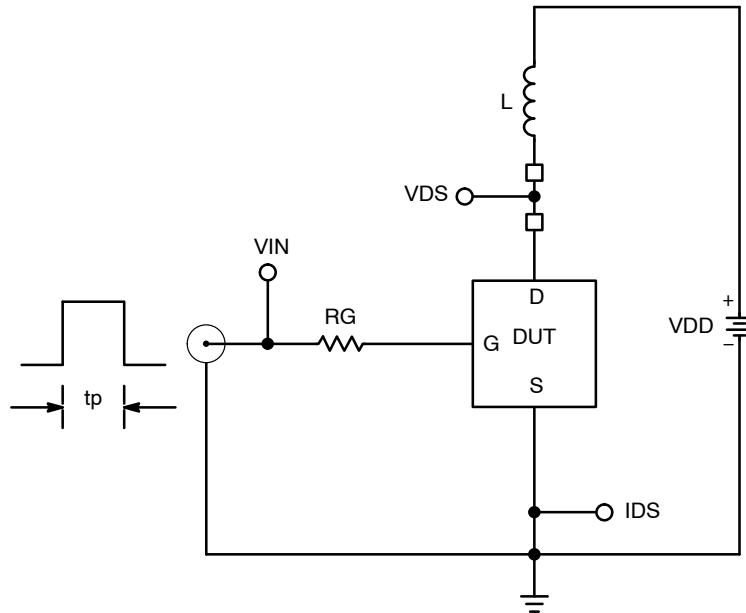


Figure 24. Inductive Load Switching Test Circuit



Figure 25. Inductive Load Switching Waveforms

# NCV8405A, NCV8405B

## ORDERING INFORMATION

| Device        | Package              | Shipping†          |
|---------------|----------------------|--------------------|
| NCV8405ASTT1G | SOT-223<br>(Pb-Free) | 1000 / Tape & Reel |
| NCV8405ASTT3G | SOT-223<br>(Pb-Free) | 4000 / Tape & Reel |
| NCV8405ADTRKG | DPAK<br>(Pb-Free)    | 2500 / Tape & Reel |
| NCV8405BDTRKG | DPAK<br>(Pb-Free)    | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN.     | NOM. | MAX. |
| A           | 1.50     | 1.63 | 1.75 |
| A1          | 0.02     | 0.06 | 0.10 |
| b           | 0.60     | 0.75 | 0.89 |
| b1          | 2.90     | 3.06 | 3.20 |
| c           | 0.24     | 0.29 | 0.35 |
| D           | 6.30     | 6.50 | 6.70 |
| E           | 3.30     | 3.50 | 3.70 |
| e           | 2.30 BSC |      |      |
| L           | 0.20     | ---  | ---  |
| L1          | 1.50     | 1.75 | 2.00 |
| He          | 6.70     | 7.00 | 7.30 |
| θ           | 0°       | ---  | 10°  |



|                  |                  |  |
|------------------|------------------|--|
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| DESCRIPTION:     | SOT-223 (TO-261) | PAGE 1 OF 2  |

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**SOT-223 (TO-261)**  
**CASE 318E-04**  
**ISSUE R**

DATE 02 OCT 2018

- |  |   |   |   |   |
|--|---|---|---|---|
| <b>STYLE 1:</b><br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR | <b>STYLE 2:</b><br>PIN 1. ANODE<br>2. CATHODE<br>3. NC<br>4. CATHODE        | <b>STYLE 3:</b><br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN           | <b>STYLE 4:</b><br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE<br>4. DRAIN   | <b>STYLE 5:</b><br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE<br>4. GATE    |
| <b>STYLE 6:</b><br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT<br>4. INPUT        | <b>STYLE 7:</b><br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2<br>4. CATHODE | <b>STYLE 8:</b><br>CANCELLED  | <b>STYLE 9:</b><br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC<br>4. GROUND | <b>STYLE 10:</b><br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE<br>4. ANODE |
| <b>STYLE 11:</b><br>PIN 1. MT 1<br>2. MT 2<br>3. GATE<br>4. MT 2             | <b>STYLE 12:</b><br>PIN 1. INPUT<br>2. OUTPUT<br>3. NC<br>4. OUTPUT         | <b>STYLE 13:</b><br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER<br>4. COLLECTOR |   |   |

**GENERIC  
 MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)  
 \*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                         |                         |  |
|-------------------------|-------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>SOT-223 (TO-261)</b> | <b>PAGE 2 OF 2</b>   |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015

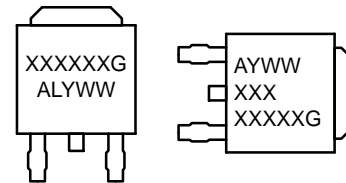


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.086     | 0.094 | 2.18        | 2.38  |
| A1  | 0.000     | 0.005 | 0.00        | 0.13  |
| b   | 0.025     | 0.035 | 0.63        | 0.89  |
| b2  | 0.028     | 0.045 | 0.72        | 1.14  |
| b3  | 0.180     | 0.215 | 4.57        | 5.46  |
| c   | 0.018     | 0.024 | 0.46        | 0.61  |
| c2  | 0.018     | 0.024 | 0.46        | 0.61  |
| D   | 0.235     | 0.245 | 5.97        | 6.22  |
| E   | 0.250     | 0.265 | 6.35        | 6.73  |
| e   | 0.090 BSC |       | 2.29 BSC    |       |
| H   | 0.370     | 0.410 | 9.40        | 10.41 |
| L   | 0.055     | 0.070 | 1.40        | 1.78  |
| L1  | 0.114 REF |       | 2.90 REF    |       |
| L2  | 0.020 BSC |       | 0.51 BSC    |       |
| L3  | 0.035     | 0.050 | 0.89        | 1.27  |
| L4  | ---       | 0.040 | ---         | 1.01  |
| Z   | 0.155     | ---   | 3.93        | ---   |

### GENERIC MARKING DIAGRAM\*



IC

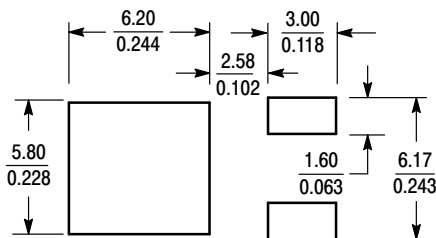
Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*




SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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| <b>NEW STANDARD:</b>    | <b>REF TO JEDEC TO-252</b>             |  |
| <b>DESCRIPTION:</b>     | <b>DPAK SINGLE GAUGE SURFACE MOUNT</b> | <b>PAGE 1 OF 2</b>   |



| ISSUE | REVISION   | DATE        |
|-------|--|-------------|
| O     | RELEASED FOR PRODUCTION. REQ. BY L. GAN  | 24 SEP 2001 |
| A     | ADDED STYLE 8. REQ. BY S. ALLEN.   | 06 AUG 2008 |
| B     | ADDED STYLE 9. REQ. BY D. WARNER.  | 16 JAN 2009 |
| C     | ADDED STYLE 10. REQ. BY S. ALLEN.  | 09 JUN 2009 |
| D     | RELABELED DRAWING TO JEDEC STANDARDS. ADDED SIDE VIEW DETAIL A. CORRECTED MARKING INFORMATION. REQ. BY D. TRUHITE.                     | 29 JUN 2010 |
| E     | ADDED ALTERNATE CONSTRUCTION BOTTOM VIEW. MODIFIED DIMENSIONS b2 AND L1. CORRECTED MARKING DIAGRAM FOR DISCRETE. REQ. BY I. CAMBALIZA. | 06 FEB 2014 |
| F     | ADDED SECOND ALTERNATE CONSTRUCTION BOTTOM VIEW. REQ. BY K. MUSTAFA.   | 21 JUL 2015 |
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**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.