

S3A3 Microcontroller Group

Datasheet

Renesas Synergy™ Platform

Synergy Microcontrollers

S3 Series

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High efficiency 48-MHz Arm® Cortex®-M4 core, 512-KB code flash memory, 96-KB SRAM, Segment LCD Controller, Capacitive Touch Sensing Unit, USB 2.0 Full-Speed, 14-Bit A/D Converter, 12-Bit D/A Converter, security and safety features.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)

- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 48 MHz
- Support for 4-GB address space
- Arm Memory Protection Unit (Arm MPU) with 8 regions
- Debug and Trace: ITM, DWT, FPB, TPIU, and ETB
- CoreSight™ debug port: JTAG-DP and SW-DP

■ Memory

- 512-KB code flash memory
- 8-KB data flash memory (100,000 erase/write cycles)
- 96-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity

- USB 2.0 Full-Speed (USBFS) module
 - On-chip transceiver with voltage regulator
 - Compliant with USB Battery Charging Specification 1.2
- Serial Communications Interface (SCI) × 6
 - UART
 - Simple IIC
 - Simple SPI
- Serial Peripheral Interface (SPI) × 2
- I²C bus interface (IIC) × 3
- Controller Area Network (CAN) module
- Serial Sound Interface Enhanced (SSIE)
- SD/MMC Host Interface (SDHI)
- Quad Serial Peripheral Interface (QSPI)
- External address space
 - 8-bit or 16-bit bus space is selectable per area

■ Analog

- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- 8-bit D/A Converter (DAC8) × 2 (for ACMPLP)
- Low Power Analog Comparator (ACMPLP) × 2
- Operational Amplifier (OPAMP) × 4
- Temperature Sensor (TSN)

■ Timers

- General PWM Timer 32-bit (GPT32) × 4
- General PWM Timer 16-bit (GPT16) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety

- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management

- Low power modes
- RealTime Clock (RTC) with calendar and Battery Backup support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 4
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption

- AES128/256
- GHASH
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)

- Segment LCD Controller (SLCDC)
 - Up to 54 segments × 4 commons
 - Up to 50 segments × 8 commons
- Capacitive Touch Sensing Unit (CTSUS)

■ Multiple Clock Sources

- Main clock oscillator (MOSC)
 - (1 to 20 MHz when VCC = 2.4 to 5.5 V)
 - (1 to 8 MHz when VCC = 1.8 to 2.4 V)
 - (1 to 4 MHz when VCC = 1.6 to 1.8 V)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO)
 - (24, 32, 48, 64 MHz when VCC = 2.4 to 5.5 V)
 - (24, 32, 48 MHz when VCC = 1.8 to 5.5 V)
 - (24, 32 MHz when VCC = 1.6 to 5.5 V)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General Purpose I/O Ports

- Up to 126 input/output pins
 - Up to 3 CMOS input
 - Up to 123 CMOS input/output
 - Up to 11 input/output 5 V tolerant
 - Up to 2 high current (20 mA)

■ Operating Voltage

- VCC: 1.6 to 5.5 V

■ Operating Temperature and Packages

- Ta = -40°C to +85°C
 - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
 - 121-pin BGA (8 mm × 8 mm, 0.65 mm pitch)
 - 100-pin LGA (7 mm × 7 mm, 0.65 mm pitch)
- Ta = -40°C to +105°C
 - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
 - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)
 - 64-pin LQFP (10 mm × 10 mm, 0.5 mm pitch)
 - 64-pin QFN (8 mm × 8 mm, 0.4 mm pitch)

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share a common set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a low-power and high-performance Arm Cortex®-M4 32-bit core running up to 48 MHz, with the following features:

- 512-KB code flash memory
- 96-KB SRAM
- Segment LCD Controller (SLCDC)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed Module (USBFS)
- 14-bit A/D Converter (ADC14)
- 12-bit D/A Converter (DAC12)
- Security features.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	<ul style="list-style-type: none"> • Maximum operating frequency: up to 48 MHz • Arm Cortex-M4 core: <ul style="list-style-type: none"> - Revision: r0p1-01rel0 - Armv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): <ul style="list-style-type: none"> - Armv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: <ul style="list-style-type: none"> - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 512 KB of code flash memory. See section 47, Flash Memory in User's Manual.
Data flash memory	8 KB of data flash memory. See section 47, Flash Memory in User's Manual.
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory in User's Manual.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the desired application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM with either parity bit or Error Correction Code (ECC). An area in SRAM0 provides error correction capability using ECC. See section 46, SRAM in User's Manual.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: <ul style="list-style-type: none"> • Single-chip mode • SCI/USB boot mode. See section 3, Operating Modes in User's Manual.
Resets	14 resets: <ul style="list-style-type: none"> • RES pin reset • Power-on reset • VBATT-selected voltage power-on reset • Independent watchdog timer reset • Watchdog timer reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	<ul style="list-style-type: none"> • Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IWDG-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low Power Mode	Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery powered area includes RTC, SOSC, LOCO, wakeup control, backup memory, VBATT_R low voltage detection, and switch between VCC and VBATT. During normal operation, the battery powered area is powered by the main power supply, which is the VCC pin. When a VCC voltage fall is detected, the power source is switched to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source is switched from the VBATT pin to the VCC pin. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.

Table 1.3 System (2 of 2)

Feature	Functional description
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. The refresh-permitted period can be set to refresh the counter and used as the condition for detecting when the system runs out of control. See section 26, Watchdog Timer (WDT) in User's Manual.
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt/interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail-safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 27, Independent Watchdog Timer (IWDT) in User's Manual.

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual.

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual.
DMA Controller (DMAC)	A 4-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual.

Table 1.6 External bus interface

Feature	Functional description
External bus	<ul style="list-style-type: none"> • CS area: Connected to the external devices (external memory interface) • QSPI area: Connected to the QSPI (external device interface).

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 4 channels and a 16-bit timer with 6 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual.
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual.
Asynchronous General Purpose Timer (AGT)	The Asynchronous General Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and they can be accessed with the AGT register. See section 24, Asynchronous General Purpose Timer (AGT) in User's Manual.
RealTime Clock (RTC)	The RealTime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 25, RealTime Clock (RTC) in User's Manual.

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communication Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: <ul style="list-style-type: none"> • Asynchronous interfaces (UART and asynchronous communications interface adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. SCI0 and SCI1 have FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 29, Serial Communications Interface (SCI) in User's Manual.
I ² C bus interface (IIC)	The 3-channel I ² C bus interface (IIC) conforms with and provides a subset of the NXP I ² C (Inter-Integrated Circuit) bus interface functions. See section 30, I ² C Bus Interface (IIC) in User's Manual.
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 32, Serial Peripheral Interface (SPI) in User's Manual.
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface digital audio devices for transmitting PCM audio data over a serial bus with the MCU. The SSIE supports an audio clock frequency of up to 25 MHz, and can be operated as a slave or master receiver/transmitter/transceiver to suit various applications. The SSIE includes 8-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 35, Serial Sound Interface Enhanced (SSIE) in User's Manual.
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 33, Quad Serial Peripheral Interface (QSPI) in User's Manual.

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 31, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging Specification. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply at 3.3 V. See section 28, USB 2.0 Full-Speed Module (USBFS) in User's Manual.
SD/MMC Host Interface (SDHI)	The Secure Digital Host Interface (SDHI) and MultiMediaCard (MMC) interface provide the functionality needed to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting different memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and support for high-speed SDR transfer modes. See section 36, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.9 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 28 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 38, 14-Bit A/D Converter (ADC14) in User's Manual.
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 39, 12-Bit D/A Converter (DAC12) in User's Manual.
8-bit D/A Converter (DAC8) for ACMPLP	The 8-bit D/A Converter (DAC8) converts data and does not include an output amplifier. The DAC8 is used only as the reference voltage for ACMPLP. See section 43, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 40, Temperature Sensor (TSN) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0, 1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 42, Low Power Analog Comparator (ACMPLP) in User's Manual.
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 41, Operational Amplifier (OPAMP) in User's Manual.

Table 1.10 Human machine interfaces

Feature	Functional description
Segment LCD Controller (SLCDC)	<p>The SLCDC provides the following functions:</p> <ul style="list-style-type: none"> • Waveform A or B selectable • The LCD driver voltage generator can switch between an internal voltage boosting method, a capacitor split method, and an external resistance division method • Automatic output of segment and common signals based on automatic display data register read • The reference voltage generated when operating the voltage boost circuit can be selected in 16 steps (contrast adjustment) • The LCD can be made to blink. <p>See section 48, Segment LCD Controller (SLCDC) in User's Manual.</p>
Capacitive Touch Sensing Unit (CTSU)	<p>The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode. See section 44, Capacitive Touch Sensing Unit (CTSU) in User's Manual.</p>

Table 1.11 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	<p>The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC generation polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 34, Cyclic Redundancy Check (CRC) Calculator in User's Manual.</p>
Data Operation Circuit (DOC)	<p>The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 45, Data Operation Circuit (DOC) in User's Manual.</p>

Table 1.12 Security

Feature	Functional description
Secure Crypto Engine 5 (SCE5)	<ul style="list-style-type: none"> • Security algorithm: <ul style="list-style-type: none"> - Symmetric algorithm: AES • Other support features: <ul style="list-style-type: none"> - TRNG (True Random Number Generator) - Hash-value generation: GHASH.

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset. Some individual devices within the group may have a subset of the features.

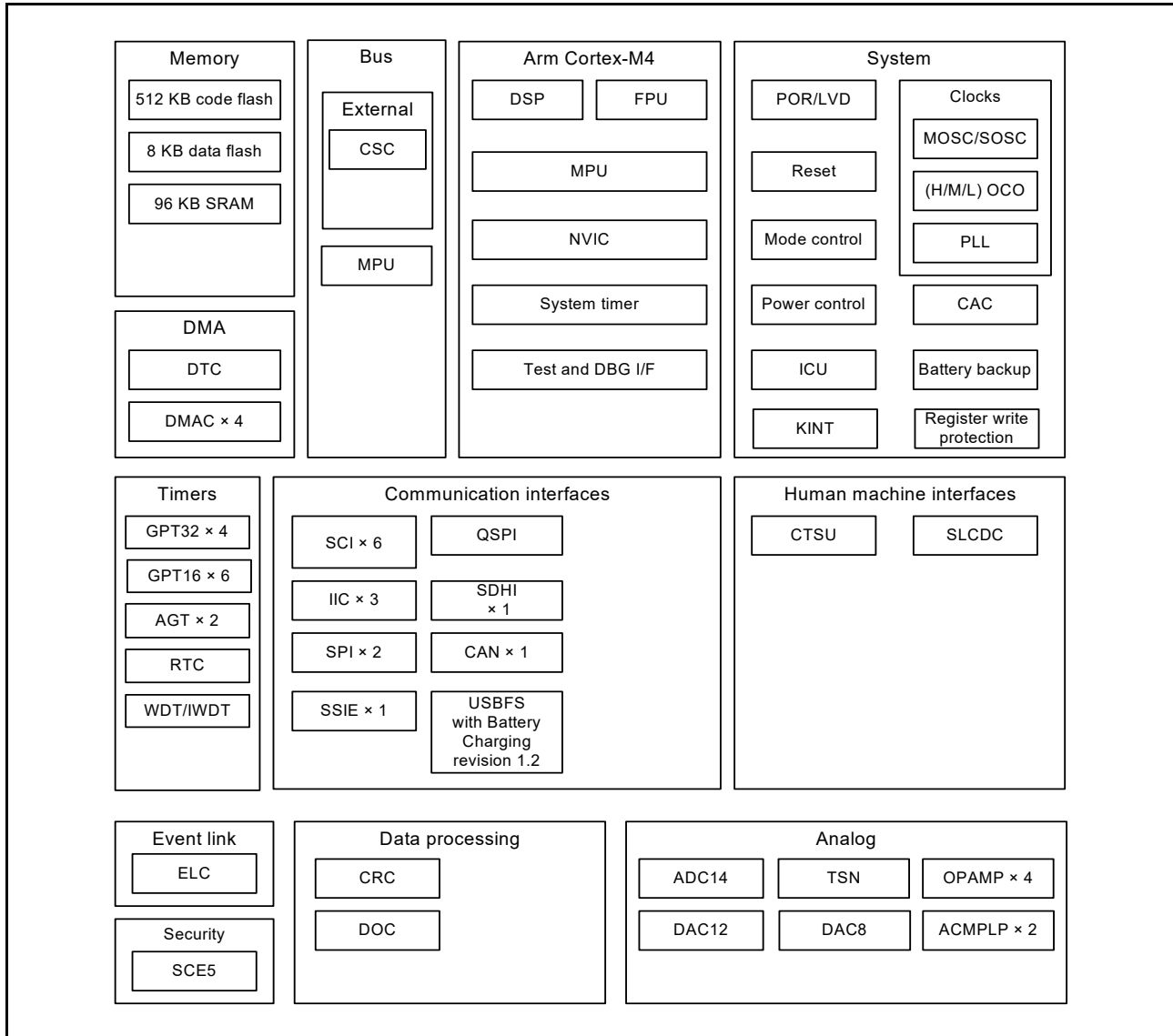


Figure 1.1 Block diagram

1.3 Part Numbering

Figure 1.2 shows how to read the product part number information, including memory capacity, and package type. Table 1.14 shows a product list.

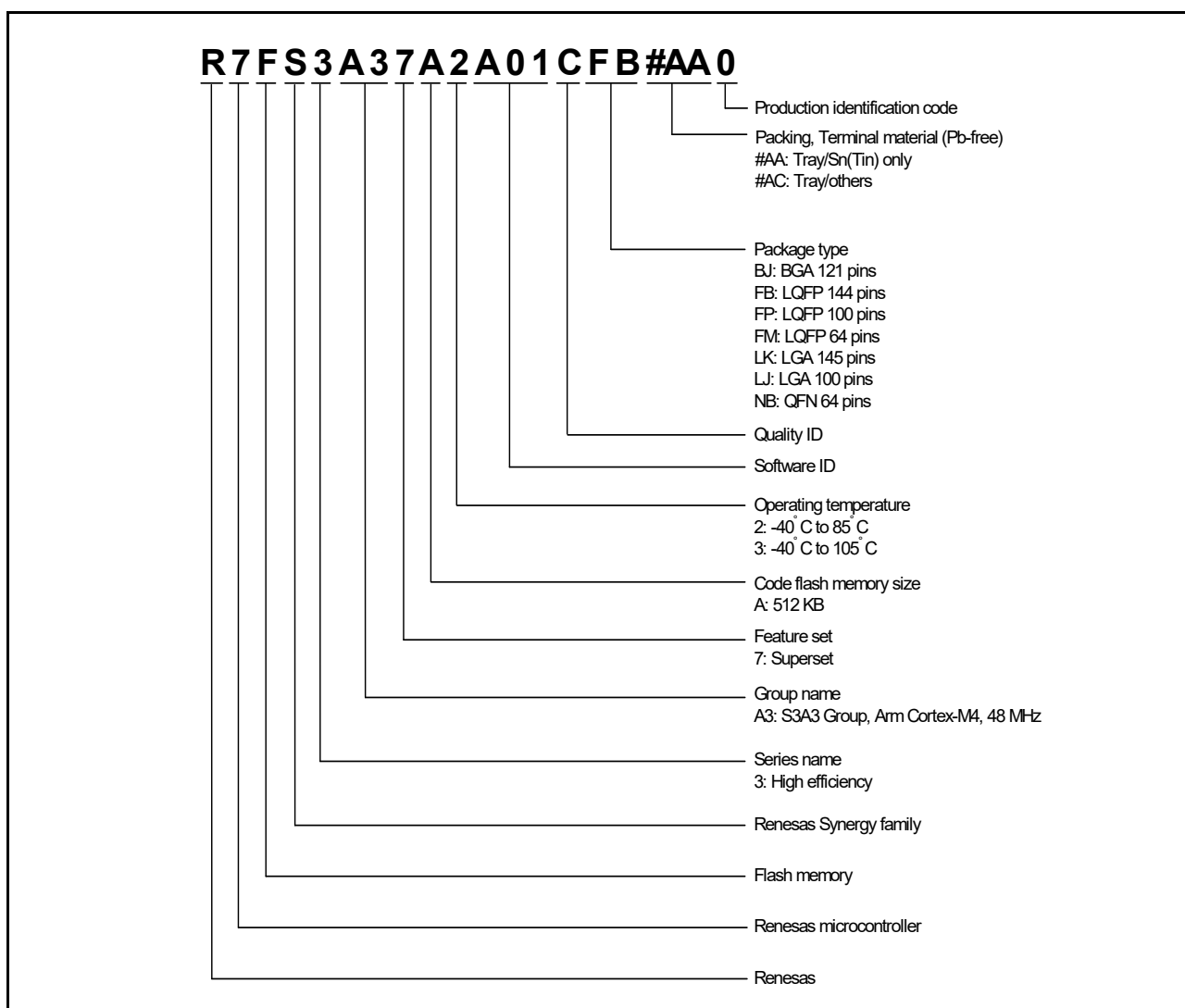


Figure 1.2 Part numbering scheme

Table 1.13 Product list

Product part number	Orderable part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FS3A37A2A01CLK	R7FS3A37A2A01CLK#AC0	PTLG0145KA-A	512 KB	8 KB	96 KB	-40 to +85°C
R7FS3A37A3A01CFB	R7FS3A37A3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS3A37A2A01CBJ	R7FS3A37A2A01CBJ#AC0	PLBG0121JA-A				-40 to +85°C
R7FS3A37A3A01CFP	R7FS3A37A3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FS3A37A2A01CLJ	R7FS3A37A2A01CLJ#AC0	PTLG0100JA-A				-40 to +85°C
R7FS3A37A3A01CFM	R7FS3A37A3A01CFM#AA0	PLQP0064KB-C				-40 to +105°C
R7FS3A37A3A01CNB	R7FS3A37A3A01CNB#AC0	PWQN0064LA-A				-40 to +105°C

1.4 Function Comparison

Table 1.14 Function comparison

Part numbers	R7FS3A37A2A01CLK	R7FS3A37A3A01CFB	R7FS3A37A2A01CBJ	R7FS3A37A3A01CFP	R7FS3A37A2A01CLJ	R7FS3A37A3A01CFM R7FS3A37A3A01CNB			
Pin count	145	144	121	100	100	64			
Package	LGA	LQFP	BGA	LQFP	LGA	LQFP/QFN			
Code flash memory	512 KB								
Data flash memory	8 KB								
SRAM	96 KB								
	Parity	80 KB							
	ECC	16 KB							
System	CPU clock	48 MHz							
	Backup registers	512 bytes							
	ICU	Yes							
	KINT	8							
Event control	ELC	Yes							
DMA	DTC	Yes							
	DMAC	4							
BUS	External bus	16-bit bus	8-bit bus			No			
Timers	GPT32	4							
	GPT16	6							
	AGT	2							
	RTC	Yes							
	WDT/IWDT	Yes							
Communication	SCI	6							
	IIC	3		2					
	SPI	2							
	SSIE	1					No		
	QSPI	1					No		
	SDHI	1					No		
	CAN	1							
	USBFS	Yes							
Analog	ADC14	28	26	25		18			
	DAC12	1							
	DAC8	2							
	ACMPLP	2							
	OPAMP	4	4	4	4	4	3		
	TSN	Yes							
HMI	SLCDC	4 com x 54 seg or 8 com x 50 seg		4 com x 46 seg or 8 com x 42 seg		4 com x 38 seg or 8 com x 34 seg		4 com x 21 seg or 8 com x 17 seg	
	CTSU	27					24		
Data processing	CRC	Yes							
	DOC	Yes							
Security	SCE5								

1.5 Pin Functions

Function	Signal	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply. Connect this pin to VSS by a 0.1- μ F capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to the VSS pin by the smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pins for setting the operating mode. The signal levels on these pins must not be changed during operation mode transition at the time of release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip debug	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	SWDIO	I/O	Serial Wire debug Data Input/Output pin
	SWCLK	Input	Serial Wire Clock pin
	SWO	Output	Serial Wire trace Output pin
External bus interface	RD	Output	Strobe signal which indicates that reading from the external bus interface space is in progress, active-low
	WR	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode, active-low
	WR0, WR1	Output	Strobe signals which indicate that either group of data bus pins (D07 to D00, D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active-low
	BC0, BC1	Output	Strobe signals which indicate that either group of data bus pins (D07 to D00, D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active-low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active-low
	CS0 to CS3	Output	Select signals for CS areas, active-low
	A00 to A23	Output	Address bus
	D00 to D15	I/O	Data bus
Battery backup	VBATWIO0 to VBATWIO2	I/O	Output wakeup signal for the VBATT wakeup control function. External event input for the VBATT wakeup control function.

Function	Signal	I/O	Description
GPT	GTETRG, GTETRGB	Input	External trigger input pin
	GTIOC0A to GTIOC9A, GTIOC0B to GTIOC9B	I/O	Input capture, Output capture, or PWM output pin
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOUWP	Output	3-phase PWM output for BLDC motor control (positive W phase)
GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)	
AGT	AGTEE0, AGTEE1	Input	External event input enable
	AGTIO0, AGTIO1	I/O	External event input and pulse output
	AGTO0, AGTO1	Output	Pulse output
	AGTOA0, AGTOA1	Output	Output compare match A output
	AGTOB0, AGTOB1	Output	Output compare match B output
RTC	RTCCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCCIC0 to RTCCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK4, SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD4, RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD4, TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS4_RTS4, CTS9_RTS9	I/O	Input/Output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active-low
	SCL0 to SCL4, SCL9	I/O	Input/output pins for the IIC clock (simple IIC)
	SDA0 to SDA4, SDA9	I/O	Input/output pins for the IIC data (simple IIC)
	SCK0 to SCK4, SCK9	I/O	Input/output pins for the clock (simple SPI)
	MISO0 to MISO4, MISO9	I/O	Input/output pins for slave transmission of data (simple SPI)
	MOSI0 to MOSI4, MOSI9	I/O	Input/output pins for master transmission of data (simple SPI)
SS0 to SS4, SS9	Input	Slave-select input pins (simple SPI), active-low	
IIC	SCL0 to SCL2	I/O	Input/output pins for clock
	SDA0 to SDA2	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pin
	SSILRCK0/SSIFS0	I/O	Word select pins
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Inputs or outputs data output from the master
	MISOA, MISOB	I/O	Inputs or outputs data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1, SSLA2, SSLA3, SSLB1, SSLB2, SSLB3	Output	Output pin for slave selection

Function	Signal	I/O	Description
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0	I/O	Master transmit data/data 0
	QIO1	I/O	Master input data/data 1
	QIO2, QIO3	I/O	Data 2, Data 3
CAN	CRX0	Input	Receive data
	CTX0	Output	Transmit data
USBFS	VSS_USB	Input	Ground pins
	VCC_USB_LDO	Input	Power supply pin for USB LDO regulator
	VCC_USB	I/O	Input: Power supply pin for USB transceiver. Output: USB LDO regulator output pin. This pin should be connected to an external capacitor.
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. This pin should be connected to the D+ pin of the USB bus.
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. This pin should be connected to the D- pin of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. This pin should be connected to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a device controller.
	USB_EXICEN	Output	Low power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	External overcurrent detection signals should be connected to these pins. VBUS comparator signals should be connected to these pins when the OTG power supply chip is connected.
	USB_ID	Input	MicroAB connector ID input signal should be connected to this pin during operation in OTG mode
SDHI	SD0CLK	Output	SD clock output pin
	SD0CMD	I/O	SD command output, response input signal pin
	SD0DAT0 to SD0DAT7	I/O	SD data bus pins
	SD0CD	Input	SD card detection pin
	SD0WP	Input	SD write-protect signal
Analog power supply	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	VREFH	Input	Analog reference voltage supply pin for D/A converter
	VREFL	Input	Analog reference ground pin for D/A converter
ADC14	AN000 to AN027	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion, active-low
DAC12	DA0	Output	Output pins for the analog signals to be processed by the D/A converter
Comparator output	VCOUT	Output	Comparator output pin
ACMPLP	CMPREF0, CMPREF1	Input	Reference voltage input pins
	CMPIN0, CMPIN1	Input	Analog voltage input pins
OPAMP	AMP0+ to AMP3+	Input	Analog voltage input pins
	AMP0- to AMP3-	Input	Analog voltage input pins
	AMP00 to AMP30	Output	Analog voltage output pins
CTSU	TS00 to TS13, TS17 to TS22, TS27 to TS31, TS34, TS35	Input	Capacitive touch detection pins (touch pins)
	TSCAP	—	Secondary power supply pin for the touch driver

Function	Signal	I/O	Description
I/O ports	P000 to P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P206, P212, P213	I/O	General-purpose input/output pins
	P214, P215	Input	General-purpose input pins
	P300 to P315	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P507, P511, P512	I/O	General-purpose input/output pins
	P600 to P606, P608 to P614	I/O	General-purpose input/output pins
	P700 to P705, P708 to P713	I/O	General-purpose input/output pins
	P800 to P809	I/O	General-purpose input/output pins
	P900 to P902, P914, P915	I/O	General-purpose input/output pins
	SLCDC	VL1, VL2, VL3, VL4	I/O
CAPH, CAPL		I/O	Capacitor connection pin for the LCD controller/driver
COM0 to COM7		Output	Common signal output pins for the LCD controller/driver
SEG00 to SEG53		Output	Segment signal output pins for the LCD controller/driver

1.6 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments.

R7FS3A37A2A01CLK															
	A	B	C	D	E	F	G	H	J	K	L	M	N		
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	P215 /XCIN	VCL	P702	P405	P402	P400	13	
12	P915/ USB_DM	P914/ USB_DP	P410	P414	P710	VSS	P213 /XTAL	P214 /XCOUT	VBATT	P701	P404	P511	VCC	12	
11	VCC_ USB	VSS_ USB	VCC_ USB_LDO	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11	
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10	
9	P203	P313	P202	P314						P004	P006	P009	P008	9	
8	P900	P901	P200	P315						P005	AVSS0	P011 /VREFLO	P010 /VREFH0	8	
7	VSS	P902	RES	P310						P007	AVCC0	P013 /VREFL	P012 /VREFH	7	
6	VCC	P201/MD	P312	P305						P505	P506	P015	P014	6	
5	P309	P311	P308	P303	NC						P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO /SWO	P114	P608	P604	P600	P105	P500	P502	P501	P507	4	
3	P808	P809	P301	P112	P115	P610	P614	P603	P107	P106	P104	P803	P802	3	
2	P302	P300/TCK /SWCLK	P111	P806	P609	P612	VSS	P605	P601	P805	P800	P101	P801	2	
1	P108/TMS /SWDIO	P110/TDI	P113	P807	P611	P613	VCC	P606	P602	P804	P103	P102	P100	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N		

Figure 1.3 Pin assignment for LGA 145-pin (top view)

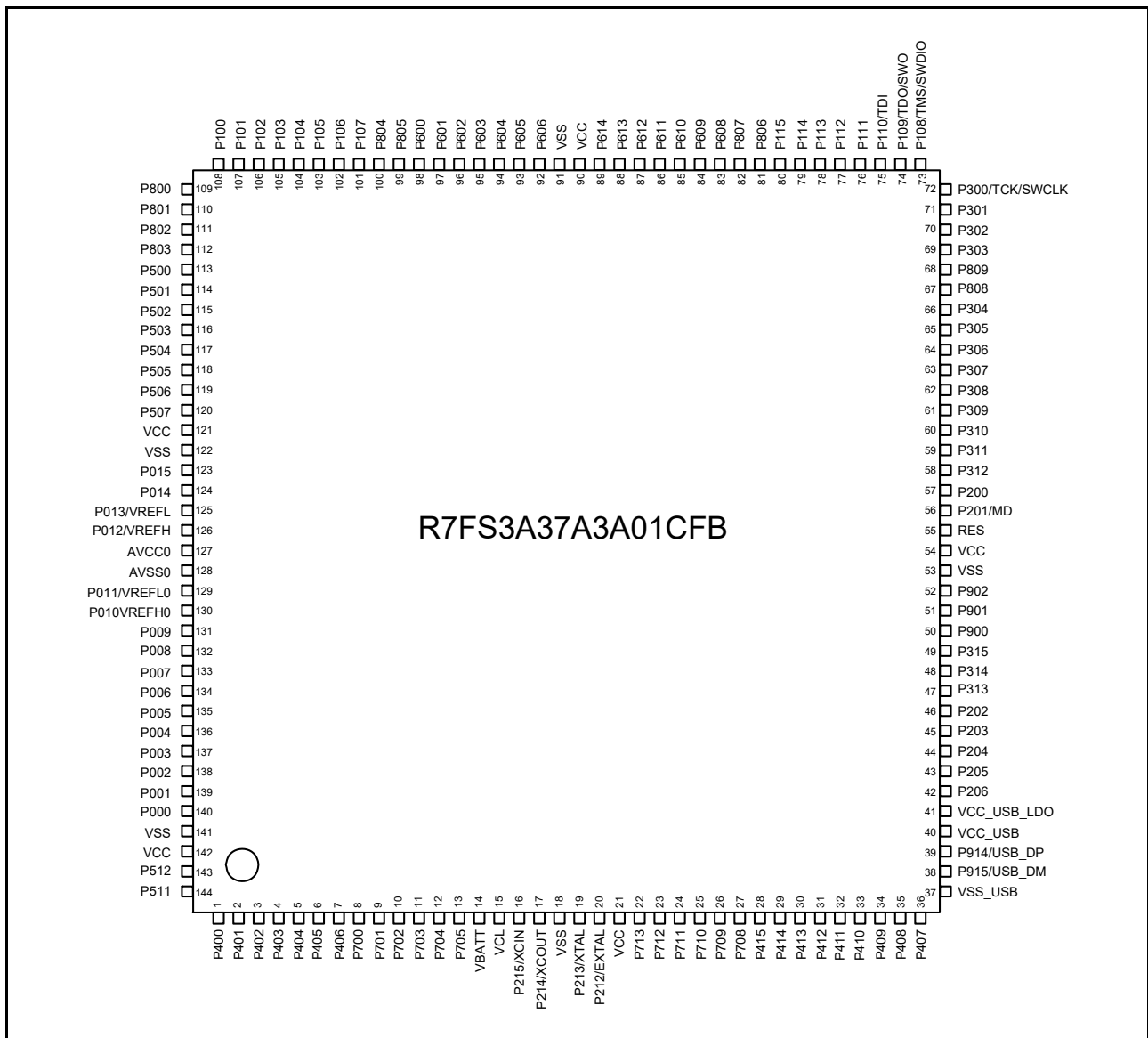


Figure 1.4 Pin assignment for LQFP 144-pin (top view)

R7FS3A37A2A01CBJ

	A	B	C	D	E	F	G	H	J	K	L	
11	P407	P408	P411	P414	P212/ EXTAL	P215/ XCIN	VCL	P406	P403	P401	P400	11
10	P915/ USB_DM	P914/ USB_DP	P410	P415	P213/ XTAL	P214/ XCOUT	VBATT	P405	P402	P511	P512	10
9	VCC_ USB	VSS_ USB	P409	P412	P708	VCC	VSS	P404	P002	P001	P000	9
8	P205	VCC_ USB_ LDO	P206	P204	P413	P710	P702	P006	P004	P003	P005	8
7	P203	P202	P313	P314	P315	P709	P701	P007	AVSS0	P011/ VREFL0	P010/ VREFH0	7
6	VSS	VCC	RES	P201/MD	P200	NC	P700	P008	AVCC0	P013/ VREFL	P012/ VREFH	6
5	P308	P309	P307	P302	P304	P612	P601	P506	P505	P015	P014	5
4	P305	P306	P808	P114	P611	P603	P600	P504	P503	VSS	VCC	4
3	P809	P303	P110/TDI	P111	P609	P604	P106	P104	P502	P500	P501	3
2	P301	P108/ TMS/ SWDIO	P113	P608	P613	P605	P602	P105	P102	P801	P800	2
1	P300/ TCK/ SWCLK	P109/ TDO/ SWO	P112	P115	P610	VCC	VSS	P107	P103	P101	P100	1
	A	B	C	D	E	F	G	H	J	K	L	

Figure 1.5 Pin assignment for BGA 121-pin (top view)

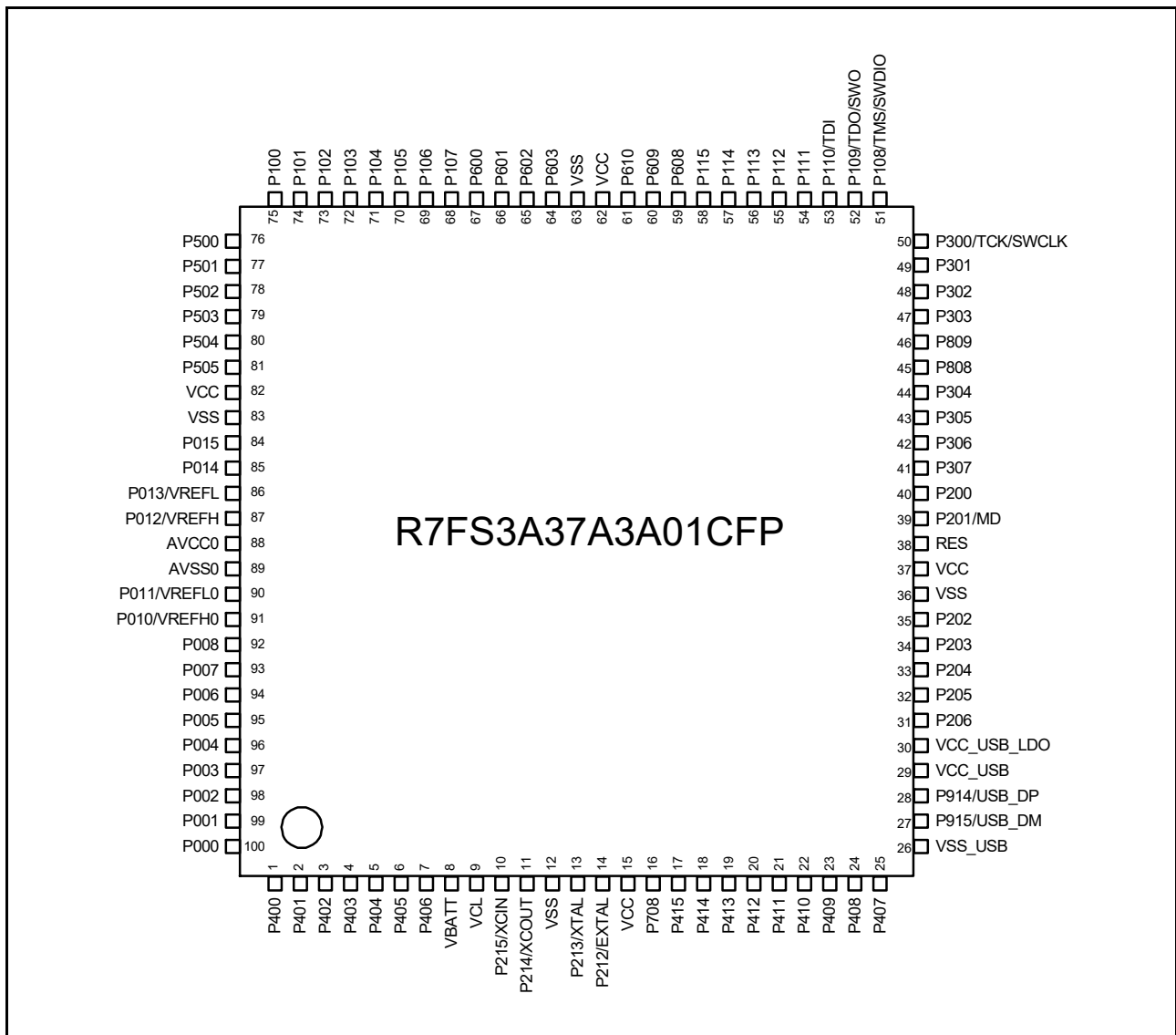


Figure 1.6 Pin assignment for LQFP 100-pin (top view)

R7FS3A37A2A01CLJ

	A	B	C	D	E	F	G	H	J	K	
10	P407	P409	P412	VCC	P212/ EXTAL	P215/ XCIN	VCL	P403	P400	P000	10
9	P915/ USB_DM	P914/ USB_DP	P413	VSS	P213/ XTAL	P214/ XCOUT	VBATT	P405	P401	P001	9
8	VCC_ USB	VSS_ USB	VCC_US B_LDO	P411	P415	P708	P404	P003	P004	P002	8
7	P205	P204	P206	P408	P414	P406	P006	P007	P008	P005	7
6	VSS	VCC	P202	P203	P410	P402	P505	AVSS0	P011/ VREFL0	P010/ VREFH0	6
5	P200	P201/MD	P307	RES	P113	P600	P504	AVCC0	P013/ VREFL	P012/ VREFH	5
4	P305	P304	P808	P306	P115	P601	P503	P100	P015	P014	4
3	P809	P303	P110/TDI	P111	P609	P602	P107	P103	VSS	VCC	3
2	P300/ TCK/ SWCLK	P302	P301	P114	P610	P603	P106	P101	P501	P502	2
1	P108/ TMS/ SWDIO	P109/ TDO/ SWO	P112	P608	VCC	VSS	P105	P104	P102	P500	1
	A	B	C	D	E	F	G	H	J	K	

Figure 1.7 Pin assignment for LGA 100-pin (top view)

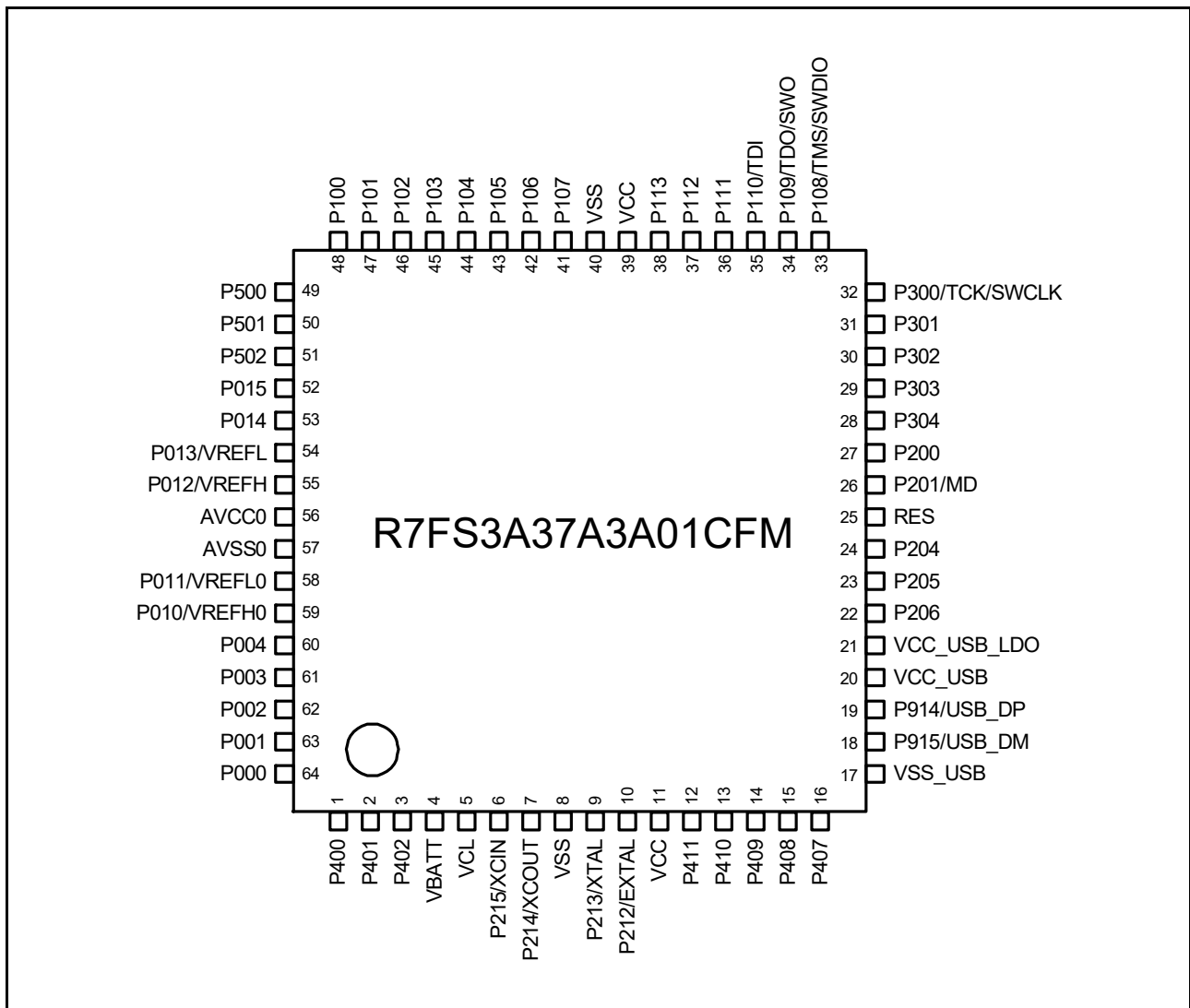


Figure 1.8 Pin assignment for LQFP 64-pin (top view)

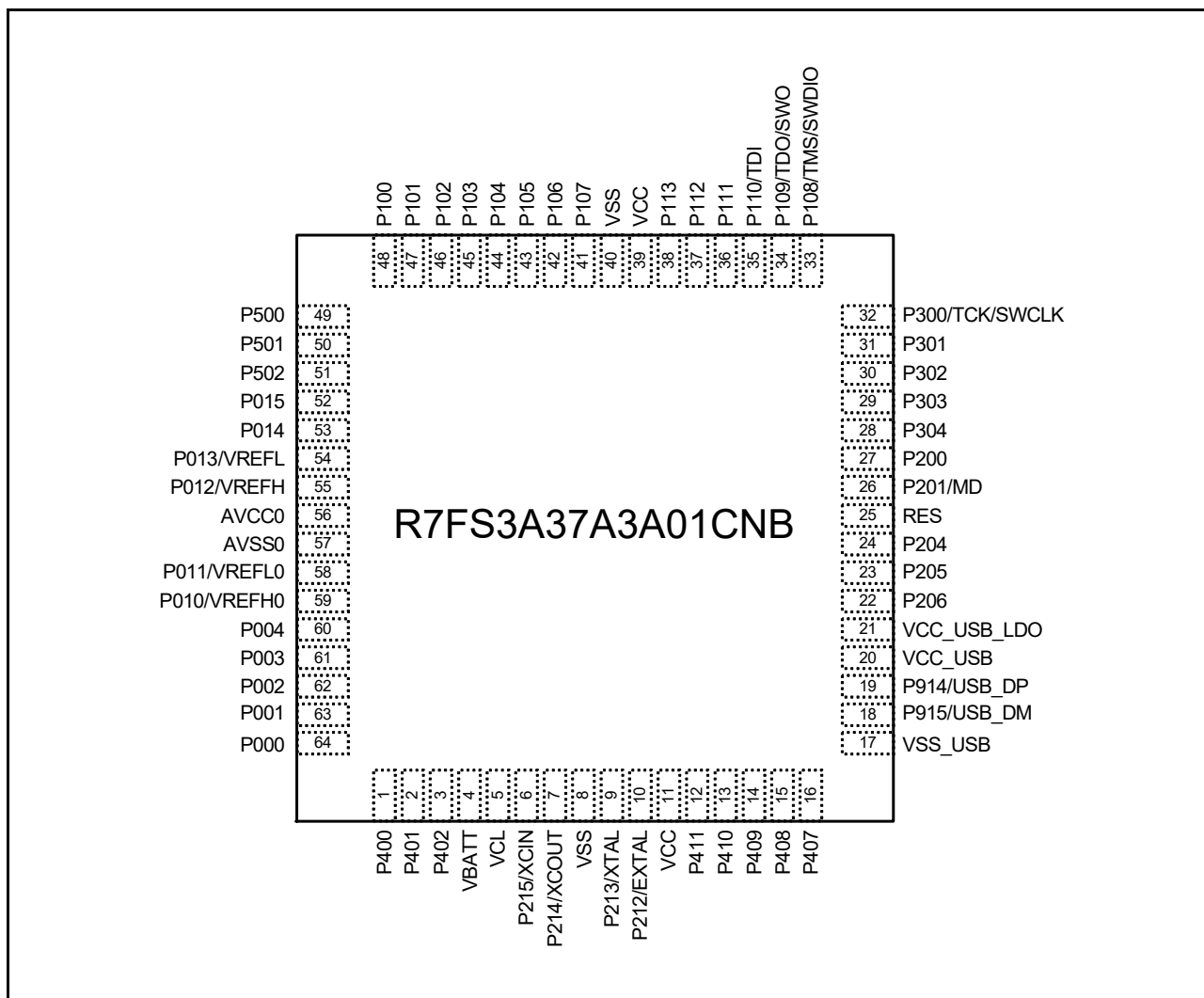


Figure 1.9 Pin assignment for QFN 64-pin (top view)

1.7 Pin Lists

Pin number	Pin name						Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	Timers				Communication interfaces				Analog			HMI		
	LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64					QFN64	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP
N13	1	L11	1	J10	1	1	CACREF	IRQ0	P400		AGTIO1		GTIOC6A			SCK1 SCK4	SCL0		AUDIO_CLK				SEG4	TS20
L11	2	K11	2	J9	2	2		IRQ5	P401			GTET RGA	GTIOC 6B		CTX0	TXD1/ MOS11 /SDA1 CTS4_ RTS4/ SS4	SDA0						SEG5	TS19
M13	3	J10	3	F6	3	3	VBAT WIO0	IRQ4	P402		AGTIO 0/ AGTIO 1			RTCIC 0	CRX0	RXD1/ MISO1 /SCL1							SEG6	TS18
K11	4	J11	4	H10			VBAT WIO1		P403		AGTIO 0/ AGTIO 1		GTIOC 3A	RTCIC 1		CTS1_ RTS1/ SS1		SSIBC K0						TS17
L12	5	H9	5	G8			VBAT WIO2		P404				GTIOC 3B	RTCIC 2				SSLR CK0/ SSIFS 0						
L13	6	H10	6	H9					P405				GTIOC 1A					SSITX D0						
J10	7	H11	7	F7					P406				GTIOC 1B				SSLA3	SSIRX D0						
H10	8	G6							P700				GTIOC 5A				MISOA							
K12	9	G7							P701				GTIOC 5B				MOSIA							
K13	10	G8							P702				GTIOC 6A				RSPC KA							
J11	11								P703				GTIOC 6B				SSLA0					VCOU T		
H11	12								P704		AGTIO 0						SSLA1							
G11	13								P705		AGTIO 0						SSLA2							
J12	14	G10	8	G9	4	4	VBATT																	
J13	15	G11	9	G10	5	5	VCL																	
H13	16	F11	10	F10	6	6	XCIN		P215															
H12	17	F10	11	F9	7	7	XCOU T		P214															
F12	18	G9	12	D9	8	8	VSS																	
G12	19	E10	13	E9	9	9	XTAL	IRQ2	P213			GTET RGA	GTIOC 0A			TXD1/ MOS11 /SDA1								
G13	20	E11	14	E10	10	10	EXTAL	IRQ3	P212		AGTE E1	GTET RGB	GTIOC 0B			RXD1/ MISO1 /SCL1								
F13	21	F9	15	D10	11	11	VCC																	
G10	22								P713		AGTIO A0		GTIOC 2A											
F11	23								P712		AGTIO B0		GTIOC 2B											
E13	24								P711		AGTE E0					CTS1_ RTS1/ SS1								
E12	25	F8							P710	A17						SCK1								
F10	26	F7						IRQ10	P709							TXD1/ MOS11 /SDA1								
D13	27	E9	16	F8				IRQ11	P708							RXD1/ MISO1 /SCL1	SSLA3							
E11	28	D10	17	E8				IRQ8	P415				GTIOC 0A				SSLA2	SDOC D						
D12	29	D11	18	E7				IRQ9	P414				GTIOC 0B				SSLA1	SDOW P						
E10	30	E8	19	C9					P413		GTOU UP					CTS0_ RTS0/ SS0	SSLA0	SDOCL K						
C13	31	D9	20	C10					P412		GTOU LO					SCK0	RSPC KA	SDOC MD						

Pin number	Pin						Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	Timers				Communication interfaces					Analog			HMI		
	LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64					QFN64	AGT	GPT_OPS, POEG	GPT	RTC	USBF,S,CAN	SCI	IIC	SP/CSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP	SLCDC
D11	32	C11	21	D8	12	12		IRQ4	P411		AGT A1	GTOV UP	GTIOC 9A			TXD0/ MOSIO /SDA0 CTS3 RTS3/ SS3		MOSIA		SD0D AT0				SEG7	TS7
C12	33	C10	22	E6	13	13		IRQ5	P410		AGT B1	GTOV LO	GTIOC 9B			SCK3 RXD0/ MISO0 /SCL0		MISOA		SD0D AT1				SEG8	TS6
B13	34	C9	23	B10	14	14		IRQ6	P409			GTOV UP	GTIOC 5A		USB E XICEN	TXD3/ MOSI3 /SDA3								SEG9	TS5
D10	35	B11	24	D7	15	15		IRQ7	P408			GTOV LO	GTIOC 5B		USB_I D	CTS1 RTS1/ SS1 RXD3/ MISO3 /SCL3		SCL0						SEG10	TS4
A13	36	A11	25	A10	16	16			P407		AGTIO 0			RTCO UT	USB_V BUS	CTS4 RTS4/ SS4		SDA0	SSLB3		ADTR G0			SEG11	TS3
B11	37	B9	26	B8	17	17	VSS_ U SB																		
A12	38	A10	27	A9	18	18			P915						USB_ DM										
B12	39	B10	28	B9	19	19			P914						USB_ DP										
A11	40	A9	29	A8	20	20	VCC_ USB																		
C11	41	B8	30	C8	21	21	VCC_ USB_ L DO																		
B10	42	C8	31	C7	22	22		IRQ0	P206	WAIT		GTIU			USB_V BUSE N	RXD4/ MISO4 /SCL4		SDA1	SSLB1		SD0D AT2			SEG12	TS1
A10	43	A8	32	A7	23	23	CLKO UT	IRQ1	P205	A16	AGTIO 1	GTIV	GTIOC 4A		USB_ OVRC URA	TXD4/ MOSI4 /SDA4 CTS9_ RTS9/ SS9		SCL1	SSLB0		SD0D AT3			SEG20	TSCA P
C10	44	D8	33	B7	24	24	CACR EF		P204	A18	AGTIO 1	GTIW	GTIOC 4B		USB_ OVRC URB	SCK4 SCK9		SCL0	RSPC KB		SD0D AT4			SEG23	TS0
A9	45	A7	34	D6				IRQ2	P203	A19			GTIOC 5A			CTS2_ RTS2/ SS2 TXD9/ MOSI9 /SDA9			MOSIB		SD0D AT5			SEG22	TSCA P
C9	46	B7	35	C6				IRQ3	P202	WR1/ BC1			GTIOC 5B			SCK2 RXD9/ MISO9 /SCL9			MISOB		SD0D AT6			SEG21	
B9	47	C7							P313	A20											SD0D AT7				
D9	48	D7							P314	A21												ADTR G0			
D8	49	E7							P315	A22						RXD4/ MISO4 /SCL4									
A8	50								P900	A23						TXD4/ MOSI4 /SDA4									
B8	51								P901		AGTIO 1					SCK4									
B7	52								P902		AGTIO 1					CTS4_ RTS4/ SS4									
A7	53	A6	36	A6			VSS																		
A6	54	B6	37	B6			VCC																		
C7	55	C6	38	D5	25	25	RES																		
B6	56	D6	39	B5	26	26	MD		P201																

Pin number													Timers				Communication interfaces					Analog			HMI				
		LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU		
C8	57	E6	40	A5	27	27			NMI	P200																			
C6	58									P312	CS3	AGTO A1																	
B5	59									P311	CS2	AGTO B1																	
D7	60									P310	A15	AGTE E1																	
A5	61	B5								P309	A14																		
C5	62	A5								P308	A13																SEG13		
A4	63	C5	41	C5						P307	A12																SEG14		
B4	64	B4	42	D4						P306	A11																SEG15		
D6	65	A4	43	A4					IRQ8	P305	A10																SEG16		
C4	66	E5	44	B4	28	28			IRQ9	P304	A09			GTIOC 7A													SEG17	TS11	
A3	67	C4	45	C4						P808																	SEG18		
B3	68	A3	46	A3						P809																	SEG19		
D5	69	B3	47	B3	29	29				P303	A08			GTIOC 7B													SEG3/COM7	TS2	
A2	70	D5	48	B2	30	30			IRQ5	P302	A07		GTOU UP	GTIOC 4A													SEG2/COM6	TS8	
C3	71	A2	49	C2	31	31			IRQ6	P301	A06	AGTIO 0	GTOU LO	GTIOC 4B													SEG1/COM5	TS9	
B2	72	A1	50	A2	32	32		TCK/SWCLK		P300			GTOU UP	GTIOC 0A															
A1	73	B2	51	A1	33	33		TMS/SWDIO		P108			GTOU LO	GTIOC 0B															
D4	74	B1	52	B1	34	34		TDO/SWO/CLKOUT		P109			GTOU UP	GTIOC 1A		CTX0	SCK1 TXD9/MOSI9/SDA9											SEG52	TS10
B1	75	C3	53	C3	35	35		TDI	IRQ3	P110			GTOV LO	GTIOC 1B		CRX0	CTS2 RTS2/SS2 RXD9/MISO9/SCL9								VCOU T		SEG53		
C2	76	D3	54	D3	36	36			IRQ4	P111	A05			GTIOC 3A													CAPH	TS12	
D3	77	C1	55	C1	37	37				P112	A04			GTIOC 3B													CAPL	TSCP	
C1	78	C2	56	E5	38	38				P113	A03			GTIOC 2A													SEG0/COM4	TS27	
E4	79	D4	57	D2						P114	A02			GTIOC 2B													SEG24	TS29	
E3	80	D1	58	E4						P115	A01			GTIOC 4A													SEG25	TS35	
D2	81									P806																	SEG26		
D1	82									P807																	SEG27		
F4	83	D2	59	D1						P608	A00/BC0			GTIOC 4B													SEG28		
E2	84	E3	60	E3						P609	CS1			GTIOC 5A													SEG29		

Pin number								Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	Timers				Communication interfaces						Analog			HMI	
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64						AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
F3	85	E1	61	E2					P610	CS0			GTIOC 5B								SD0D AT3				SEG30	
E1	86	E4							P611																SEG31	
F2	87	F5							P612	D08															SEG32	
F1	88	E2							P613	D09															SEG33	
G3	89								P614	D10															SEG34	
G1	90	F1	62	E1	39	39	VCC																			
G2	91	G1	63	F1	40	40	VSS																			
H1	92								P606						RTCO UT										SEG35	
H2	93	F2							P605	D11			GTIOC 8A												SEG36	
G4	94	F3							P604	D12			GTIOC 8B												SEG37	
H3	95	F4	64	F2					P603	D13			GTIOC 7A			CTS9_RTS9/SS9					SD0D AT4				SEG38	
J1	96	G2	65	F3					P602	EBCLK			GTIOC 7B			TXD9/MOSI9/SDA9					SD0D AT5				SEG39	
J2	97	G5	66	F4					P601	WR/WR0			GTIOC 6A			RXD9/MISO9/SCL9					SD0D AT6				SEG40	
H4	98	G4	67	F5					P600	RD			GTIOC 6B			SCK9					SD0D AT7				SEG41	
K2	99								P805				GTIOC 9A												SEG42	
K1	100								P804				GTIOC 9B												SEG43	
J3	101	H1	68	G3	41	41		KR07	P107	D07			GTIOC 8A												COM3	
K3	102	G3	69	G2	42	42		KR06	P106	D06			GTIOC 8B					SSLA3							COM2	
J4	103	H2	70	G1	43	43		KR05/IRQ0	P105	D05		GTET RGA	GTIOC 1A					SSLA2							COM1	TS34
L3	104	H3	71	H1	44	44		KR04/IRQ1	P104	D04		GTET RGB	GTIOC 1B			RXD0/MISO0/SCL0		SSLA1							COM0	TS13
L1	105	J1	72	H3	45	45		KR03	P103	D03		GTOW UP	GTIOC 2A		CTX0	CTS0_RTS0/SS0		SSLA0				AN019		CMPEF1	VL4	
M1	106	J2	73	J1	46	46		KR02	P102	D02	AGT0	GTOW LO	GTIOC 2B		CRX0	SCK0 TXD2/MOSI2/SDA2		RSPCKA				AN020/ADTRG0		CMPI1	VL3	
M2	107	K1	74	H2	47	47		KR01/IRQ1	P101	D01	AGTE0	GTET RGB	GTIOC 5A			TXD0/MOSI0/SDA0 CTS1_RTS1/SS1	SDA1	MOSIA				AN021		CMPEF0	VL2	
N1	108	L1	75	H4	48	48		KR00/IRQ2	P100	D00	AGTIO0	GTET RGA	GTIOC 5B			RXD0/MISO0/SCL0 SCK1	SCL1	MISOA				AN022		CMPI0	VL1	
L2	109	L2							P800	D14															SEG44	
N2	110	K2							P801	D15															SEG45	
N3	111								P802																SEG46	
M3	112								P803																SEG47	
K4	113	K3	76	K1	49	49			P500		AGT0A0	GTIU	GTIOC 2A			USB_V BUSE N			QSPCLK						SEG48	CMPEF1
M4	114	L3	77	J2	50	50			P501		AGT0B0	GTIV	GTIOC 2B			USB_OVRC URA	TXD3/MOSI3/SDA3		QSSL						SEG49	CMPI1
L4	115	J3	78	K2	51	51			P502			GTIW	GTIOC 3B			USB_OVRC URB	RXD3/MISO3/SCL3		QIO0						SEG50	CMPEF0

Pin number	Pin package										Timers				Communication interfaces					Analog			HMI				
	LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	AGT	GPT_OPS, POEG	GPT	RTC	USB_E XICEN	CTS2 RTS2/ SS2 SCK3	SCI	IIC	SP/CSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
K5	116	J4	79	G4					P503			GTET RGA			USB_1 D				QIO1			AN023		CMPIN 0	SEG51		
L5	117	H4	80	G5					P504	ALE		GTET RGB			USB_1 D				QIO2			AN024					
K6	118	J5	81	G6				IRQ14	P505										QIO3			AN025					
L6	119	H5						IRQ15	P506													AN026					
N4	120								P507													AN027					
N5	121	L4	82	K3			VCC																				
M5	122	K4	83	J3			VSS																				
M6	123	K5	84	J4	52	52		IRQ7	P015													AN010				TS28	
N6	124	L5	85	K4	53	53			P014													AN009	DA0				
M7	125	K6	86	J5	54	54	VREFL		P013													AN008	AMP1+				
N7	126	L6	87	K5	55	55	VREFH		P012													AN007	AMP1-				
L7	127	J6	88	H5	56	56	AVCC0																				
L8	128	J7	89	H6	57	57	AVSS0																				
M8	129	K7	90	J6	58	58	VREFL0	IRQ15	P011													AN006	AMP2+			TS31	
N8	130	L7	91	K6	59	59	VREFH0	IRQ14	P010													AN005	AMP2-			TS30	
M9	131							IRQ13	P009													AN015					
N9	132	H6	92	J7				IRQ12	P008													AN014					
K7	133	H7	93	H7					P007													AN013	AMP3 O				
L9	134	H8	94	G7				IRQ11	P006													AN012	AMP3-				
K8	135	L8	95	K7				IRQ10	P005													AN011	AMP3+				
K9	136	J8	96	J8	60	60		IRQ3	P004													AN004	AMP2 O				
K10	137	K8	97	H8	61	61			P003													AN003	AMP1 O				
M10	138	J9	98	K8	62	62		IRQ2	P002													AN002	AMP0 O				
N10	139	K9	99	K9	63	63		IRQ7	P001													AN001	AMP0-			TS22	
L10	140	L9	100	K10	64	64		IRQ6	P000													AN000	AMP0+			TS21	
N11	141						VSS																				
N12	142						VCC																				
M11	143	L10						IRQ14	P512			GTIOC 0A			CTX0	TXD4/ MOS14 /SDA4	SCL2										
M12	144	K10						IRQ15	P511			GTIOC 0B			CRX0	RXD4/ MISO4 /SCL4	SDA2										
E5		F6					NC																				

2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

$VCC^{*1} = AVCC0 = VCC_USB^{*2} = VCC_USB_LDO^{*2} = 1.6$ to $5.5V$, $V_{RERH} = V_{REFH0} = 1.6$ to $AVCC0$, $V_{BATT} = 1.6$ to $3.6V$, $V_{SS} = AVSS0 = V_{REFL} = \bar{V}_{REFL0} = V_{SS_USB} = 0V$, $T_a = T_{opr}$

Note 1. The typical condition is set to $VCC = 3.3V$.

Note 2. When USBFS is not used.

Figure 2.1 shows the timing conditions.

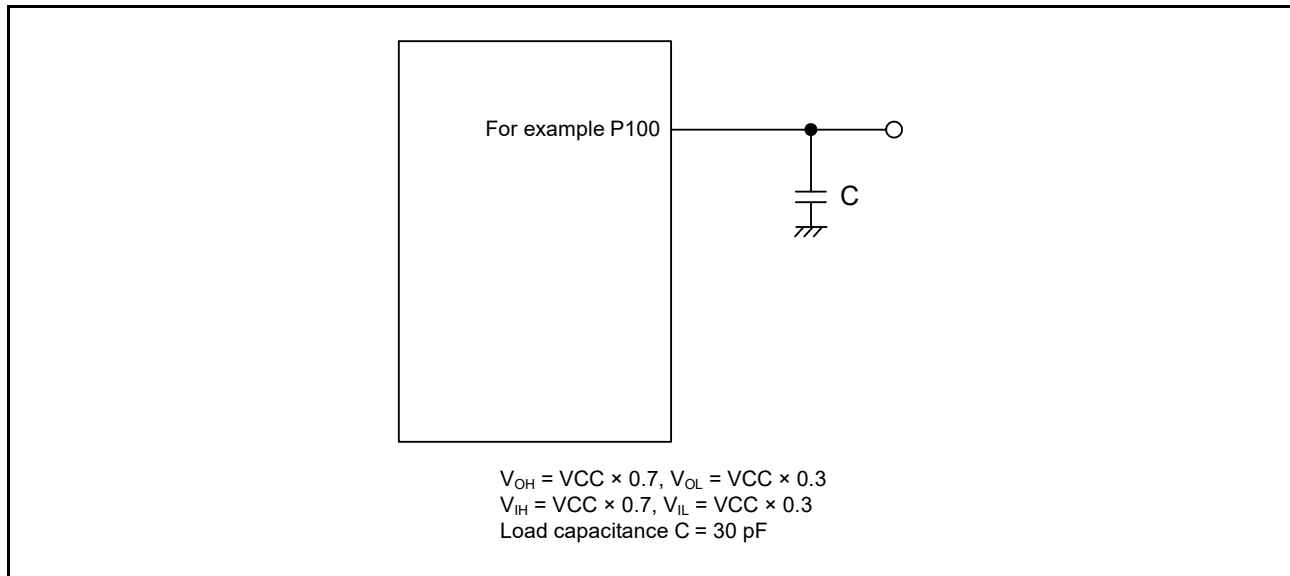


Figure 2.1 Input or output timing measurement conditions

The measurement conditions of timing specifications in each peripheral are recommended for the best peripheral operation. However, make sure to adjust driving abilities of each pin to meet your conditions.

Each function pin used for the same function must select the same drive ability. If the I/O drive ability of each function pin is mixed, the AC specification of each function is not guaranteed.

2.1 Absolute Maximum Ratings

Table 2.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC	-0.5 to +6.5	V
Input voltage	5V-tolerant ports*1	V_{in}	-0.3 to +6.5
	P000 to P015	V_{in}	-0.3 to AVCC0 + 0.3
	Others	V_{in}	-0.3 to VCC + 0.3
Reference power supply voltage	VREFH0	-0.3 to +6.5	V
	VREFH		V
VBATT power supply voltage	VBATT	-0.5 to +6.5	V
Analog power supply voltage	AVCC0	-0.5 to +6.5	V
USB power supply voltage	VCC_USB	-0.5 to +6.5	V
	VCC_USB_LDO	-0.5 to +6.5	V
Analog input voltage	When AN000 to AN015 are used	V_{AN}	-0.3 to AVCC0 + 0.3
	When AN016 to AN027 are used		-0.3 to VCC + 0.3
LCD voltage	VL1 voltage	V_{L1}	-0.3 to +2.8
	VL2 voltage	V_{L2}	-0.3 to +6.5
	VL3 voltage	V_{L3}	-0.3 to +6.5
	VL4 voltage	V_{L4}	-0.3 to +6.5
Operating temperature*2,*3,*4	T_{opr}	-40 to +105	°C
		-40 to +85	
Storage temperature	T_{stg}	-55 to +125	°C

Note 1. Ports P205, P206, P400 to P404, P407, P408, P511, P512 are 5V-tolerant.

Note 2. See [section 2.2.1, Tj/Ta Definition](#).

Note 3. Contact Renesas Electronics sales office for information on derating operation under $T_a = +85^{\circ}\text{C}$ to $+105^{\circ}\text{C}$. Derating is the systematic reduction of load for improved reliability.

Note 4. The upper limit of operating temperature is 85°C or 105°C , depending on the product. For details, see [section 1.3, Part Numbering](#).

Caution: Permanent damage to the MCU may result if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors of high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, and between the VREFH and VREFL pins. Place capacitors of about 0.1 μF as close as possible to every power supply pin and use the shortest and heaviest possible traces. Also, connect capacitors as stabilization capacitance.

Connect the VCL pin to a VSS pin by a 4.7 μF capacitor. The capacitor must be placed close to the pin.

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up might cause malfunction and the abnormal current that passes in the device at this time might cause degradation of internal elements.

Table 2.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC*1, *2	When USBFS is not used	1.6	-	5.5	V
		When USBFS is used USB Regulator Disable	VCC_USB	-	3.6	V
		When USBFS is used USB Regulator Enable	VCC_USB _LDO	-	5.5	V
	VSS	-	0	-	V	
USB power supply voltages	VCC_USB	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable (Input)	3.0	3.3	3.6	V
	VCC_USB_LDO	When USBFS is not used	-	VCC	-	V
		When USBFS is used USB Regulator Disable	-	VCC	-	V
		When USBFS is used USB Regulator Enable	3.8	-	5.5	V
	VSS_USB	-	0	-	V	
VBATT power supply voltage	VBATT	When the battery backup function is not used	-	VCC	-	V
		When the battery backup function is used	1.6	-	3.6	V
Analog power supply voltages	AVCC0*1, *2		1.6	-	5.5	V
	AVSS0		-	0	-	V
	VREFH0	When used as ADC14 Reference	1.6	-	AVCC0	V
	VREFL0		-	0	-	V
	VREFH	When used as DAC12 Reference	1.6	-	AVCC0	V
	VREFL		-	0	-	V

Note 1. Use AVCC0 and VCC under the following conditions:

AVCC0 and VCC can be set individually within the operating range when $VCC \geq 2.2\text{ V}$ and $AVCC0 \geq 2.2\text{ V}$

$AVCC0 = VCC$ when $VCC < 2.2\text{ V}$ or $AVCC0 < 2.2\text{ V}$

Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.

2.2 DC Characteristics

2.2.1 T_j/T_a Definition

Table 2.3 DC characteristics

Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T _j	-	125	°C	High-speed mode Middle-speed mode Low-voltage mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta_{ja} \times \text{total power consumption (W)}$, where total power consumption = $(V_{CC} - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CCmax} \times V_{CC}$.

Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see [section 1.3, Part Numbering](#). If the part number shows the operation temperature at 85°C, then the maximum value of T_j is 105°C, otherwise, it is 125°C.

2.2.2 I/O V_{IH}, V_{IL}

Table 2.4 I/O V_{IH}, V_{IL} (1)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LDO = 2.7 to 5.5V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Schmitt trigger input voltage	IIC*1 (except for SMBus)	V _{IH}	VCC × 0.7	-	5.8	V	-
		V _{IL}	-	-	VCC × 0.3		
		ΔV _T	VCC × 0.05	-	-		
	RES, NMI Other peripheral input pins excluding IIC	V _{IH}	VCC × 0.8	-	-		
		V _{IL}	-	-	VCC × 0.2		
		ΔV _T	VCC × 0.1	-	-		
Input voltage (except for Schmitt trigger input pin)	IIC (SMBus)*2	V _{IH}	2.2	-	-	-	VCC = 3.6 to 5.5 V
		V _{IH}	2.0	-	-		VCC = 2.7 to 3.6 V
		V _{IL}	-	-	0.8		
	5V-tolerant ports*3	V _{IH}	VCC × 0.8	-	5.8		
		V _{IL}	-	-	VCC × 0.2		
	P914, P915	V _{IH}	VCC_USB × 0.8	-	VCC_USB + 0.3		
		V _{IL}	-	-	VCC_USB × 0.2		
	P000 to P015	V _{IH}	AVCC0 × 0.8	-	-		
		V _{IL}	-	-	AVCC0 × 0.2		
	EXTAL D00 to D15 Input ports pins except for P000 to P015, P914, P915	V _{IH}	VCC × 0.8	-	-		
		V _{IL}	-	-	VCC × 0.2		
	When V _{BATT} power supply is selected	P402, P403, P404	V _{IH}	V _{BATT} × 0.8	-		V _{BATT} + 0.3
V _{IL}			-	-	V _{BATT} × 0.2		
ΔV _T			V _{BATT} × 0.05	-	-		

Note 1. P205, P206, P400, P401, P407, P408, P511, P512 (total 8 pins).

Note 2. P100, P101, P204, P205, P206, P400, P401, P407, P408, P511, P512 (total 11 pins).

Note 3. P205, P206, P400 to P404, P407, P408, P511, P512 (total 11 pins).

Table 2.5 I/O V_{IH} , V_{IL} (2)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LDO} = 1.6$ to 2.7 V, $V_{BATT} = 1.6$ to 3.6 V, $V_{SS} = AV_{SS0} = 0$ V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Schmitt trigger input voltage	RES, NMI Peripheral input pins	V_{IH}	$V_{CC} \times 0.8$	-	-	V	-
		V_{IL}	-	-	$V_{CC} \times 0.2$		
		ΔV_T	$V_{CC} \times 0.01$	-	-		
Input voltage (except for Schmitt trigger input pin)	5V-tolerant ports*1	V_{IH}	$V_{CC} \times 0.8$	-	5.8		
		V_{IL}	-	-	$V_{CC} \times 0.2$		
	P914, P915	V_{IH}	$V_{CC_USB} \times 0.8$	-	$V_{CC_USB} + 0.3$		
		V_{IL}	-	-	$V_{CC_USB} \times 0.2$		
	P000 to P015	V_{IH}	$AV_{CC0} \times 0.8$	-	-		
		V_{IL}	-	-	$AV_{CC0} \times 0.2$		
	EXTAL D0 to D15 Input ports pins except for P000 to P015, P914, P915	V_{IH}	$V_{CC} \times 0.8$	-	-		
		V_{IL}	-	-	$V_{CC} \times 0.2$		
When V_{BATT} power supply is selected	P402, P403, P404	V_{IH}	$V_{BATT} \times 0.8$	-	$V_{BATT} + 0.3$		
		V_{IL}	-	-	$V_{BATT} \times 0.2$		
		ΔV_T	$V_{BATT} \times 0.01$	-	-		

Note 1. P205, P206, P400 to P404, P407, P408, P511, P512 (total 11 pins)

2.2.3 I/O I_{OH} , I_{OL} **Table 2.6** I/O I_{OH} , I_{OL} (1 of 2)

Conditions: VCC = AVCC0 = VCC_USB = VCC_USB_LCO = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P212, P213	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P408	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive for IIC Fast-mode*4 VCC = 2.7 to 5.5 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Port P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 VCC = 2.7 to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 VCC = 3.0 to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P115, P201 to P204, P300 to P315, P500 to P503, P600 to P606, P608 to P614, P800 to P809, P900 to P902 (total 67 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
Other output pin*3	Low drive*1	I_{OH}	-	-	-4.0	mA	
		I_{OL}	-	-	4.0	mA	
	Middle drive*2	I_{OH}	-	-	-8.0	mA	
		I_{OL}	-	-	8.0	mA	

Table 2.6 I/O I_{OH} , I_{OL} (2 of 2)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LCO} = 1.6$ to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	
Permissible output current (Max value per pin)	Ports P212, P213	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Port P408	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive for IIC Fast-mode*4 $V_{CC} = 2.7$ to 5.5 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 $V_{CC} = 3.0$ to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Port P409	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2 $V_{CC} = 2.7$ to 3.0 V	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		Middle drive*2 $V_{CC} = 3.0$ to 5.5 V	I_{OH}	-	-	-20.0	mA
			I_{OL}	-	-	20.0	mA
	Ports P100 to P115, P201 to P204, P300 to P315, P500 to P503, P600 to P606, P608 to P614, P800 to P809, P900 to P902 (total 67 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P914, P915	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
Other output pin*3	Low drive*1	I_{OH}	-	-	-4.0	mA	
		I_{OL}	-	-	4.0	mA	
	Middle drive*2	I_{OH}	-	-	-8.0	mA	
		I_{OL}	-	-	8.0	mA	
Permissible output current (max value total pins)	Total of ports P000 to P015	$\Sigma I_{OH}(\max)$	-	-	-30	mA	
		$\Sigma I_{OL}(\max)$	-	-	30	mA	
	Ports P914, P915	$\Sigma I_{OH}(\max)$	-	-	-4.0	mA	
		$\Sigma I_{OL}(\min)$	-	-	4.0	mA	
	Total of all output pin*5	$\Sigma I_{OH}(\max)$	-	-	-60	mA	
		$\Sigma I_{OL}(\max)$	-	-	60	mA	

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 μ s.

Note 1. This is the value when low driving ability is selected with the Port Drive Capability bit in PmnPFS register.

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.

Note 3. Except for ports P200, P214, P215, which are input ports.

Note 4. This is the value when middle driving ability for IIC Fast-mode is selected with the Port Drive Capability bit in PmnPFS register.

Note 5. For details on the permissible output current used with CTSU, see [section 2.11, CTSU Characteristics](#).

2.2.4 I/O V_{OH} , V_{OL} , and Other Characteristics**Table 2.7** I/O V_{OH} , V_{OL} (1)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LCO} = 4.0$ to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC*1	V_{OL}	-	-	0.4	V	$I_{OL} = 3.0$ mA	
		$V_{OL}^{*2,*5}$	-	-	0.6		$I_{OL} = 6.0$ mA	
	Ports P408, P409*2, *3	V_{OH}	$V_{CC} - 1.0$	-	-		$I_{OH} = -20$ mA	
		V_{OL}	-	-	1.0		$I_{OL} = 20$ mA	
	Ports P000 to P015	Low drive	V_{OH}	$AV_{CC0} - 0.8$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 2.0$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.8$	-		-	$I_{OH} = -4.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 4.0$ mA
	Ports P914, P915	V_{OH}	$V_{CC_USB} - 0.8$	-	-		$I_{OH} = -2.0$ mA	
		V_{OL}	-	-	0.8		$I_{OL} = 2.0$ mA	
	Other output pins*4	Low drive	V_{OH}	$V_{CC} - 0.8$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 2.0$ mA
		Middle drive*6	V_{OH}	$V_{CC} - 0.8$	-		-	$I_{OH} = -4.0$ mA
			V_{OL}	-	-		0.8	$I_{OL} = 4.0$ mA

Note 1. P100, P101, P204, P205, P206, P400, P401, P407, P408, P511, P512 (total 11 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for ports P200, P214, P215, which are input ports.

Note 5. This is the value when middle driving ability for IIC is selected with the Port Drive Capability bit in PmnPFS register for P408.

Note 6. Except for P212, P213.

Table 2.8 I/O V_{OH} , V_{OL} (2)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LCO} = 2.7$ to 4.0 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Output voltage	IIC*1	V_{OL}	-	-	0.4	V	$I_{OL} = 3.0$ mA	
		$V_{OL}^{*2,*5}$	-	-	0.6		$I_{OL} = 6.0$ mA	
	Ports P408, P409*2, *3	V_{OH}	$V_{CC} - 1.0$	-	-		$I_{OH} = -20$ mA $V_{CC} = 3.3$ V	
		V_{OL}	-	-	1.0		$I_{OL} = 20$ mA $V_{CC} = 3.3$ V	
	Ports P000 to P015	Low drive	V_{OH}	$AV_{CC0} - 0.5$	-		-	$I_{OH} = -1.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 1.0$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.5$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 2.0$ mA
	Ports P914, P915	V_{OH}	$V_{CC_USB} - 0.5$	-	-		$I_{OH} = -1.0$ mA	
		V_{OL}	-	-	0.5		$I_{OL} = 1.0$ mA	
	Other output pins*4	Low drive	V_{OH}	$V_{CC} - 0.5$	-		-	$I_{OH} = -1.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 1.0$ mA
		Middle drive*6	V_{OH}	$V_{CC} - 0.5$	-		-	$I_{OH} = -2.0$ mA
			V_{OL}	-	-		0.5	$I_{OL} = 2.0$ mA

Note 1. P100, P101, P204, P205, P206, P400, P401, P407, P408, P511, P512 (total 11 pins).

Note 2. This is the value when middle driving ability is selected with the Port Drive Capability bit in PmnPFS register.

Note 3. Based on characterization data, not tested in production.

Note 4. Except for ports P200, P214, P215, which are input ports.

Note 5. This is the value when middle driving ability for IIC is selected with the Port Drive Capability bit in PmnPFS register for P408.

Note 6. Except for P212, P213.

Table 2.9 I/O V_{OH} , V_{OL} (3)Conditions: $V_{CC} = AV_{CC0} = V_{CC_USB} = V_{CC_USB_LCO} = 1.6$ to 2.7 V

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	Ports P000 to P015	Low drive	V_{OH}	$AV_{CC0} - 0.3$	-	-	V	$I_{OH} = -0.5$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 0.5$ mA
		Middle drive	V_{OH}	$AV_{CC0} - 0.3$	-	-		$I_{OH} = -1.0$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 1.0$ mA
	Ports P914, P915	V_{OH}	$V_{CC_USB} - 0.3$	-	-	$I_{OH} = -0.5$ mA		
		V_{OL}	-	-	0.3	$I_{OL} = 0.5$ mA		
	Other output pins*1	Low drive	V_{OH}	$V_{CC} - 0.3$	-	-		$I_{OH} = -0.5$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 0.5$ mA
		Middle drive*2	V_{OH}	$V_{CC} - 0.3$	-	-		$I_{OH} = -1.0$ mA
			V_{OL}	-	-	0.3		$I_{OL} = 1.0$ mA

Note 1. Except for ports P200, P214, P215, which are input ports.

Note 2. Except for P212, P213.

Table 2.10 I/O other characteristicsConditions: $V_{CC} = AV_{CC0} = 1.6$ to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	RES, P200, P214, P215	$ I_{in} $	-	-	1.0	μ A	$V_{in} = 0$ V $V_{in} = V_{CC}$
Three-state leakage current (off state)	5V-tolerant ports	$ I_{TSI} $	-	-	1.0	μ A	$V_{in} = 0$ V $V_{in} = 5.8$ V
	Other ports (except for ports P200, P214, P215 and 5 V tolerant)		-	-	1.0		$V_{in} = 0$ V $V_{in} = V_{CC}$
Input pull-up resistor	All ports (except for ports P200, P214, P215, P914, P915)	R_U	10	20	50	k Ω	$V_{in} = 0$ V
Input capacitance	P914, P915, P100 to P103, P111, P112, P200	C_{in}	-	-	30	pF	$V_{in} = 0$ V $f = 1$ MHz $T_a = 25^\circ$ C
	Other input pins		-	-	15		

2.2.5 I/O Pin Output Characteristics of Low Drive Capacity

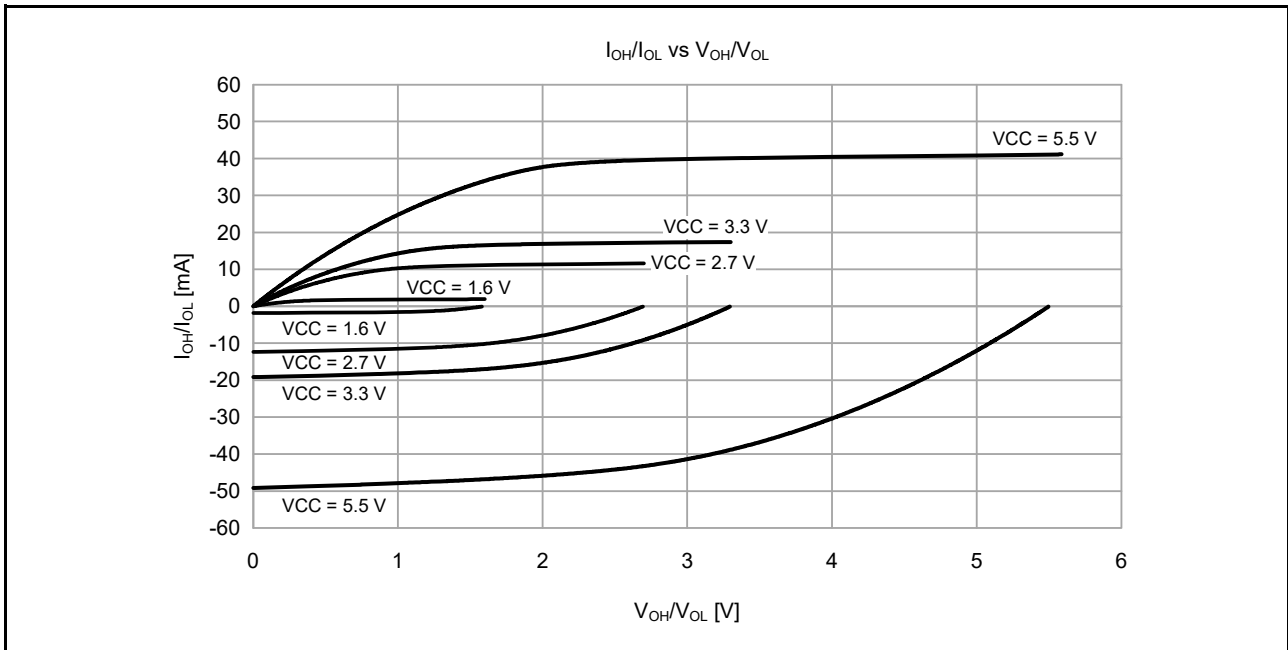


Figure 2.2 VOH/VOL and IOH/IOL voltage characteristics at Ta = 25°C when low drive output is selected (reference data)

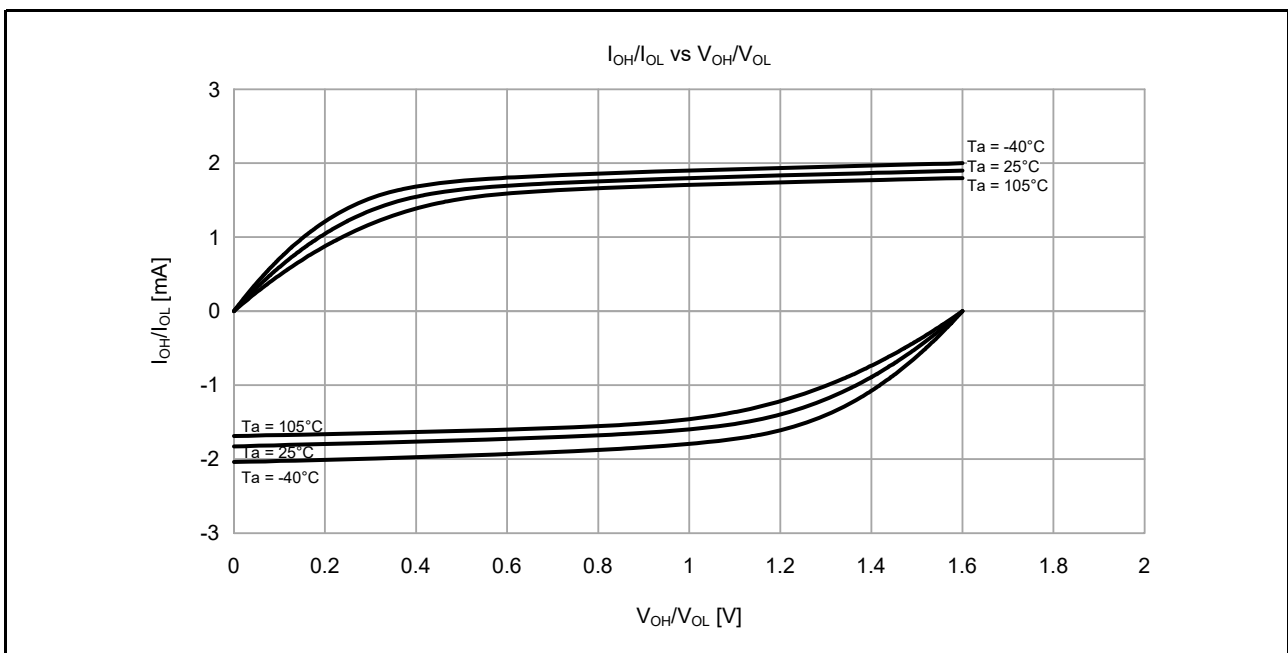


Figure 2.3 VOH/VOL and IOH/IOL temperature characteristics at VCC = 1.6 V when low drive output is selected (reference data)

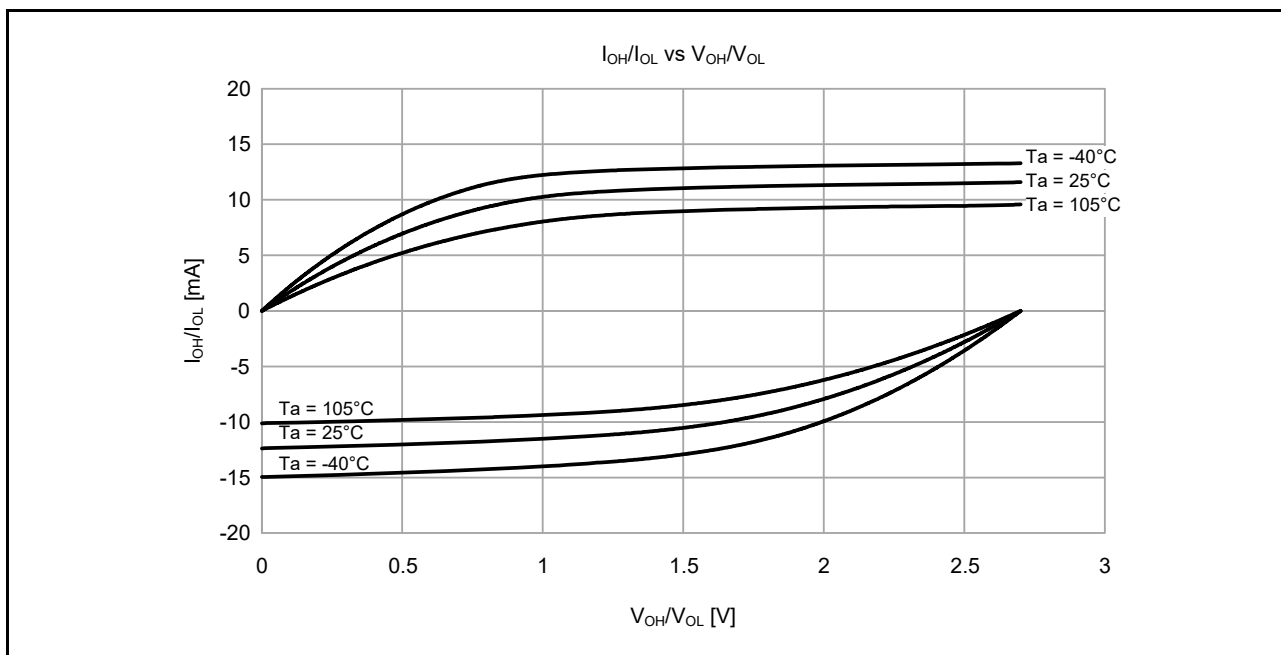


Figure 2.4 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7$ V when low drive output is selected (reference data)

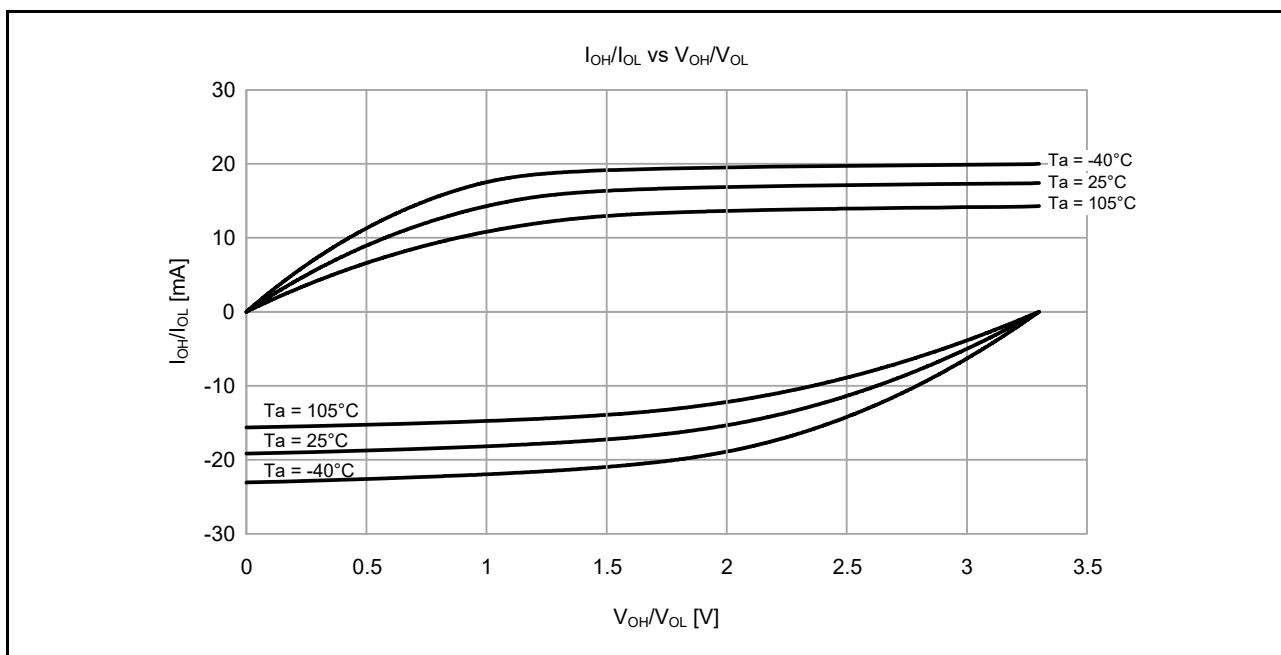


Figure 2.5 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3$ V when low drive output is selected (reference data)

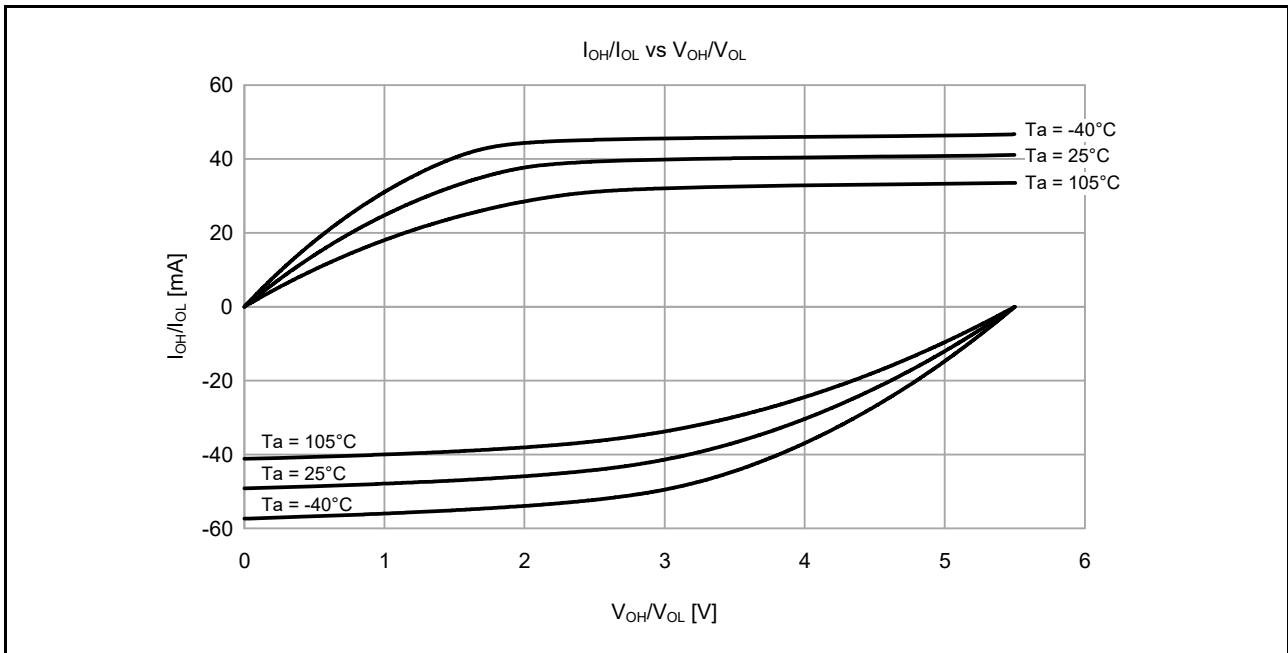


Figure 2.6 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5$ V when low drive output is selected (reference data)

2.2.6 I/O Pin Output Characteristics of Middle Drive Capacity

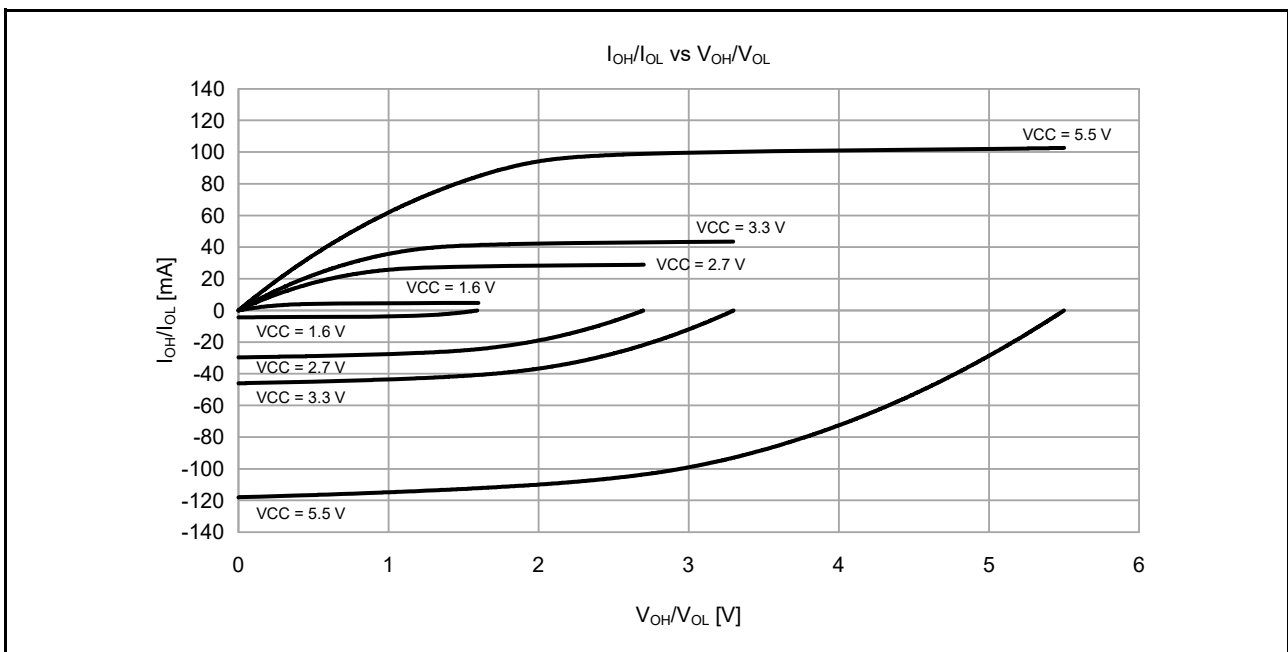


Figure 2.7 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ\text{C}$ when middle drive output is selected (reference data)

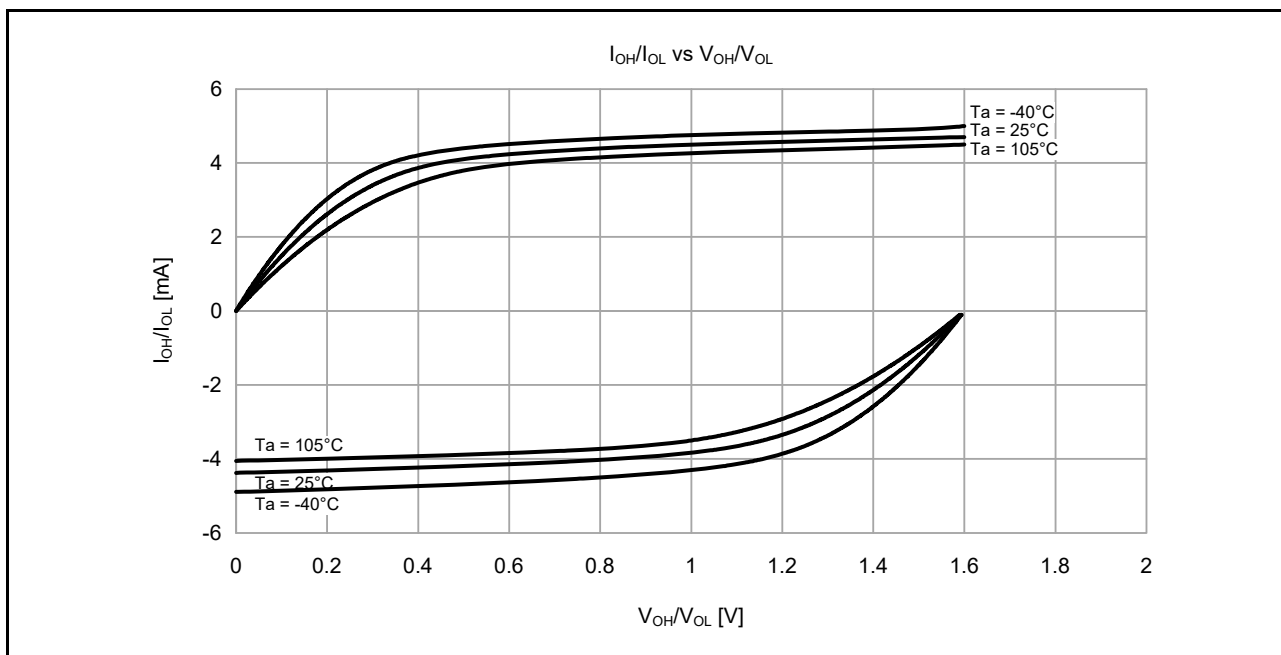


Figure 2.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 1.6$ V when middle drive output is selected (reference data)

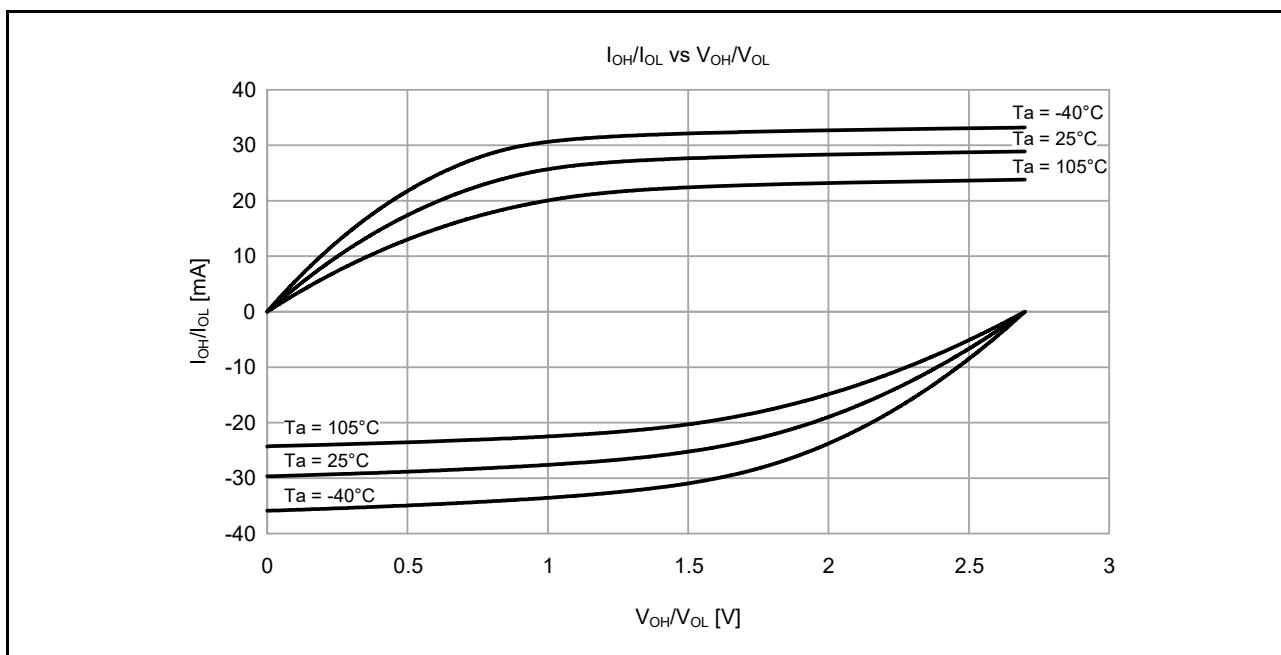


Figure 2.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7$ V when middle drive output is selected (reference data)

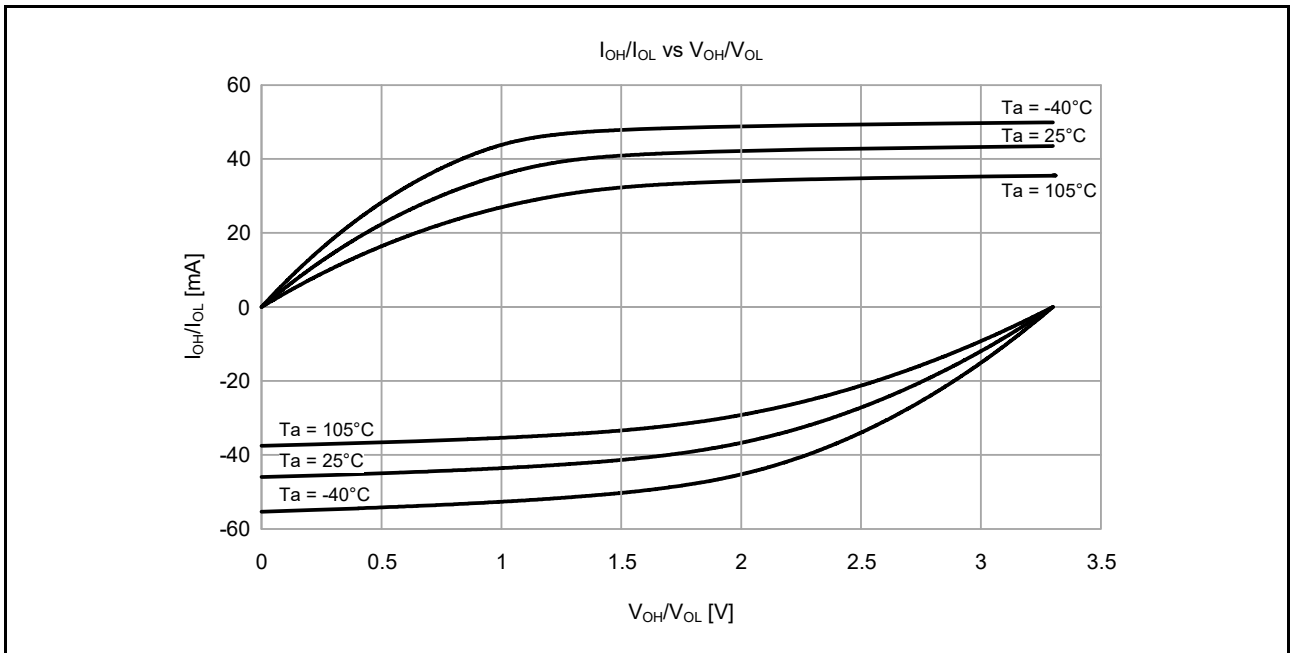


Figure 2.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3$ V when middle drive output is selected (reference data)

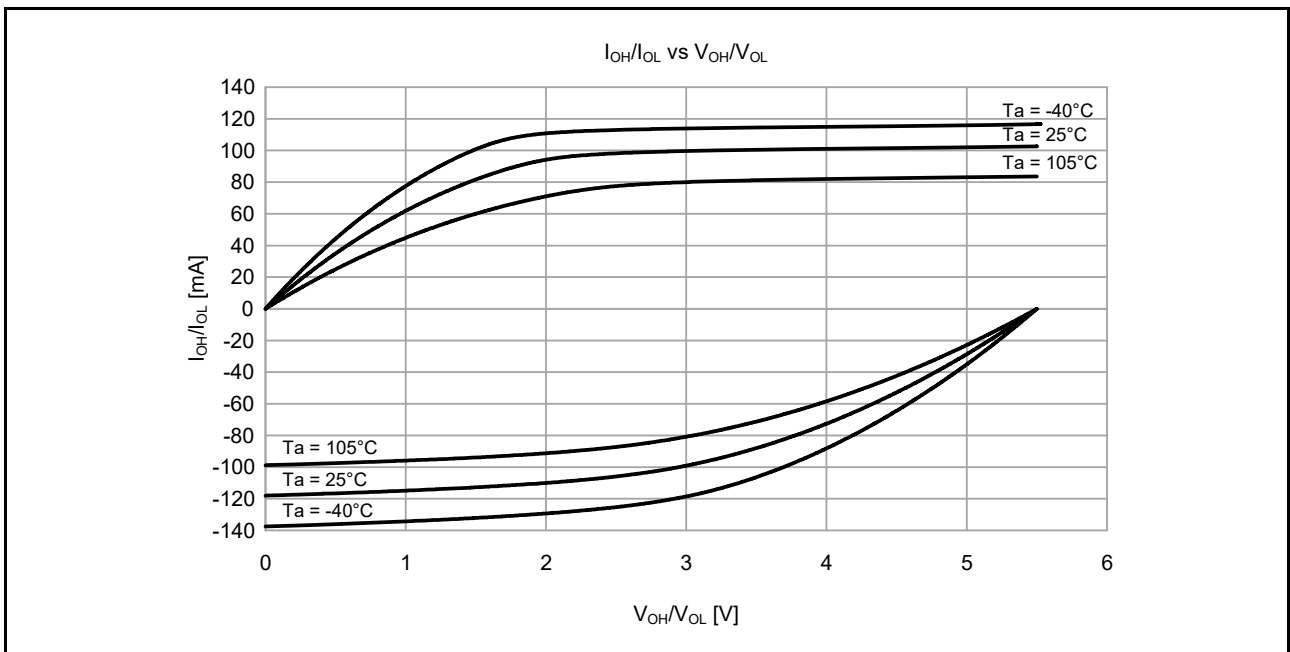


Figure 2.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5$ V when middle drive output is selected (reference data)

2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

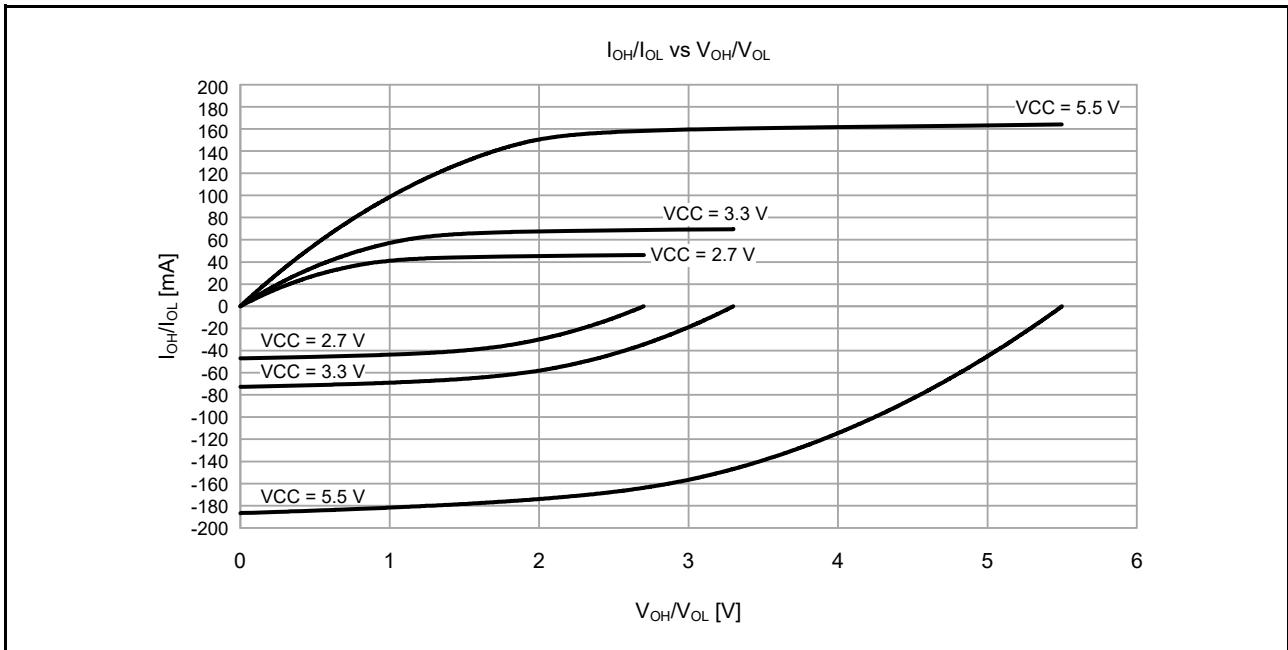


Figure 2.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at $T_a = 25^\circ\text{C}$ when middle drive output is selected (reference data)

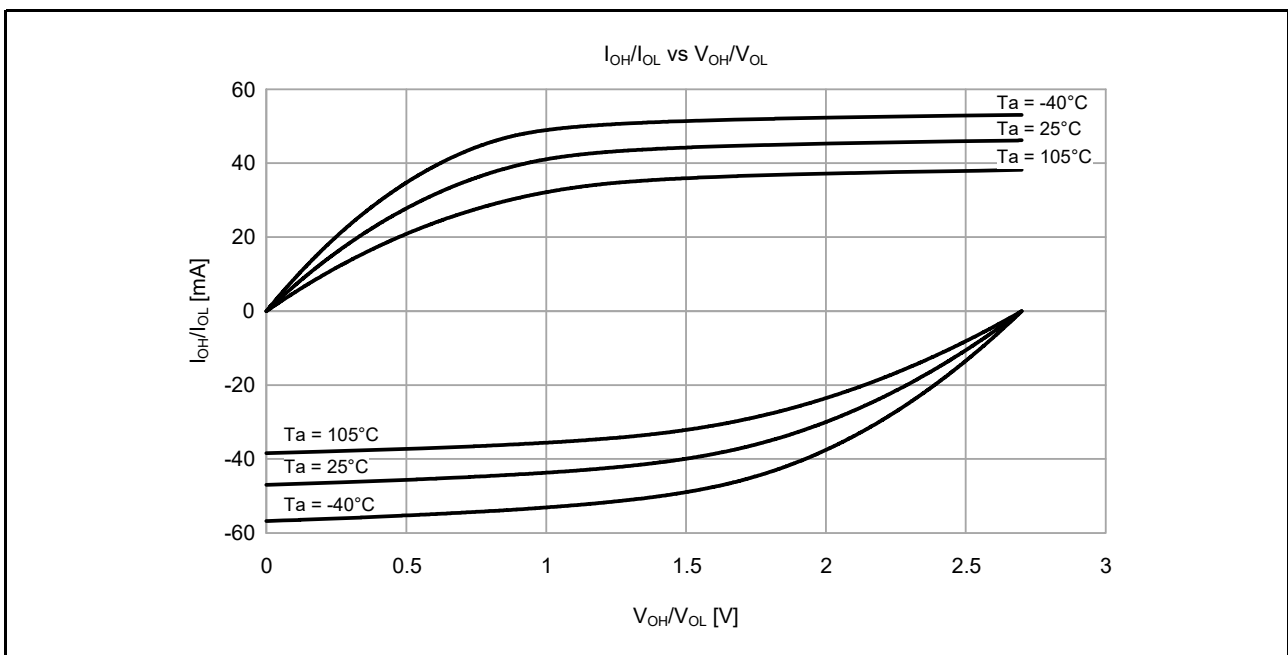


Figure 2.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 2.7\text{V}$ when middle drive output is selected (reference data)

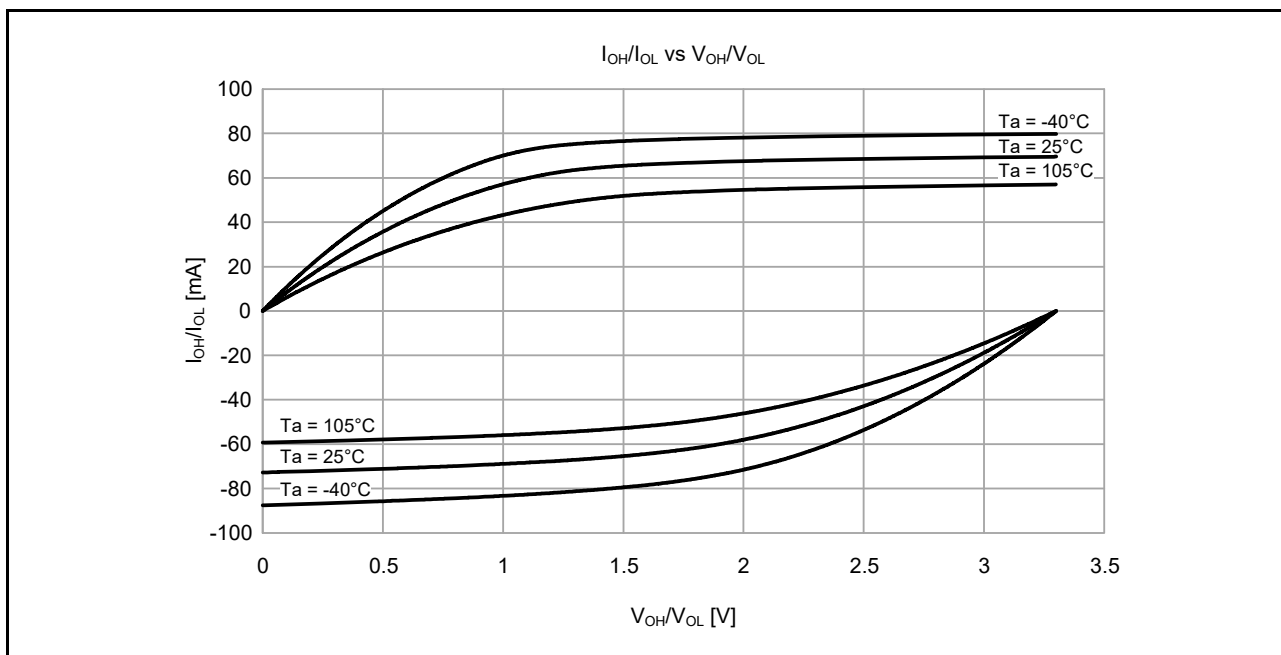


Figure 2.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 3.3\text{ V}$ when middle drive output is selected (reference data)

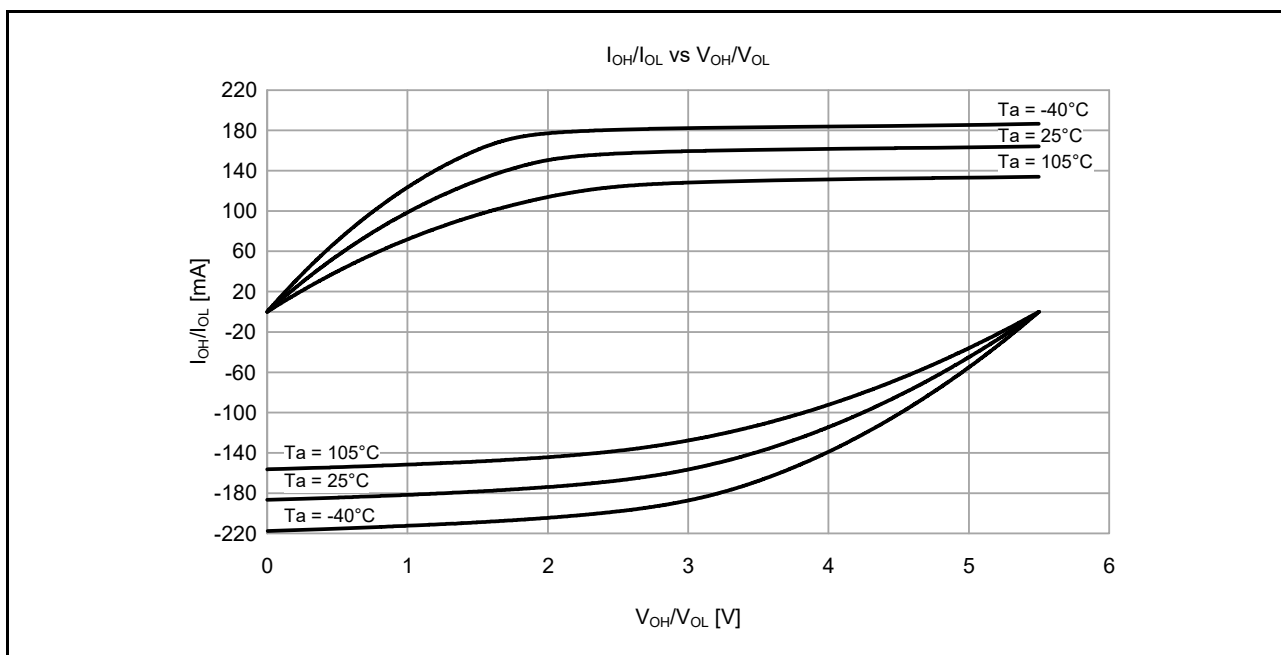


Figure 2.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at $V_{CC} = 5.5\text{ V}$ when middle drive output is selected (reference data)

2.2.8 IIC I/O Pin Output Characteristics

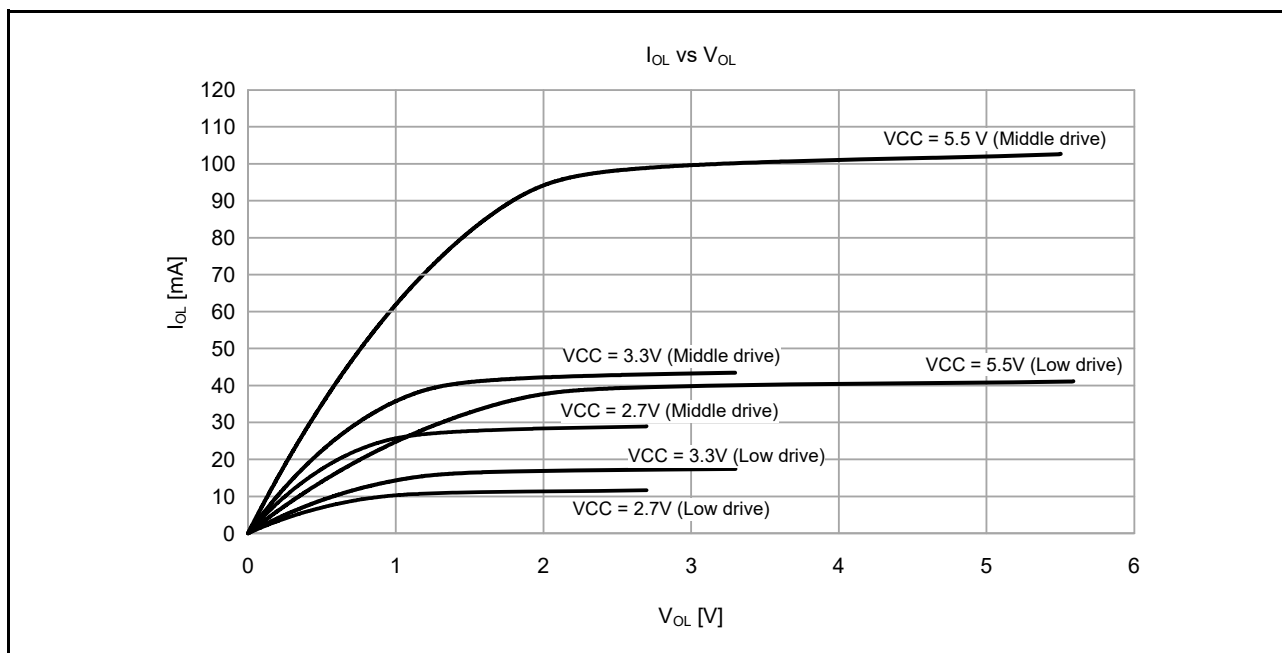


Figure 2.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C

2.2.9 Operating and Standby Current

Table 2.11 Operating and standby current (1) (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions		
Supply current*1	High-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 48 MHz	I _{CC}	8.4	-	mA	*7		
				ICLK = 32 MHz		5.9	-				
				ICLK = 16 MHz		3.5	-				
				ICLK = 8 MHz		2.3	-				
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 48 MHz		17.9	-				
				ICLK = 32 MHz		12.4	-				
				ICLK = 16 MHz		7.0	-				
				ICLK = 8 MHz		4.3	-				
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 48 MHz		21.2	-			*9	
				ICLK = 32 MHz		16.0	-			*8	
				ICLK = 16 MHz		8.8	-				
				ICLK = 8 MHz		5.1	-				
		All peripheral clock enabled, code executing from SRAM*5	ICLK = 48 MHz	-	56.0	*9					
			Increase during BGO operation*6				2.5		-	-	
		Middle-speed mode*2	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 12 MHz	I _{CC}	2.5		-	mA	*7
					ICLK = 8 MHz		2.1		-		
					ICLK = 1 MHz		1.0		-		
					ICLK = 12 MHz		5.2		-		
	All peripheral clock disabled, CoreMark code executing from flash*5			ICLK = 8 MHz	4.0		-				
				ICLK = 1 MHz	1.3		-				
				ICLK = 12 MHz	6.5		-	*8			
				ICLK = 8 MHz	4.8		-				
	All peripheral clock enabled, while (1) code executing from flash*5			ICLK = 1 MHz	1.6		-				
				ICLK = 12 MHz	-		23.0				
Sleep mode	All peripheral clock disabled*5			ICLK = 12 MHz	1.4		-	*7			
				ICLK = 8 MHz	1.3		-				
			ICLK = 1 MHz	0.9	-						
	All peripheral clock enabled*5		ICLK = 12 MHz	5.3	-	*8					
			ICLK = 8 MHz	4.0	-						
			ICLK = 1 MHz	1.5	-						
Increase during BGO operation*6				2.5	-	-					

Table 2.11 Operating and standby current (1) (2 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter					Symbol	Typ*10	Max	Unit	Test conditions		
Supply current*1	Low-speed mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 1 MHz	I _{CC}	0.4	-	mA	*7		
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 1 MHz		0.6	-				
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 1 MHz		1.1	-			*8	
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 1 MHz		-	2.5				
		Sleep mode	All peripheral clock disabled*5	ICLK = 1 MHz		0.3	-		*7		
			All peripheral clock enabled*5	ICLK = 1 MHz		1.0	-		*8		
	Low-voltage mode*3	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 4 MHz		I _{CC}	1.8	-	mA	*7	
			All peripheral clock disabled, CoreMark code executing from flash*5	ICLK = 4 MHz			3.0	-			
			All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 4 MHz			3.3	-			*8
			All peripheral clock enabled, code executing from SRAM*5	ICLK = 4 MHz			-	9.0			
		Sleep mode	All peripheral clock disabled*5	ICLK = 4 MHz			1.4	-		*7	
			All peripheral clock enabled*5	ICLK = 4 MHz			2.9	-		*8	
Subosc-speed mode*4	Normal mode	All peripheral clock disabled, while (1) code executing from flash*5	ICLK = 32.768 kHz	I _{CC}	9.3	-	μA	*8			
		All peripheral clock enabled, while (1) code executing from flash*5	ICLK = 32.768 kHz		17.2	-					
		All peripheral clock enabled, code executing from SRAM*5	ICLK = 32.768 kHz		-	106.0					
	Sleep mode	All peripheral clock disabled*5	ICLK = 32.768 kHz		6.0	-					
		All peripheral clock enabled*5	ICLK = 32.768 kHz		14.0	-					

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The clock source is HOCO.

Note 3. The clock source is MOCO.

Note 4. The clock source is the sub-clock oscillator.

Note 5. This does not include BGO operation.

Note 6. This is the increase for programming or erasure of the flash memory for data storage during program execution.

Note 7. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are set to divided by 64.

Note 8. FCLK, BCLK, PCLKA, PCLKB, PCLKC and PCLKD are the same frequency as that of ICLK.

Note 9. FCLK, BCLK, and PCLKB are set to divided by 2 and PCLKA, PCLKC and PCLKD are the same frequency as that of ICLK.

Note 10. VCC = 3.3 V.

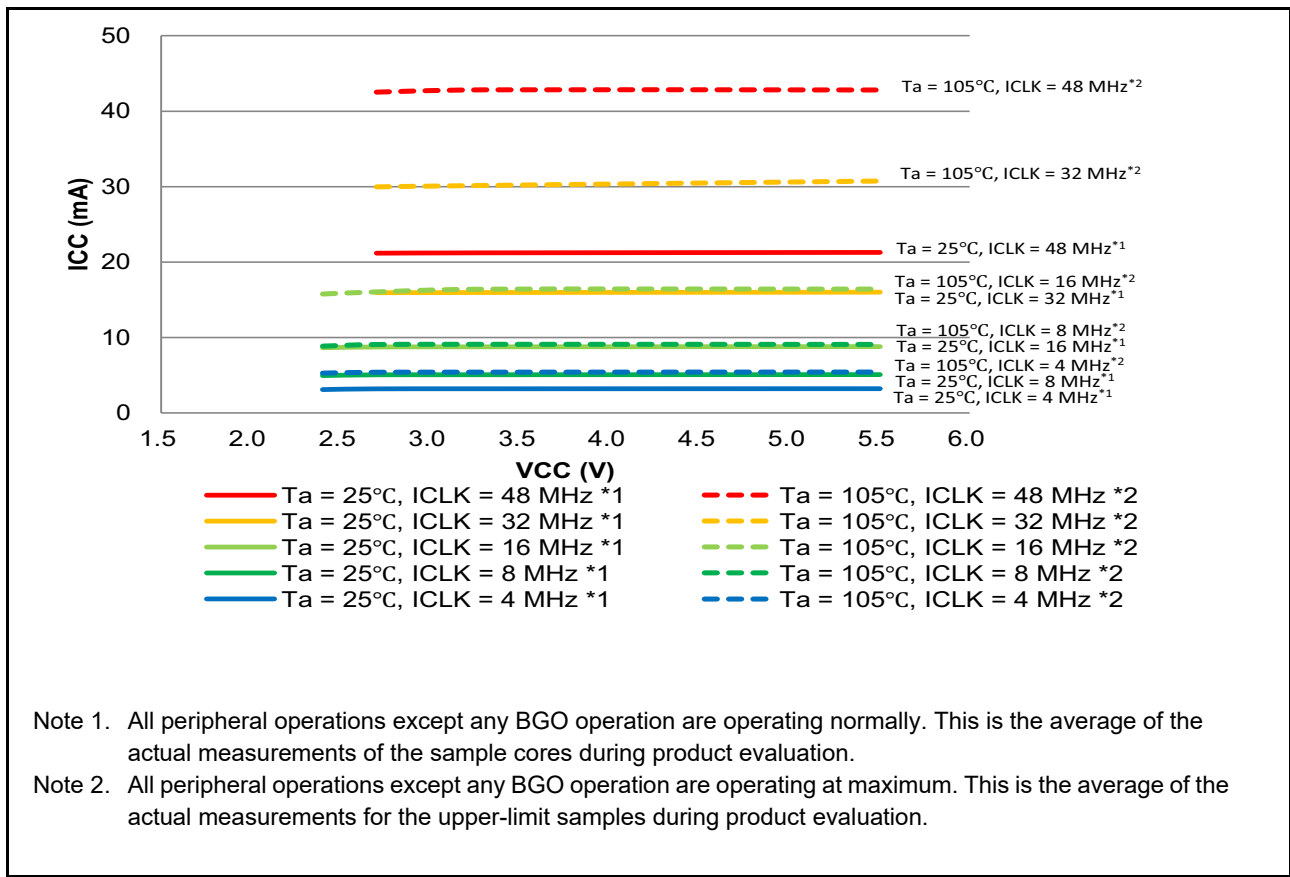


Figure 2.17 Voltage dependency in high-speed mode (reference data)

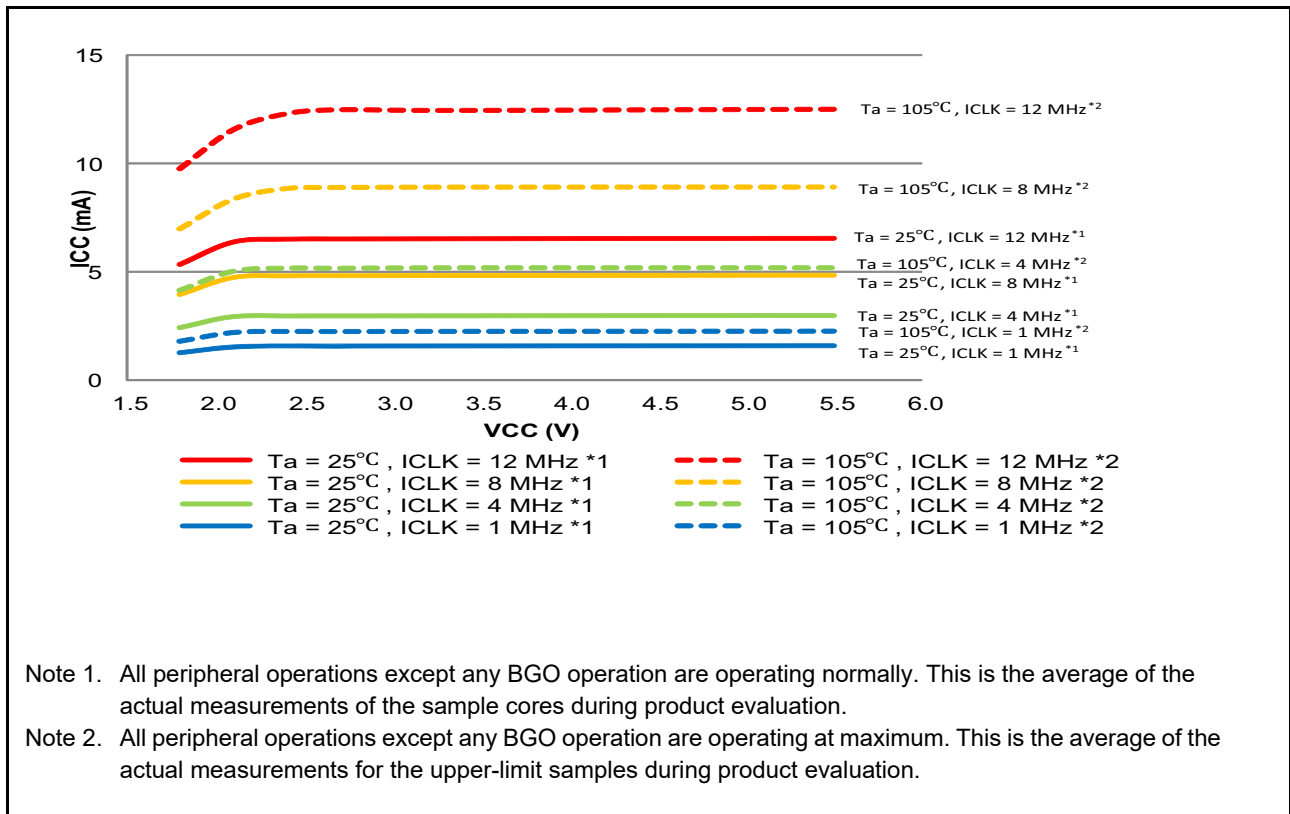


Figure 2.18 Voltage dependency in middle-speed mode (reference data)

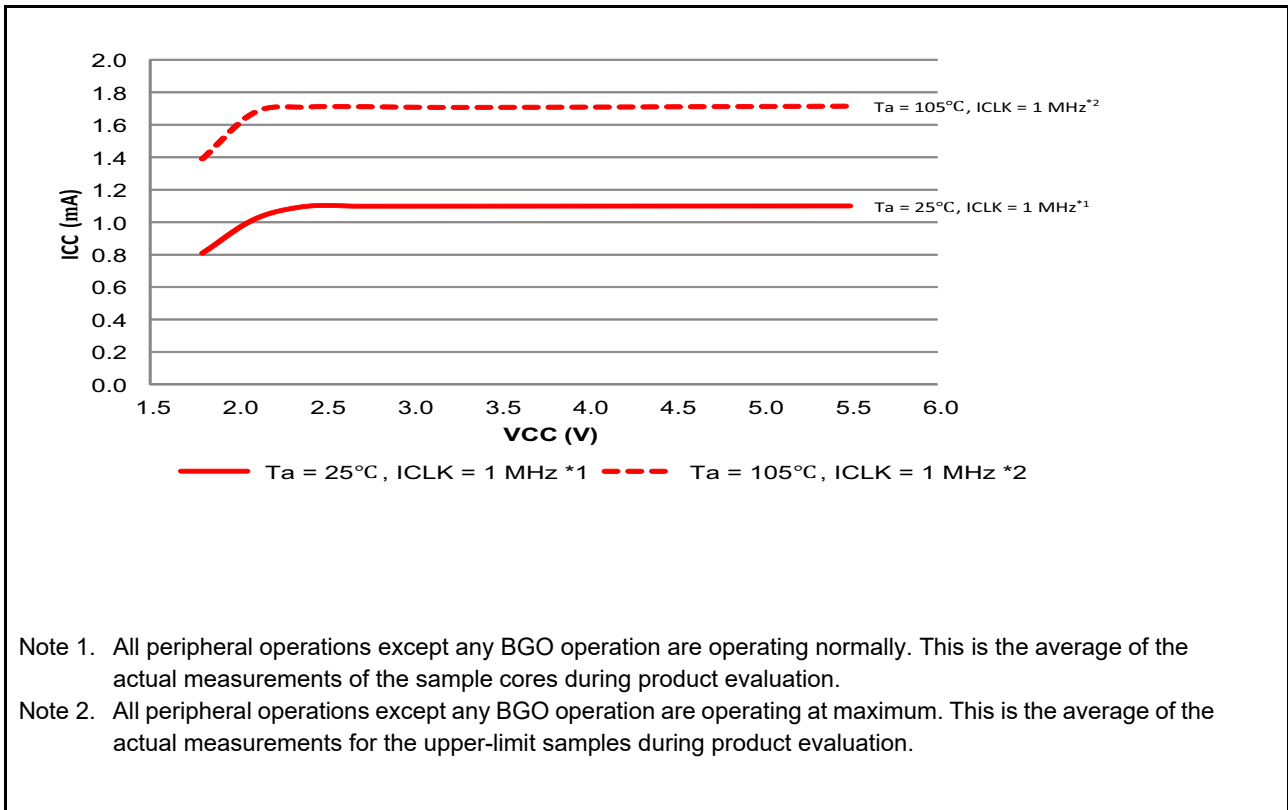


Figure 2.19 Voltage dependency in low-speed mode (reference data)

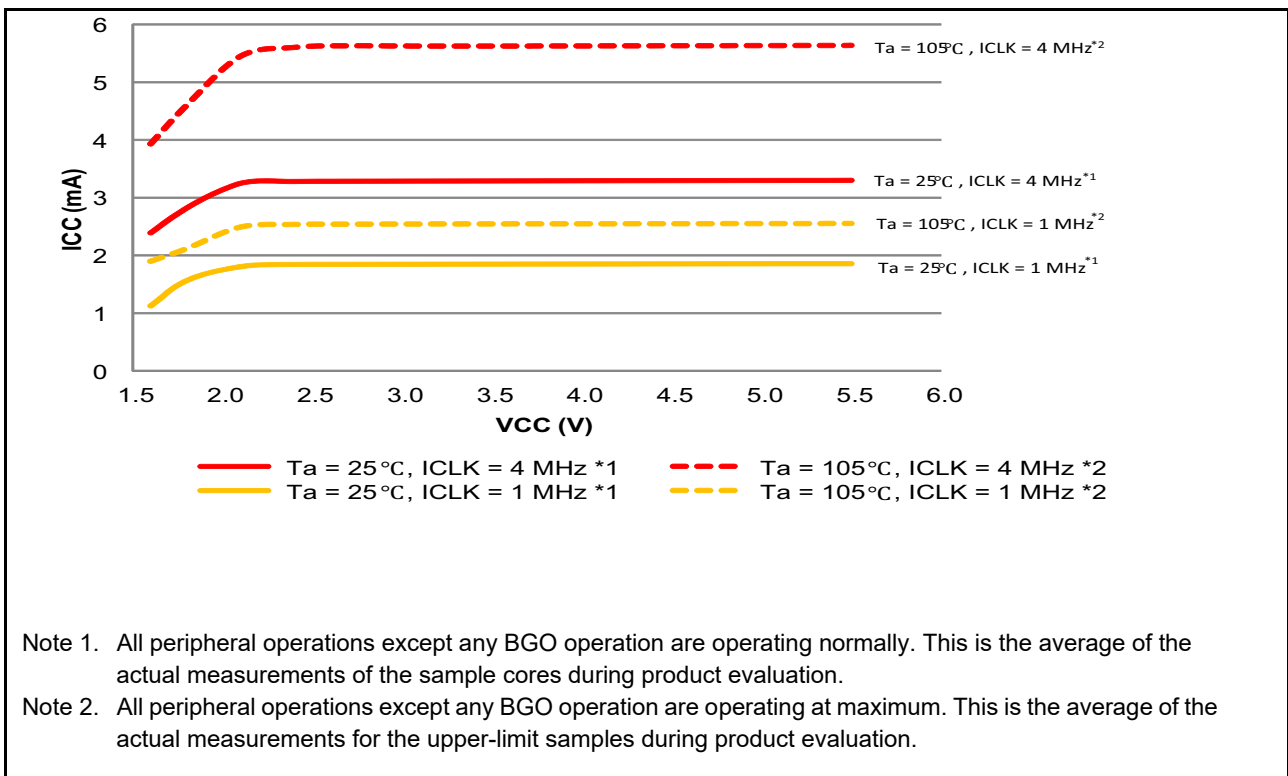


Figure 2.20 Voltage dependency in low-voltage mode (reference data)

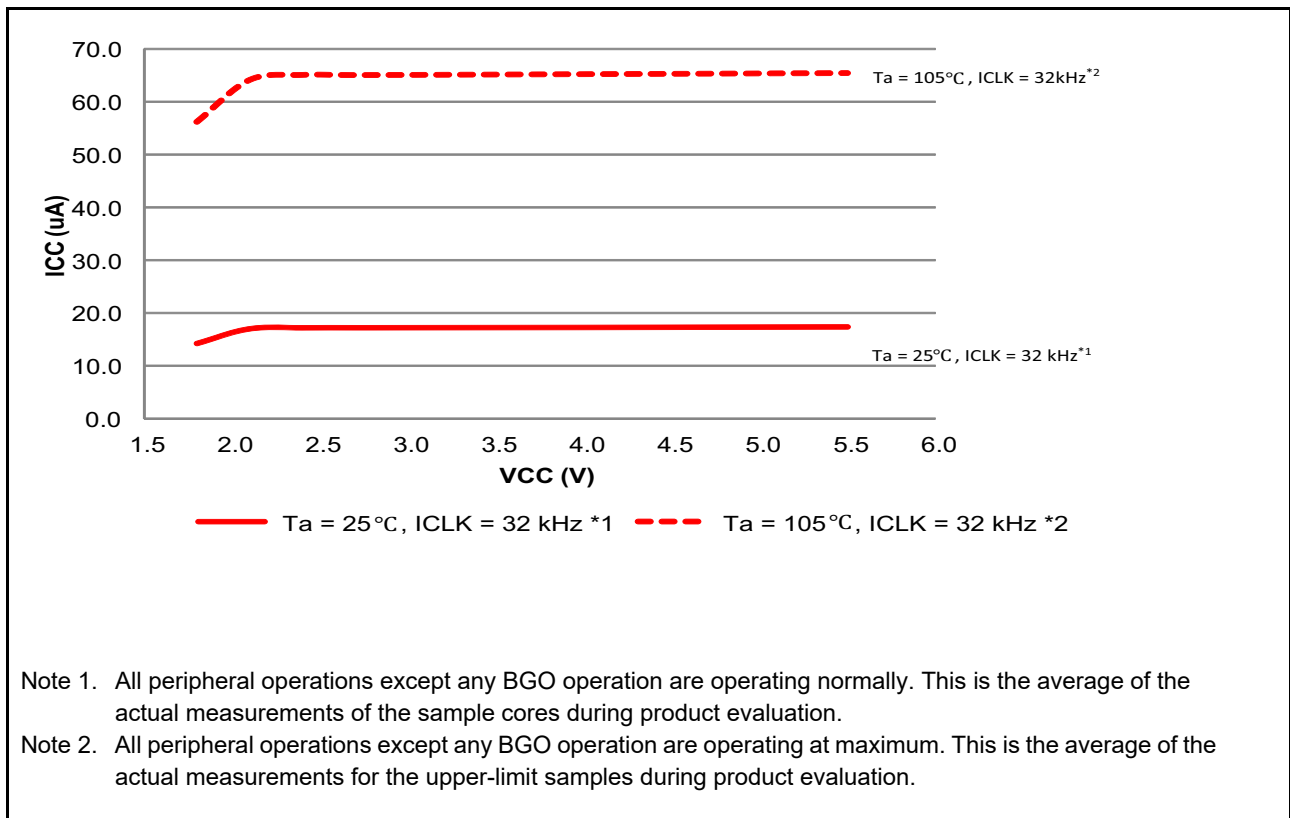


Figure 2.21 Voltage dependency in subosc-speed mode (reference data)

Table 2.12 Operating and standby current (2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter	Symbol	Typ*4	Max	Unit	Test conditions		
Supply current*1	Software Standby mode*2	I _{CC}	T _a = 25°C	0.9	5.0	µA	PSMCR.PSMC[1:0] = 01b (48-KB SRAM on)
			T _a = 55°C	1.5	8.1		
			T _a = 85°C	3.6	22.1		
			T _a = 105°C	8.8	57.5		
			T _a = 25°C	1.0	5.6		PSMCR.PSMC[1:0] = 00b (All SRAM on)
			T _a = 55°C	1.6	8.4		
			T _a = 85°C	4.3	26.7		
			T _a = 105°C	10.6	69.7		
	Increment for RTC operation with low-speed on-chip oscillator*3	0.5	-	-			
	Increment for RTC operation with sub-clock oscillator*3	0.4	-	SOMCR.SODRV[1:0] are 11b (Low power mode 3)			
1.2		-	SOMCR.SODRV[1:0] are 00b (Normal mode)				

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

Note 2. The IWDT and LVD are not operating.

Note 3. Includes the current of sub-oscillation circuit or low-speed on-chip oscillator.

Note 4. VCC = 3.3 V.

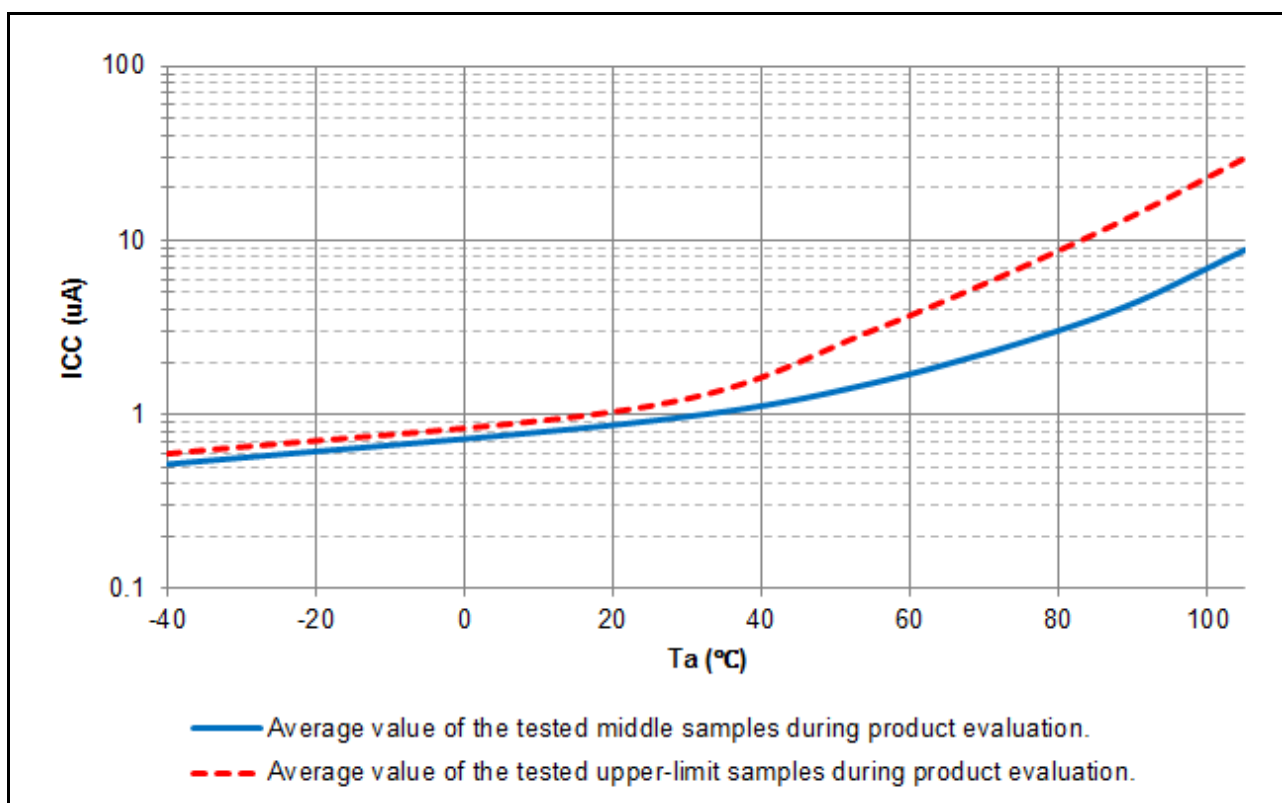


Figure 2.22 Temperature dependency in Software Standby mode 48-KB SRAM on (reference data)

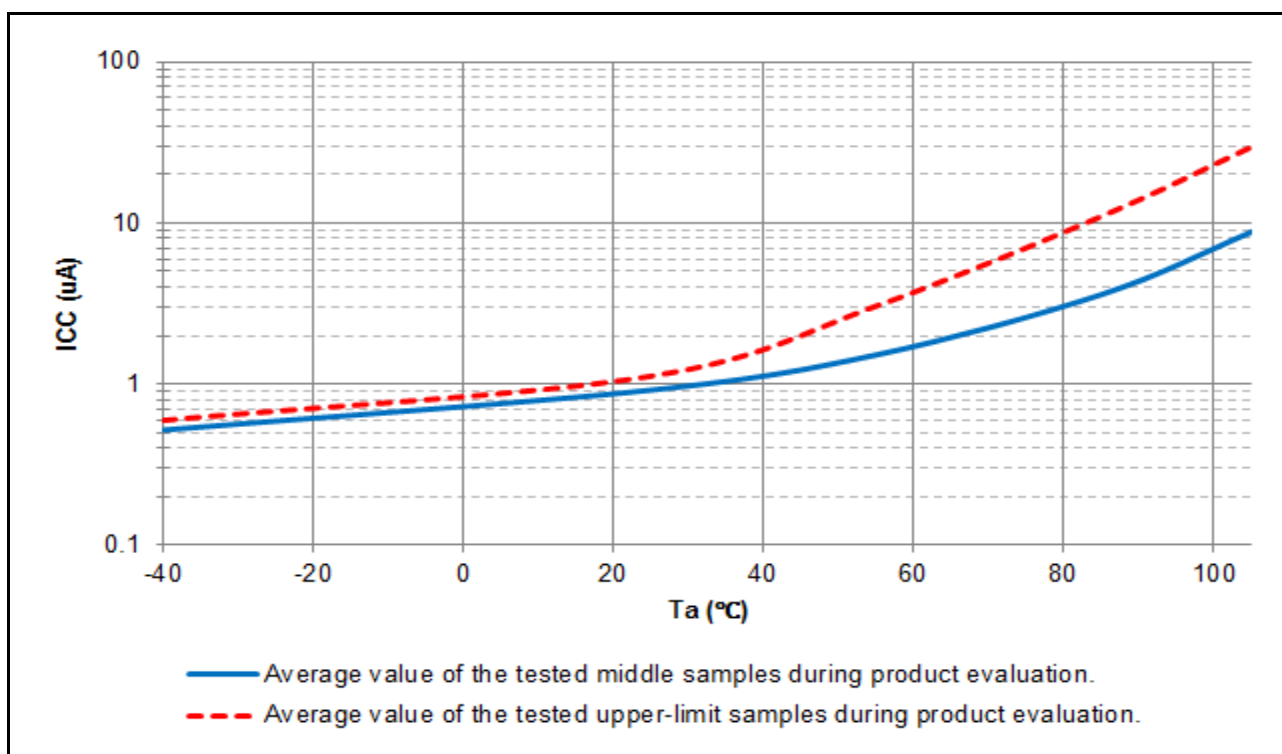


Figure 2.23 Temperature dependency in Software Standby mode all SRAM on (reference data)

Table 2.13 Operating and standby current (3)

Conditions: VCC = AVCC0 = 0V, VBATT = 1.6 to 3.6 V, VSS = AVSS0 = 0V

Parameter		Symbol	Typ	Max	Unit	Test conditions	
Supply current*1	RTC operation when VCC is off	I _{CC}	0.8	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)	
							T _a = 25°C
							T _a = 55°C
							T _a = 85°C
			0.9	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 11b (Low power mode 3)	
							T _a = 25°C
							T _a = 55°C
							T _a = 85°C
			1.2	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)	
							T _a = 25°C
							T _a = 55°C
							T _a = 85°C
			1.3	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)	
							T _a = 25°C
T _a = 55°C							
T _a = 85°C							
1.6	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
1.8	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
2.1	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
2.3	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
1.7	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
1.9	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
2.2	-	μA	VBATT = 2.0 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			
2.4	-	μA	VBATT = 3.3 V SOMCR.SORDRV[1:0] = 00b (Normal mode)				
				T _a = 25°C			
				T _a = 55°C			
				T _a = 85°C			

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.

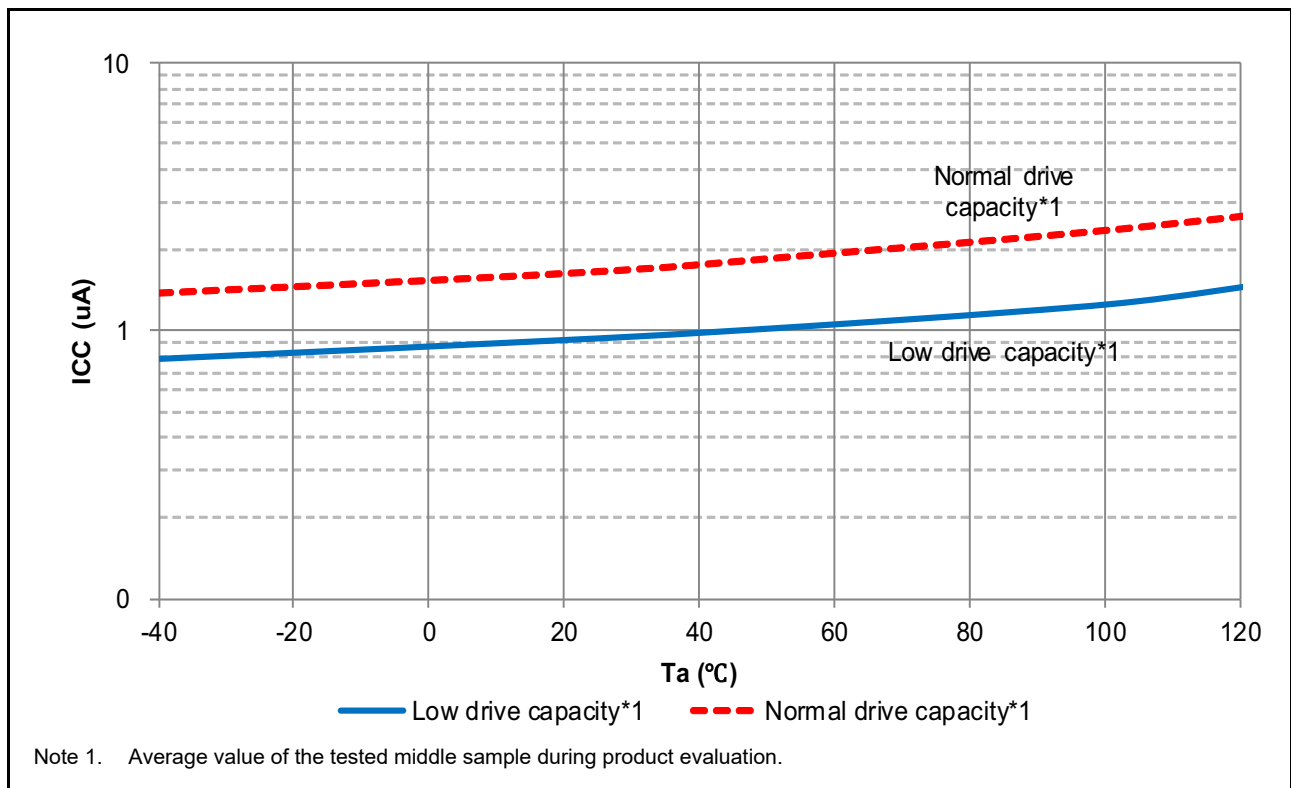


Figure 2.24 Temperature dependency of RTC operation with VCC off (reference data)

Table 2.14 Operating and standby current (4)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V, VREFH0 = 2.7 V to AVCC0

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	-	-	3.0	mA	-	
	During A/D conversion (at low power conversion)		-	-	1.0	mA	-	
	During D/A conversion (per channel)*1		-	0.4	0.8	mA	-	
	Waiting for A/D and D/A conversion (all units)*6		-	-	1.0	μ A	-	
Reference power supply current	During A/D conversion	I_{REFH0}	-	-	150	μ A	-	
	Waiting for A/D conversion (all units)		-	-	60	nA	-	
	During D/A conversion	I_{REFH}	-	50	100	μ A	-	
	Waiting for D/A conversion (all units)		-	-	100	μ A	-	
Temperature sensor		I_{TNS}	-	75	-	μ A	-	
Low-Power Analog Comparator operating current	Window mode	I_{CMPLP}	-	15	-	μ A	-	
	Comparator High-speed mode		-	10	-	μ A	-	
	Comparator Low-speed mode		-	2	-	μ A	-	
	Comparator Low-speed mode using DAC8		-	820	-	μ A	-	
Operational Amplifier operating current	Low power mode	I_{AMP}	1 unit operating	-	2.5	4.0	μ A	-
			2 units operating	-	4.5	8.0	μ A	-
			3 units operating	-	6.5	11.0	μ A	-
			4 units operating	-	8.5	14.0	μ A	-
	High speed mode		1 unit operating	-	140	220	μ A	-
			2 units operating	-	280	410	μ A	-
			3 units operating	-	420	600	μ A	-
			4 units operating	-	560	780	μ A	-
LCD operating current	External resistance division method $f_{LCD} = f_{SUB} = 128$ Hz, 1/3 bias, and 4-time slice	I_{LCD1}^{*5}	-	0.34	-	μ A	-	
	Internal voltage boosting method (VLCD.VLCD = 04) $f_{LCD} = f_{SUB} = 128$ Hz, 1/3 bias, and 4-time slice	I_{LCD2}^{*5}	-	0.92	-	μ A	-	
	Capacitor split method $f_{LCD} = f_{SUB} = 128$ Hz, 1/3 bias, and 4-time slice	I_{LCD3}^{*5}	-	0.19	-	μ A	-	
USB operating current	During USB communication operation under the following settings and conditions: • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.	I_{USBH}^{*2}	-	4.3 (VCC) 0.9 (VCC_USB)*4	-	mA	-	
	During USB communication operation under the following settings and conditions: • Device controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) \times 1, bulk IN transfer (64 bytes) \times 1 • Connect the host device via a 1-meter USB cable from the USB port.	I_{USBF}^{*2}	-	3.6 (VCC) 1.1 (VCC_USB)*4	-	mA	-	
	During suspended state under the following setting and conditions: • Device controller operation is set to full-speed mode (pull up the USB_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.	I_{SUSP}^{*3}	-	0.35 (VCC) 170 (VCC_USB)*4	-	μ A	-	

Note 1. The reference power supply current is included in the power supply current value for D/A conversion.

Note 2. Current consumed only by the USBFS.

Note 3. Includes the current supplied from the pull-up resistor of the USB_DP pin to the pull-down resistor of the host device, in addition to the current consumed by the MCU during the suspended state.

Note 4. When VCC = VCC_USB = 3.3 V.

Note 5. Current flowing only to the LCD controller. Not including the current that flows through the LCD panel.

Note 6. When the MCU is in Software Standby mode or the MSTPCR.DMSTPD16 (ADC140 Module Stop bit) is in the module-stop state.

2.2.10 VCC Rise and Fall Gradient and Ripple Frequency

Table 2.15 Rise and fall gradient characteristics

Conditions: VCC = AVCC0 = 0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Power-on VCC rising gradient	Voltage monitor 0 reset disabled at startup (normal startup)	SrVCC	0.02	-	2	ms/V	-
	Voltage monitor 0 reset enabled at startup*1		0.02	-	-		
	SCI/USB Boot mode*2		0.02	-	2		

Note 1. When OFS1.LVDAS = 0.

Note 2. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of the OFS1.LVDAS bit.

Table 2.16 Rising and falling gradient and ripple frequency characteristics

Conditions: VCC = AVCC0 = VCC_USB = 1.6 to 5.5 V

The ripple voltage must meet the allowable ripple frequency $f_r(VCC)$ within the range between the VCC upper limit (5.5 V) and lower limit (1.6 V).

When VCC change exceeds VCC $\pm 10\%$, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_r(VCC)$	-	-	10	kHz	Figure 2.25 $V_{r(VCC)} \leq VCC \times 0.2$
		-	-	1	MHz	Figure 2.25 $V_{r(VCC)} \leq VCC \times 0.08$
		-	-	10	MHz	Figure 2.25 $V_{r(VCC)} \leq VCC \times 0.06$
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC $\pm 10\%$

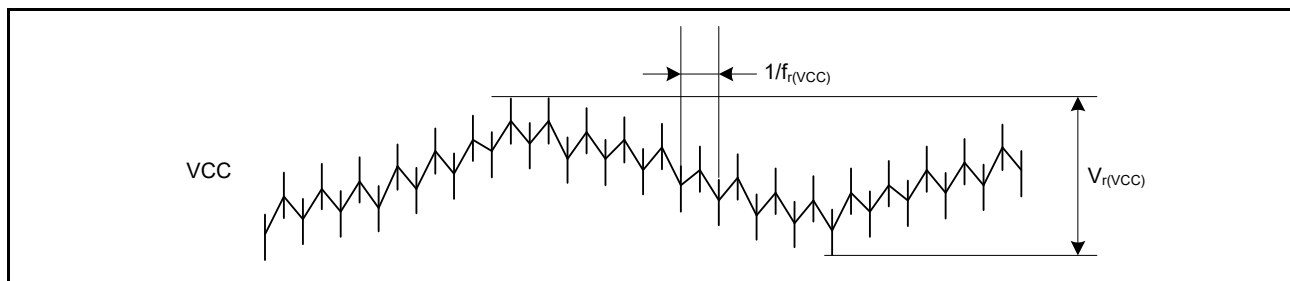


Figure 2.25 Ripple waveform

2.3 AC Characteristics

2.3.1 Frequency

Table 2.17 Operation frequency value in high-speed operating mode

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	48	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	24	
		2.4 to 2.7 V		-	-	16	
	EBCLK pin output	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	8	

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of FCLK must be $\pm 3.5\%$ while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.
- Note 5. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.22, Clock timing](#).

Table 2.18 Operation frequency value in Middle-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	12	MHz
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	12	
		2.4 to 2.7 V		0.032768	-	12	
		1.8 to 2.4 V		0.032768	-	8	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	12	
		1.8 to 2.4 V		-	-	8	
	EBCLK pin output	2.7 to 3.6 V		-	-	12	
		2.4 to 2.7 V		-	-	8	
		1.8 to 2.4 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be $\pm 3.5\%$ while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.22, Clock timing](#).

Table 2.19 Operation frequency value in Low-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max*4	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	0.032768	-	1	MHz
		FlashIF clock (FCLK)*1, *3		1.8 to 5.5 V	0.032768	-	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	1	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	1	
	External bus clock (BCLK)*3	1.8 to 5.5 V		-	-	1	
	EBCLK pin output	1.8 to 5.5 V		-	-	1	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory.

Note 2. The lower-limit frequency of PCLKC is 1 MHz when the A/D converter is in use.

- Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.
- Note 4. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.22, Clock timing](#).

Table 2.20 Operation frequency value in low-voltage mode

Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1, *2, *4	1.6 to 5.5 V		0.032768	-	4	
	Peripheral module clock (PCLKA)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKC)*3, *4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*4	1.6 to 5.5 V		-	-	4	
	External bus clock (BCLK)*4	1.6 to 5.5 V		-	-	4	
	EBCLK pin output	1.8 to 5.5 V		-	-	4	
1.6 to 1.8 V		-	-	2			

- Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
- Note 2. The frequency accuracy of FCLK must be $\pm 3.5\%$ while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
- Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
- Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.
- Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see [Table 2.22, Clock timing](#).

Table 2.21 Operation frequency value in Subosc-speed mode

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1, *3	1.8 to 5.5 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	37.6832	
	External bus clock (BCLK)*3	1.8 to 5.5 V		-	-	37.6832	
	EBCLK pin output	1.8 to 5.5 V		-	-	37.6832	

- Note 1. Programming and erasing the flash memory is not possible.
- Note 2. The 14-bit A/D converter cannot be used.
- Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

2.3.2 Clock Timing

Table 2.22 Clock timing (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
EBCLK pin output cycle time	VCC = 2.7 V or above	t_{Bcyc}	83.3	-	-	ns	Figure 2.26
	VCC = 1.8 V or above		125	-	-		
	VCC = 1.6 V or above		500	-	-		
EBCLK pin output high pulse width	VCC = 2.7 V or above	t_{CH}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output low pulse width	VCC = 2.7 V or above	t_{CL}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EBCLK pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EXTAL external clock input cycle time	t_{Xcyc}	50	-	-	ns	Figure 2.27	
EXTAL external clock input high pulse width	t_{XH}	20	-	-	ns		
EXTAL external clock input low pulse width	t_{XL}	20	-	-	ns		
EXTAL external clock rising time	t_{Xr}	-	-	5	ns		
EXTAL external clock falling time	t_{Xf}	-	-	5	ns		
EXTAL external clock input wait time*1	t_{EXWT}	0.3	-	-	μ s	-	
EXTAL external clock input frequency	f_{EXTAL}	-	-	20	MHz	$2.4 \leq VCC \leq 5.5$	
		-	-	8		$1.8 \leq VCC < 2.4$	
		-	-	1		$1.6 \leq VCC < 1.8$	
Main clock oscillator oscillation frequency	f_{MAIN}	1	-	20	MHz	$2.4 \leq VCC \leq 5.5$	
		1	-	8		$1.8 \leq VCC < 2.4$	
		1	-	4		$1.6 \leq VCC < 1.8$	
Main clock oscillation stabilization wait time (crystal)*9	$t_{MAINOSCWT}$	-	-	-*9	ms		
LOCO clock oscillation frequency	f_{LOCO}	27.8528	32.768	37.6832	kHz	-	
LOCO clock oscillation stabilization time	t_{LOCO}	-	-	100	μ s	Figure 2.28	
IWDT-dedicated clock oscillation frequency	f_{ILOCO}	12.75	15	17.25	kHz	-	
MOCO clock oscillation frequency	f_{MOCO}	6.8	8	9.2	MHz	-	
MOCO clock oscillation stabilization time	t_{MOCO}	-	-	1	μ s	-	

Table 2.22 Clock timing (2 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions		
HOCO clock oscillation frequency	$f_{\text{HOCO}24}$	23.64	24	24.36	MHz	Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5		
		22.68	24	25.32		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8		
		23.76	24	24.24		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5		
		23.52	24	24.48		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5		
	$f_{\text{HOCO}32}$	31.52	32	32.48		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5		
		30.24	32	33.76		Ta = -40 to 85°C 1.6 ≤ VCC < 1.8		
		31.68	32	32.32		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5		
		31.36	32	32.64		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5		
	$f_{\text{HOCO}48}^{*4}$	47.28	48	48.72		Ta = -40 to -20°C 1.8 ≤ VCC ≤ 5.5		
		47.52	48	48.48		Ta = -20 to 85°C 1.8 ≤ VCC ≤ 5.5		
		47.04	48	48.96		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5		
	$f_{\text{HOCO}64}^{*5}$	63.04	64	64.96		Ta = -40 to -20°C 2.4 ≤ VCC ≤ 5.5		
		63.36	64	64.64		Ta = -20 to 85°C 2.4 ≤ VCC ≤ 5.5		
		62.72	64	65.28		Ta = 85 to 105°C 2.4 ≤ VCC ≤ 5.5		
	HOCO clock oscillation stabilization time ^{*6, *7}	Except low-voltage mode	$t_{\text{HOCO}24}$	-		-	μs	Figure 2.29
			$t_{\text{HOCO}32}$	-		-		
$t_{\text{HOCO}48}$			-	-				
$t_{\text{HOCO}64}$			-	-				
Low-Voltage mode		$t_{\text{HOCO}24}$	-	-				
		$t_{\text{HOCO}32}$	-	-				
		$t_{\text{HOCO}48}$	-	-				
		$t_{\text{HOCO}64}$	-	-				
PLL input frequency ^{*2}	f_{PLLIN}	4	-	12.5	MHz	-		
PLL circuit oscillation frequency ^{*2}	f_{PLL}	24	-	64	MHz	-		
PLL clock oscillation stabilization time ^{*8}	t_{PLL}	-	-	55.5	μs	Figure 2.31		
PLL free-running oscillation frequency	f_{PLLFR}	-	8	-	MHz	-		
Sub-clock oscillator oscillation frequency	f_{SUB}	-	32.768	-	kHz	-		
Sub-clock oscillation stabilization time ^{*3}	t_{SUBOSC}	-	-	- ^{*3}	s	Figure 2.32		

Note 1. Time until the clock can be used after the Main Clock Oscillator Stop bit (MOSCCR.MOSTP) is set to 0 (operating) when the external clock is stable.

Note 2. The VCC range that the PLL can be used is 2.4 to 5.5 V.

Note 3. After changing the setting of the SOSCCR.SOSTP bit so that the sub-clock oscillator operates, only start using the sub-clock oscillator after the sub-clock oscillation stabilization wait time elapses, that is greater than or equal to the value recommended by the oscillator manufacturer.

Note 4. The 48-MHz HOCO can be used within a VCC range of 1.8 V to 5.5 V.

Note 5. The 64-MHz HOCO can be used within a VCC range of 2.4 V to 5.5 V.

Note 6. This is a characteristic when HOCOCCR.HCSTP bit is set to 0 (oscillation) in MOCO stop state.

When HOCOCCR.HCSTP bit is set to 0 (oscillation) during MOCO oscillation, this specification is shortened by 1 μs.

Note 7. Whether stabilization time has elapsed can be confirmed by OCSF.HOCOSF.

Note 8. This is a characteristic when PLLCR.PLLSTP bit is set to 0 (operation) in MOCO stop state.

When PLLCR.PLLSTP bit is set to 0 (operation) during MOCO oscillation, this specification is shortened by 1 μs.

Note 9. When setting up the main clock, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended stabilization time. After changing the setting of the MOSCCR.MOSTP bit so that the main clock oscillator operates, read the OCSF.MOSCSF flag to confirm that it is 1, then start using the main clock.

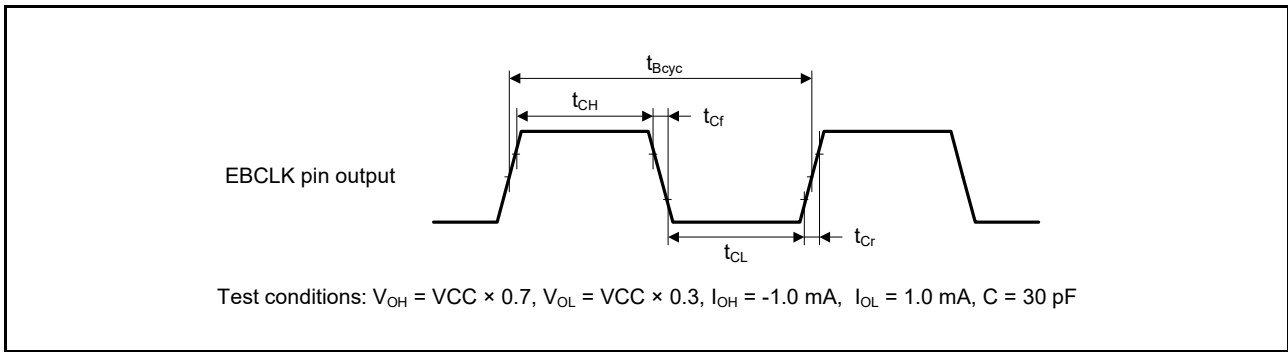


Figure 2.26 EBCLK pin output timing

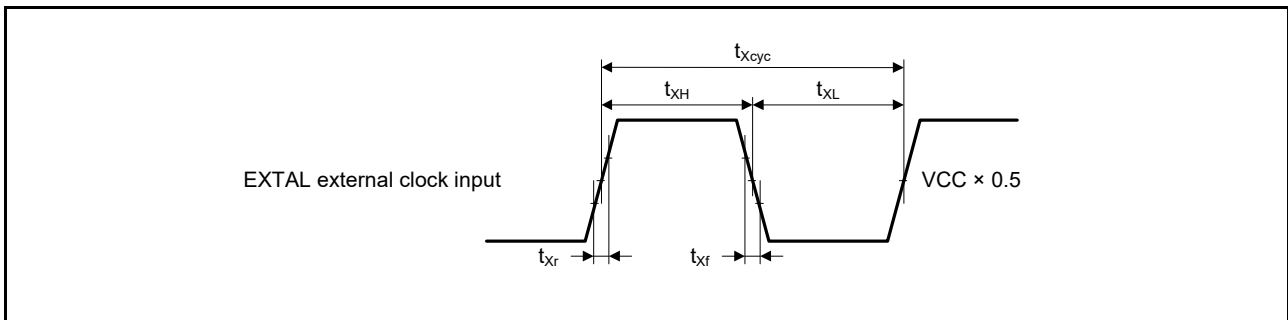


Figure 2.27 EXTAL external clock input timing

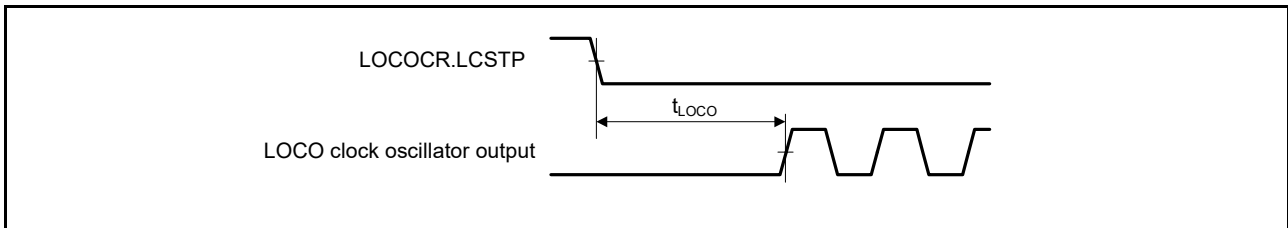


Figure 2.28 LOCO clock oscillation start timing

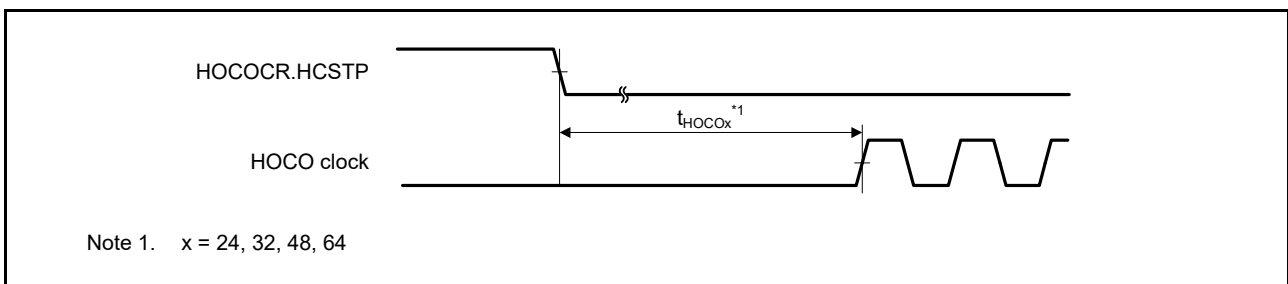


Figure 2.29 HOCO clock oscillation start timing (started by setting HOCOOCR.HCSTP bit)

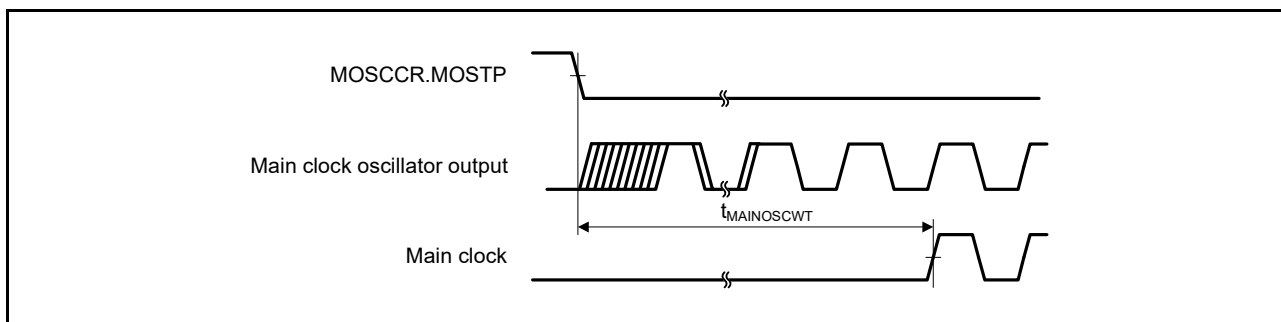


Figure 2.30 Main clock oscillation start timing

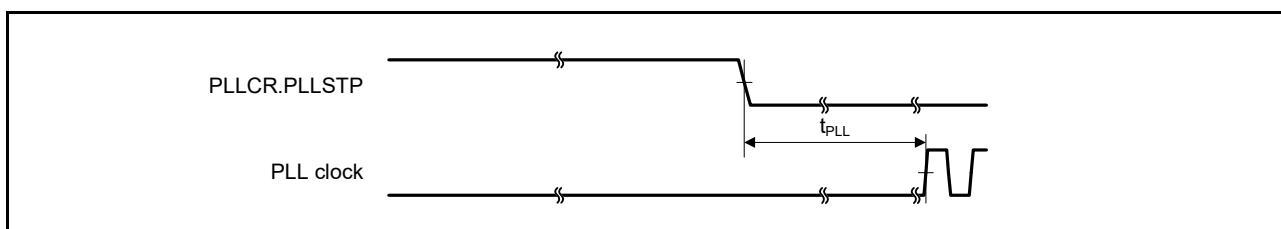


Figure 2.31 PLL clock oscillation start timing (PLL is operated after main clock oscillation has settled)

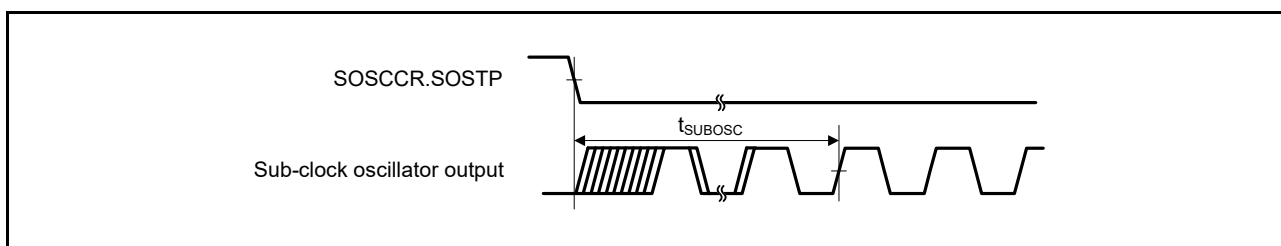


Figure 2.32 Sub-clock oscillation start timing

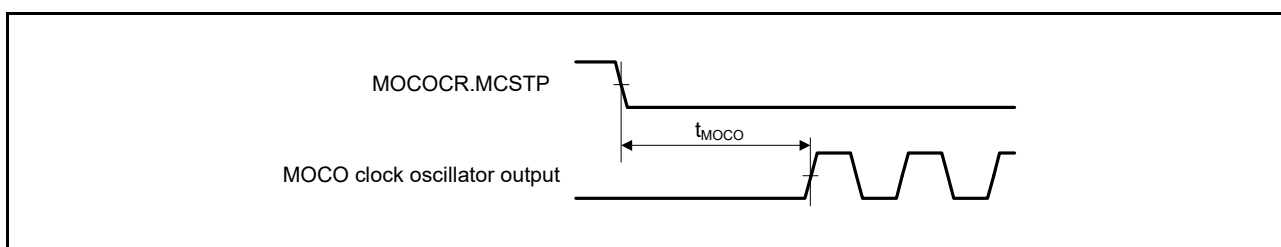


Figure 2.33 MOCO clock oscillation start timing

2.3.3 Reset Timing

Table 2.23 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 2.34
	Other than above	t_{RESW}	30	-	-	μ s	Figure 2.35
Wait time after RES cancellation (at power-on)	LVD0: enable*1	t_{RESWT}	-	0.7	-	ms	Figure 2.34
	LVD0: disable*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0: enable*1	t_{RESWT2}	-	0.5	-	ms	Figure 2.35
	LVD0: disable*2		-	0.05	-		
Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, Stack pointer error reset, Software reset)	LVD0: enable*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0: disable*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

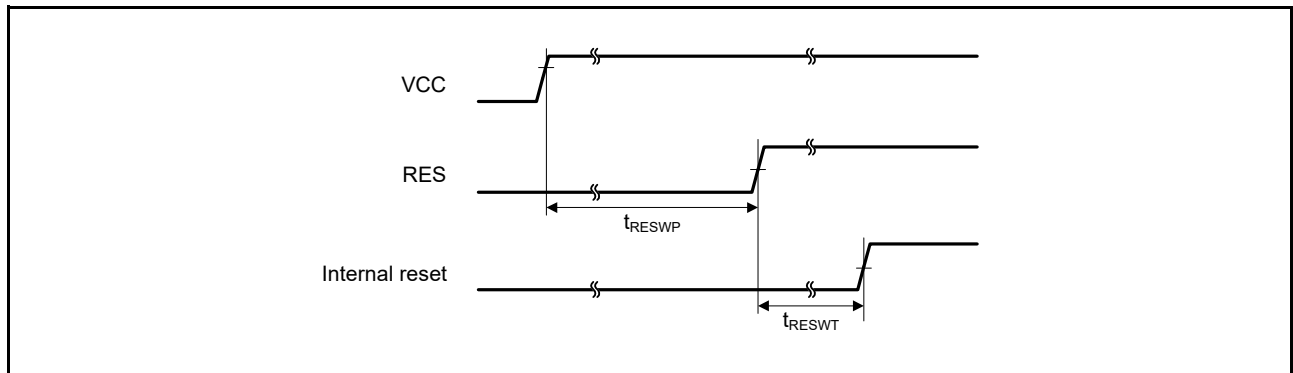


Figure 2.34 Reset input timing at power-on

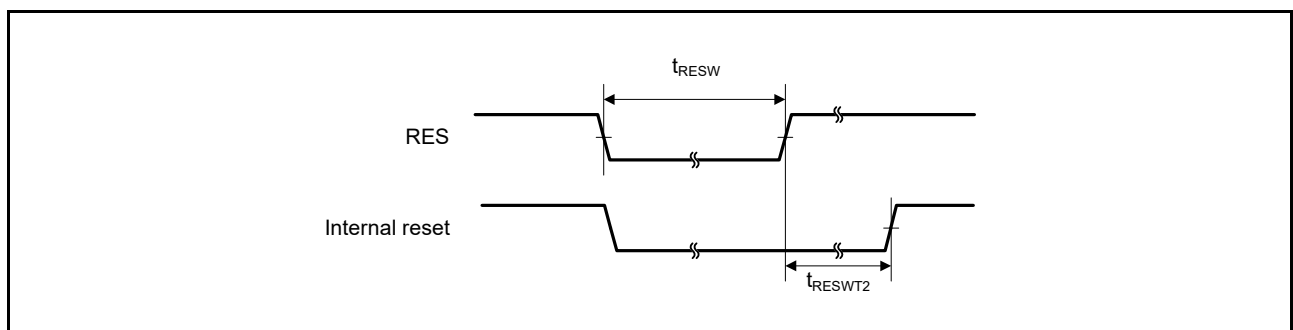


Figure 2.35 Reset input timing (1)

2.3.4 Wakeup Time

Table 2.24 Timing of recovery from low power modes (1)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions	
Recovery time from Software Standby mode*1	High-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (20 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.36	
			System clock source is PLL (48 MHz) with Main clock oscillator*2	t _{SBYPC}	-	2	3	ms		
		External clock input to main clock oscillator	System clock source is main clock oscillator (20 MHz)*3	t _{SBYEX}	-	14	25	μs		
			System clock source is PLL (48 MHz) with Main clock oscillator*3	t _{SBYPE}	-	53	76	μs		
		System clock source is HOCO*4 (HOCO clock is 32 MHz)			t _{SBYHO}	-	43	52		μs
		System clock source is HOCO*4 (HOCO clock is 48 MHz)			t _{SBYHO}	-	44	52		μs
		System clock source is HOCO*5 (HOCO clock is 64 MHz)			t _{SBYHO}	-	82	110		μs
		System clock source is MOCO			t _{SBYMO}	-	16	25		μs

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Note 4. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 05h.

Note 5. The HOCO Clock Wait Control Register (HOCOWTCR) is set to 06h.

Table 2.25 Timing of recovery from low power modes (2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions	
Recovery time from Software Standby mode*1	Middle-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (12 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.36	
			System clock source is PLL (24 MHz) with main clock oscillator*2	t _{SBYPC}	-	2	3	ms		
		External clock input to main clock oscillator	System clock source is main clock oscillator (12 MHz)*3	t _{SBYEX}	-	2.9	10	μs		
			System clock source is PLL (24 MHz) with main clock oscillator*3	t _{SBYPE}	-	49	76	μs		
		System clock source is HOCO (24 MHz)			t _{SBYHO}	-	38	50		μs
		System clock source is MOCO			t _{SBYMO}	-	3.5	5.5		μs

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.26 Timing of recovery from low power modes (3)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-speed mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (1 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.36
		External clock input to main clock oscillator	System clock source is main clock oscillator (1 MHz)*3	t _{SBYEX}	-	28	50	μs	
		System clock source is MOCO		t _{SBYMO}	-	25	35	μs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.27 Timing of recovery from low power modes (4)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Low-voltage mode	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator (4 MHz)*2	t _{SBYMC}	-	2	3	ms	Figure 2.36
		External clock input to main clock oscillator	System clock source is main clock oscillator (4 MHz)*3	t _{SBYEX}	-	108	130	μs	
		System clock source is HOCO		t _{SBYHO}	-	108	130	μs	

Note 1. The division ratio of ICK, BCK, FCK, and PCKx is the minimum division ratio within the allowable frequency range. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined by the following expression.

Note 2. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h.

Note 3. The Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 00h.

Table 2.28 Timing of recovery from low power modes (5)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Subosc-speed mode	System clock source is sub-clock oscillator (32.768 kHz)	t _{SBYSC}	-	0.85	1	ms	Figure 2.36
		System clock source is LOCO (32.768 kHz)	t _{SBYLO}	-	0.85	1.2	ms	

Note 1. The sub-clock oscillator or LOCO itself continues to oscillate in Software Standby mode during Subosc-speed mode.

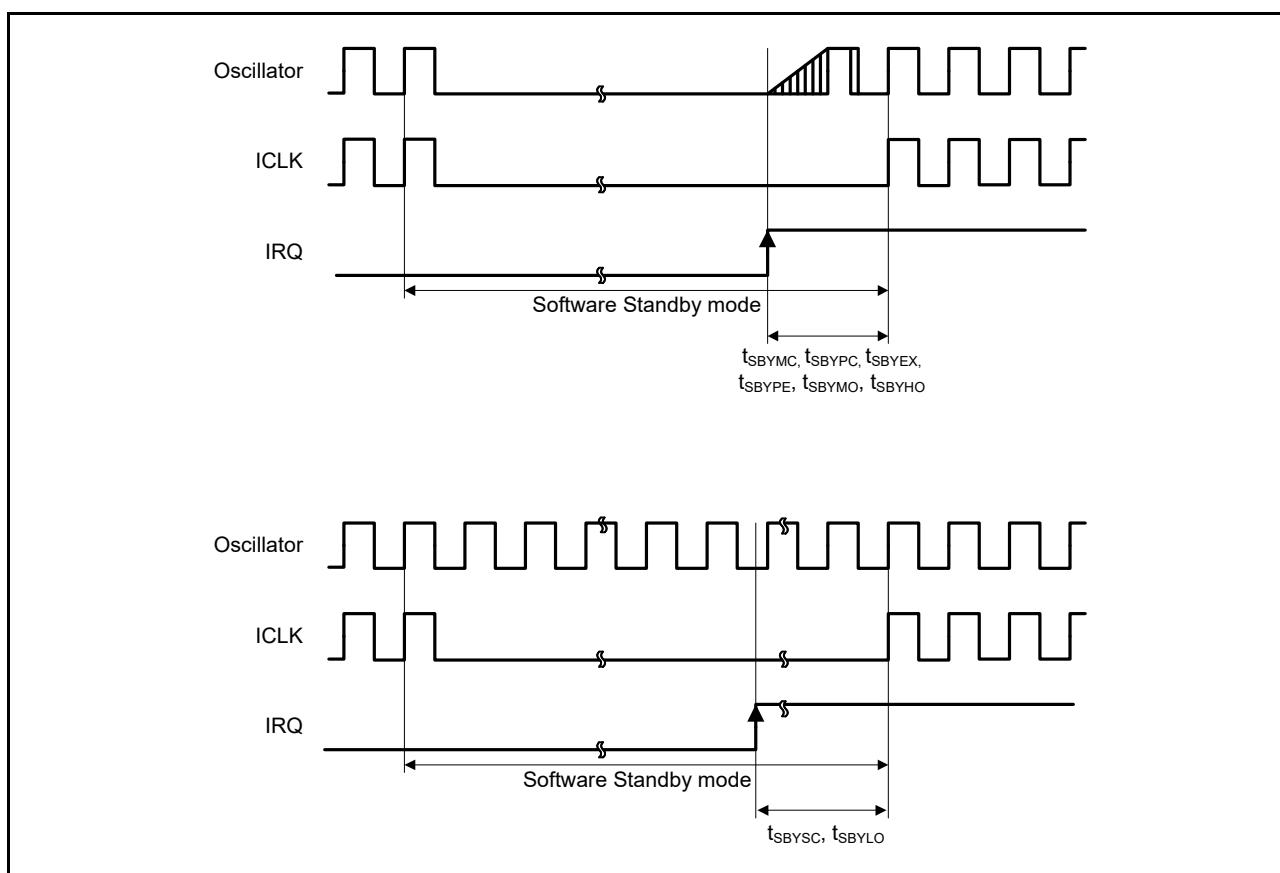


Figure 2.36 Software Standby mode cancellation timing

Table 2.29 Timing of recovery from low power modes (6)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Recovery time from Software Standby mode to Snooze mode	High-speed mode System clock source is HOCO	t_{SNZ}	-	36	45	μs	Figure 2.37
	Middle-speed mode System clock source is MOCO	t_{SNZ}	-	1.3	3.6	μs	
	Low-speed mode System clock source is MOCO	t_{SNZ}	-	10	13	μs	
	Low-voltage mode System clock source is HOCO	t_{SNZ}	-	87	110	μs	

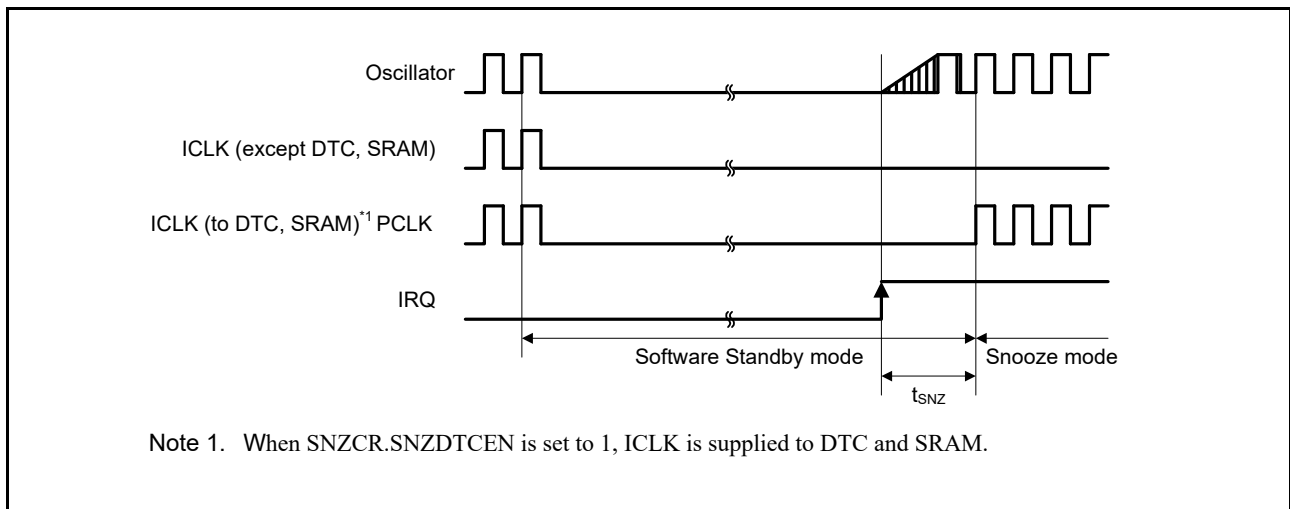


Figure 2.37 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.30 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{\text{Pcyc}} \times 2 \leq 200$ ns
		$t_{\text{Pcyc}} \times 2^{*1}$	-	-			$t_{\text{Pcyc}} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{\text{NMICK}} \times 3 \leq 200$ ns
		$t_{\text{NMICK}} \times 3.5^{*2}$	-	-			$t_{\text{NMICK}} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{\text{Pcyc}} \times 2 \leq 200$ ns
		$t_{\text{Pcyc}} \times 2^{*1}$	-	-			$t_{\text{Pcyc}} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{\text{IRQCK}} \times 3 \leq 200$ ns
		$t_{\text{IRQCK}} \times 3.5^{*3}$	-	-			$t_{\text{IRQCK}} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.

Note 1. t_{Pcyc} indicates the cycle of PCLKB.

Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.

Note 3. t_{IRQCK} indicates the cycle of the IRQ_i digital filter sampling clock (i = 0 to 15).

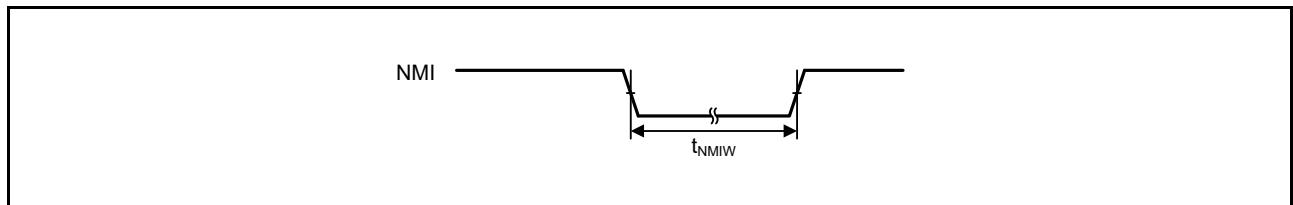


Figure 2.38 NMI interrupt input timing

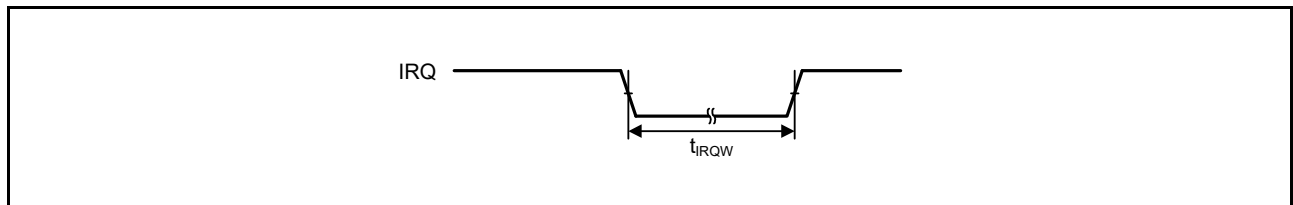


Figure 2.39 IRQ interrupt input timing

2.3.6 Bus Timing

Table 2.31 Bus timing (1)

Conditions: Low drive output is selected in the Port Drive Capability in PmnPFS register

VCC = 2.7 to 5.5 V

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $C = 30$ pF

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.42 to Figure 2.45
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
ALE delay time	t_{ALED}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	37	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	37	-	ns	Figure 2.46
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.32 Bus timing (2)

Conditions: Low drive output is selected in the Port Drive Capability in PmnPFS register

VCC = 2.4 to 2.7 V

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, $C = 30$ pF

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	55	ns	Figure 2.42 to Figure 2.45
Byte control delay	t_{BCD}	-	55	ns	
CS delay	t_{CSD}	-	55	ns	
ALE delay time	t_{ALED}	-	55	ns	
RD delay	t_{RSD}	-	55	ns	
Read data setup time	t_{RDS}	45	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	55	ns	
Write data delay	t_{WDD}	-	55	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	45	-	ns	Figure 2.46
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.33 Bus timing (3)

Conditions: Low drive output is selected in the Port Drive Capability in PmnPFS register

VCC = 1.8 to 2.4 V

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, C = 30 pF

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	90	ns	Figure 2.42 to Figure 2.45
Byte control delay	t_{BCD}	-	90	ns	
CS delay	t_{CSD}	-	90	ns	
ALE delay time	t_{ALED}	-	90	ns	
RD delay	t_{RSD}	-	90	ns	
Read data setup time	t_{RDS}	70	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	90	ns	
Write data delay	t_{WDD}	-	90	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	70	-	ns	Figure 2.46
WAIT hold time	t_{WTH}	0	-	ns	

Table 2.34 Bus timing (4)

Conditions: Low drive output is selected in the Port Drive Capability in PmnPFS register

VCC = 1.6 to 1.8 V

Output load conditions: $V_{OH} = VCC \times 0.5$, $V_{OL} = VCC \times 0.5$, C = 30 pF

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	120	ns	Figure 2.42 to Figure 2.45
Byte control delay	t_{BCD}	-	120	ns	
CS delay	t_{CSD}	-	120	ns	
ALE delay time	t_{ALED}	-	120	ns	
RD delay	t_{RSD}	-	120	ns	
Read data setup time	t_{RDS}	90	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR delay	t_{WRD}	-	120	ns	
Write data delay	t_{WDD}	-	120	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	90	-	ns	Figure 2.46
WAIT hold time	t_{WTH}	0	-	ns	

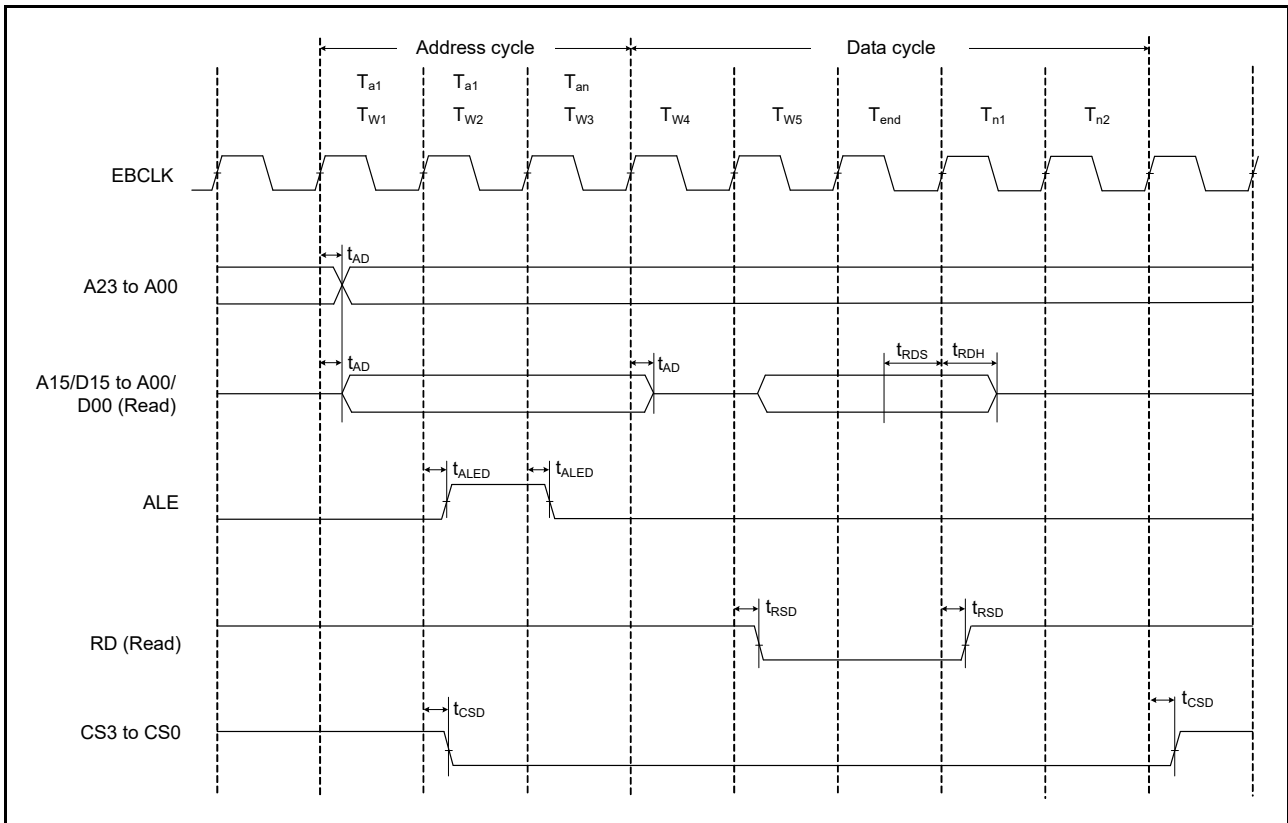


Figure 2.40 Address/data multiplexed bus read access timing

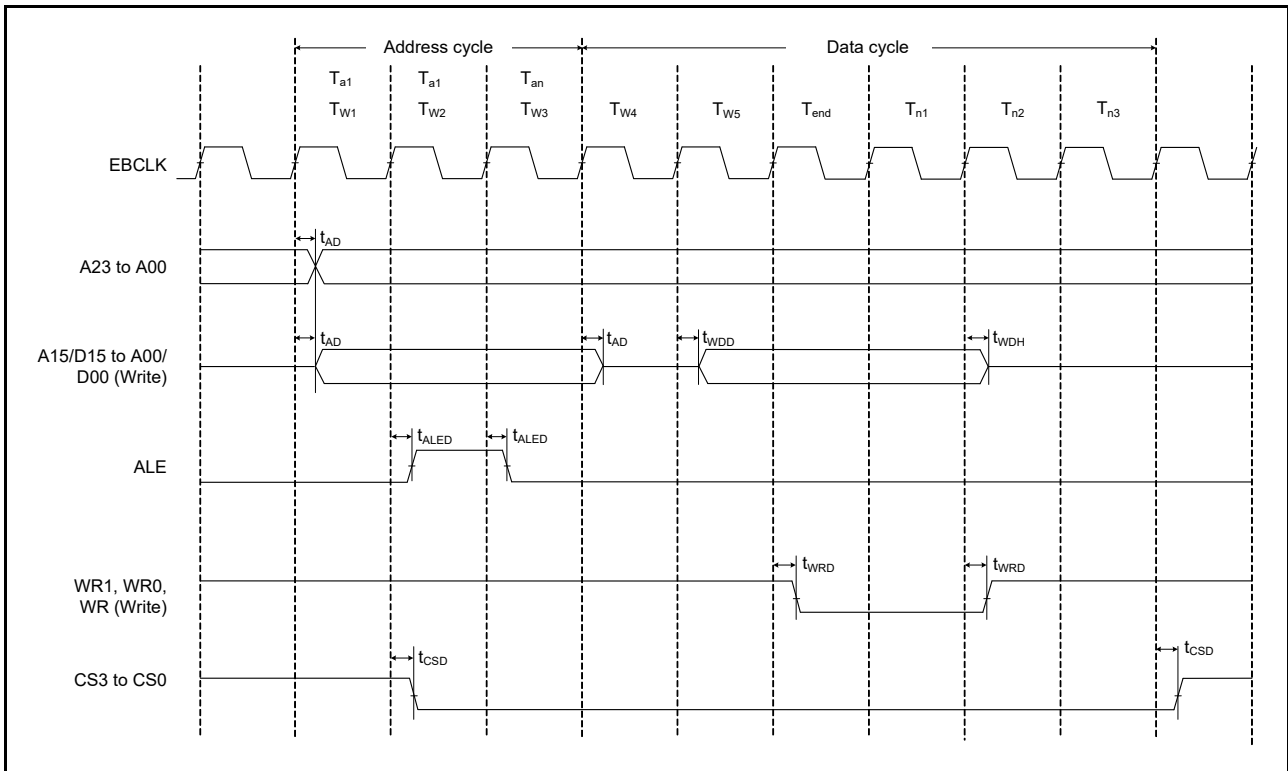


Figure 2.41 Address/data multiplexed bus write access timing

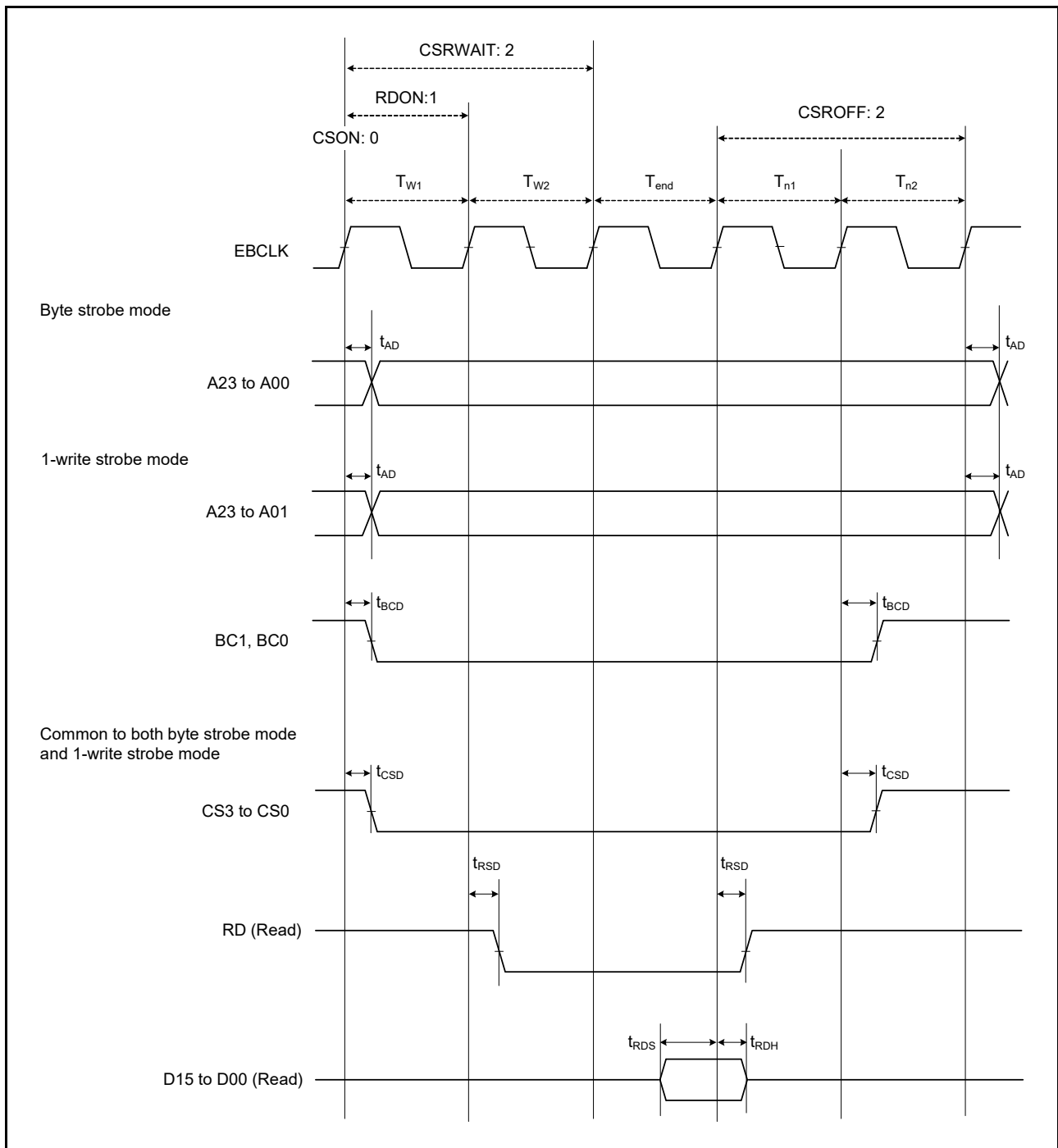


Figure 2.42 External bus timing/normal read cycle (bus clock synchronized)

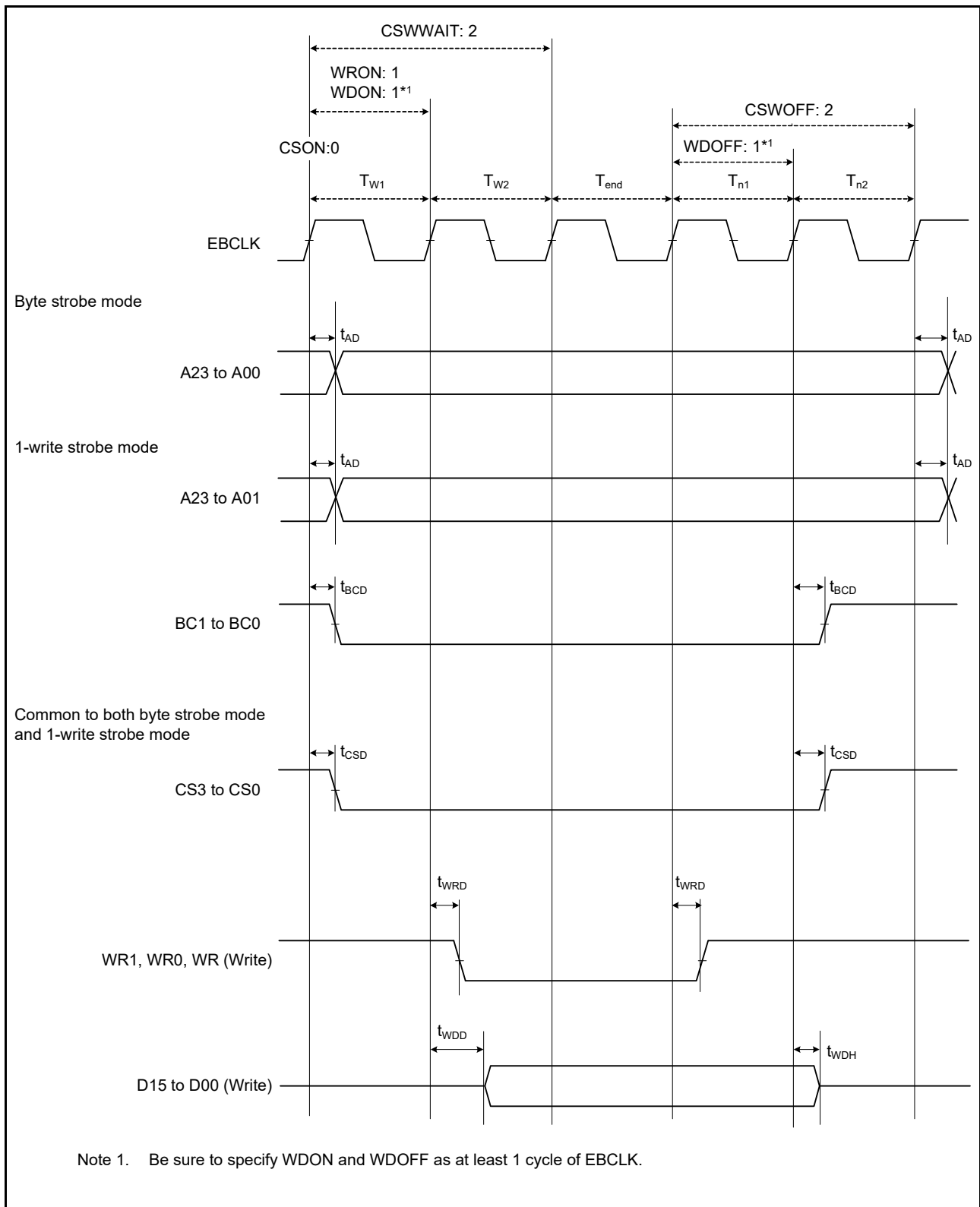


Figure 2.43 External bus timing/normal write cycle (bus clock synchronized)

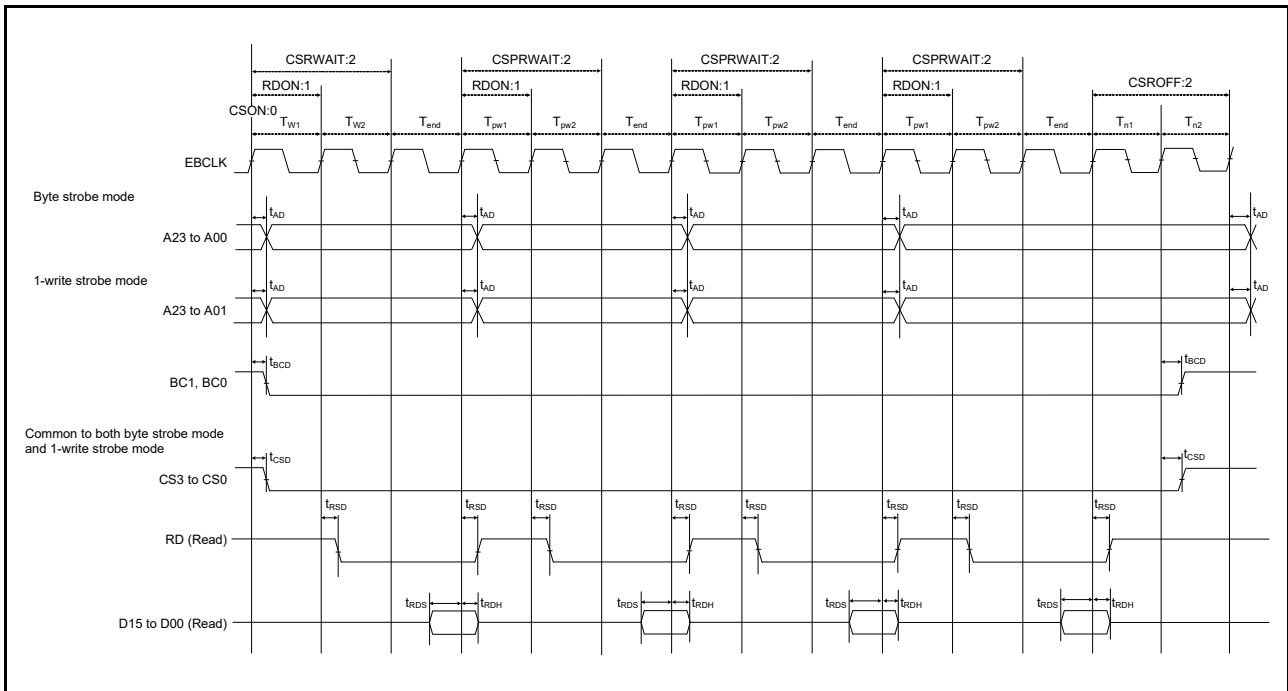
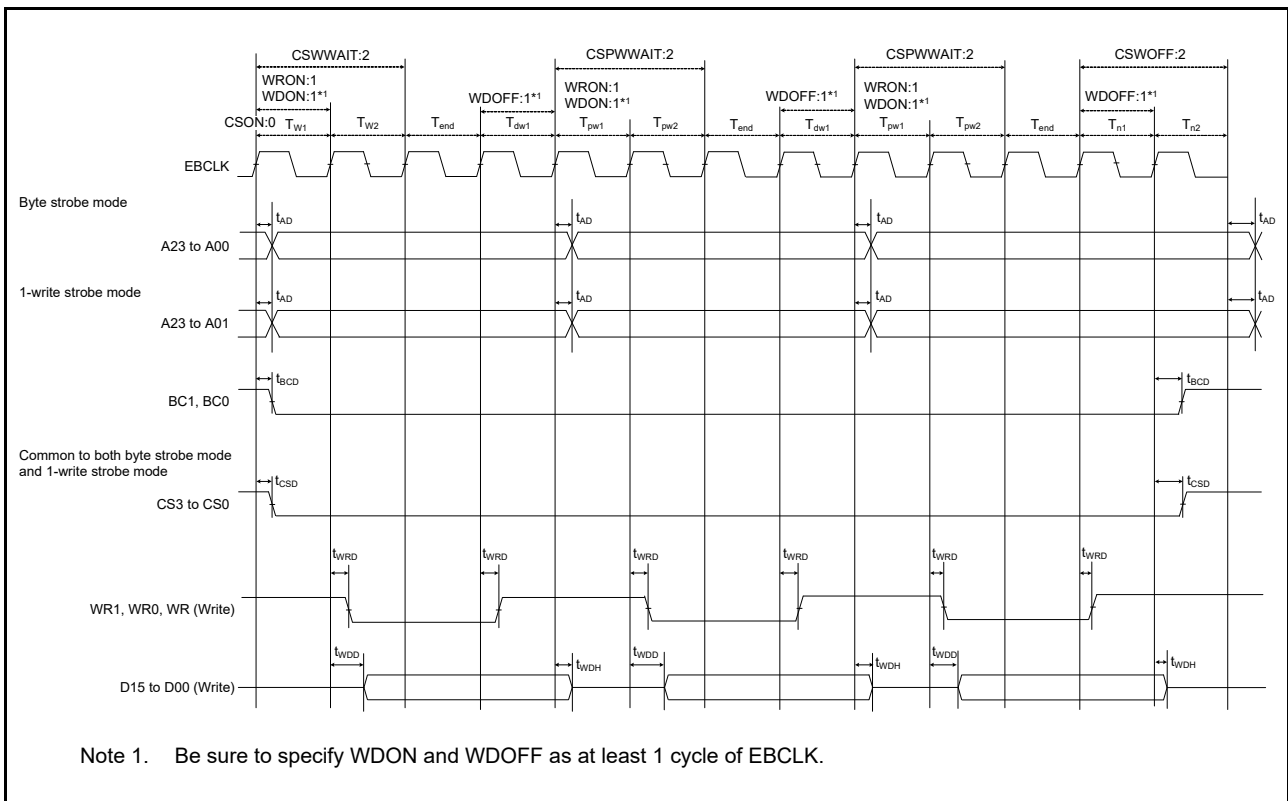


Figure 2.44 External bus timing/page read cycle (bus clock synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least 1 cycle of EBCLK.

Figure 2.45 External bus timing/page write cycle (bus clock synchronized)

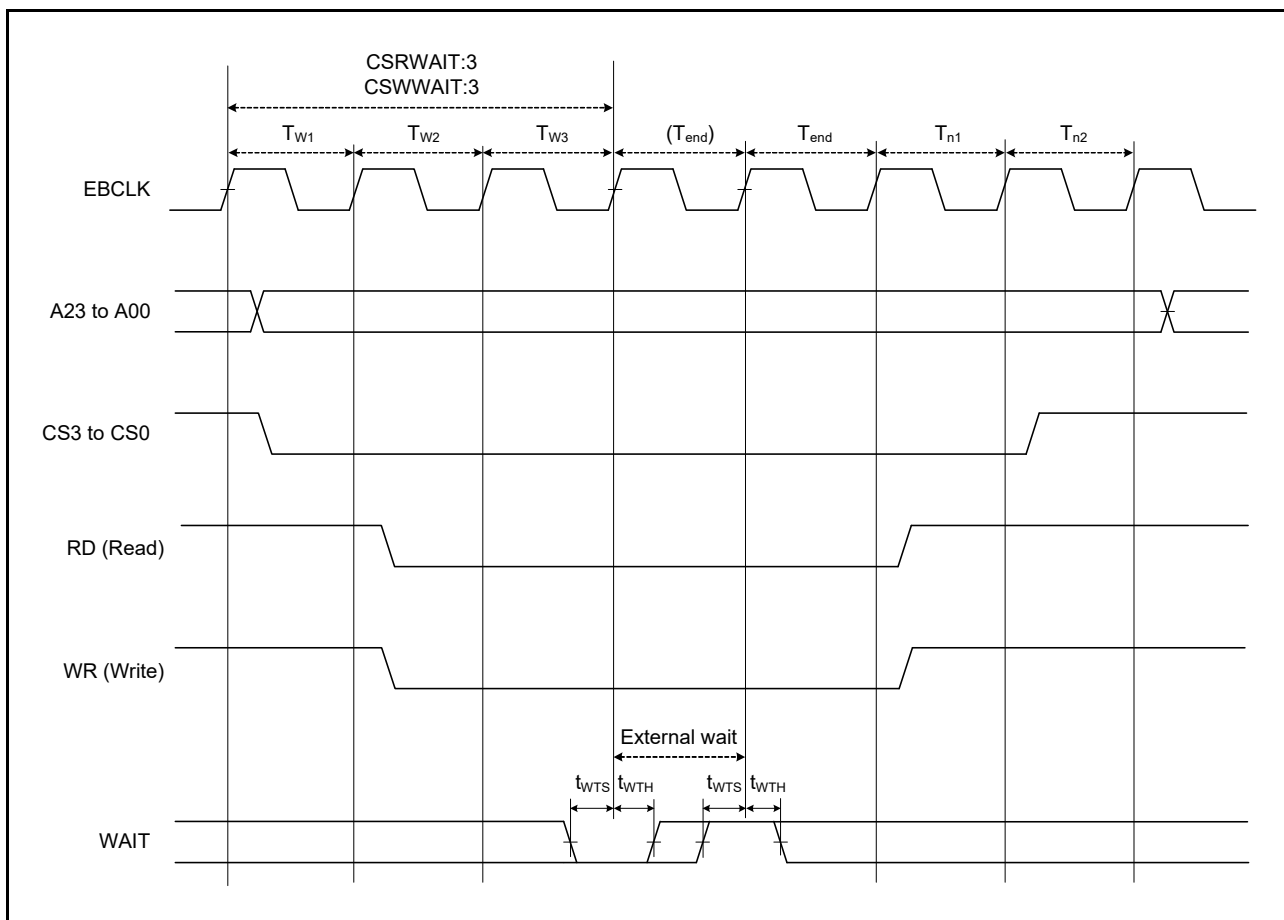


Figure 2.46 External bus timing/external wait control

2.3.7 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 Trigger Timing

Table 2.35 I/O Ports, POEG, GPT, AGT, KINT, and ADC14 trigger timing

Parameter		Symbol	Min	Max	Unit	Test conditions	
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.47	
	Input/output data cycle (P002, P003, P004, P007)	t_{POCyc}	10	-	us		
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.48	
GPT	Input capture pulse width	Single edge	t_{GTICW}	1.5	t_{PDcyc}	Figure 2.49	
		Dual edge		2.5			
AGT	AGTIO, AGTEE input cycle	$2.7\text{ V} \leq VCC \leq 5.5\text{ V}$	t_{ACYC}^{*1}	250	ns	Figure 2.50	
		$2.4\text{ V} \leq VCC < 2.7\text{ V}$		500			
		$1.8\text{ V} \leq VCC < 2.4\text{ V}$		1000			
		$1.6\text{ V} \leq VCC < 1.8\text{ V}$		2000			
	AGTIO, AGTEE input high level width, low-level width	$2.7\text{ V} \leq VCC \leq 5.5\text{ V}$	t_{ACKWH} , t_{ACKWL}	100	ns		
		$2.4\text{ V} \leq VCC < 2.7\text{ V}$		200			
		$1.8\text{ V} \leq VCC < 2.4\text{ V}$		400			
		$1.6\text{ V} \leq VCC < 1.8\text{ V}$		800			
	AGTIO, AGTO, AGTOA, AGTOB output cycle	$2.7\text{ V} \leq VCC \leq 5.5\text{ V}$	t_{ACYC2}	62.5	ns		Figure 2.50
		$2.4\text{ V} \leq VCC < 2.7\text{ V}$		125			
		$1.8\text{ V} \leq VCC < 2.4\text{ V}$		250			
		$1.6\text{ V} \leq VCC < 1.8\text{ V}$		500			
ADC14	14-bit A/D converter trigger input pulse width	t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.51	
KINT	KRn (n = 00 to 07) pulse width	t_{KR}	250	-	ns	Figure 2.52	

Note 1. Constraints on AGTIO input: $t_{Pcyc} \times 2 < t_{ACYC}$

Note: t_{Pcyc} : PCLKB cycle, t_{PDcyc} : PCLKD cycle

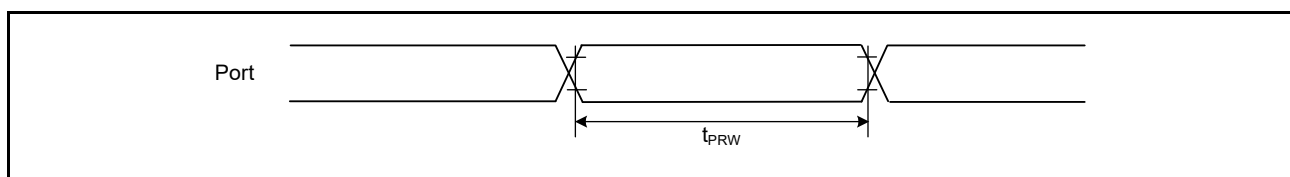


Figure 2.47 I/O ports input timing

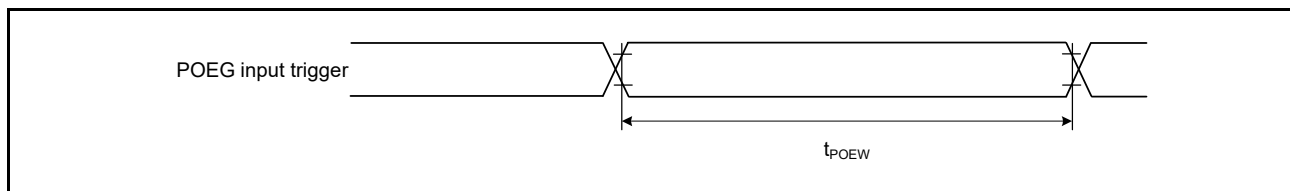


Figure 2.48 POEG input trigger timing

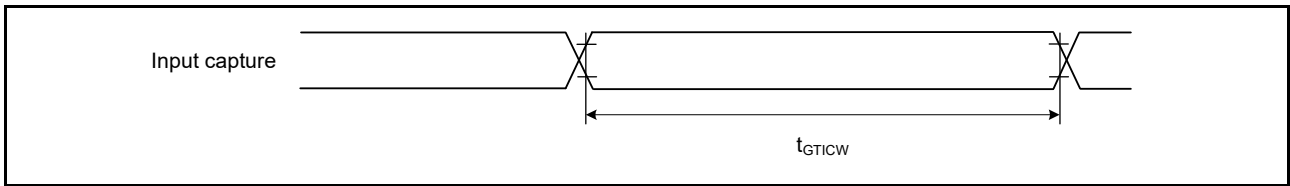


Figure 2.49 GPT input capture timing

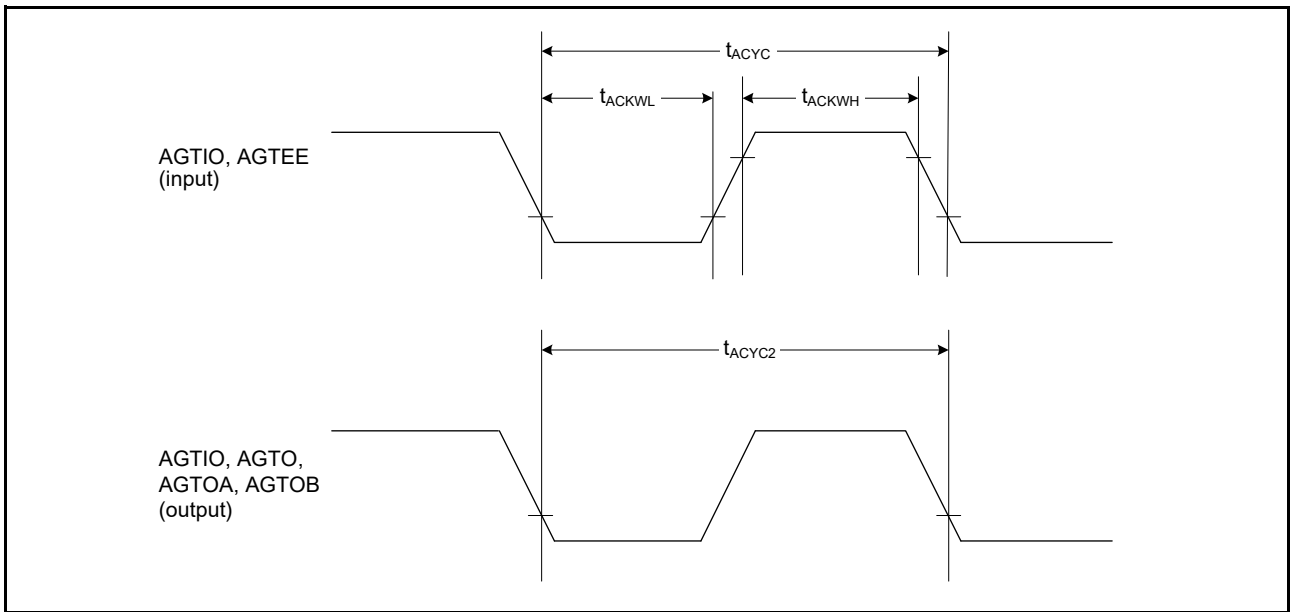


Figure 2.50 AGT I/O timing

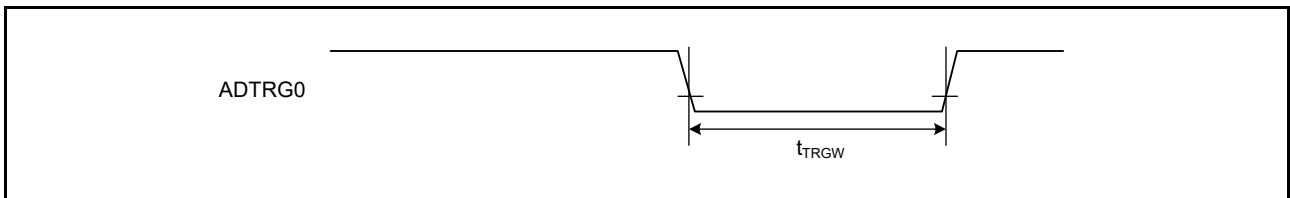


Figure 2.51 ADC14 trigger input timing

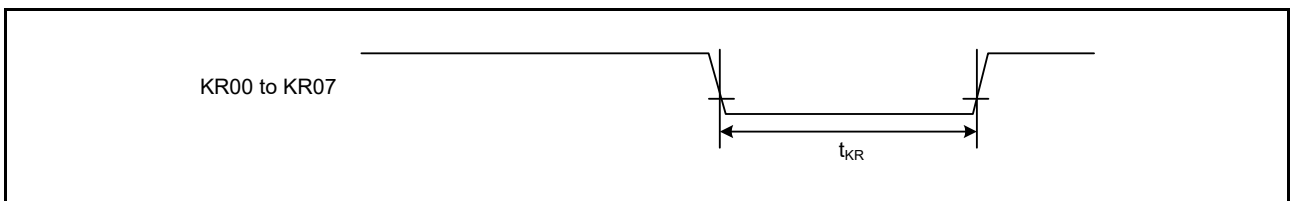


Figure 2.52 Key interrupt input timing

2.3.8 CAC Timing

Table 2.36 CAC timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc}^{*1} \leq t_{cac}^{*2}$	$4.5 \times t_{cac} + 3 \times t_{PBcyc}^{*1}$	-	-	ns	-
		$t_{PBcyc}^{*1} > t_{cac}^{*2}$	$5 \times t_{cac} + 6.5 \times t_{PBcyc}^{*1}$	-	-	ns	-

Note 1. t_{pBcyc} : PCLKB cycle.

Note 2. t_{cac} : CAC count clock source cycle.

2.3.9 SCI Timing

Table 2.37 SCI timing (1)

Parameter		Symbol	Min	Max	Unit*1	Test conditions			
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 2.53		
		Clock synchronous		6	-				
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}			
	Input clock rise time		t_{SCKr}	-	20	ns			
	Input clock fall time		t_{SCKf}	-	20	ns			
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}			
		Clock synchronous		4	-				
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}			
	Output clock rise time		t_{SCKr}	1.8 V or above	-	20		ns	
				1.6 V or above	-	30			
	Output clock fall time		t_{SCKf}	1.8 V or above	-	20		ns	
				1.6 V or above	-	30			
	Transmit data delay (master)	Clock synchronous	t_{TXD}	1.8 V or above	-	40		ns	Figure 2.54
				1.6 V or above	-	45			
Transmit data delay (slave)	Clock synchronous	t_{TXD}	2.7 V or above	-	55	ns			
			2.4 V or above	-	60				
			1.8 V or above	-	100				
			1.6 V or above	-	125				
Receive data setup time (master)	Clock synchronous	t_{RXS}	2.7 V or above	45	-	ns			
			2.4 V or above	55	-				
			1.8 V or above	90	-				
			1.6 V or above	110	-				
Receive data setup time (slave)	Clock synchronous	t_{RXS}	2.7 V or above	40	-	ns			
			1.6 V or above	45	-				
Receive data hold time (master)	Clock synchronous	t_{RXH}	5	-	ns				
Receive data hold time (slave)	Clock synchronous	t_{RXH}	40	-	ns				

Note 1. t_{pcyc} : PCLKA cycle.

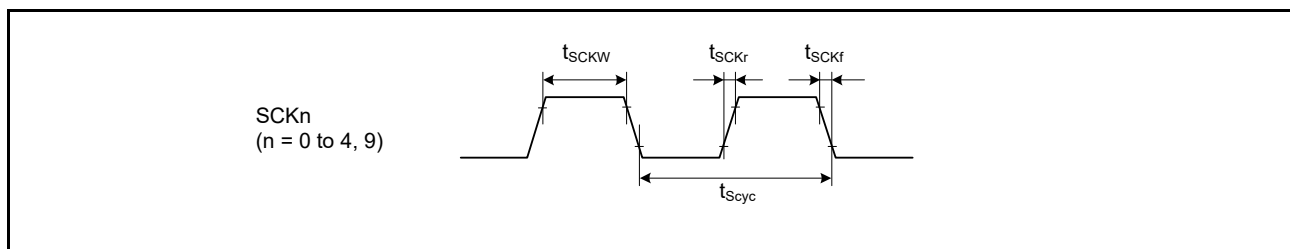


Figure 2.53 SCK clock input timing

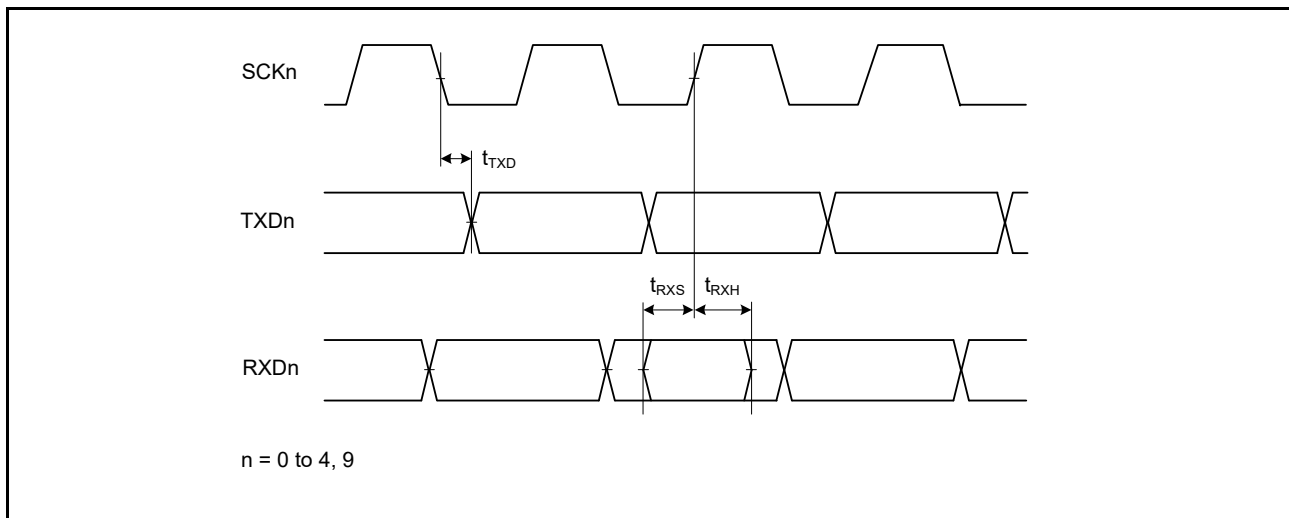


Figure 2.54 SCI input/output timing in clock synchronous mode

Table 2.38 SCI timing (2) (1 of 2)

Parameter			Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 2.55
	SCK clock cycle input (slave)			6	65536		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time		t_{SPCKr} , t_{SPCKf}	-	20	ns	
		-		30			
Data input setup time	Master	2.7 V or above	t_{SU}	45	-	ns	Figure 2.56 to Figure 2.59
		2.4 V or above		55	-		
		1.8 V or above		80	-		
		1.6 V or above		110	-		
	Slave	2.7 V or above		40	-		
		1.6 V or above		45	-		
Data input hold time	Master		t_H	33.3	-	ns	
	Slave			40	-		
SS input setup time			t_{LEAD}	1	-	t_{SPcyc}	
SS input hold time			t_{LAG}	1	-	t_{SPcyc}	
Data output delay	Master	1.8 V or above	t_{OD}	-	40	ns	
		1.6 V or above		-	50		
	Slave	2.4 V or above		-	65		
		1.8 V or above		-	100		
		1.6 V or above		-	125		
Data output hold time	Master	2.7 V or above	t_{OH}	-10	-	ns	
		2.4 V or above		-20	-		
		1.8 V or above		-30	-		
		1.6 V or above		-40	-		
	Slave				-10		-
	Data rise and fall time	Master		1.8 V or above	t_{Dr} , t_{Df}		-
1.6 V or above			-	30			
Slave		1.8 V or above	-	20			
		1.6 V or above	-	30			

Table 2.38 SCI timing (2) (2 of 2)

Parameter	Symbol	Min	Max	Unit	Test conditions
Simple SPI Slave access time	t_{SA}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	Figure 2.58 and Figure 2.59
Slave output release time	t_{REL}	-	10 (PCLKA > 32 MHz), 6 (PCLKA ≤ 32 MHz)	t_{Pcyc}	

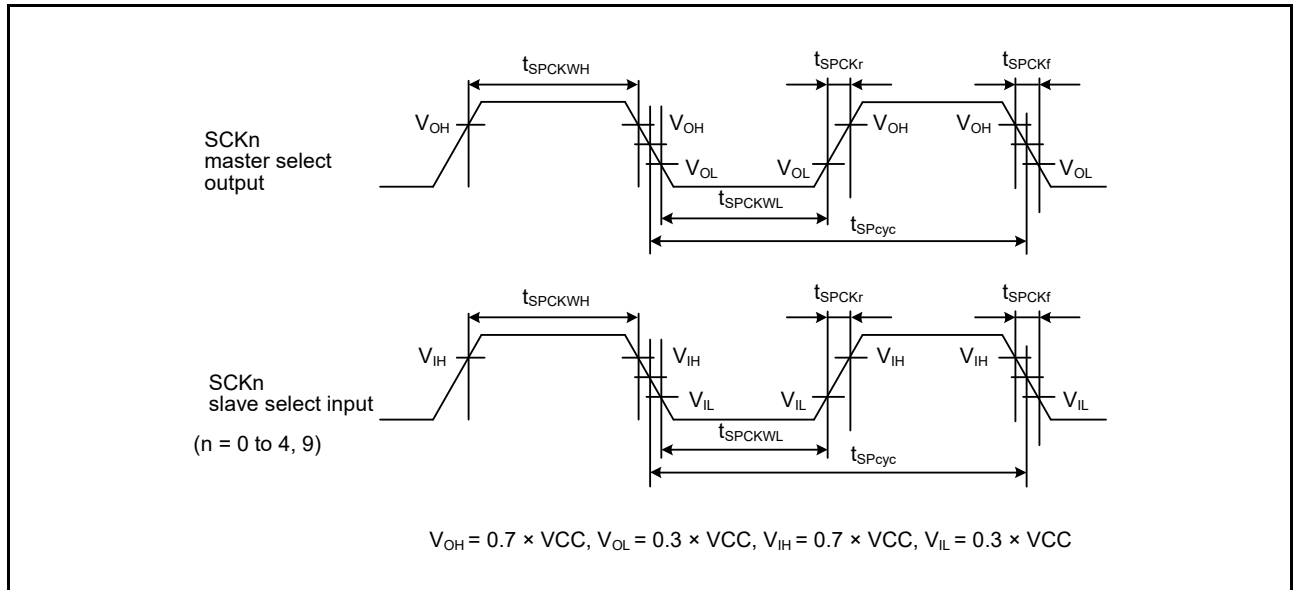


Figure 2.55 SCI simple SPI mode clock timing

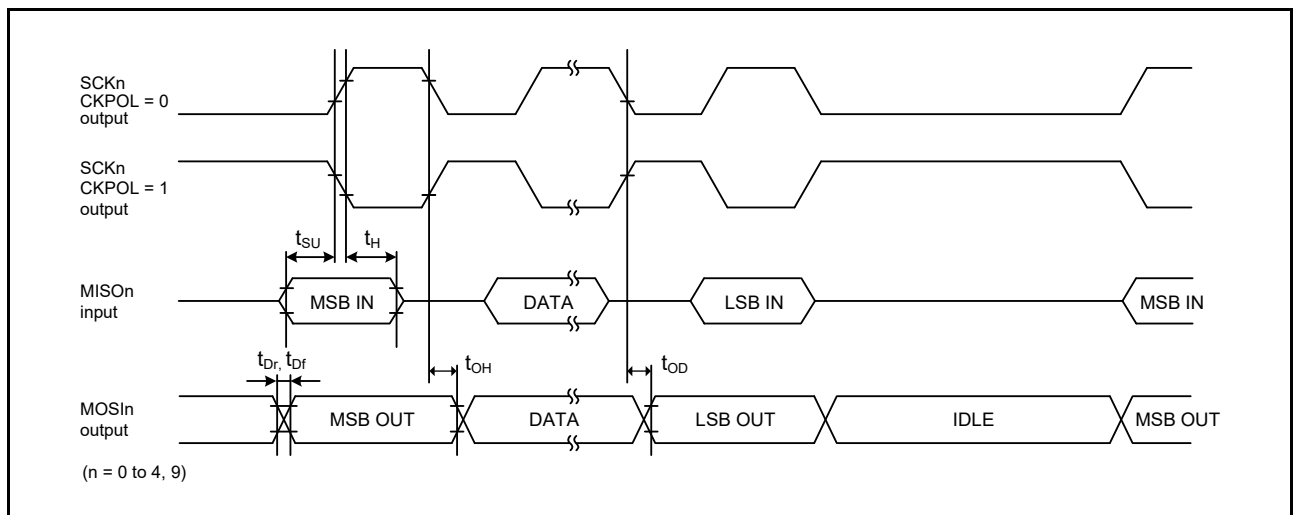


Figure 2.56 SCI simple SPI mode timing (master, CKPH = 1)

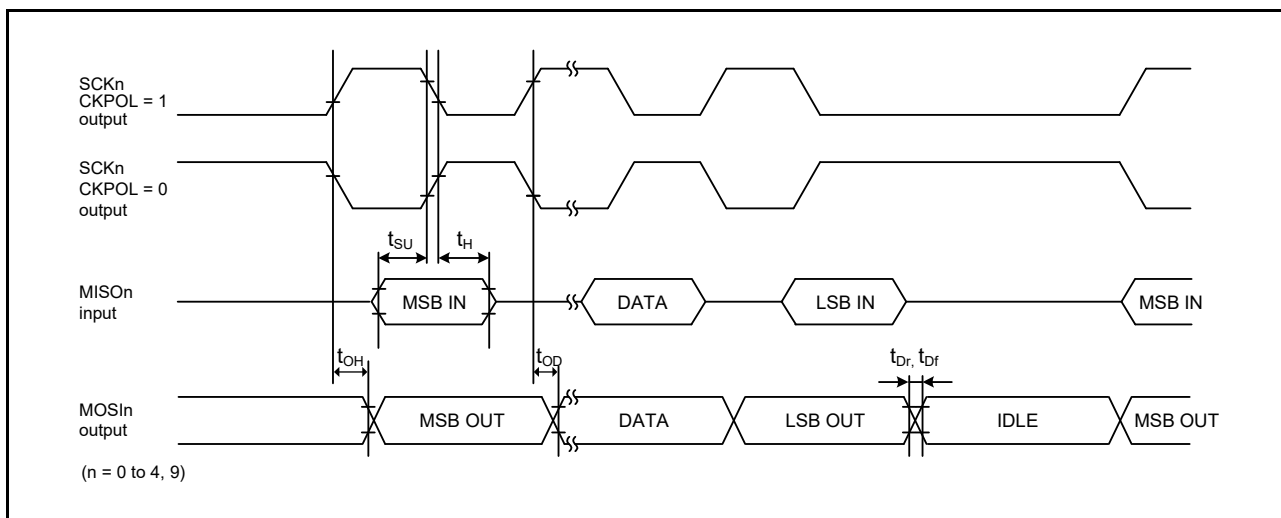


Figure 2.57 SCI simple SPI mode timing (master, CKPH = 0)

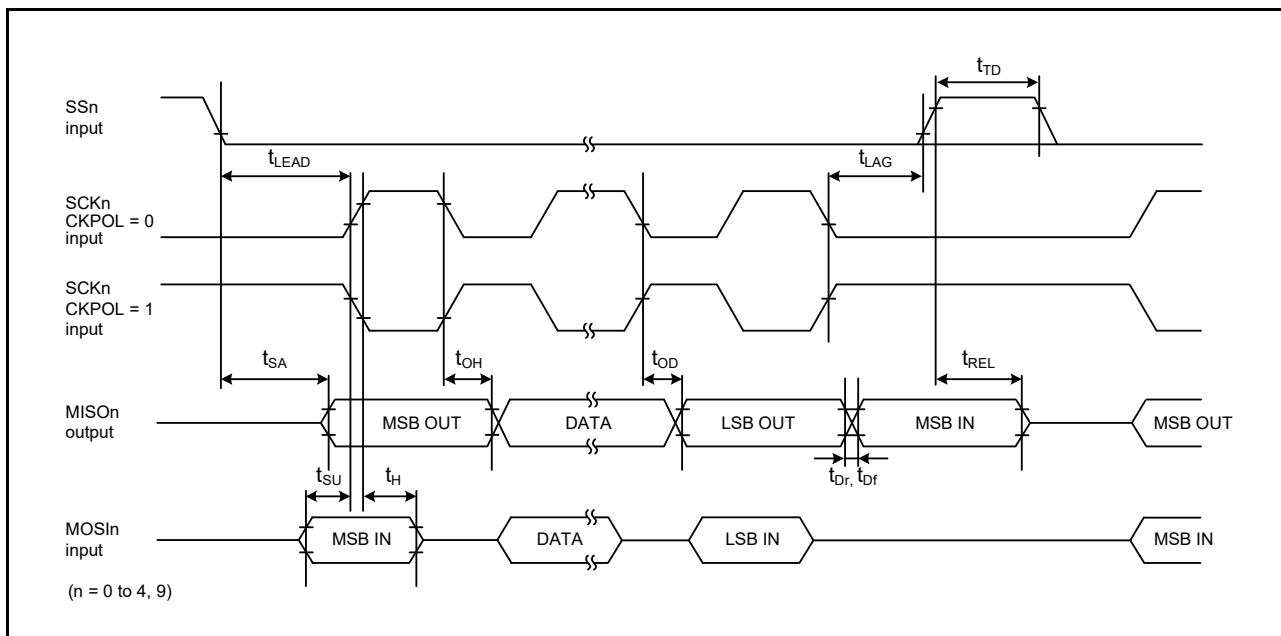


Figure 2.58 SCI simple SPI mode timing (slave, CKPH = 1)

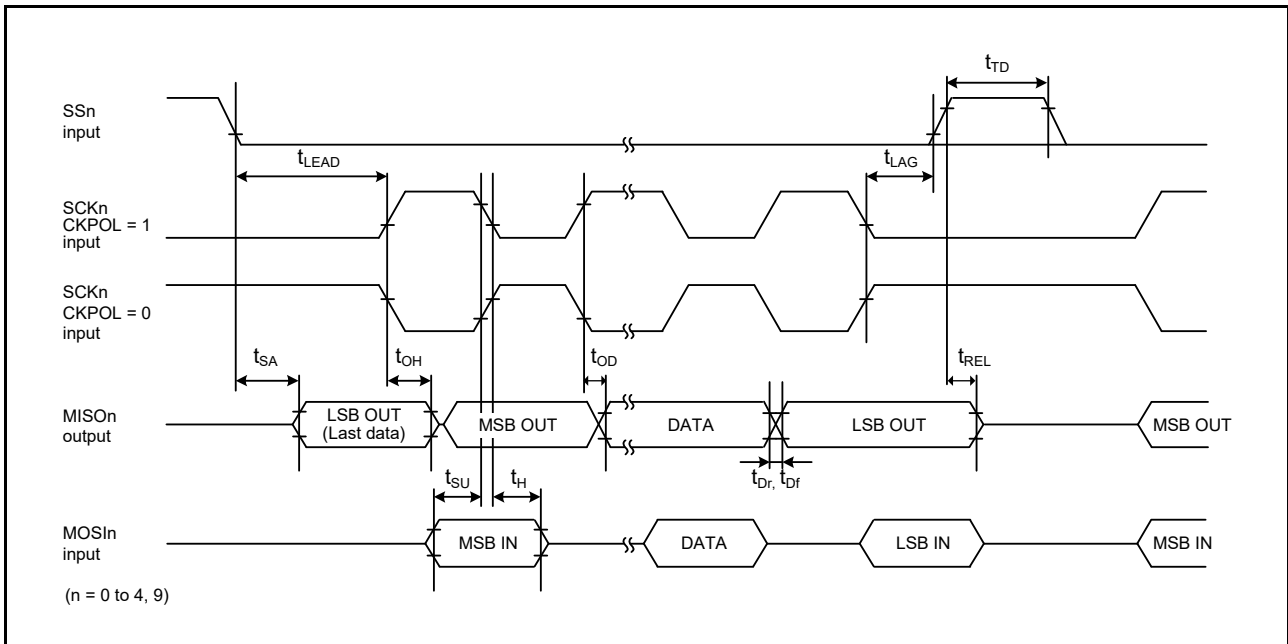


Figure 2.59 SCI simple SPI mode timing (slave, CKPH = 0)

Table 2.39 SCI timing (3)

Conditions: VCC = 2.7 to 5.5 V

Parameter	Symbol	Min	Max	Unit	Test conditions	
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.60
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICyc}^{*1}$	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*2}	-	400	pF	
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.60 For all ports except P408, use PmnPFS.DSCR of middle drive. For port P408, use PmnPFS.DSCR1 /DSCR of middle drive for IIC fast-mode.
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	$4 \times t_{IICyc}^{*1}$	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b^{*2}	-	400	pF	

Note 1. t_{IICyc} : Clock cycle selected by the SMR.CKS[1:0] bits.

Note 2. C_b indicates the total capacity of the bus line.

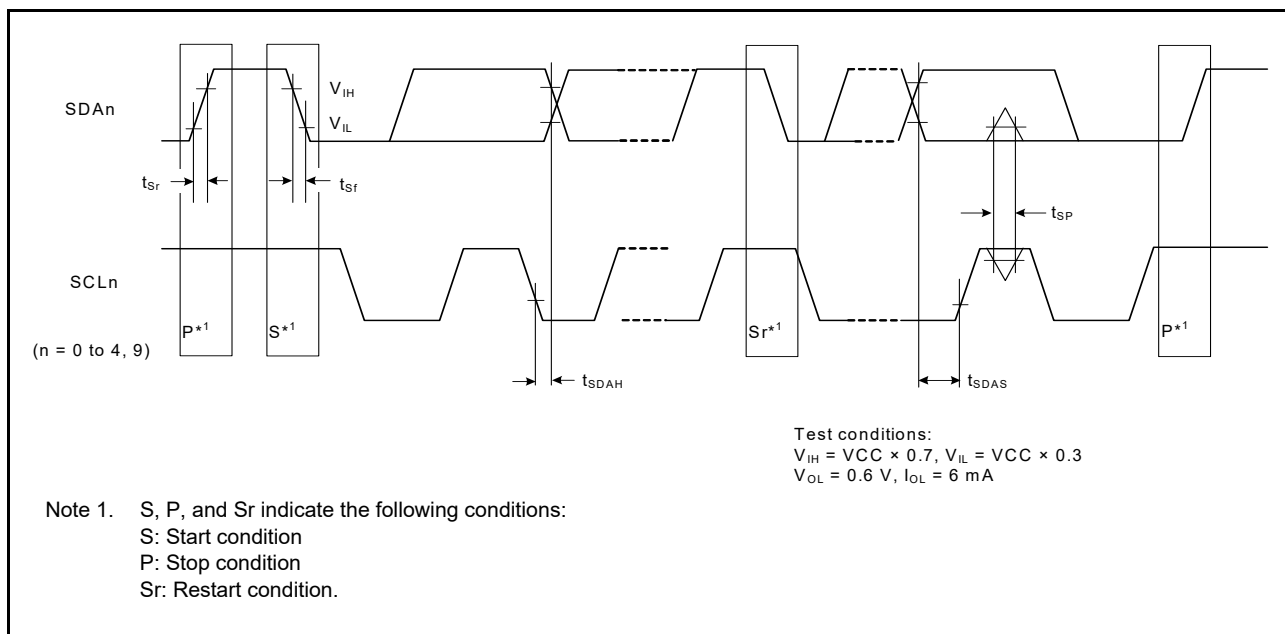


Figure 2.60 SCI simple IIC mode timing

2.3.10 SPI Timing

Table 2.40 SPI timing (1 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

Parameter			Symbol	Min	Max	Unit*1	Test conditions	
SPI	RSPCK clock cycle	Master	t_{SPCyc}	2*4	4096	t_{PCyc}	Figure 2.61	
		Slave		6	4096			
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns		
		Slave		$3 \times t_{PCyc}$	-			
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPCyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	-	ns		
		Slave		$3 \times t_{PCyc}$	-			
	RSPCK clock rise and fall time	Output	2.7 V or above	t_{SPCKr} , t_{SPCKf}	-	10		ns
			2.4 V or above		-	15		
			1.8 V or above		-	20		
			1.6 V or above		-	30		
Input		-	1	μ s				
Data input setup time	Master	t_{SU}	10	-	ns	Figure 2.62 to Figure 2.67		
	Slave		2.4 V or above	10			-	
			1.8 V or above	15			-	
			1.6 V or above	20			-	
Data input hold time	Master (RSPCK is PCLKA/2)	t_{HF}	0	-	ns			
	Master (RSPCK is other than above.)	t_H	t_{PCyc}	-				
	Slave	t_H	20	-				
SSL setup time	Master	1.8 V or above	t_{LEAD}	$-30 + N \times t_{SPCyc}^{*2}$	-	ns		
				$-50 + N \times t_{SPCyc}^{*2}$	-			
	Slave	$6 \times t_{PCyc}$	-					
SSL hold time	Master	t_{LAG}	$-30 + N \times t_{SPCyc}^{*3}$	-	ns			
	Slave		$6 \times t_{PCyc}$	-				

Table 2.40 SPI timing (2 of 2)

Conditions: Middle drive output is selected in the Port Drive Capability in PmnPFS register

Parameter			Symbol	Min	Max	Unit*1	Test conditions	
SPI	Data output delay	Master	2.7 V or above	t_{OD}	-	14	ns	Figure 2.62 to Figure 2.67
			2.4 V or above		-	20		
			1.8 V or above		-	25		
			1.6 V or above		-	30		
		Slave	2.7 V or above		-	50		
			2.4 V or above		-	60		
			1.8 V or above		-	85		
			1.6 V or above		-	110		
Data output hold time	Master		t_{OH}	0	-	ns		
	Slave			0	-			
Successive transmission delay	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns		
	Slave			$6 \times t_{Pcyc}$	-			
MOSI and MISO rise and fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	-	10	ns		
		2.4 V or above		-	15			
		1.8 V or above		-	20			
		1.6 V or above		-	30			
	Input	-		1	μs			
SSL rise and fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	-	10	ns		
		2.4 V or above		-	15			
		1.8 V or above		-	20			
		1.6 V or above		-	30			
	Input	-		1	μs			
Slave access time		2.4 V or above	t_{SA}	-	$2 \times t_{Pcyc} + 100$	ns	Figure 2.66 and Figure 2.67	
		1.8 V or above		-	$2 \times t_{Pcyc} + 140$			
		1.6 V or above		-	$2 \times t_{Pcyc} + 180$			
Slave output release time		2.4 V or above	t_{REL}	-	$2 \times t_{Pcyc} + 100$	ns		
		1.8 V or above		-	$2 \times t_{Pcyc} + 140$			
		1.6 V or above		-	$2 \times t_{Pcyc} + 180$			

Note 1. t_{Pcyc} : PCLKA cycle.

Note 2. N is set as an integer from 1 to 8 by the SPCKD register.

Note 3. N is set as an integer from 1 to 8 by the SSLND register.

Note 4. The upper limit of RSPCK is 16 MHz.

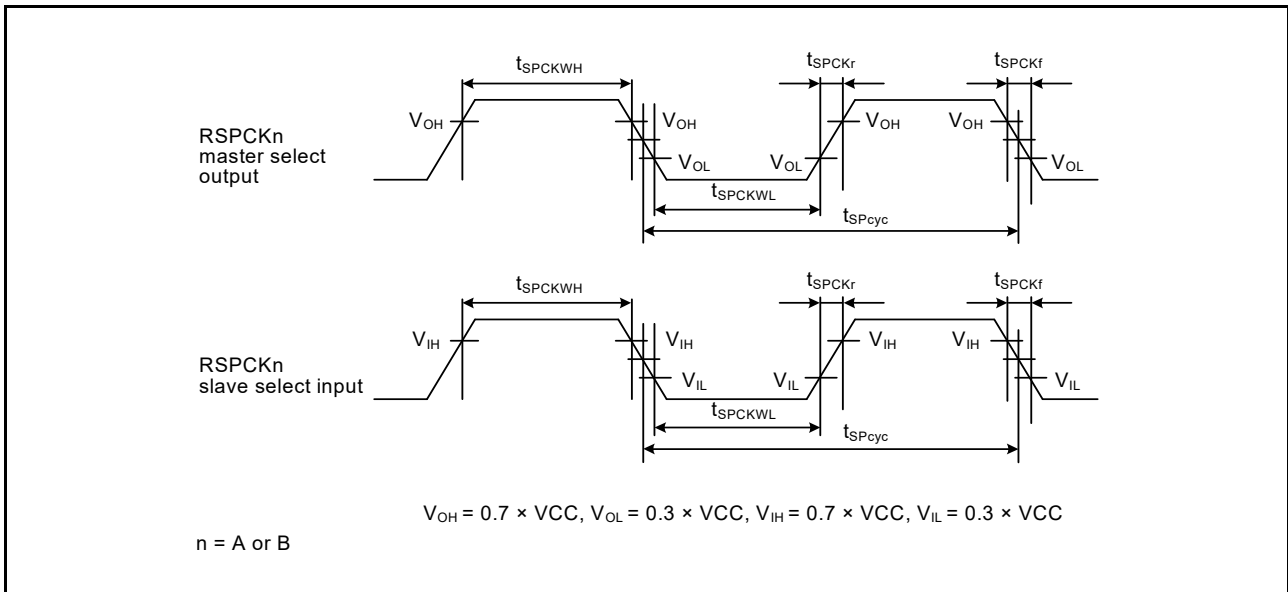


Figure 2.61 SPI clock timing

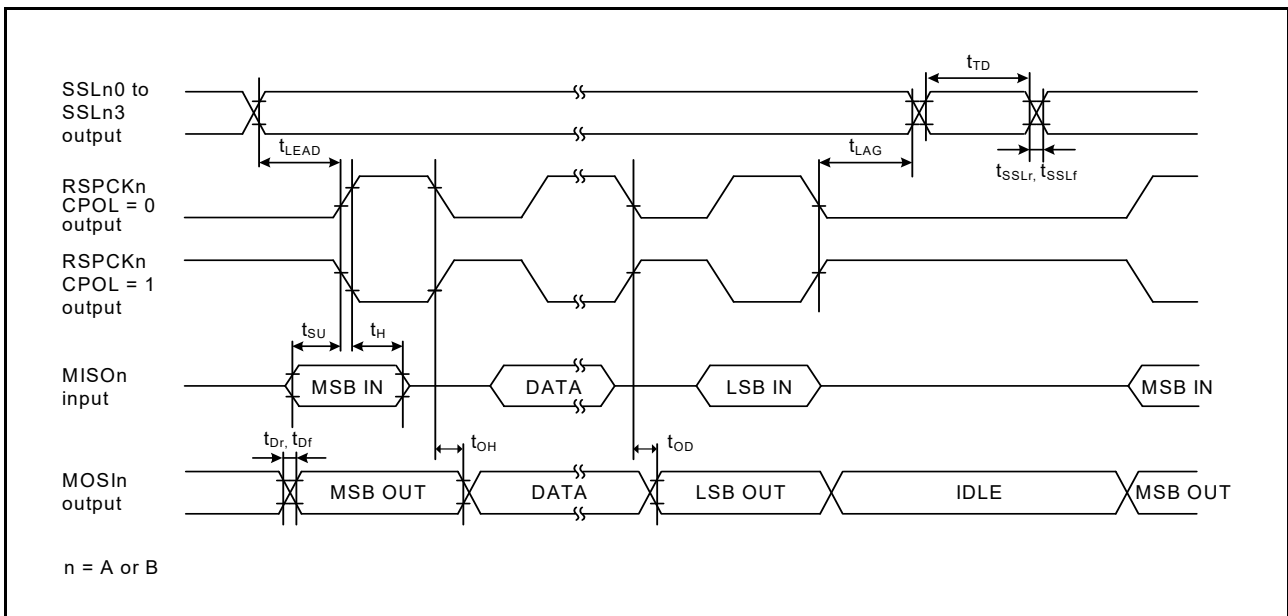


Figure 2.62 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to any value other than 1/2)

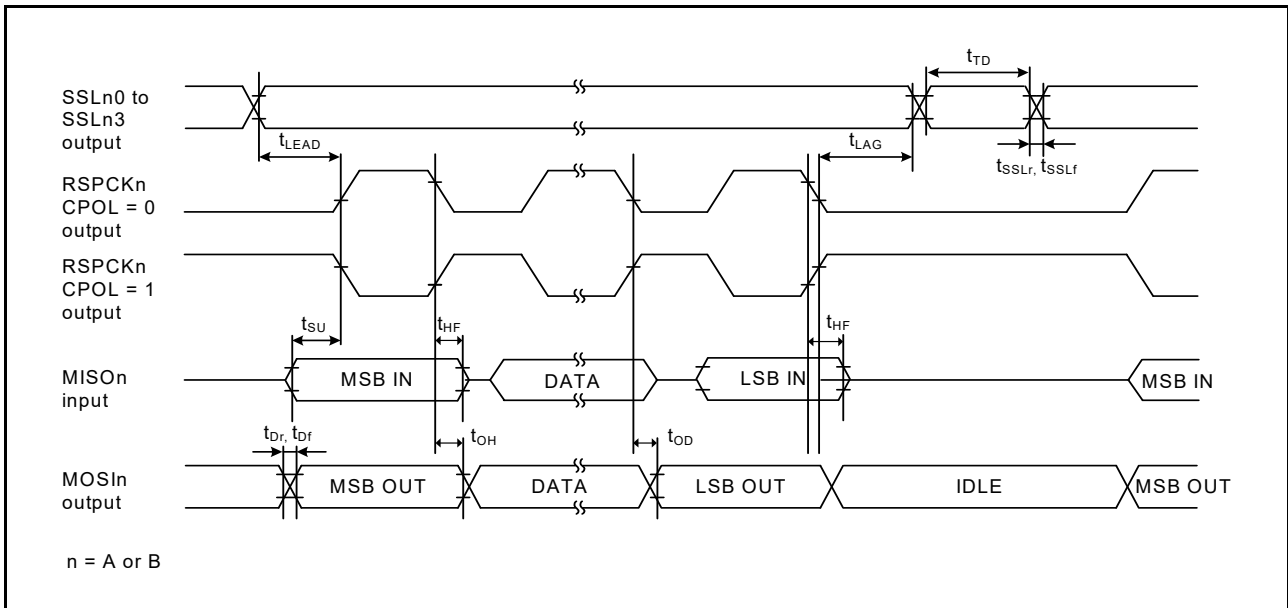


Figure 2.63 SPI timing (master, CPHA = 0) (bit rate: PCLKA division ratio is set to 1/2)

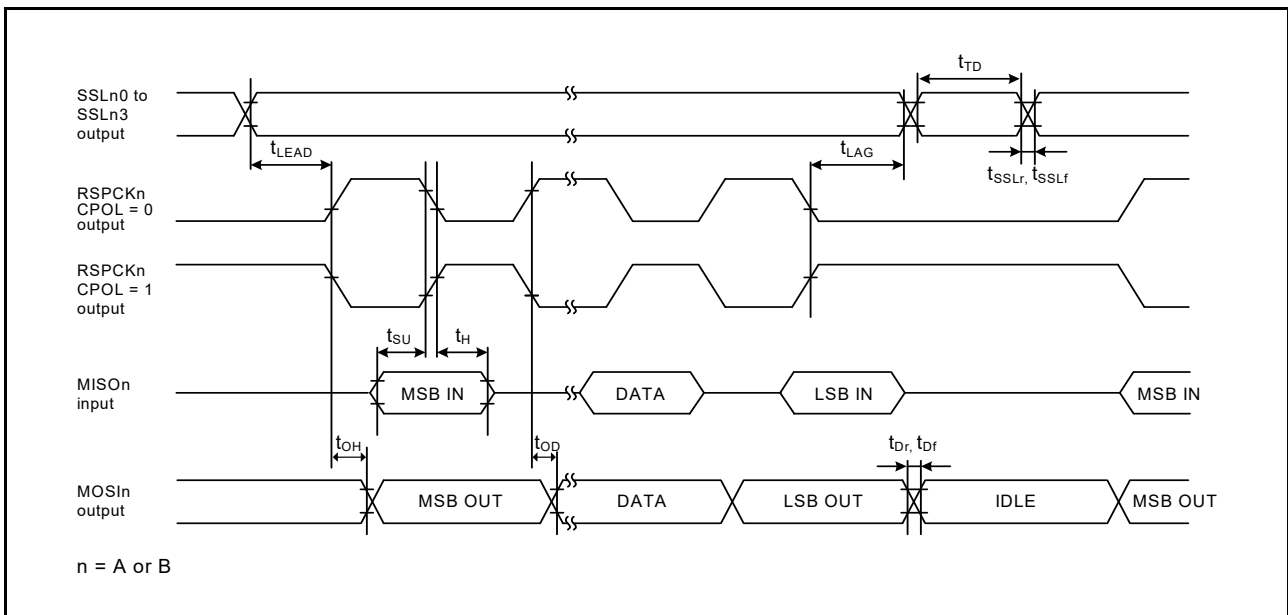


Figure 2.64 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to any value other than 1/2)

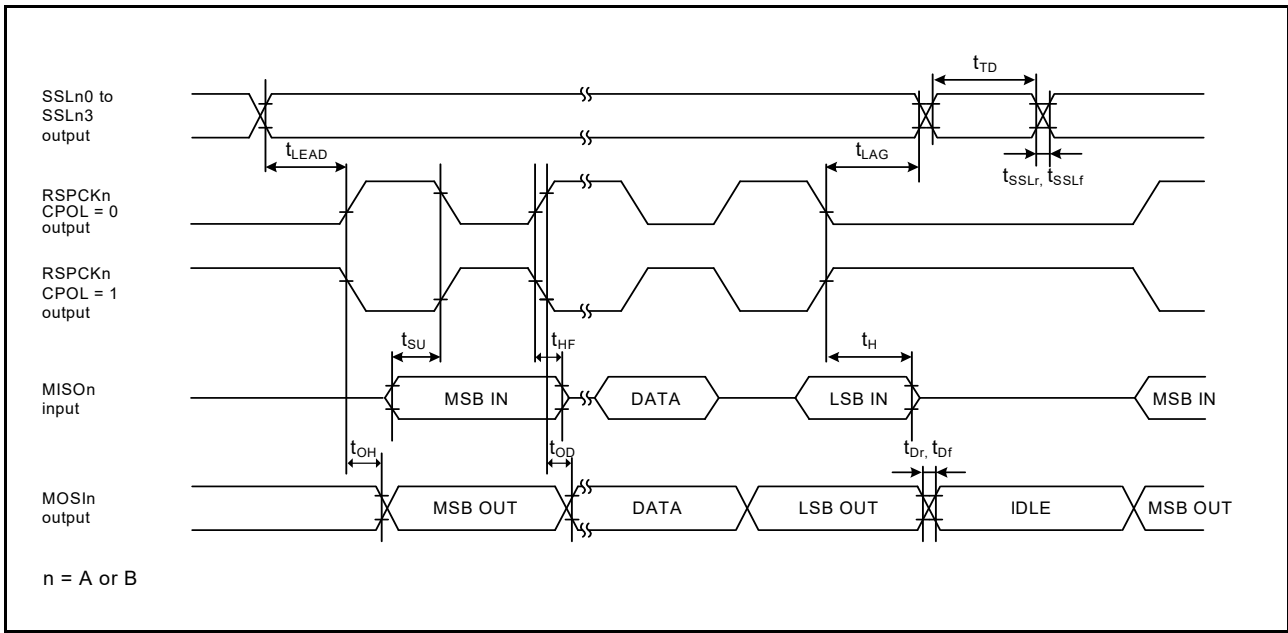


Figure 2.65 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to 1/2)

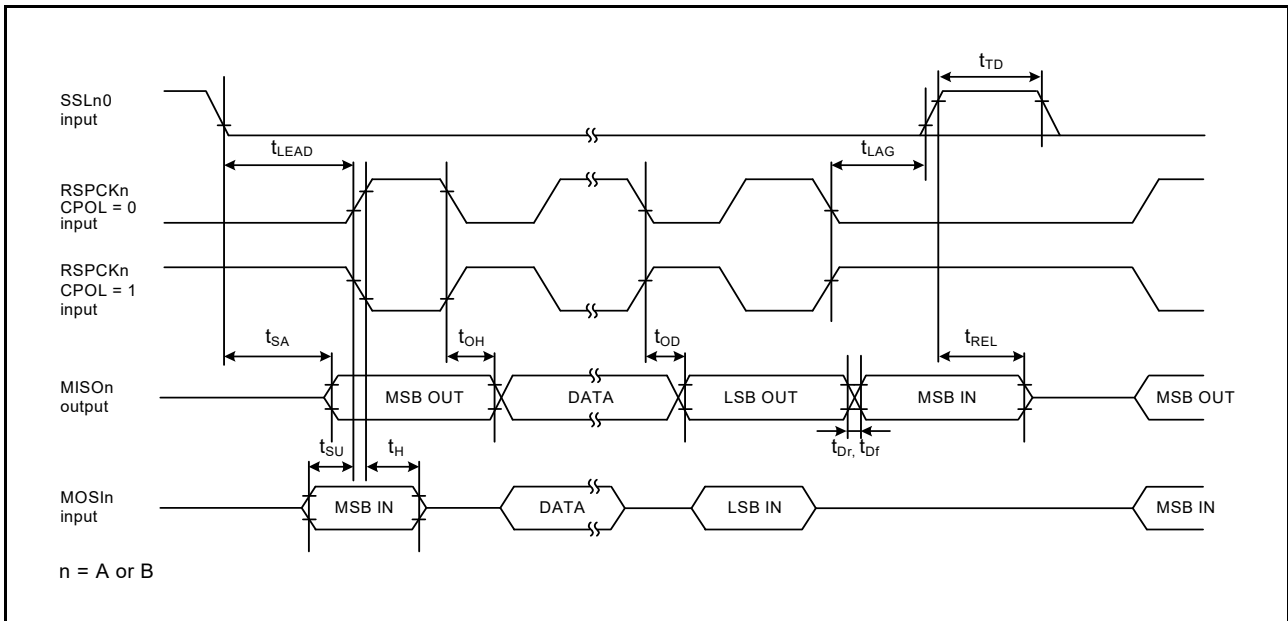


Figure 2.66 SPI timing (slave, CPHA = 0)

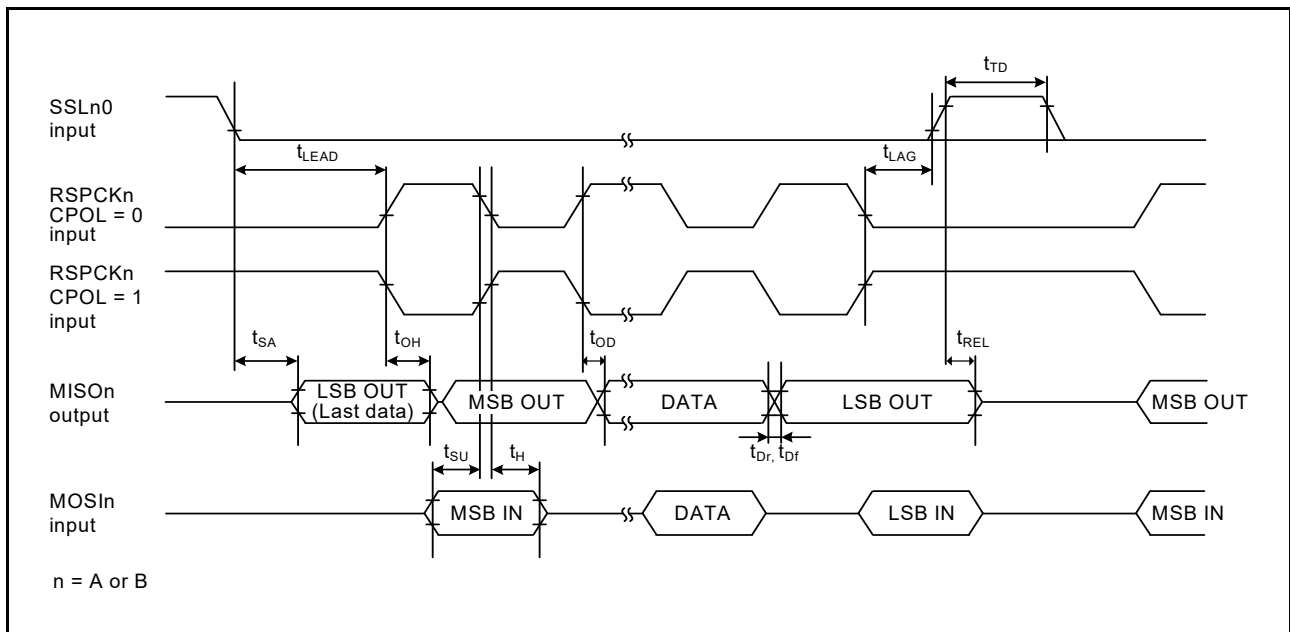


Figure 2.67 SPI timing (slave, CPHA = 1)

2.3.11 QSPI Timing

Table 2.41 QSPI timing

Conditions: VCC = 1.8 to 5.5 V

Conditions: Middle drive output is selected in the Port Drive Capability bit in PmnPFS register

Parameter		Symbol	Min	Max	Unit*1	Test conditions	
QSPI	QSPCLK clock cycle	t_{QScyc}	2^4	48	t_{Pcyc}	Figure 2.68	
	QSPCLK clock high-level pulse width	t_{QSWH}	$t_{QScyc} \times 0.4$	-	ns		
	QSPCLK clock low-level pulse width	t_{QSWL}	$t_{QScyc} \times 0.4$	-	ns		
	Data input setup time	t_{SU}	25	-	ns	Figure 2.69	
	Data input hold time	t_{IH}	2	-	ns		
	SSL setup time	t_{LEAD}	$(N + 0.5) \times t_{QScyc} - 15^*2$	$(N + 0.5) \times t_{QScyc} + 100^*2$	ns		
	SSL hold time	t_{LAG}	$(N + 0.5) \times t_{QScyc} - 15^*3$	$(N + 0.5) \times t_{QScyc} + 100^*3$	ns		
	Data output delay	t_{OD}	2.7 V or above	-	14		ns
			2.4 V or above	-	20		
			1.8 V or above	-	30		
	Data output hold time	t_{OH}	2.7 V or above	-3.3	-		ns
			1.8 V or above	-10	-		
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}		

Note 1. t_{Pcyc} : PCLKA cycle.

Note 2. N is set to 0 or 1 in SFMSLD.

Note 3. N is set to 0 or 1 in SFMSHD.

Note 4. The upper limit of QSPCLK is 16MHz.

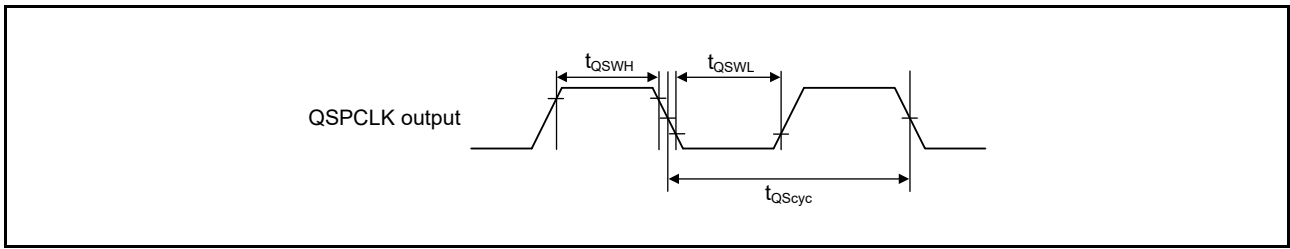


Figure 2.68 QSPI clock timing

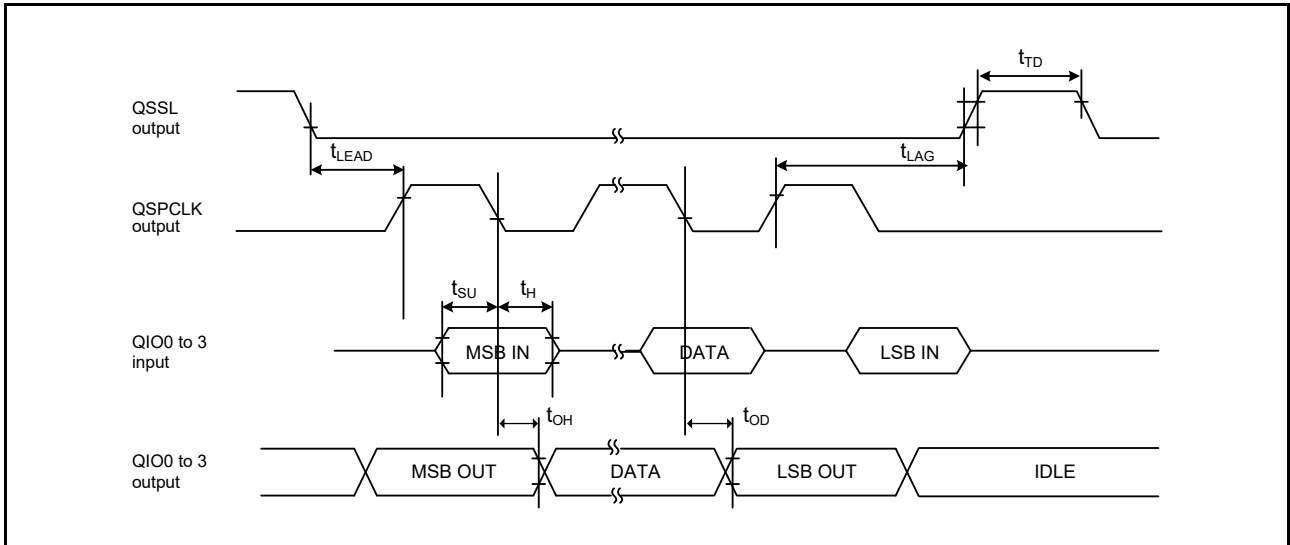


Figure 2.69 Transfer/receive timing

2.3.12 IIC Timing

Table 2.42 IIC timing
Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	Min*1	Max	Unit	Test conditions
IIC (standard mode, SMBus)	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 1300$	-	ns	Figure 2.70
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	$1 (5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
SCL, SDA capacitive load	C_b	-	400	pF		
IIC (Fast mode)	SCL input cycle time	t_{SCL}	$6 (12) \times t_{IICcyc} + 600$	-	ns	Figure 2.70 For all ports except P408, use PmnPFS.DS CR of middle drive. For port P408, use PmnPFS.DS CR1/DSCR of middle drive for IIC fast-mode.
	SCL input high pulse width	t_{SCLH}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL input low pulse width	t_{SCLL}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	300	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	$1 (4) \times t_{IICcyc}$	ns	
	SDA input bus free time (When wakeup function is disabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 300$	-	ns	
	SDA input bus free time (When wakeup function is enabled)	t_{BUF}	$3 (6) \times t_{IICcyc} + 4 \times t_{Pcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is disabled)	t_{STAH}	$t_{IICcyc} + 300$	-	ns	
	START condition input hold time (When wakeup function is enabled)	t_{STAH}	$1(5) \times t_{IICcyc} + t_{Pcyc} + 300$	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	$t_{IICcyc} + 50$	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
SCL, SDA capacitive load	C_b	-	400	pF		

Note: t_{IICcyc} : IIC internal reference clock (IIC ϕ) cycle, t_{Pcyc} : PCLKB cycle

Note 1. The value in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.

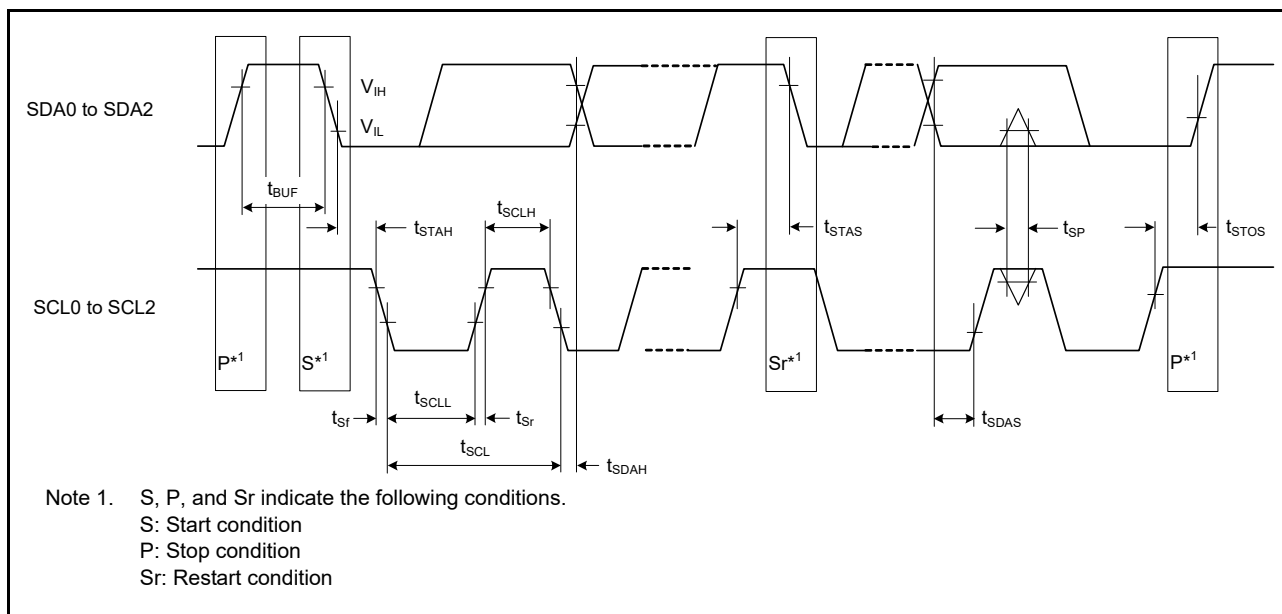


Figure 2.70 I²C bus interface input/output timing

2.3.13 SSIE Timing

Table 2.43 SSIE timing

Conditions: VCC = 1.6 to 5.5 V

Parameter		Symbol	Min	Max	Unit	Test conditions
SSIE	AUDIO_CLK input frequency	t_{AUDIO}	2.7 V or above	25	MHz	-
			1.6 V or above	4		
Output clock period		t_{O}	250	-	ns	Figure 2.71
Input clock period		t_{I}	250	-	ns	
Clock high pulse width	1.8 V or above	t_{HC}	100	-	ns	
	1.6 V or above		200	-		
Clock low pulse width	1.8 V or above	t_{LC}	100	-	ns	
	1.6 V or above		200	-		
Clock rise time		t_{RC}	-	25	ns	
Data delay	2.7 V or above	t_{DTR}	-	65	ns	Figure 2.72, Figure 2.73
	1.8 V or above		-	105		
	1.6 V or above		-	140		
Set-up time	2.7 V or above	t_{SR}	65	-	ns	
	1.8 V or above		90	-		
	1.6 V or above		140	-		
Hold time		t_{HTR}	40	-	ns	
SSITXD0 output delay from SSILRCK/SSIFS change time	1.8 V or above	T_{DTRW}	-	105	ns	Figure 2.74
	1.6 V or above		-	140		

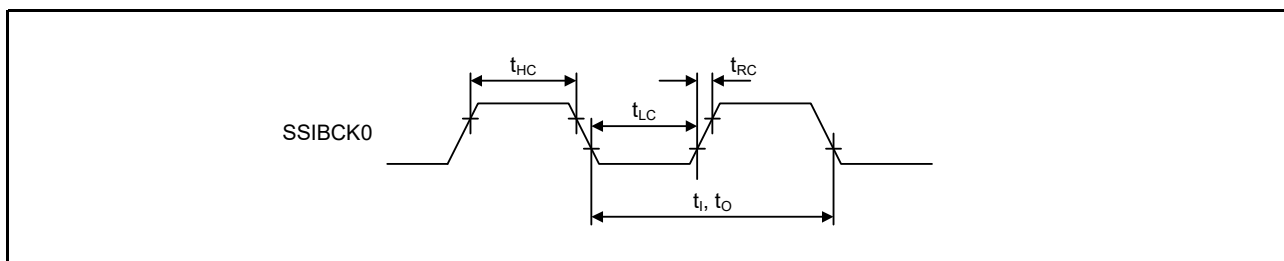


Figure 2.71 SSIE clock input/output timing

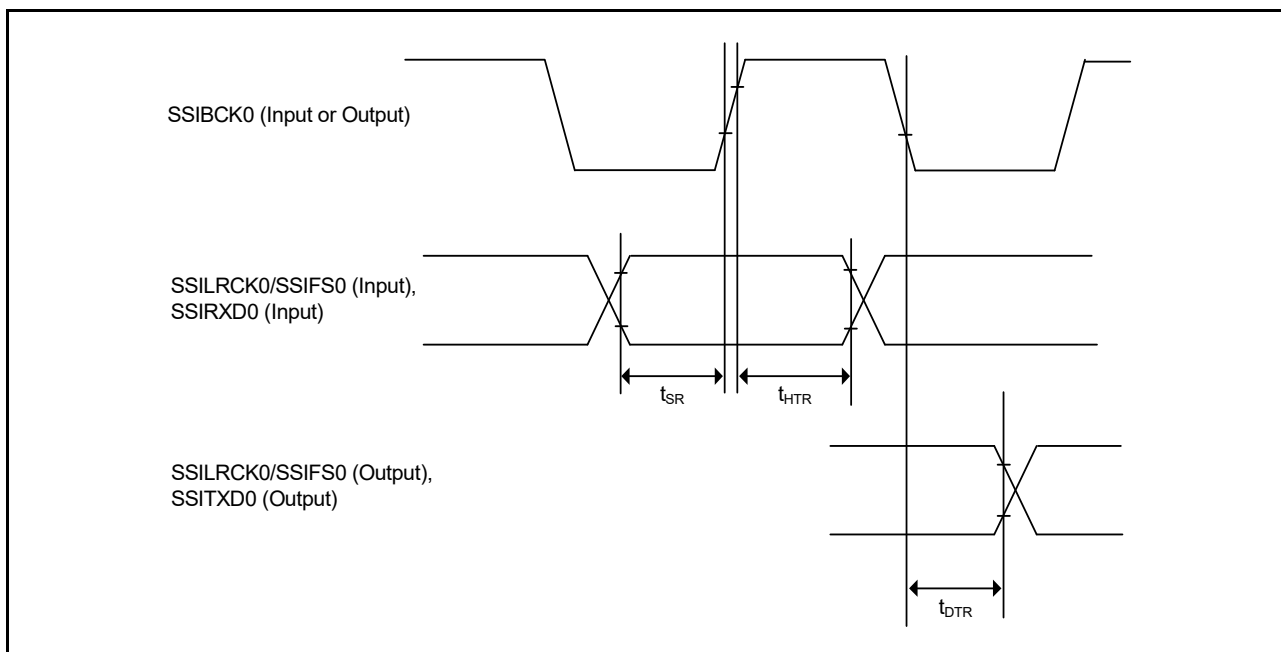


Figure 2.72 SSIE data transmit/receive timing (SSICR.BCKP = 0)

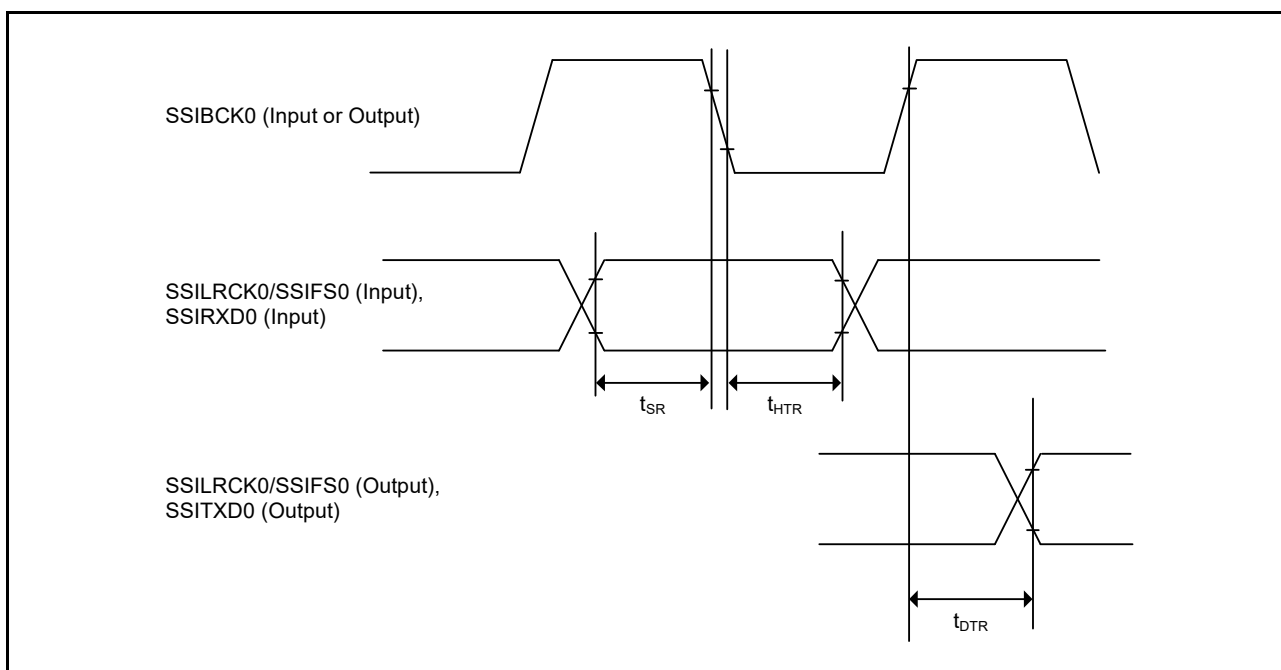


Figure 2.73 SSIE data transmit/receive timing (SSICR.BCKP = 1)

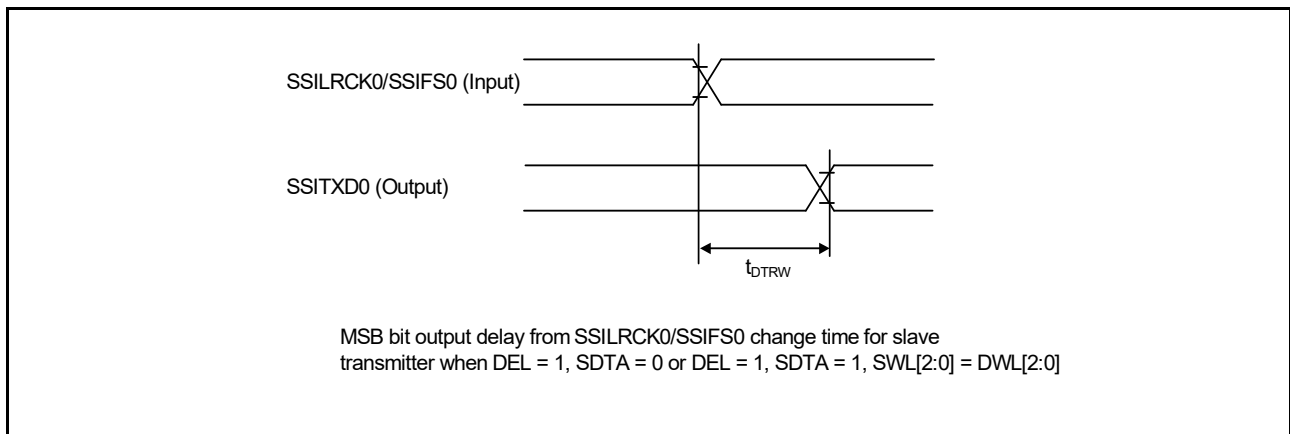


Figure 2.74 SSIE data output delay from SSILRCK0/SSIFS0 change time

2.3.14 SD/MMC Host Interface Timing

Table 2.44 SD/MMC host interface signal timing

Conditions: VCC = 2.7 to 5.5 V

Middle drive output is selected in the Port Drive Capability in PmnPFS register

Parameter	Symbol	Min	Max	Unit	Test conditions
SDCLK clock cycle	t_{SDCYC}	62.5	-	ns	Figure 2.75
SDCLK clock high-level pulse width	t_{SDWH}	18.25	-	ns	
SDCLK clock low-level pulse width	t_{SDWL}	18.25	-	ns	
SDCLK clock rising time	t_{SDLH}	-	10	ns	
SDCLK clock falling time	t_{SDHL}	-	10	ns	
SDCMD/SDDAT output data delay	t_{SDODLY}	-18.25	18.25	ns	
SDCMD/SDDAT input data setup	t_{SDIS}	9.25	-	ns	
SDCMD/SDDAT input data hold	t_{SDIH}	23.25	-	ns	

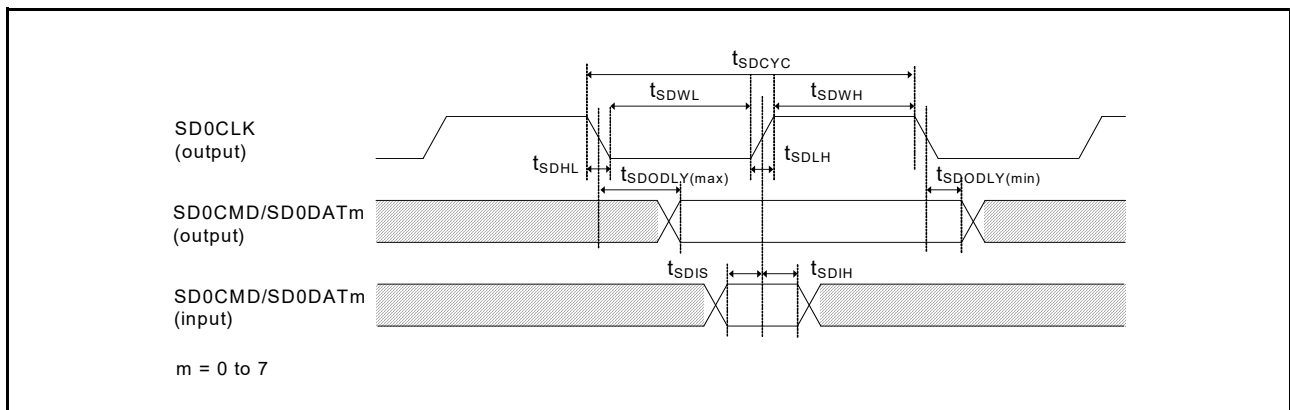


Figure 2.75 SD/MMC host interface signal timing

2.3.15 CLKOUT Timing

Table 2.45 CLKOUT timing

Parameter		Symbol	Min	Max	Unit*1	Test conditions	
CLKOUT	CLKOUT pin output cycle*1	VCC = 2.7 V or above	t _{Cyc}	62.5	-	ns	Figure 2.76
		VCC = 1.8 V or above		125	-		
		VCC = 1.6 V or above		250	-		
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t _{CH}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t _{CL}	15	-	ns	
		VCC = 1.8 V or above		30	-		
		VCC = 1.6 V or above		150	-		
	CLKOUT pin output rise time	VCC = 2.7 V or above	t _{Cr}	-	12	ns	
		VCC = 1.8 V or above		-	25		
		VCC = 1.6 V or above		-	50		
CLKOUT pin output fall time	VCC = 2.7 V or above	t _{Cf}	-	12	ns		
	VCC = 1.8 V or above		-	25			
	VCC = 1.6 V or above		-	50			

Note 1. When the EXTAL external clock input or an oscillator is used with division by 1 (the CKOCR.CKOSSEL[2:0] bits are 011b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.

Note 2. When the MOCO is selected as the clock output source (the CKOCR.CKOSSEL[2:0] bits are 001b), set the clock output division ratio selection to be divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

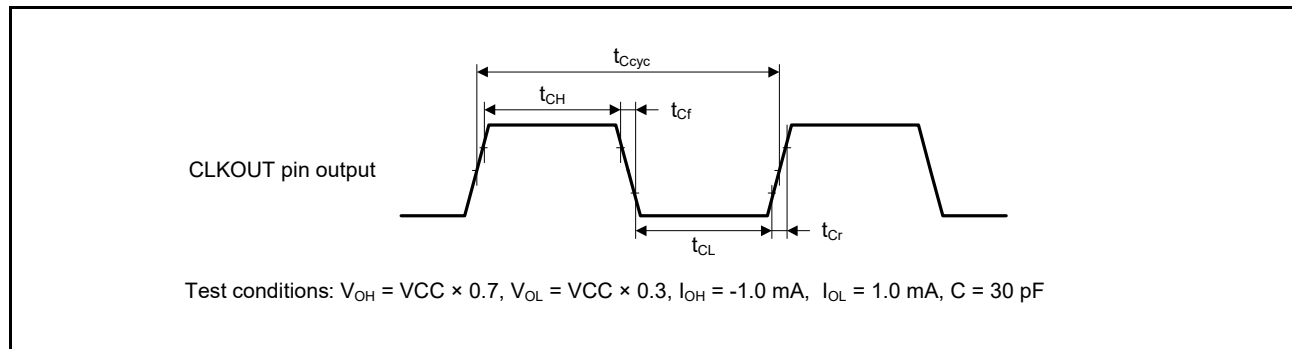


Figure 2.76 CLKOUT output timing

2.4 USB Characteristics

2.4.1 USBFS Timing

Table 2.46 USB characteristics

Conditions: VCC = VCC_USB = 3.0 to 3.6 V, Ta = -20 to +85°C (USBCLKSEL = 1), Ta = -40 to +105°C (USBCLKSEL = 0)

Parameter		Symbol	Min	Max	Unit	Test conditions	
Input characteristics	Input high level voltage	V_{IH}	2.0	-	V	-	
	Input low level voltage	V_{IL}	-	0.8	V	-	
	Differential input sensitivity	V_{DI}	0.2	-	V	USB_DP - USB_DM	
	Differential common mode range	V_{CM}	0.8	2.5	V	-	
Output characteristics	Output high level voltage	V_{OH}	2.8	VCC_USB	V	$I_{OH} = -200 \mu A$	
	Output low level voltage	V_{OL}	0.0	0.3	V	$I_{OL} = 2 \text{ mA}$	
	Cross-over voltage	V_{CRS}	1.3	2.0	V	Figure 2.77, Figure 2.78, Figure 2.79	
	Rise time	FS	t_r	4	20		ns
		LS		75	300		
	Fall time	FS	t_f	4	20		ns
		LS		75	300		
	Rise/fall time ratio	FS	t_r/t_f	90	111.11		%
LS			80	125			
Output resistance	Z_{DRV}	28	44	Ω	(Adjusting the resistance of external elements is not required.)		
VBUS characteristics	VBUS input voltage	V_{IH}	$VCC \times 0.8$	-	V	-	
		V_{IL}	-	$VCC \times 0.2$	V	-	
Pull-up, pull-down	Pull-down resistor	R_{PD}	14.25	24.80	k Ω	-	
	Pull-up resistor	R_{PUI}	0.9	1.575	k Ω	During idle state	
		R_{PUA}	1.425	3.09	k Ω	During reception	
Battery Charging Specification Ver 1.2	D + sink current	I_{DP_SINK}	25	175	μA	-	
	D - sink current	I_{DM_SINK}	25	175	μA	-	
	DCD source current	I_{DP_SRC}	7	13	μA	-	
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-	
	D + source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA	
	D - source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA	

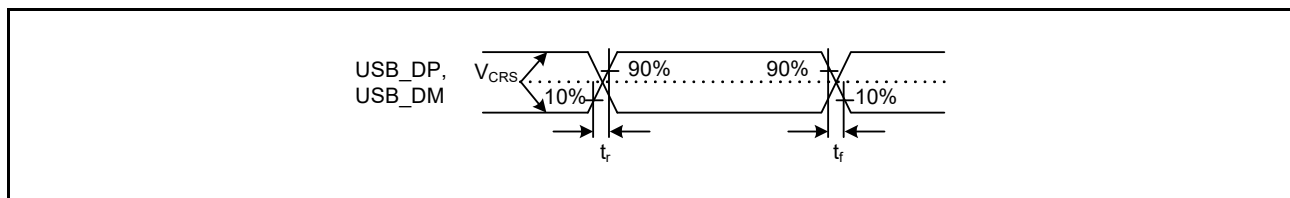


Figure 2.77 USB_DP and USB_DM output timing

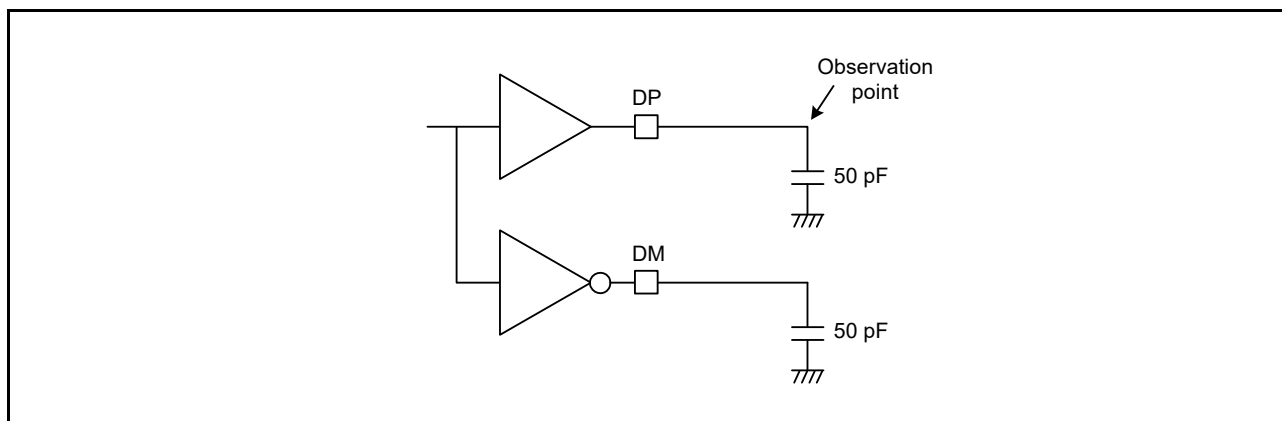


Figure 2.78 Test circuit for Full-Speed (FS) connection

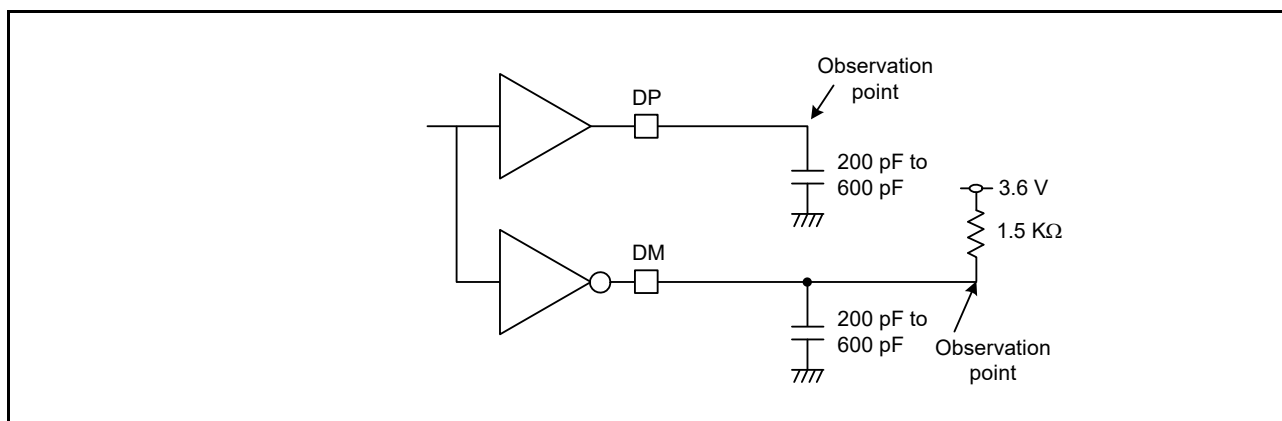


Figure 2.79 Test circuit for Low-Speed (LS) connection

2.4.2 USB External Supply

Table 2.47 USB regulator

Parameter	Min	Typ	Max	Unit	Test conditions	
VCC_USB supply current	VCC_USB_LDO ≥ 3.8V	-	-	50	mA	-
	VCC_USB_LDO ≥ 4.5V	-	-	100	mA	-
VCC_USB supply voltage	3.0	-	3.6	V	-	

2.5 ADC14 Characteristics

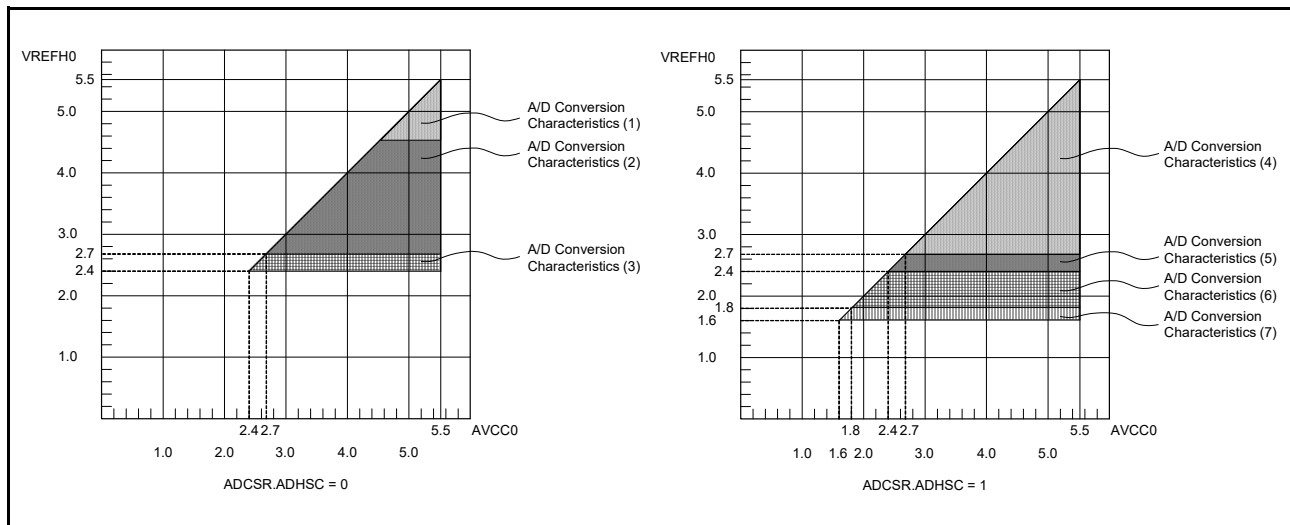


Figure 2.80 AVCC0 to VREFH0 voltage range

Table 2.48 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)

Conditions: $V_{CC} = AV_{CC0} = 4.5$ to 5.5 V, $V_{REFH0} = 4.5$ to 5.5 VReference voltage range applied to the V_{REFH0} and V_{REFL0} .

Parameter	Min	Typ	Max	Unit	Test conditions	
Frequency	1	-	64	MHz	-	
Analog input capacitance*2	Cs	-	8 (reference data)	pF	High-precision channel	
		-	9 (reference data)	pF	Normal-precision channel	
Analog input resistance	Rs	-	2.5 (reference data)	k Ω	High-precision channel	
		-	6.7 (reference data)	k Ω	Normal-precision channel	
Analog input voltage range	Ain	0	VREFH0	V	-	
12-bit mode						
Resolution	-	-	12	Bit	-	
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 k Ω	0.70	-	-	μ s	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.13	-	-	μ s	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error	-	± 0.5	± 4.5	LSB	High-precision channel	
			± 6.0	LSB	Other than above	
Full-scale error	-	± 0.75	± 4.5	LSB	High-precision channel	
			± 6.0	LSB	Other than above	
Quantization error	-	± 0.5	-	LSB	-	
Absolute accuracy	-	± 1.25	± 5.0	LSB	High-precision channel	
			± 8.0	LSB	Other than above	
DNL differential nonlinearity error	-	± 1.0	-	LSB	-	
INL integral nonlinearity error	-	± 1.0	± 3.0	LSB	-	
14-bit mode						
Resolution	-	-	14	Bit	-	

Table 2.48 A/D conversion characteristics (1) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	0.80	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.22	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error			±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error			±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error			±0.5	-	LSB	-
Absolute accuracy			±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error			±4.0	-	LSB	-
INL integral nonlinearity error			±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.49 A/D conversion characteristics (2) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	48	MHz	-
Analog input capacitance*2	Cs			8 (reference data)	pF	High-precision channel
				9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs			2.5 (reference data)	kΩ	High-precision channel
				6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution				12	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ			0.94	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
				1.50	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error			±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error			±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error			±0.5	-	LSB	-
Absolute accuracy			±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error			±1.0	-	LSB	-
INL integral nonlinearity error			±1.0	±3.0	LSB	-
14-bit mode						

Table 2.49 A/D conversion characteristics (2) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 48 MHz)	Permissible signal source impedance Max. = 0.3 kΩ	1.06	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		1.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.50 A/D conversion characteristics (3) in high-speed A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	32	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.41	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.25	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-

Table 2.50 A/D conversion characteristics (3) in high-speed A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 32 MHz)	Permissible signal source impedance Max. = 1.3 kΩ	1.59	-	-	μs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
		2.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.51 A/D conversion characteristics (4) in low power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	24	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.25	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.38	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		-	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-

Table 2.51 A/D conversion characteristics (4) in low power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.7 to 5.5 V, VREFH0 = 2.7 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions	
INL integral nonlinearity error	-	±1.0	±3.0	LSB	-	
14-bit mode						
Resolution	-	-	14	Bit	-	
Conversion time*1 (Operation at PCLKC = 24 MHz)	Permissible signal source impedance Max. = 1.1 kΩ	2.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		3.63	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error			±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error			±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error			±0.5	-	LSB	-
Absolute accuracy			±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error			±4.0	-	LSB	-
INL integral nonlinearity error			±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.52 A/D conversion characteristics (5) in low power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter	Min	Typ	Max	Unit	Test conditions	
Frequency	1	-	16	MHz	-	
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
		-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution	-	-	12	Bit	-	
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.38	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.06	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error			±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error			±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error			±0.5	-	LSB	-
Absolute accuracy			±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above

Table 2.52 A/D conversion characteristics (5) in low power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 2.4 to 5.5 V, VREFH0 = 2.4 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 16 MHz)	Permissible signal source impedance Max. = 2.2 kΩ	3.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		5.44	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±2.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Full-scale error		-	±3.0	±18	LSB	High-precision channel
				±24.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±5.0	±20	LSB	High-precision channel
				±32.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.53 A/D conversion characteristics (6) in low power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	8	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
		-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	3.8 (reference data)	kΩ	High-precision channel
		-	-	8.2 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	6.75	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
		10.13	-	-	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-

Table 2.53 A/D conversion characteristics (6) in low power A/D conversion mode (2 of 2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.8 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Absolute accuracy		-	±3.0	±8.0	LSB	High-precision channel
				±12.0	LSB	Other than above
DNL differential nonlinearity error		-	±1.0	-	LSB	-
INL integral nonlinearity error		-	±1.0	±3.0	LSB	-
14-bit mode						
Resolution		-	-	14	Bit	-
Conversion time*1 (Operation at PCLKC = 8 MHz)	Permissible signal source impedance Max. = 5 kΩ	7.50	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
				10.88	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±4.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Full-scale error		-	±6.0	±30.0	LSB	High-precision channel
				±40.0	LSB	Other than above
Quantization error		-	±0.5	-	LSB	-
Absolute accuracy		-	±12.0	±32.0	LSB	High-precision channel
				±48.0	LSB	Other than above
DNL differential nonlinearity error		-	±4.0	-	LSB	-
INL integral nonlinearity error		-	±4.0	±12.0	LSB	-

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (Cin), see [section 2.2.4, I/O V_{OH}, V_{OL}, and Other Characteristics](#).

Table 2.54 A/D conversion characteristics (7) in low power A/D conversion mode (1 of 2)

Conditions: VCC = AVCC0 = 1.6 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V), VREFH0 = 1.6 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

Parameter		Min	Typ	Max	Unit	Test conditions
Frequency		1	-	4	MHz	-
Analog input capacitance*2	Cs	-	-	8 (reference data)	pF	High-precision channel
				9 (reference data)	pF	Normal-precision channel
Analog input resistance	Rs	-	-	13.1 (reference data)	kΩ	High-precision channel
				14.3 (reference data)	kΩ	Normal-precision channel
Analog input voltage range	Ain	0	-	VREFH0	V	-
12-bit mode						
Resolution		-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 4 MHz)	Permissible signal source impedance Max. = 9.9 kΩ	13.5	-	-	μs	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
				20.25	μs	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error		-	±1.0	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above
Full-scale error		-	±1.5	±7.5	LSB	High-precision channel
				±10.0	LSB	Other than above

Table 2.54 A/D conversion characteristics (7) in low power A/D conversion mode (2 of 2)

Conditions: $V_{CC} = AV_{CC0} = 1.6$ to 5.5 V ($AV_{CC0} = V_{CC}$ when $V_{CC} < 2.0$ V), $V_{REFH0} = 1.6$ to 5.5 V
Reference voltage range applied to the V_{REFH0} and V_{REFL0} .

Parameter	Min	Typ	Max	Unit	Test conditions	
Quantization error	-	± 0.5	-	LSB	-	
Absolute accuracy	-	± 3.0	± 8.0	LSB	High-precision channel	
			± 12.0	LSB	Other than above	
DNL differential nonlinearity error	-	± 1.0	-	LSB	-	
INL integral nonlinearity error	-	± 1.0	± 3.0	LSB	-	
14-bit mode						
Resolution	-	-	14	Bit	-	
Conversion time*1 (Operation at PCLKC = 4 MHz)	Permissible signal source impedance Max. = 9.9 k Ω	15.0	-	-	μ s	High-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 0Dh
					μ s	Normal-precision channel ADCSR.ADHSC = 1 ADSSTRn.SST[7:0] = 28h
Offset error	-	± 4.0	± 30.0	LSB	High-precision channel	
			± 40.0	LSB	Other than above	
Full-scale error	-	± 6.0	± 30.0	LSB	High-precision channel	
			± 40.0	LSB	Other than above	
Quantization error	-	± 0.5	-	LSB	-	
Absolute accuracy	-	± 12.0	± 32.0	LSB	High-precision channel	
			± 48.0	LSB	Other than above	
DNL differential nonlinearity error	-	± 4.0	-	LSB	-	
INL integral nonlinearity error	-	± 4.0	± 12.0	LSB	-	

Note: The characteristics apply when no pin functions other than 14-bit A/D converter input are used. Absolute accuracy does not include quantization errors. Offset error, full-scale error, DNL differential nonlinearity error, and INL integral nonlinearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The number of sampling states is indicated for the test conditions.

Note 2. Except for I/O input capacitance (C_{in}), see [section 2.2.4, I/O \$V_{OH}\$, \$V_{OL}\$, and Other Characteristics](#).

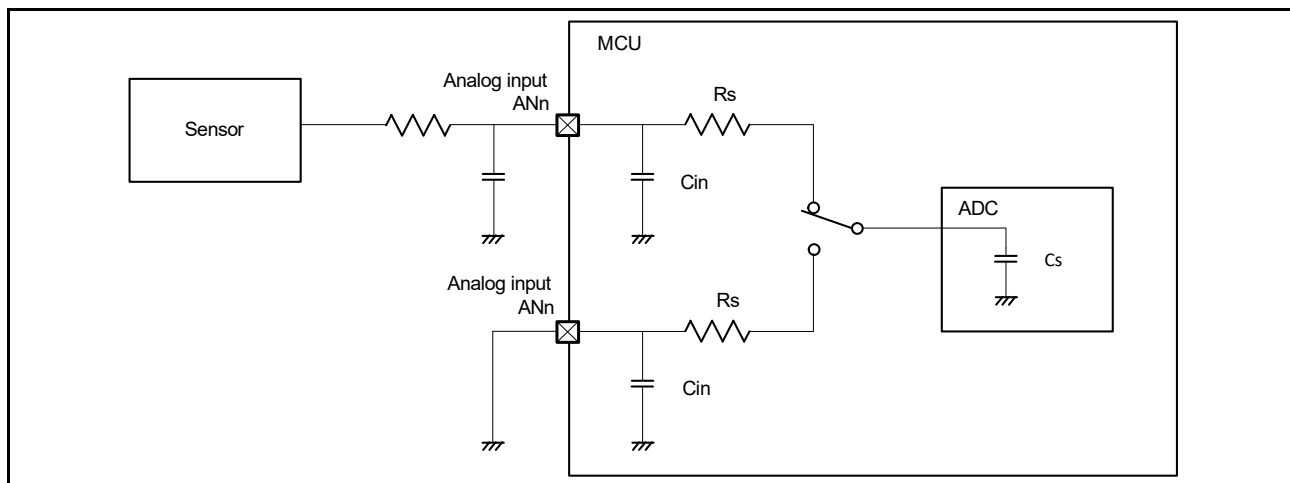
**Figure 2.81 Equivalent circuit for analog input**

Table 2.55 14-bit A/D converter channel classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN015	AVCC0 = 1.6 to 5.5 V	Pins AN000 to AN015 cannot be used as general I/O, IRQ2, IRQ3 inputs, and TS transmission, when the A/D converter is in use
Normal-precision channel	AN016 to AN027		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 5.5 V	-
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 5.5 V	-

Table 2.56 A/D internal reference voltage characteristics

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Frequency*3	1	-	2	MHz	-
Sampling time*4	5.0	-	-	μs	-

Note 1. The internal reference voltage cannot be selected for input channels when AVCC0 < 2.0 V.

Note 2. The 14-bit A/D internal reference voltage indicates the voltage when the internal reference voltage is input to the 14-bit A/D converter.

Note 3. This is a parameter for ADC14 when the internal reference voltage is used as a high-potential reference voltage.

Note 4. This is a parameter for ADC14 when the internal reference voltage is selected for an analog input channel in ADC14.

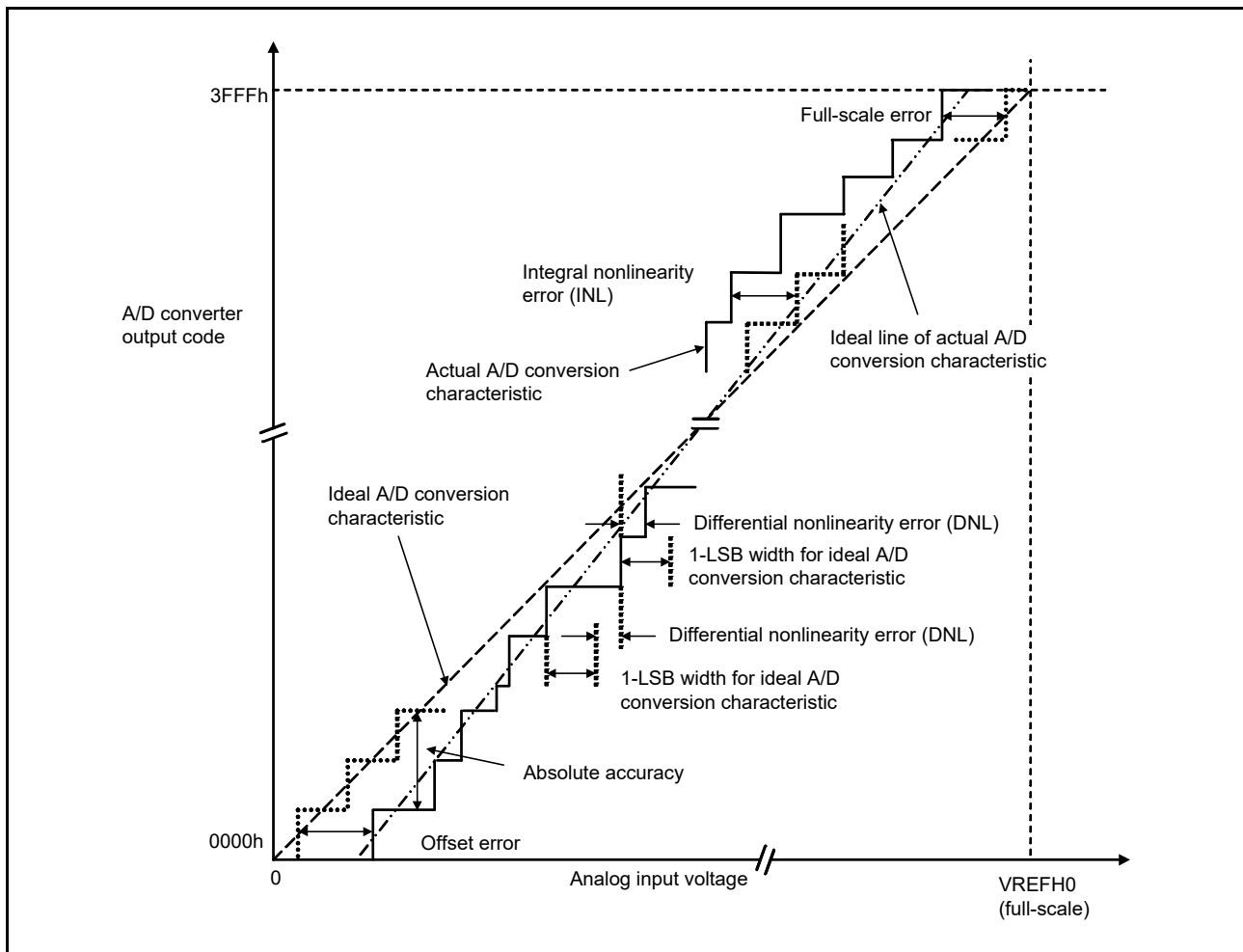


Figure 2.82 Illustration of 14-bit A/D converter characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as the analog input voltage. For example, if 12-bit resolution is used and the reference voltage $V_{REFH0} = 3.072$ V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If analog input voltage is 6 mV, an absolute accuracy of ± 5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actually output code.

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.57 D/A conversion characteristics (1)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Reference voltage = VREFH or VREFL selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	AVCC0 – 0.47	V	-
DNL differential nonlinearity error	-	±0.5	±1.0	LSB	-
INL integral nonlinearity error	-	±2.0	±8.0	LSB	-
Offset error	-	-	±20	mV	-
Full-scale error	-	-	±20	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

Table 2.58 D/A conversion characteristics (2)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Reference voltage = AVCC0 or AVSS0 selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	AVCC0 – 0.47	V	-
DNL differential nonlinearity error	-	±0.5	±2.0	LSB	-
INL integral nonlinearity error	-	±2.0	±8.0	LSB	-
Offset error	-	-	±30	mV	-
Full-scale error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

Table 2.59 D/A conversion characteristics (3)

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Reference voltage = internal reference voltage selected

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	bit	-
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	-
Resistive load	30	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.35	-	Vbgr	V	-
DNL differential nonlinearity error	-	±2.0	±16.0	LSB	-
INL integral nonlinearity error	-	±8.0	±16.0	LSB	-
Offset error	-	-	±30	mV	-
Output impedance	-	5	-	Ω	-
Conversion time	-	-	30	μs	-

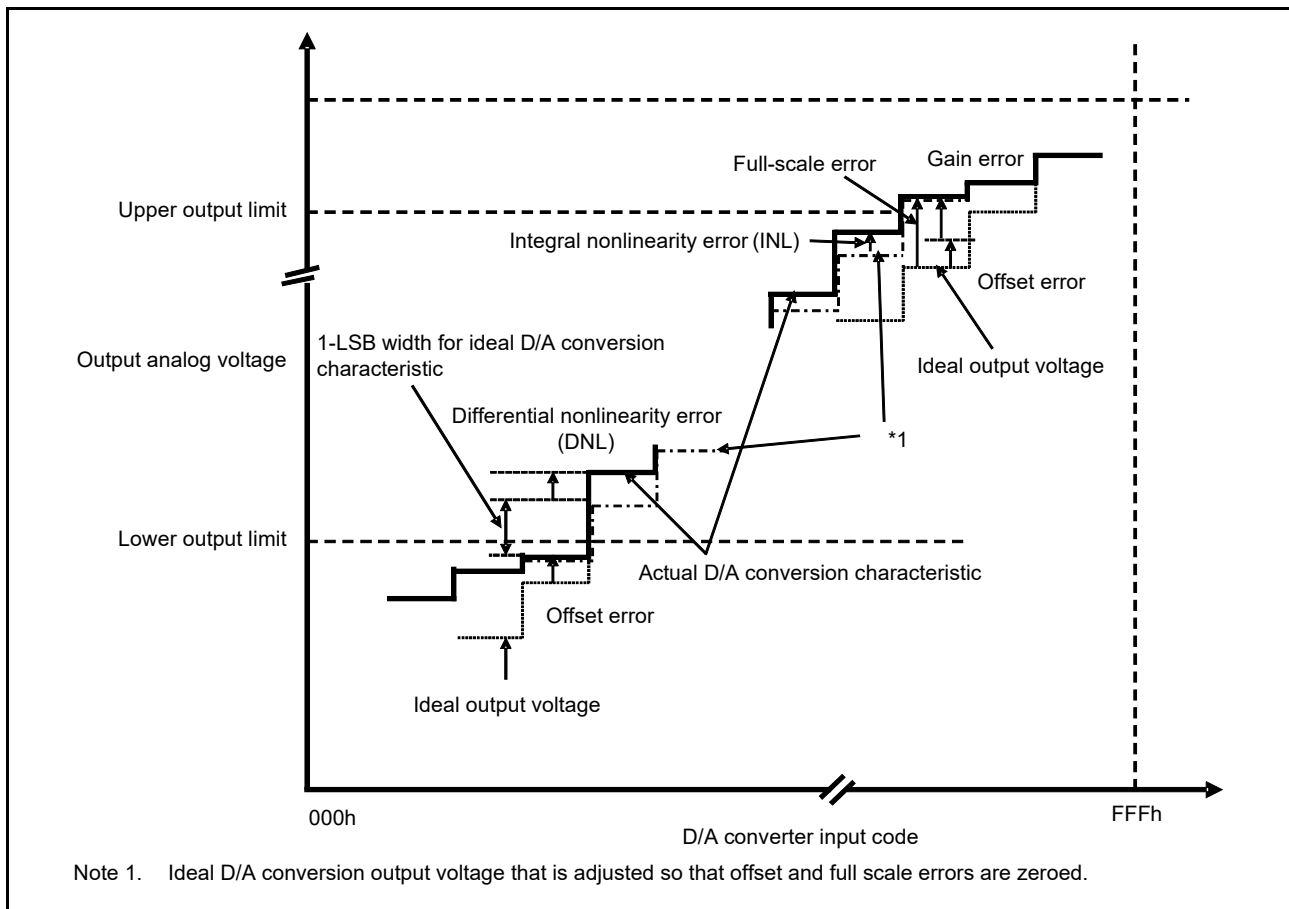


Figure 2.83 Illustration of D/A converter characteristic terms

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal output voltage based on the ideal conversion characteristic when the measured offset and full-scale errors are zeroed, and the actual output voltage.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between 1-LSB voltage width based on the ideal D/A conversion characteristics and the width of the actual output voltage.

Offset error

Offset error is the difference between the highest actual output voltage that falls below the lower output limit and the ideal output voltage based on the input code.

Full-scale error

Full-scale error is the difference between the lowest actual output voltage that exceeds the upper output limit and the ideal output voltage based on the input code.

2.7 TSN Characteristics

Table 2.60 TSN characteristics

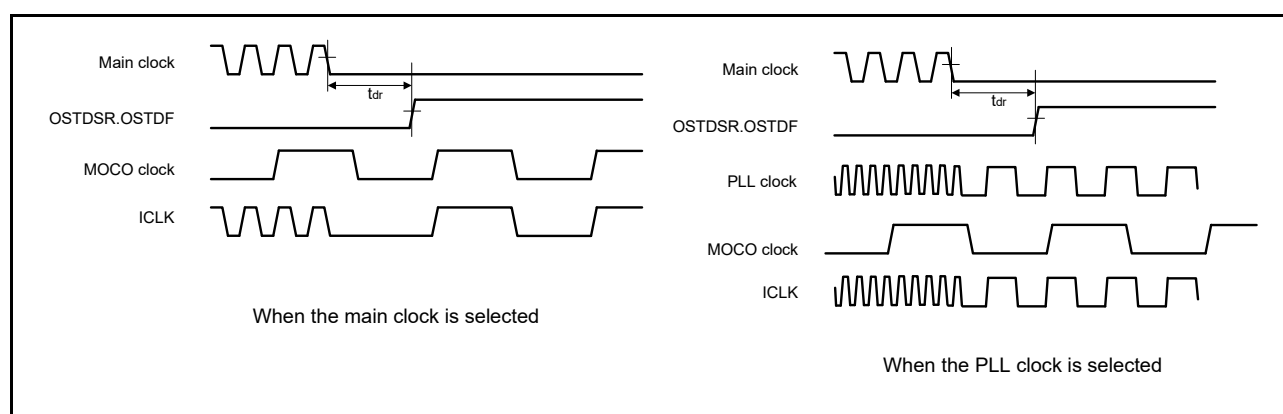
Conditions: VCC = AVCC0 = 2.0 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.5	-	°C	2.4 V or above
	-	-	±2.0	-	°C	Below 2.4 V
Temperature slope	-	-	-3.65	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.05	-	V	VCC = 3.3 V
Temperature sensor start time	t _{START}	-	-	5	µs	-
Sampling time	-	5	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.61 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t _{dr}	-	-	1	ms	Figure 2.84


Figure 2.84 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.62 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V _{POR}	1.27	1.42	1.57	V	Figure 2.85, Figure 2.86
	Voltage detection circuit (LVD0)*2	V _{det0_0}	3.68	3.85	4.00	V	Figure 2.87 At falling edge VCC
		V _{det0_1}	2.68	2.85	2.96		
		V _{det0_2}	2.38	2.53	2.64		
		V _{det0_3}	1.78	1.90	2.02		
		V _{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V _{det1_0}	4.13	4.29	4.45	V	Figure 2.88 At falling edge VCC
		V _{det1_1}	3.98	4.16	4.30		
		V _{det1_2}	3.86	4.03	4.18		
		V _{det1_3}	3.68	3.86	4.00		
		V _{det1_4}	2.98	3.10	3.22		
		V _{det1_5}	2.89	3.00	3.11		
		V _{det1_6}	2.79	2.90	3.01		
		V _{det1_7}	2.68	2.79	2.90		
		V _{det1_8}	2.58	2.68	2.78		
		V _{det1_9}	2.48	2.58	2.68		
		V _{det1_A}	2.38	2.48	2.58		
		V _{det1_B}	2.10	2.20	2.30		
		V _{det1_C}	1.84	1.96	2.05		
		V _{det1_D}	1.74	1.86	1.95		
V _{det1_E}		1.63	1.75	1.84			
V _{det1_F}	1.60	1.65	1.73				
Voltage detection circuit (LVD2)*4	V _{det2_0}	4.11	4.31	4.48	V	Figure 2.89 At falling edge VCC	
	V _{det2_1}	3.97	4.17	4.34			
	V _{det2_2}	3.83	4.03	4.20			
	V _{det2_3}	3.64	3.84	4.01			

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.

Note 2. # in the symbol V_{det0_#} denotes the value of the OFS1.VDSEL1[2:0] bits.

Note 3. # in the symbol V_{det1_#} denotes the value of the LVDLVL.R.LVD1LVL[4:0] bits.

Note 4. # in the symbol V_{det2_#} denotes the value of the LVDLVL.R.LVD2LVL[2:0] bits.

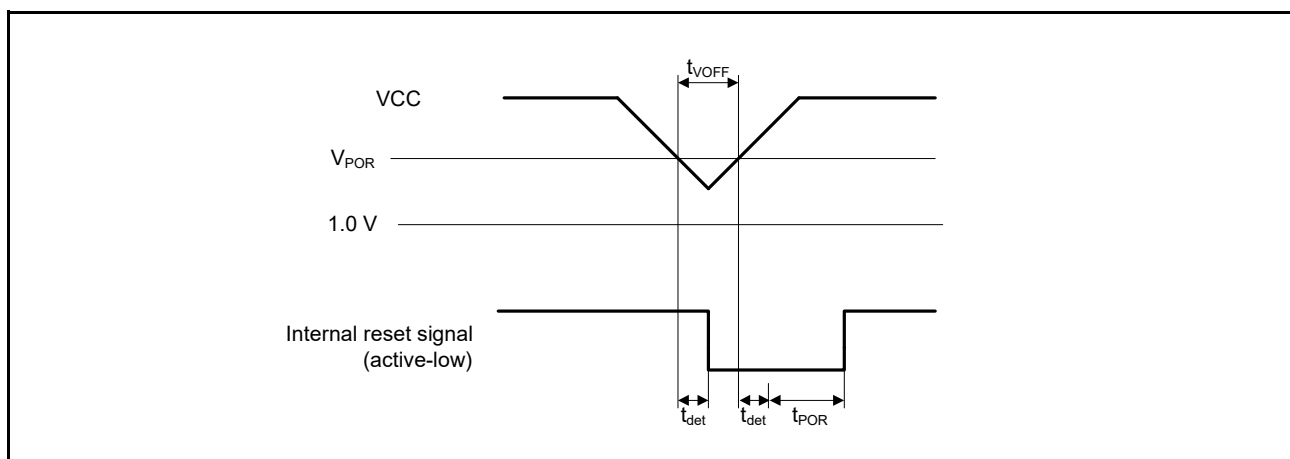
Table 2.63 Power-on reset circuit and voltage detection circuit characteristics (2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Wait time after power-on reset cancellation	LVD0:enable	t_{POR}	-	1.7	-	ms	-
	LVD0:disable	t_{POR}	-	1.3	-	ms	-
Wait time after voltage monitor 0,1,2 reset cancellation	LVD0:enable*1	$t_{LVD0,1,2}$	-	0.6	-	ms	-
	LVD0:disable*2	$t_{LVD1,2}$	-	0.2	-	ms	-
Response delay*3		t_{det}	-	-	350	μ s	Figure 2.85, Figure 2.86
Minimum VCC down time		t_{VOFF}	450	-	-	μ s	Figure 2.85, VCC = 1.0 V or above
Power-on reset enable time		t_W (POR)	1	-	-	ms	Figure 2.86, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		t_d (E-A)	-	-	300	μ s	Figure 2.88, Figure 2.89
Hysteresis width (POR)		V_{PORH}	-	110	-	mV	-
Hysteresis width (LVD0, LVD1, and LVD2)		V_{LVH}	-	60	-	mV	LVD0 selected
			-	100	-		V_{det1_0} to V_{det1_2} selected
			-	60	-		V_{det1_3} to V_{det1_g} selected
			-	50	-		V_{det1_A} or V_{det1_B} selected
			-	40	-		V_{det1_C} or V_{det1_F} selected
			-	60	-		LVD2 selected

Note 1. When OFS1.LVDAS = 0.

Note 2. When OFS1.LVDAS = 1.

Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det0} , V_{det1} , and V_{det2} for the POR/LVD.

**Figure 2.85 Voltage detection reset timing**

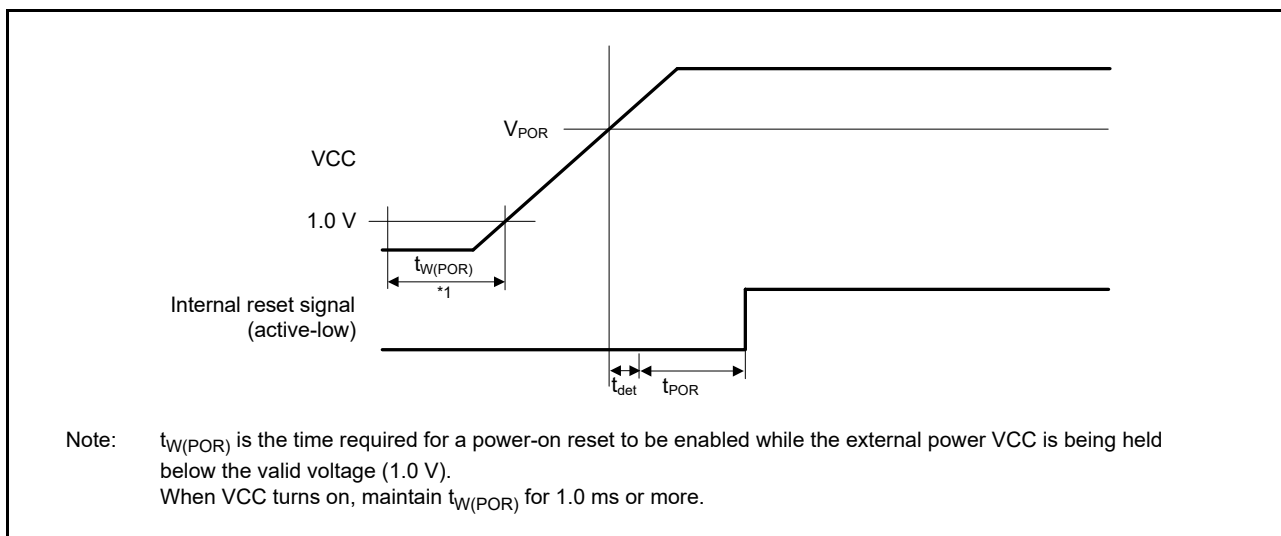


Figure 2.86 Power-on reset timing

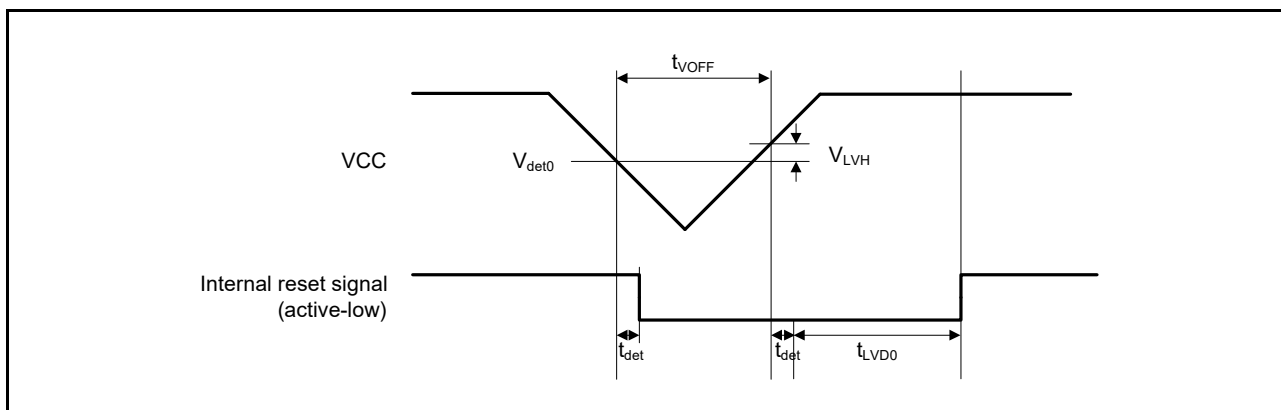


Figure 2.87 Voltage detection circuit timing (V_{det0})

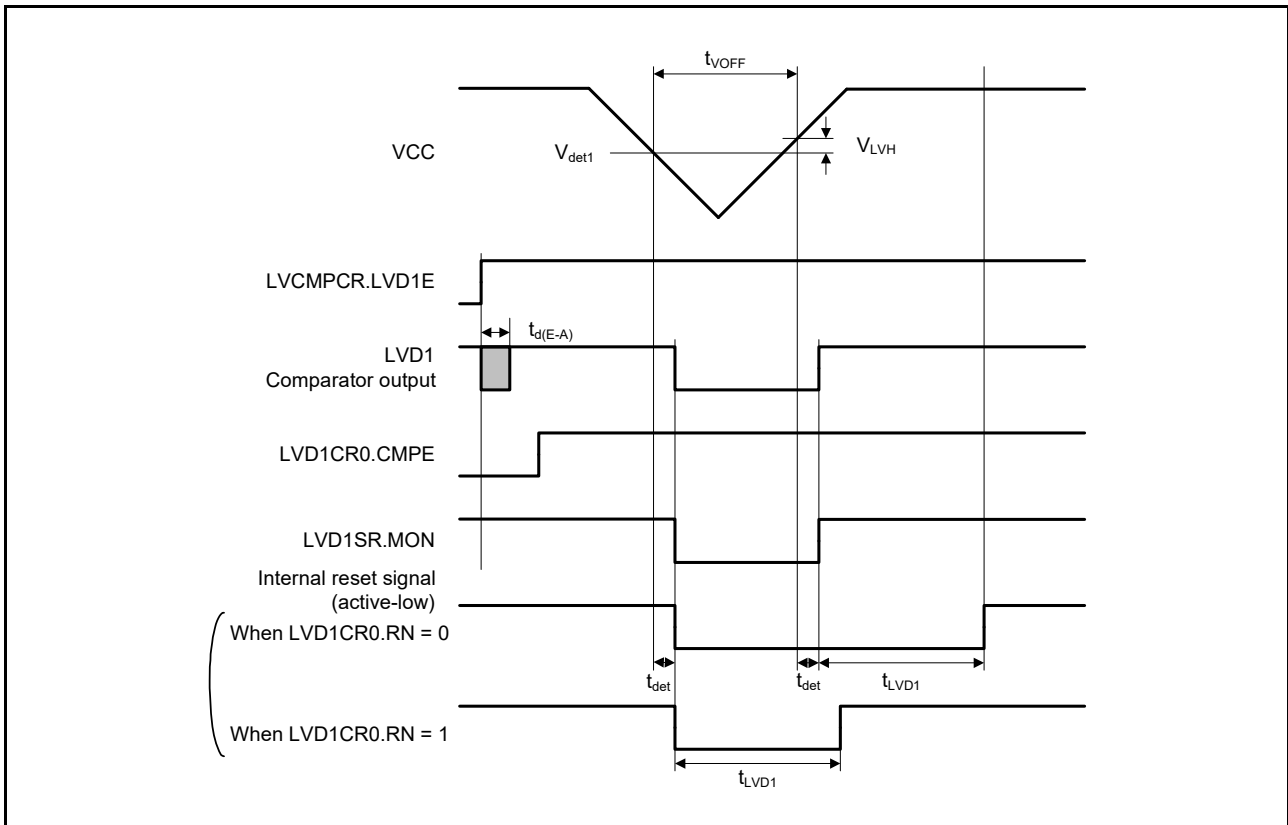


Figure 2.88 Voltage detection circuit timing (V_{det1})

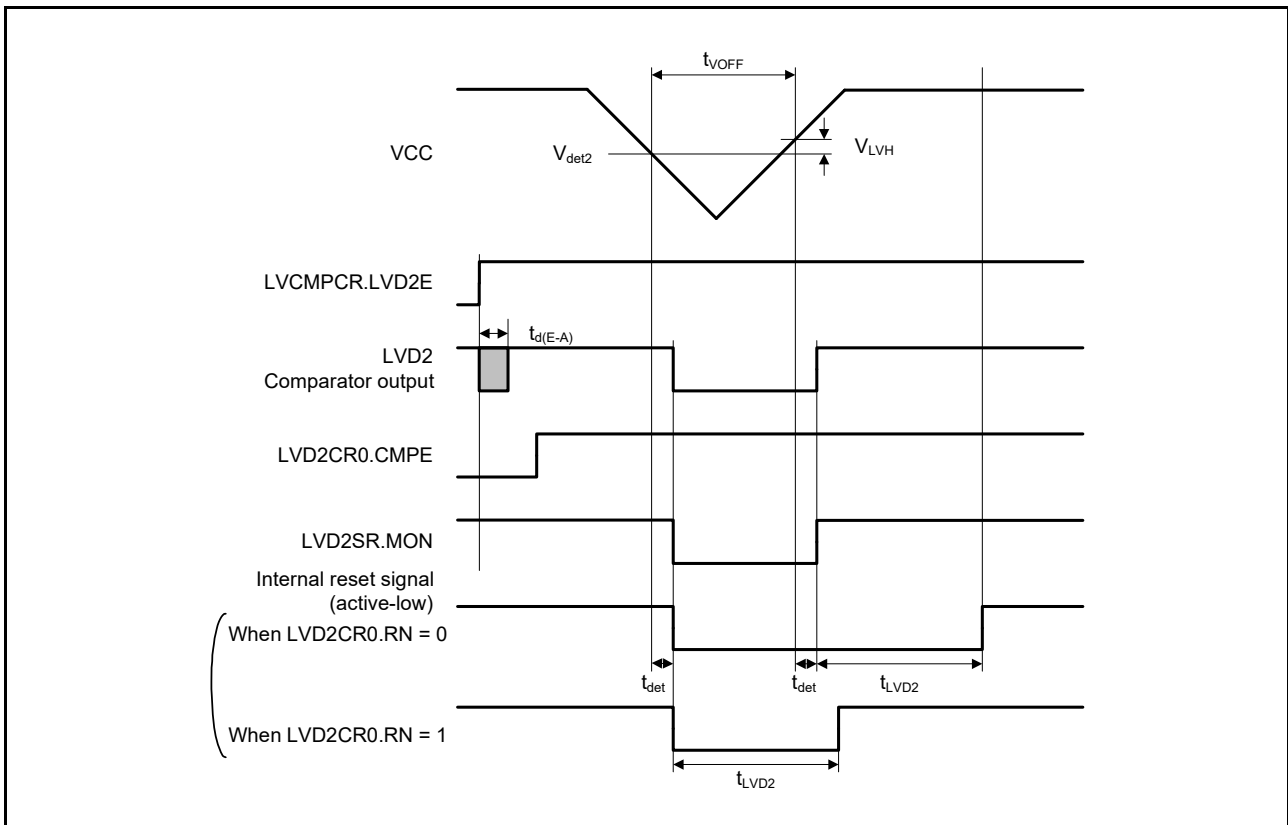


Figure 2.89 Voltage detection circuit timing (V_{det2})

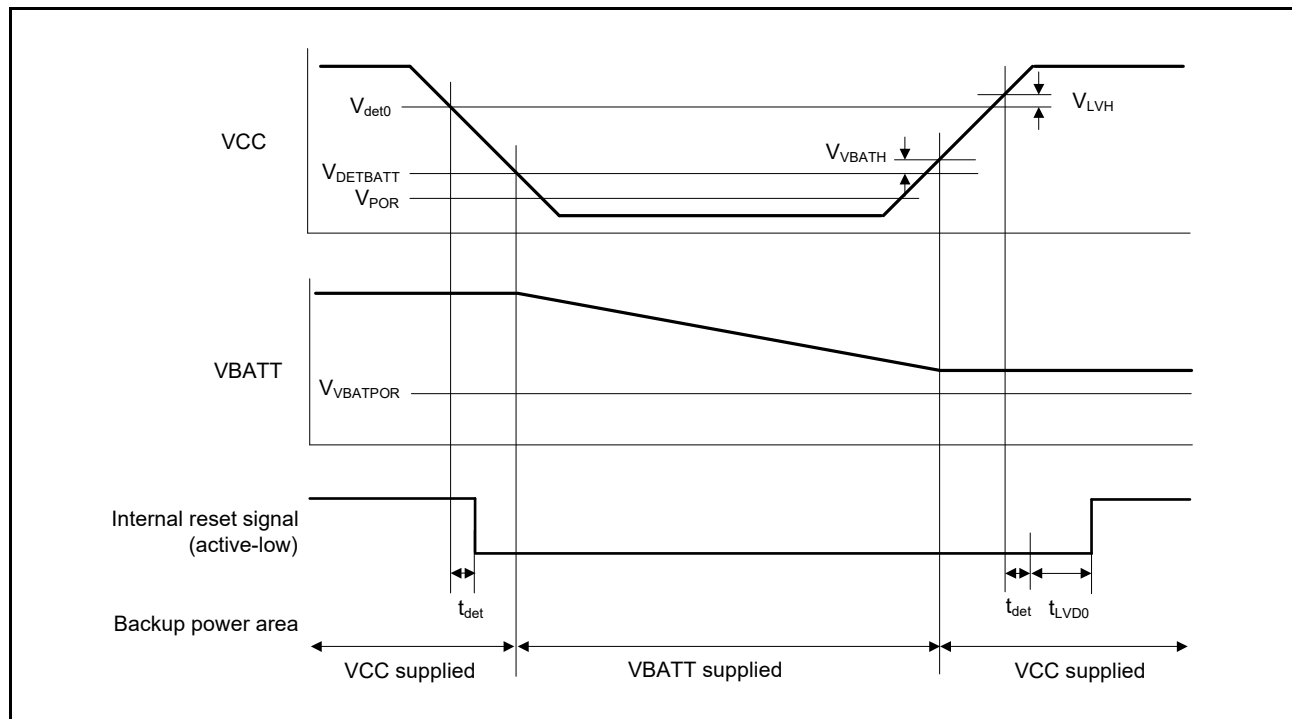
2.10 VBATT Characteristics

Table 2.64 Battery backup function characteristics

Conditions: VCC = AVCC0 = 1.6V to 5.5V, VBATT = 1.6 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
Voltage level for switching to battery backup (falling)	V_{DETBATT}	1.99	2.09	2.19	V	Figure 2.90, Figure 2.91	
Hysteresis width for switching to battery back up	V_{VBATTH}	-	100	-	mV		
VCC-off period for starting power supply switching	t_{VOFFBATT}	300	-	-	μs	-	
Voltage detection level VBATT_Power-on reset (VBATT_POR)	V_{VBATPOR}	1.30	1.40	1.50	V	Figure 2.90, Figure 2.91	
Wait time after VBATT_POR reset time cancellation	t_{VBATPOR}	-	-	3	mS	-	
Level for detection of voltage drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 10b	$V_{\text{DETBATLVD}}$	2.11	2.2	2.29	V	Figure 2.92
	VBTLVDLVL[1:0] = 11b		1.92	2	2.08	V	
Hysteresis width for VBATT pin LVD	$V_{\text{VBATLVDTH}}$	-	50	-	mV	-	
VBATT pin LVD operation stabilization time	$t_{\text{d_vbat}}$	-	-	300	μs	Figure 2.92	
VBATT pin LVD response delay time	$t_{\text{det_vbat}}$	-	-	350	μs	-	
Allowable voltage change rising/falling gradient	$dt/dVCC$	1.0	-	-	ms/V	-	
VCC voltage level for access to the VBATT backup registers	V_{BKBATT}	1.8	-	-	V	-	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup (V_{DETBATT}).

**Figure 2.90 Power supply switching and LVD0 reset timing**

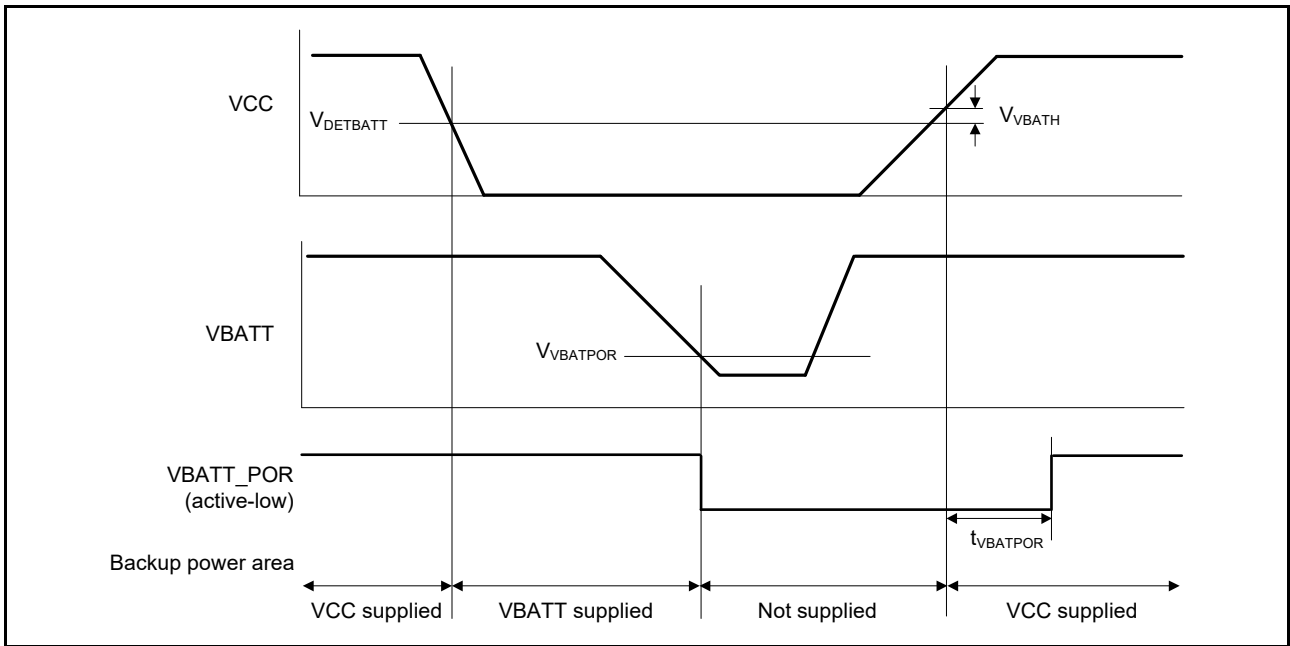


Figure 2.91 VBATT_POR reset timing

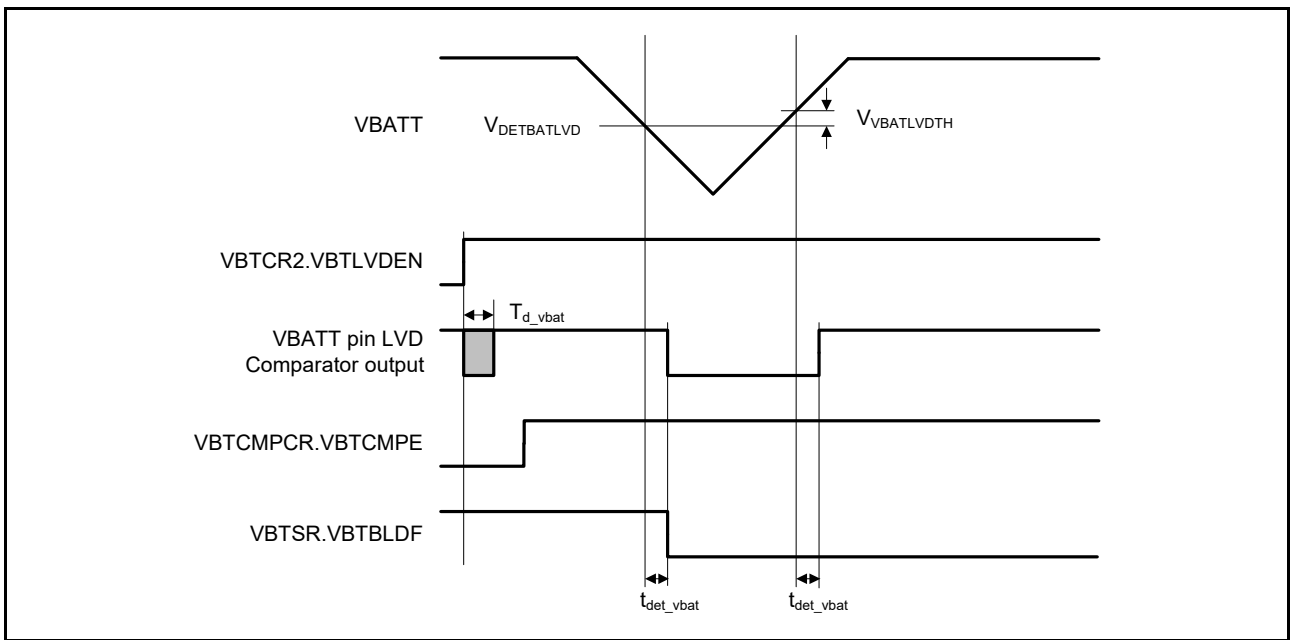


Figure 2.92 VBATT pin voltage detection circuit timing

Table 2.65 VBATT-I/O characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
VBATWIO n I/O output characteristics (n = 0 to 2)	VCC > V _{DET} BATT	VCC = 4.0 to 5.5 V	V _{OH}	VCC - 0.8	-	-	V	I _{OH} = -200 μA
			V _{OL}	-	-	0.8		I _{OL} = 200 μA
		VCC = 2.7 to 4.0 V	V _{OH}	VCC - 0.5	-	-		I _{OH} = -100 μA
			V _{OL}	-	-	0.5		I _{OL} = 100 μA
		VCC = V _{DET} BATT to 2.7 V	V _{OH}	VCC - 0.3	-	-		I _{OH} = -50 μA
			V _{OL}	-	-	0.3		I _{OL} = 50 μA
	VCC < V _{DET} BATT	VBATT = 2.7 to 3.6 V	V _{OH}	V _{BATT} - 0.5	-	-		I _{OH} = -100 μA
			V _{OL}	-	-	0.5		I _{OL} = 100 μA
		VBATT = 1.6 to 2.7 V	V _{OH}	V _{BATT} - 0.3	-	-		I _{OH} = -50 μA
			V _{OL}	-	-	0.3		I _{OL} = 50 μA

2.11 CTSU Characteristics

Table 2.66 CTSU characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C _{tscap}	9	10	11	nF	-
TS pin capacitive load	C _{base}	-	-	50	pF	-
Permissible output high current	ΣI _{oH}	-	-	-24	mA	When the mutual capacitance method is applied

2.12 Segment LCD Controller Characteristics

2.12.1 Resistance Division Method

[Static Display Mode]

Table 2.67 Resistance division method LCD characteristics (1)

Conditions: $V_{L4} \leq V_{CC} \leq 5.5 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.0	-	VCC	V	-

[1/2 Bias Method, 1/4 Bias Method]

Table 2.68 Resistance division method LCD characteristics (2)

Conditions: $V_{L4} \leq V_{CC} \leq 5.5 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.7	-	VCC	V	-

[1/3 Bias Method]

Table 2.69 Resistance division method LCD characteristics (3)

Conditions: $V_{L4} \leq V_{CC} \leq 5.5 \text{ V}$

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
LCD drive voltage	V_{L4}	2.5	-	VCC	V	-

2.12.2 Internal Voltage Boosting Method

[1/3 Bias Method]

Table 2.70 Internal voltage boosting method LCD characteristics

Conditions: $V_{CC} = 1.8 \text{ V to } 5.5 \text{ V}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions	
LCD output voltage variation range	V_{L1}	C1 to C4*1 = 0.47 μF	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
			VLCD = 0Ch	1.30	1.40	1.48	V	-
			VLCD = 0Dh	1.35	1.45	1.53	V	-
			VLCD = 0Eh	1.40	1.50	1.58	V	-
			VLCD = 0Fh	1.45	1.55	1.63	V	-
			VLCD = 10h	1.50	1.60	1.68	V	-
			VLCD = 11h	1.55	1.65	1.73	V	-
VLCD = 12h	1.60	1.70	1.78	V	-			
VLCD = 13h	1.65	1.75	1.83	V	-			
Doubler output voltage	V_{L2}	C1 to C4*1 = 0.47 μF	$2 \times V_{L1} - 0.1$	$2 \times V_{L1}$	$2 \times V_{L1}$	V	-	
Tripler output voltage	V_{L4}	C1 to C4*1 = 0.47 μF	$3 \times V_{L1} - 0.15$	$3 \times V_{L1}$	$3 \times V_{L1}$	V	-	
Reference voltage setup time*2	t_{VL1S}		5	-	-	ms	Figure 2.93	
LCD output voltage variation range*3	t_{VLWT}	C1 to C4*1 = 0.47 μF	500	-	-	ms		

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND
 C3: A capacitor connected between VL2 and GND
 C4: A capacitor connected between VL4 and GND
 C1 = C2 = C3 = C4 = 0.47 μ F \pm 30%

Note 2. This is the time required to wait from when the reference voltage is specified using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET[1:0] bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

[1/4 Bias Method]

Table 2.71 Internal voltage boosting method LCD characteristics

Conditions: VCC = 1.8 V to 5.5 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions	
LCD output voltage variation range	V_{L1}	C1 to C5*1 = 0.47 μ F	VLCD = 04h	0.90	1.0	1.08	V	-
			VLCD = 05h	0.95	1.05	1.13	V	-
			VLCD = 06h	1.00	1.10	1.18	V	-
			VLCD = 07h	1.05	1.15	1.23	V	-
			VLCD = 08h	1.10	1.20	1.28	V	-
			VLCD = 09h	1.15	1.25	1.33	V	-
			VLCD = 0Ah	1.20	1.30	1.38	V	-
			VLCD = 0Bh	1.25	1.35	1.43	V	-
		VLCD = 0Ch	1.30	1.40	1.48	V	-	
Doubler output voltage	V_{L2}	C1 to C5*1 = 0.47 μ F	$2V_{L1} - 0.08$	$2V_{L1}$	$2V_{L1}$	V	-	
Tripler output voltage	V_{L3}	C1 to C5*1 = 0.47 μ F	$3V_{L1} - 0.12$	$3V_{L1}$	$3V_{L1}$	V	-	
Quadruply output voltage	V_{L4} *4	C1 to C5*1 = 0.47 μ F	$4V_{L1} - 0.16$	$4V_{L1}$	$4V_{L1}$	V	-	
Reference voltage setup time*2	t_{VL1S}		5	-	-	ms	Figure 2.93	
LCD output voltage variation range*3	t_{VLWT}	C1 to C5*1 = 0.47 μ F	500	-	-	ms		

Note 1. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL
 C2: A capacitor connected between VL1 and GND
 C3: A capacitor connected between VL2 and GND
 C4: A capacitor connected between VL3 and GND
 C5: A capacitor connected between VL4 and GND
 C1 = C2 = C3 = C4 = C5 = 0.47 μ F \pm 30%

Note 2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected (by setting the MDSET1 and MDSET0 bits in the LCDM0 register to 01b) if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

Note 3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 4. V_{L4} must be 5.5 V or lower.

2.12.3 Capacitor Split Method

[1/3 Bias Method]

Table 2.72 Internal voltage boosting method LCD characteristics

Conditions: VCC = 2.2 V to 5.5 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage*1	V_{L4}	C1 to C4 = 0.47 μ F*2	-	VCC	-	V	-
VL2 voltage*1	V_{L2}	C1 to C4 = 0.47 μ F*2	$2/3 \times V_{L4} - 0.07$	$2/3 \times V_{L4}$	$2/3 \times V_{L4} + 0.07$	V	-
VL1 voltage*1	V_{L1}	C1 to C4 = 0.47 μ F*2	$1/3 \times V_{L4} - 0.08$	$1/3 \times V_{L4}$	$1/3 \times V_{L4} + 0.08$	V	-
Capacitor split wait time*1	t_{WAIT}		100	-	-	ms	Figure 2.93

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between VL1 and GND

C3: A capacitor connected between VL2 and GND

C4: A capacitor connected between VL4 and GND

C1 = C2 = C3 = C4 = 0.47 μ F \pm 30%.

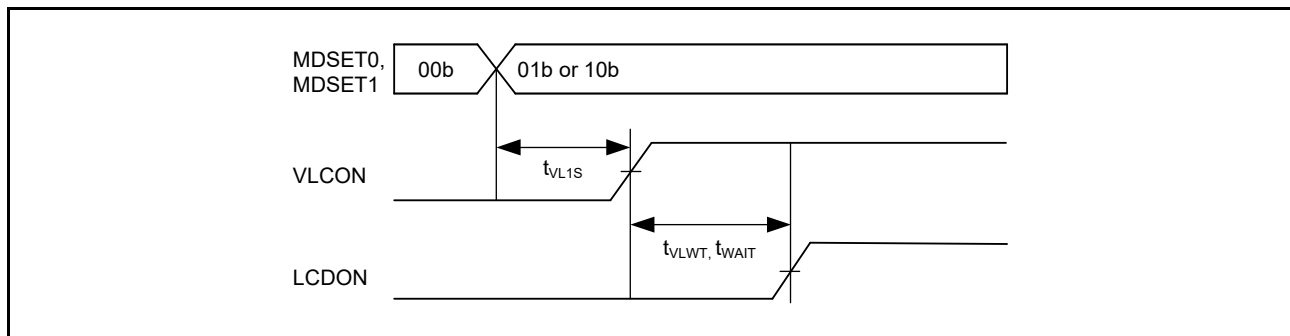


Figure 2.93 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

2.13 Comparator Characteristics

Table 2.73 ACMPLP characteristics

Conditions: VCC = 1.8 to 5.5 V

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Reference voltage range	Standard mode	IVREFn (n=0,1)	VREF	0	-	VCC-1.4	V	-
	Window mode*2	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC-1.4	V	-
Input voltage range		VI	0	-	VCC	V	-	
Internal reference voltage		-	1.36	1.44	1.50	V	-	
Output delay	High-speed mode	Td	-	-	1.2	μ s	VCC = 3.0 Slew rate of input signal > 50 mV/ μ s	
	Low-speed mode		-	-	5	μ s		
	Window mode		-	-	2	μ s		
Offset voltage*1	High-speed mode	-	-	-	50	mV	-	
	Low-speed mode	-	-	-	40	mV	-	
	Window mode	-	-	-	60	mV	-	
Operation stabilization wait time		T _{cmp}	100	-	-	μ s	-	

Note 1. When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to $2.5 \times VCC/256$.

Note 2. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 \geq 0.2 V.

2.14 OPAMP Characteristics

Table 2.74 OPAMP characteristics

Conditions: VCC = AVCC0 = 1.8 to 5.5 V (AVCC0 = VCC when VCC < 2.0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Common mode input range	Vicm1	Low-power mode	0.2	-	AVCC0 – 0.5	V	
	Vicm2	High-speed mode	0.3	-	AVCC0 – 0.6	V	
Output voltage range	Vo1	Low-power mode	0.1	-	AVCC0 – 0.1	V	
	Vo2	High-speed mode	0.1	-	AVCC0 – 0.1	V	
Input offset voltage	Vioff	3 σ	-10	-	10	mV	
Open gain	Av		60	120	-	dB	
Gain-bandwidth (GB) product	GBW1	Low-power mode	-	0.04	-	MHz	
	GBW2	High-speed mode	-	1.7	-	MHz	
Phase margin	PM	CL = 20 pF	50	-	-	deg	
Gain margin	GM	CL = 20 pF	10	-	-	dB	
Equivalent input noise	Vnoise1	f = 1 kHz	Low-power mode	-	230	-	nV/ $\sqrt{\text{Hz}}$
	Vnoise2	f = 10 kHz		-	200	-	nV/ $\sqrt{\text{Hz}}$
	Vnoise3	f = 1 kHz	High-speed mode	-	90	-	nV/ $\sqrt{\text{Hz}}$
	Vnoise4	f = 2 kHz		-	70	-	nV/ $\sqrt{\text{Hz}}$
Power supply reduction ratio	PSRR		-	90	-	dB	
Common mode signal reduction ratio	CMRR		-	90	-	dB	
Stabilization wait time	Tstd1	CL = 20 pF Only operational amplifier is activated *1	Low-power mode	650	-	-	μs
	Tstd2		High-speed mode	13	-	-	μs
	Tstd3	CL = 20 pF Operational amplifier and reference current circuit are activated simultaneously	Low-power mode	650	-	-	μs
	Tstd4		High-speed mode	13	-	-	μs
Settling time	Tset1	CL = 20 pF	Low-power mode	-	-	750	μs
	Tset2		High-speed mode	-	-	13	μs
Slew rate	Tslew1	CL = 20 pF	Low-power mode	-	0.02	-	V/ μs
	Tslew2		High-speed mode	-	1.1	-	V/ μs
Load current	Iload1	Low power mode	-100	-	100	μA	
	Iload2	High-speed mode	-100	-	100	μA	
Load capacitance	CL		-	-	20	pF	

Note 1. When the operational amplifier reference current circuit is activated in advance.

2.15 Flash Memory Characteristics

2.15.1 Code Flash Memory Characteristics

Table 2.75 Code flash characteristics (1)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erasure cycle*1	N _{PEC}	1000	-	-	Times	-
Data hold time	After 1000 times of N _{PEC}	t _{DRP}	20*2, *3	-	-	Year T _a = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 1,000), erasing can be done n times for each block. For instance, when 8-byte programming is performed 256 times for different addresses in 2-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled (overwriting is prohibited).

Note 2. Characteristic when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. This result is obtained from reliability testing.

Table 2.76 Code flash characteristics (2)

High-speed operating mode

Conditions: VCC = 2.7 to 5.5 V

Parameter	Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
Programming time	8-byte	t _{P8}	-	116	998	-	54	506	μs
Erasure time	2-KB	t _{E2K}	-	9.03	287	-	5.67	222	ms
Blank check time	8-byte	t _{BC8}	-	-	56.8	-	-	16.6	μs
	2-KB	t _{BC2K}	-	-	1899	-	-	140	μs
Erase suspended time		t _{SED}	-	-	22.5	-	-	10.7	μs
Startup area switching setting time		t _{SAS}	-	21.7	585	-	12.1	447	ms
Access window time		t _{AWS}	-	21.7	585	-	12.1	447	ms
OCD/serial programmer ID setting time		t _{OSIS}	-	21.7	585	-	12.1	447	ms
Flash memory mode transition wait time 1		t _{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t _{MS}	5	-	-	5	-	-	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

Table 2.77 Code flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	8-byte	t _{PG}	-	157	1411	-	101	966	μs
Erase time	2-KB	t _{E2K}	-	9.10	289	-	6.10	228	ms
Blank check time	8-byte	t _{BC8}	-	-	87.7	-	-	52.5	μs
	2-KB	t _{BC2K}	-	-	1930	-	-	414	μs
Erase suspended time		t _{SED}	-	-	32.7	-	-	21.6	μs
Startup area switching setting time		t _{SAS}	-	22.5	592	-	14.0	464	ms
Access window time		t _{AWS}	-	22.5	592	-	14.0	464	ms
OCD/serial programmer ID setting time		t _{OSIS}	-	22.5	592	-	14.0	464	ms
Flash memory mode transition wait time 1		t _{DIS}	2	-	-	2	-	-	μs
Flash memory mode transition wait time 2		t _{MS}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

2.15.2 Data Flash Memory Characteristics

Table 2.78 Data flash characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Reprogramming/erase cycle*1		N _{DPEC}	100000	1000000	-	Times	-
Data hold time	After 10000 times of N _{DPEC}	t _{DDRP}	20*2, *3	-	-	Year	Ta = +85°C
	After 100000 times of N _{DPEC}		5*2, *3	-	-	Year	
	After 1000000 times of N _{DPEC}		-	1*2, *3	-	-	Year

Note 1. The reprogram/erase cycle is the number of erasure for each block. When the reprogram/erase cycle is n times (n = 100,000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1,000 times for different addresses in 1-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasure is not enabled. (overwriting is prohibited).

Note 2. Characteristics when using the flash memory programmer and the self-programming library provided by Renesas Electronics.

Note 3. These results are obtained from reliability testing.

Table 2.79 Data flash characteristics (2)

High-speed operating mode

Conditions: VCC = 2.7 to 5.5 V

Parameter		Symbol	FCLK = 4 MHz			FCLK = 32 MHz			Unit
			Min	Typ	Max	Min	Typ	Max	
Programming time	1-byte	t _{DP1}	-	52.4	463	-	42.1	387	μs
Erase time	1-KB	t _{DE1K}	-	8.98	286	-	6.42	237	ms
Blank check time	1-byte	t _{DBC1}	-	-	24.3	-	-	16.6	μs
	1-KB	t _{DBC1K}	-	-	1872	-	-	512	μs
Suspended time during erasing		t _{DSED}	-	-	13.0	-	-	10.7	μs
Data flash STOP recovery time		t _{DSTOP}	5	-	-	5	-	-	μs

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

Table 2.80 Data flash characteristics (3)

Middle-speed operating mode

Conditions: VCC = 1.8 to 5.5 V, Ta = -40 to +85°C

Parameter	Symbol	FCLK = 4 MHz			FCLK = 8 MHz			Unit	
		Min	Typ	Max	Min	Typ	Max		
Programming time	1-byte	t _{DP1}	-	94.7	886	-	89.3	849	μs
Erase time	1-KB	t _{DE1K}	-	9.59	299	-	8.29	273	ms
Blank check time	1-byte	t _{DBC1}	-	-	56.2	-	-	52.5	μs
	1-KB	t _{DBC1K}	-	-	2.17	-	-	1.51	ms
Suspended time during erasing		t _{DSER}	-	-	23.0	-	-	21.7	μs
Data flash STOP recovery time		t _{DSTOP}	720	-	-	720	-	-	ns

Note: Does not include the time until each operation of the flash memory is started after instructions are executed by software.

Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note: The frequency accuracy of FCLK must be ±3.5%. Confirm the frequency accuracy of the clock source.

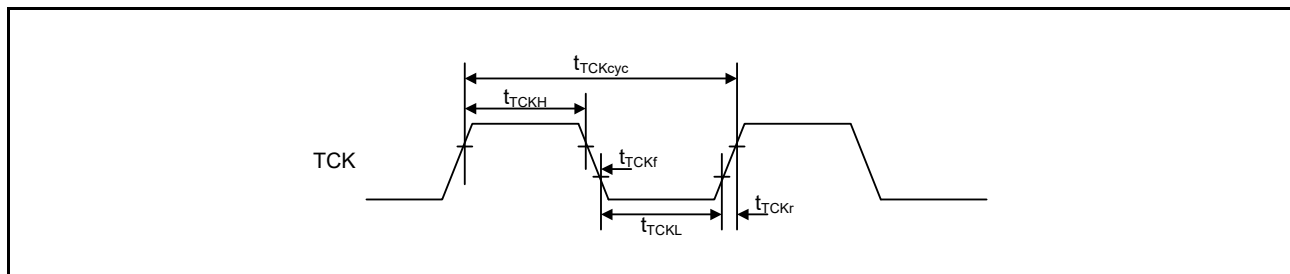
2.16 Boundary Scan

Table 2.81 Boundary scan

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t _{TCKcyc}	100	-	-	ns	Figure 2.94
TCK clock high pulse width	t _{TCKH}	45	-	-	ns	
TCK clock low pulse width	t _{TCKL}	45	-	-	ns	
TCK clock rise time	t _{TCKr}	-	-	5	ns	
TCK clock fall time	t _{TCKf}	-	-	5	ns	
TMS setup time	t _{TMSS}	20	-	-	ns	Figure 2.95
TMS hold time	t _{TMSH}	20	-	-	ns	
TDI setup time	t _{TDIS}	20	-	-	ns	
TDI hold time	t _{TDIH}	20	-	-	ns	
TDO data delay	t _{TDOD}	-	-	70	ns	Figure 2.96
Boundary Scan circuit start up time*1	t _{BSSTUP}	t _{RESWP}	-	-	-	

Note 1. Boundary scan does not function until power-on-reset becomes negative.

**Figure 2.94 Boundary scan TCK timing**

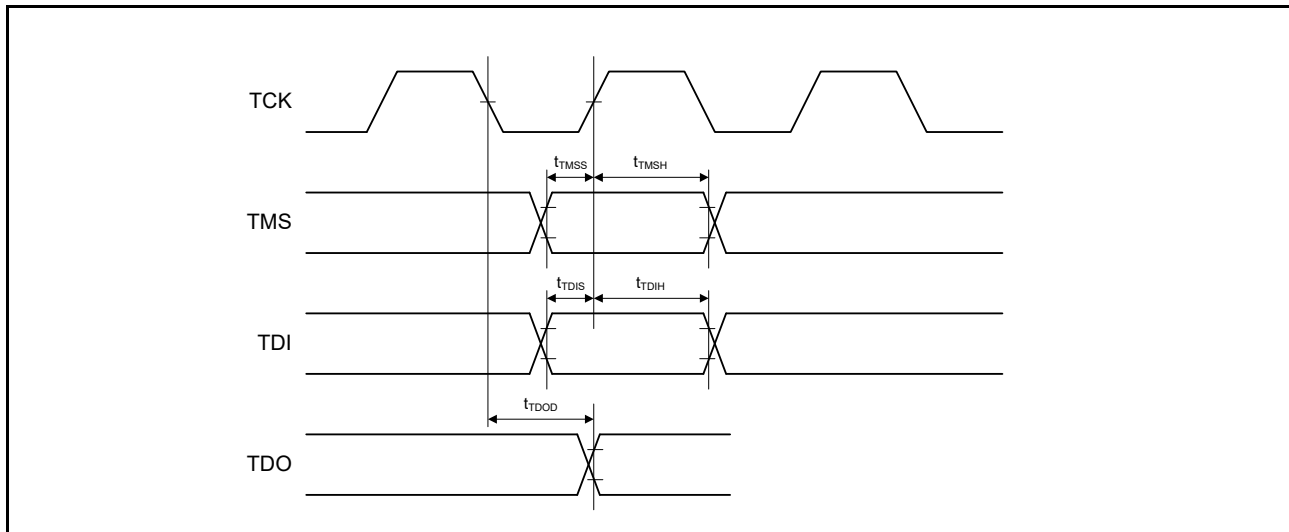


Figure 2.95 Boundary scan input/output timing

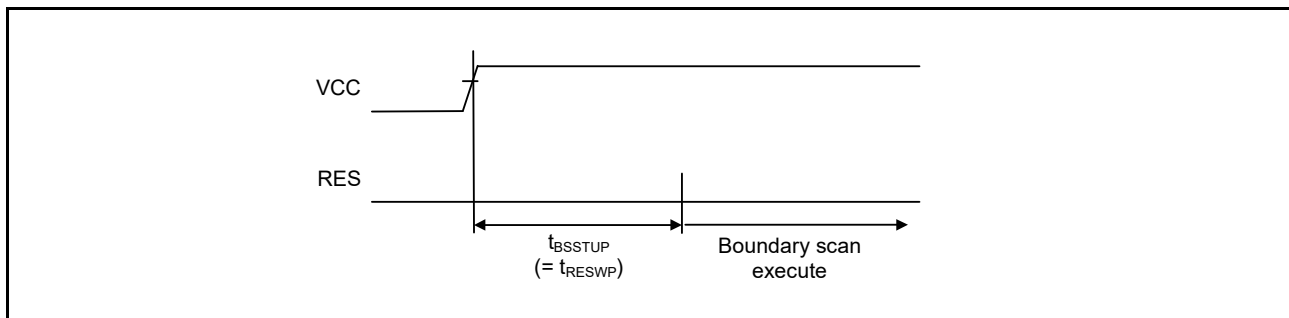


Figure 2.96 Boundary scan circuit start up timing

2.17 Joint Test Action Group (JTAG)

Table 2.82 JTAG (debug) characteristics (1)

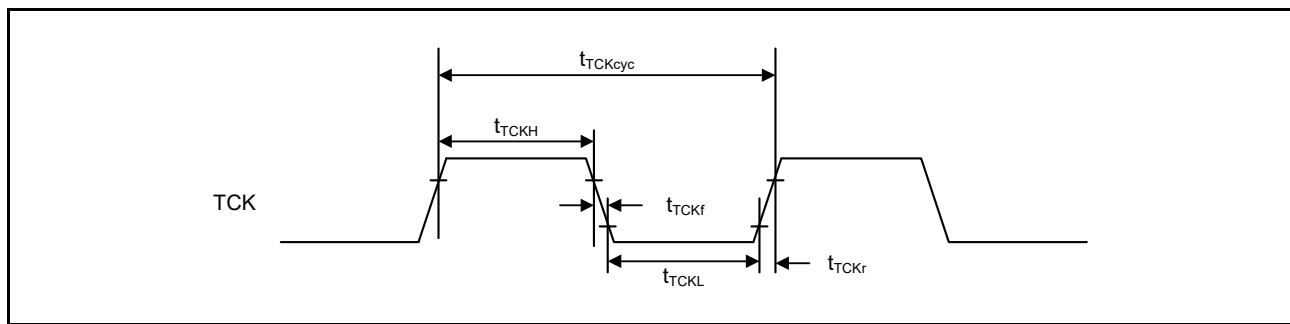
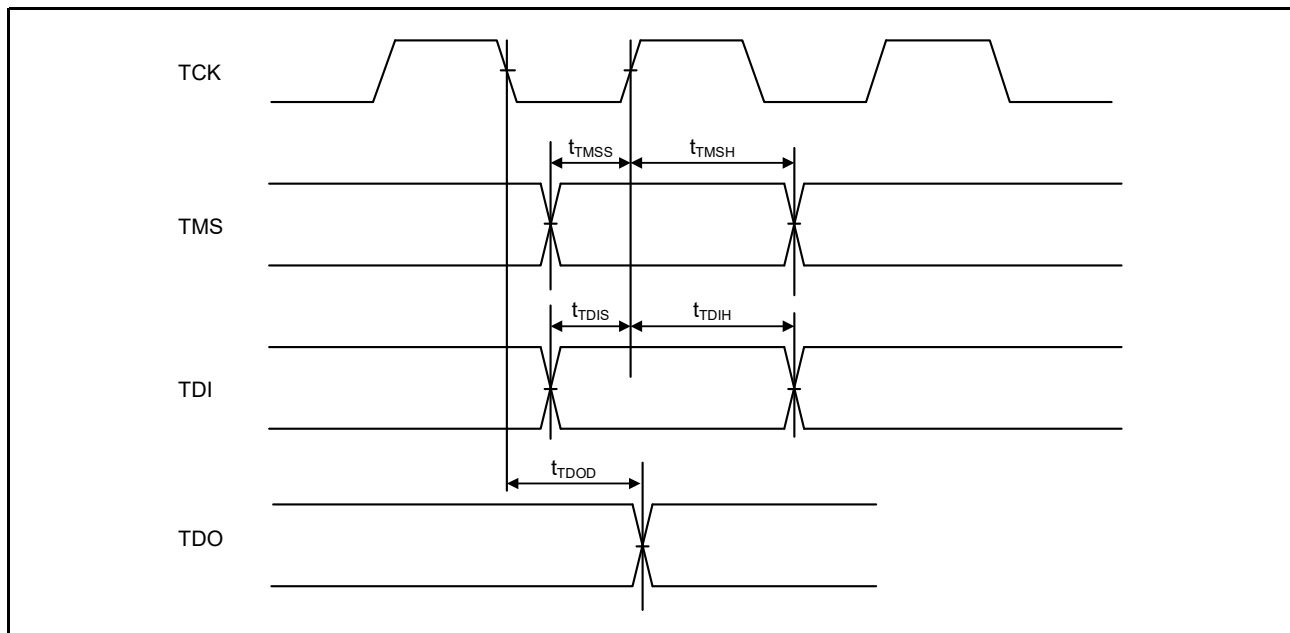
Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	80	-	-	ns	Figure 2.97
TCK clock high pulse width	t_{TCKH}	35	-	-	ns	
TCK clock low pulse width	t_{TCKL}	35	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	16	-	-	ns	Figure 2.98
TMS hold time	t_{TMSh}	16	-	-	ns	
TDI setup time	t_{TDis}	16	-	-	ns	
TDI hold time	t_{TDIH}	16	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	70	ns	

Table 2.83 JTAG (debug) characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	250	-	-	ns	Figure 2.97
TCK clock high pulse width	t_{TCKH}	120	-	-	ns	
TCK clock low pulse width	t_{TCKL}	120	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	50	-	-	ns	Figure 2.98
TMS hold time	t_{TMSh}	50	-	-	ns	
TDI setup time	t_{TDis}	50	-	-	ns	
TDI hold time	t_{TDIH}	50	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	150	ns	

**Figure 2.97 JTAG TCK timing****Figure 2.98 JTAG input/output timing**

2.17.1 Serial Wire Debug (SWD)

Table 2.84 SWD characteristics (1)

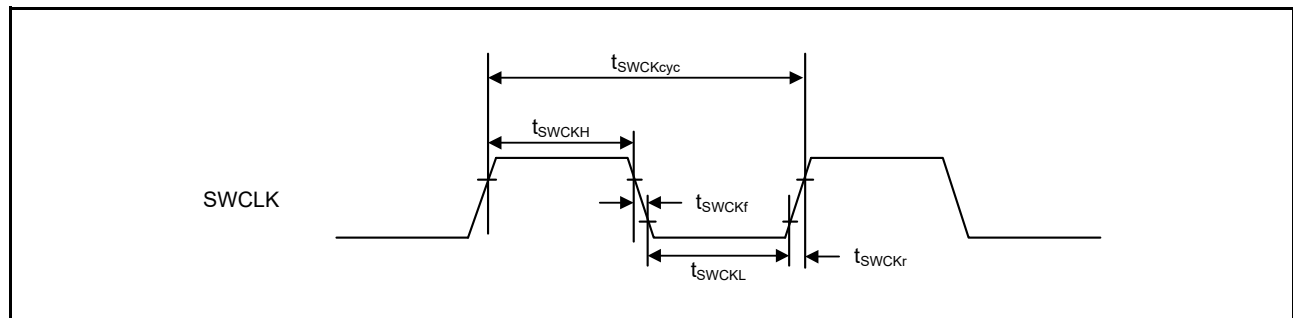
Conditions: VCC = 2.4 to 5.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t_{SWCKcyc}	80	-	-	ns	Figure 2.99
SWCLK clock high pulse width	t_{SWCKH}	35	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	35	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	16	-	-	ns	Figure 2.100
SWDIO hold time	t_{SWDH}	16	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	70	ns	

Table 2.85 SWD characteristics (2)

Conditions: VCC = 1.6 to 2.4 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	t_{SWCKcyc}	250	-	-	ns	Figure 2.99
SWCLK clock high pulse width	t_{SWCKH}	120	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	120	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	50	-	-	ns	Figure 2.100
SWDIO hold time	t_{SWDH}	50	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	150	ns	

**Figure 2.99 SWD SWCLK timing**

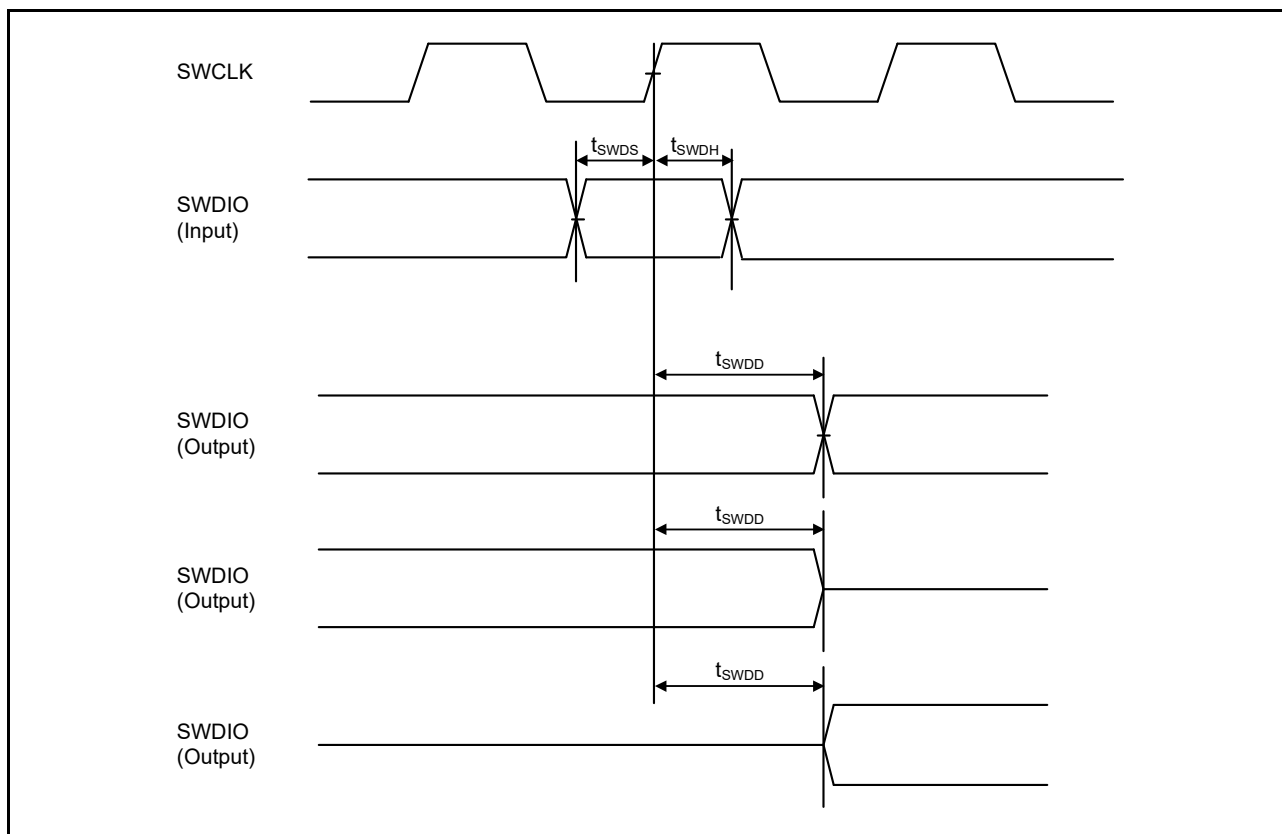


Figure 2.100 SWD input/output timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings is displayed in “Packages” on the Renesas Electronics Corporation website.

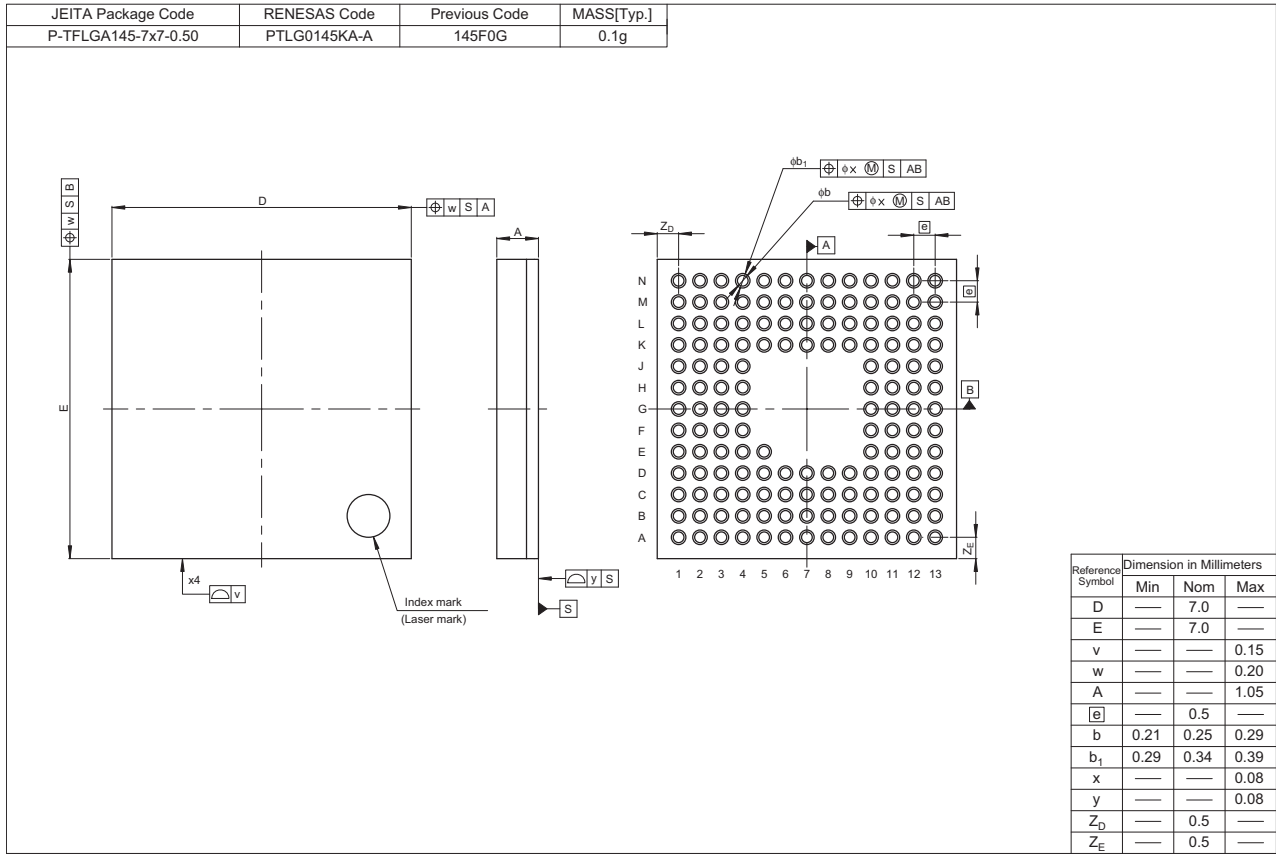


Figure 1.1 LGA 145-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm

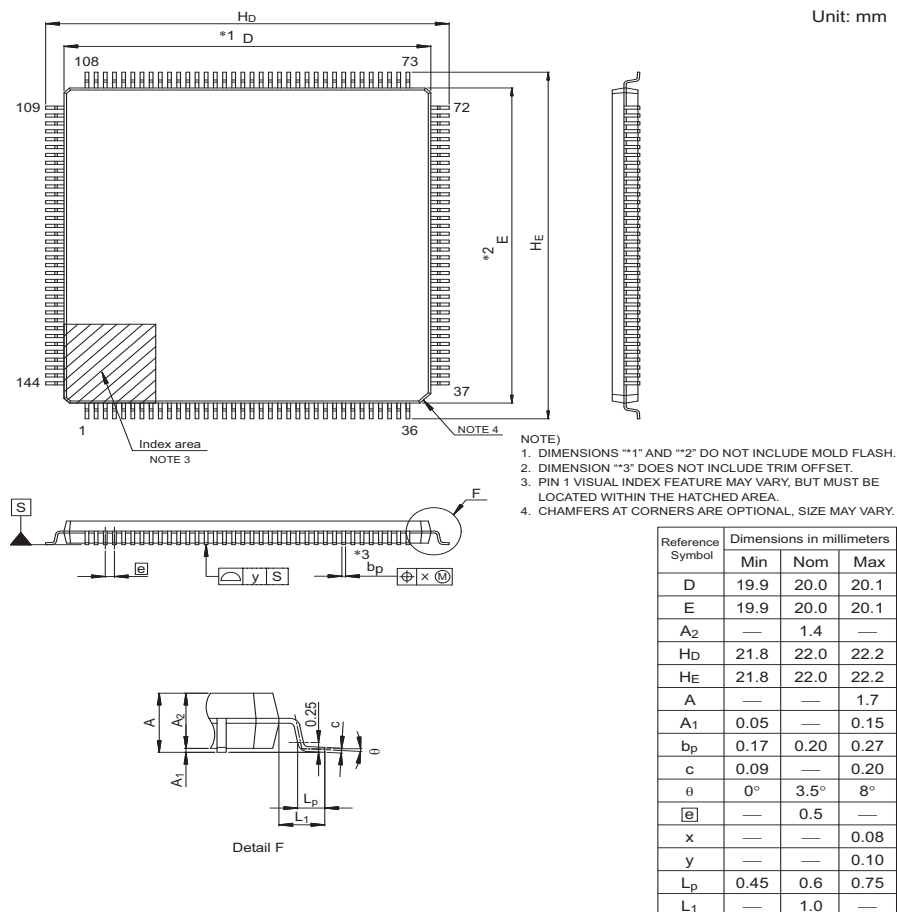
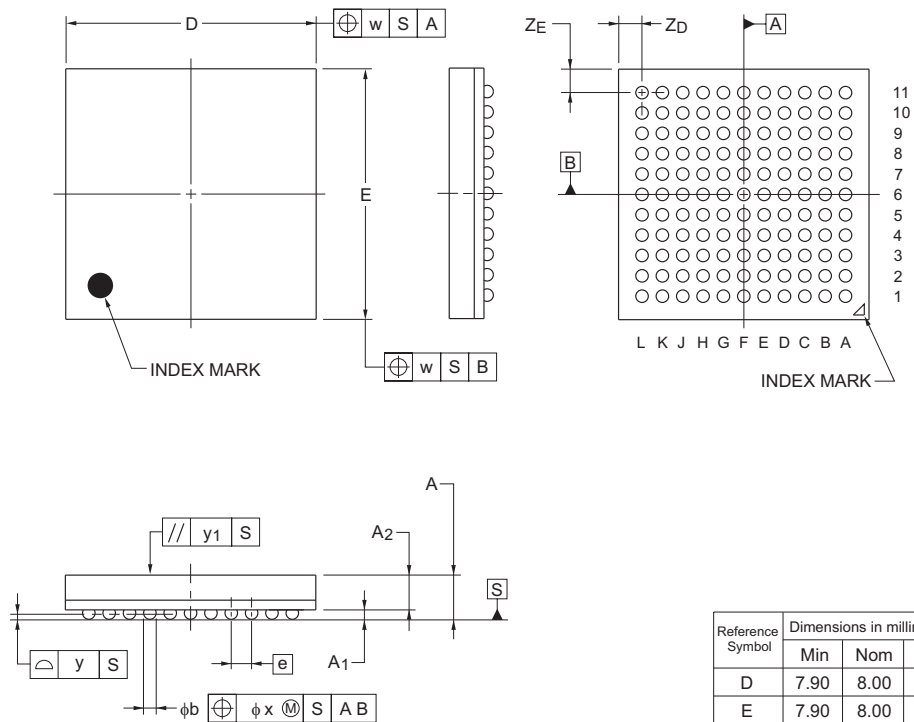


Figure 1.2 LQFP 144-pin

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JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFBGA121-8x8-0.65	PLBG0121JA-A	—	0.15

Unit: mm



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	7.90	8.00	8.10
E	7.90	8.00	8.10
w	—	0.20	—
A	1.11	1.21	1.31
A ₁	0.25	0.30	0.35
A ₂	—	0.91	—
e	—	0.65	—
b	0.35	0.40	0.45
x	—	0.08	—
y	—	0.10	—
y ₁	—	0.20	—
Z _D	—	0.75	—
Z _E	—	0.75	—

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Figure 1.3 BGA 121-pin

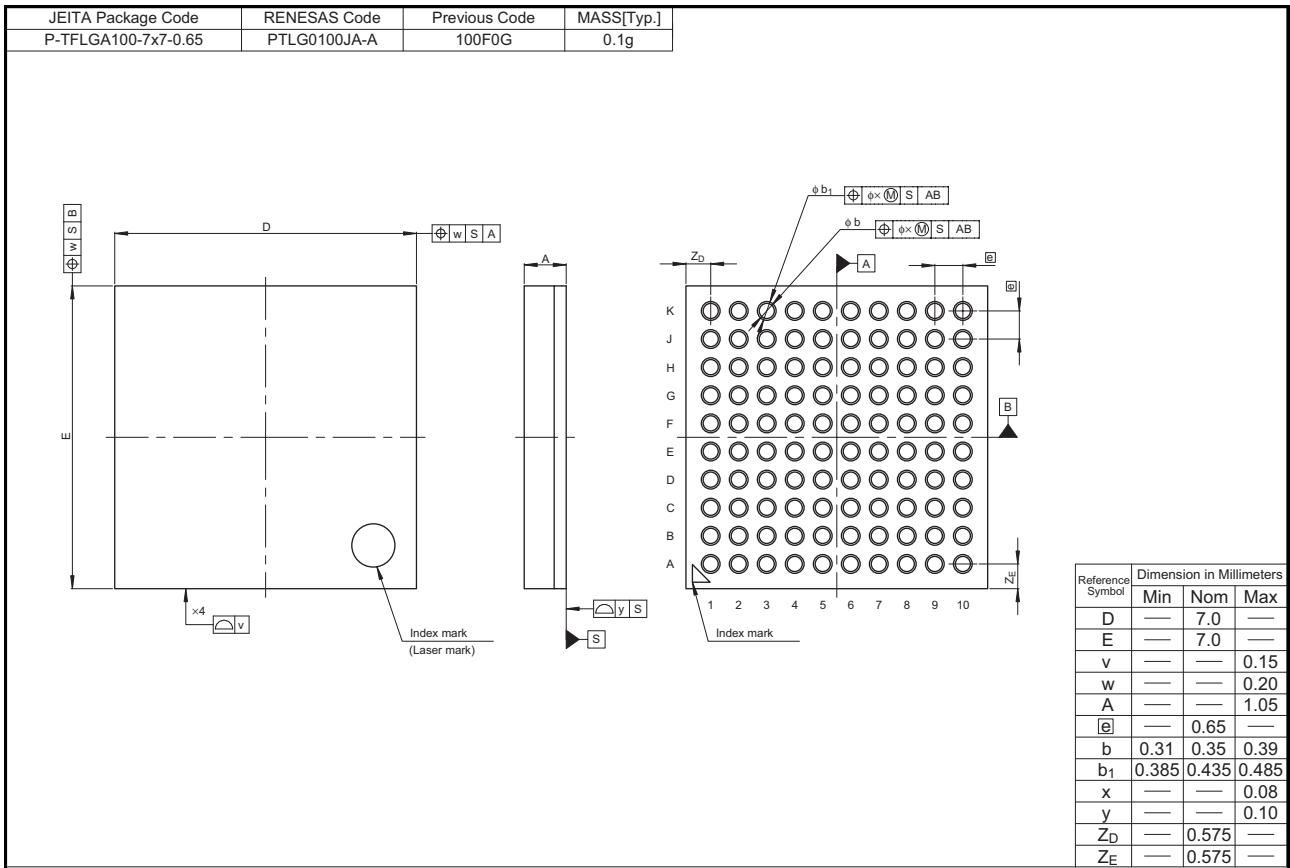
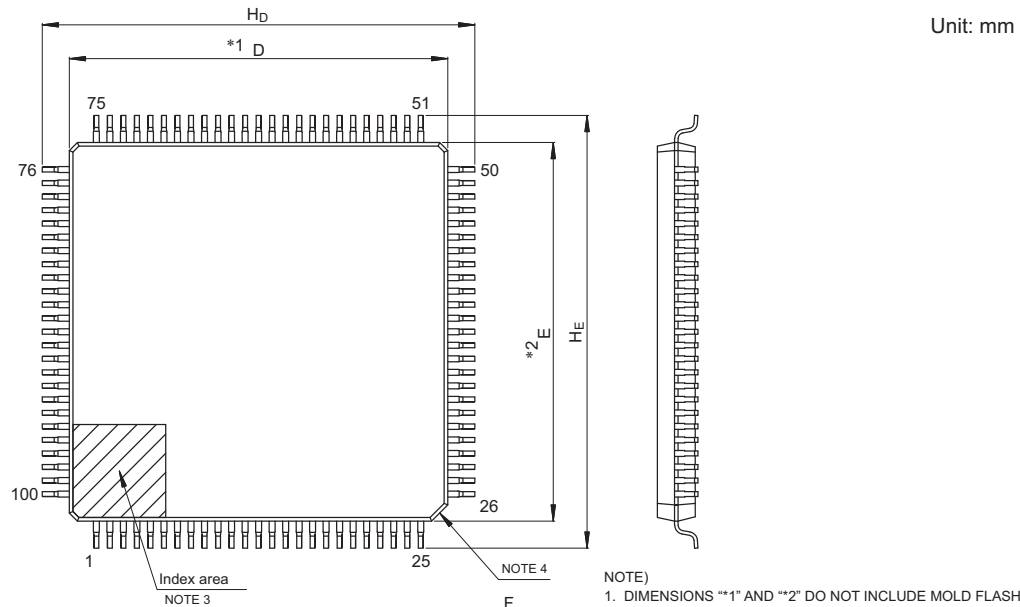


Figure 1.4 LGA 100-pin

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6



- NOTE)
1. DIMENSIONS “*1” AND “*2” DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION “*3” DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

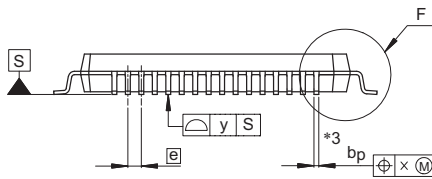
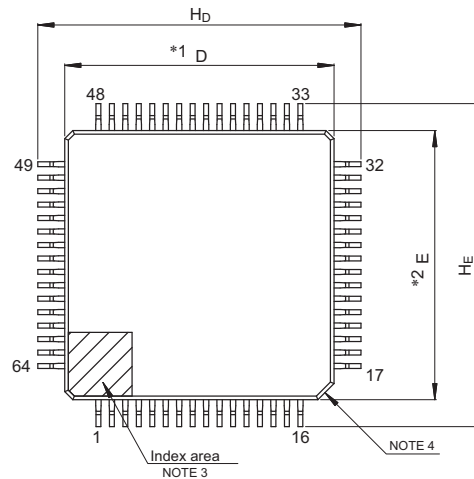
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
ⓔ	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

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Figure 1.5 LQFP 100-pin

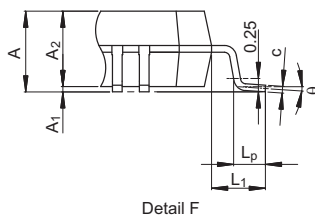
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



NOTE)

1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

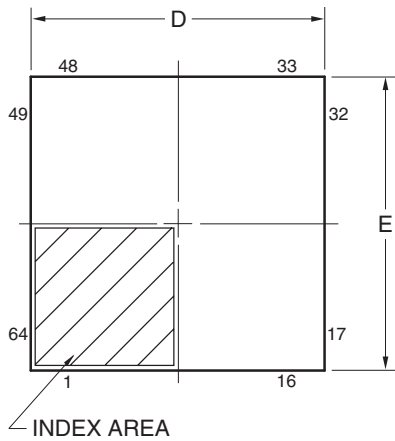


Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A ₂	—	1.4	—
H _D	11.8	12.0	12.2
H _E	11.8	12.0	12.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

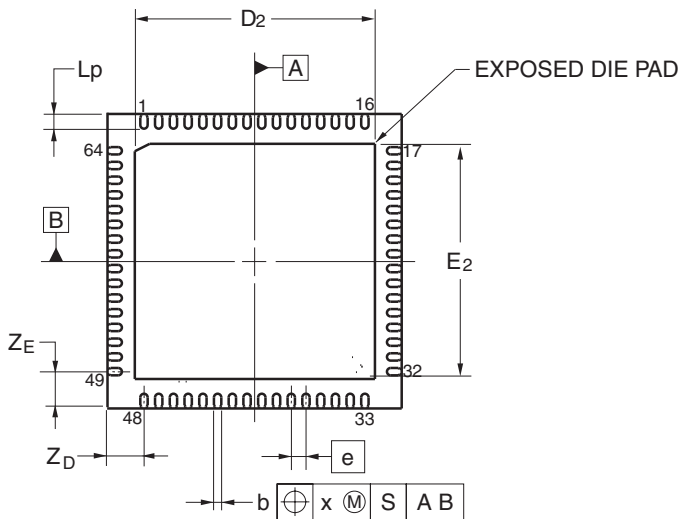
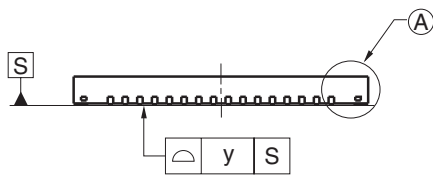
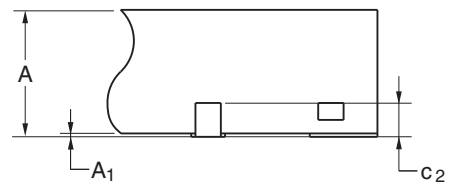
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Figure 1.6 LQFP 64-pin

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-3	0.16



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	7.95	8.00	8.05
E	7.95	8.00	8.05
A	—	—	0.80
A ₁	0.00	—	—
b	0.17	0.20	0.23
e	—	0.40	—
L _p	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z _D	—	1.00	—
Z _E	—	1.00	—
c ₂	0.15	0.20	0.25
D ₂	—	6.50	—
E ₂	—	6.50	—

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Figure 1.7 QFN 64-pin

Revision History	S3A3 Microcontroller Group Datasheet
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Rev.	Date	Summary
1.00	Feb 23, 2016	1st release
1.10	Jul 3, 2018	Updated for 1.10

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

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Software glossary	renesassynergy.com/softwareglossary
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S3A3 Microcontroller Group Datasheet

Publication Date: Rev.1.10 Jul 3, 2018

Published by: Renesas Electronics Corporation

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)



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Renesas Electronics America Inc.

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
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Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

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Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
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No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
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Телефон: 8 (812) 309 58 32 (многоканальный)

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Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.