CMOS Digital Integrated Circuits Silicon Monolithic

74VHC161FT,74VHC163FT

1. Functional Description

- Synchronous Presettable 4-Bit Counter

74VHC161FT: Binary , Asynchronous Clear
74VHC163FT: Binary , Synchronous Clear

2. General

The 74VHC161FT and 74VHC163FT are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate C^{2}MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ inputs are active on low logic level.

Presetting of each IC's is synchronous to the rising edge of CK.

The clear function of the 74VHC163FT is synchronous to CK, while the 74VHC161FT are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages

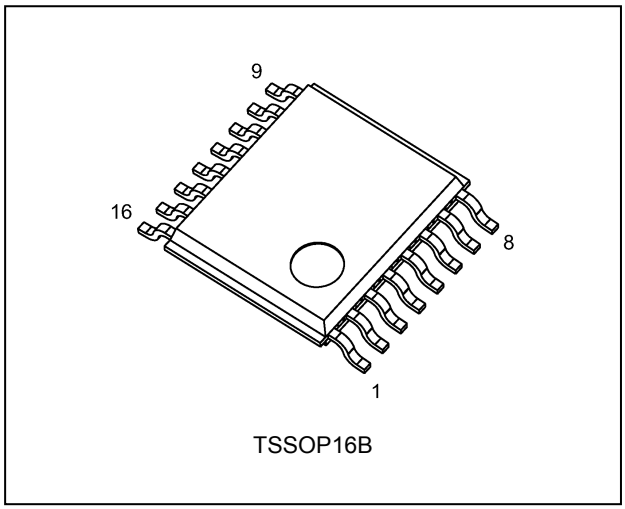
3. Features

(1) AEC-Q100 (Rev. H) (Note 1)
(2) Wide operating temperature range: T_{opr} = -40 to 125 °C
(3) High speed: f_{MAX} = 185 MHz (typ.) at V_{CC} = 5 V
(4) Low power dissipation: I_{CC} = 4.0 μA (max) at T_a = 25 °C
(5) High noise immunity: $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (min)
(6) Power-down protection is provided on all inputs.
(7) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
(8) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 V to 5.5 V
(9) Low noise: V_{OLP}=0.8 V (max)
(10) Pin and function compatible with 74 series (AC/HC/AHC/LV etc.) 161 or 163 type.

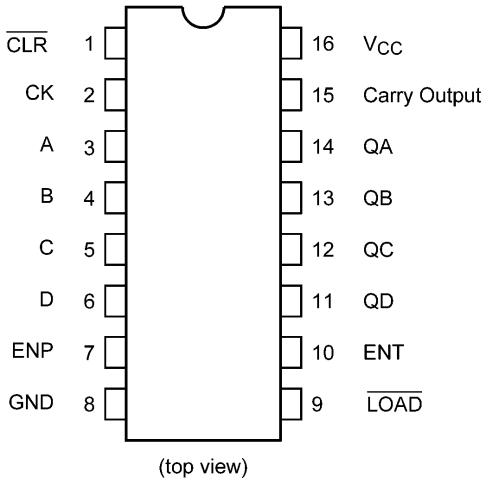
Note 1: This device is compliant with the reliability requirements of AEC-Q100. For details, contact your Toshiba sales representative.

Start of commercial production
2014-12

4. Packaging

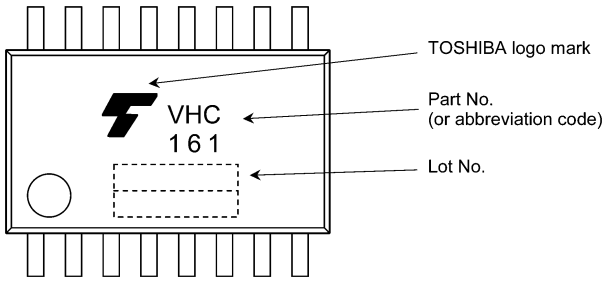


5. Pin Assignment

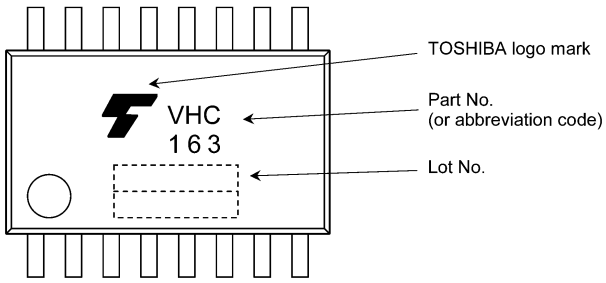


6. Marking

74VHC161FT

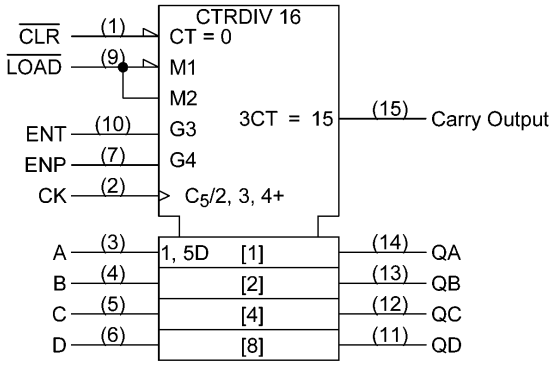


74VHC163FT

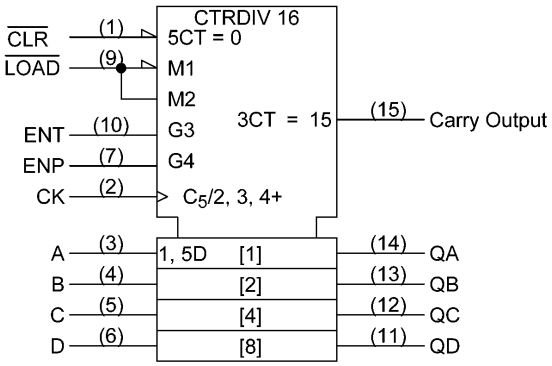


7. IEC Logic Symbol

74VHC161FT



74VHC163FT



8. Truth Table

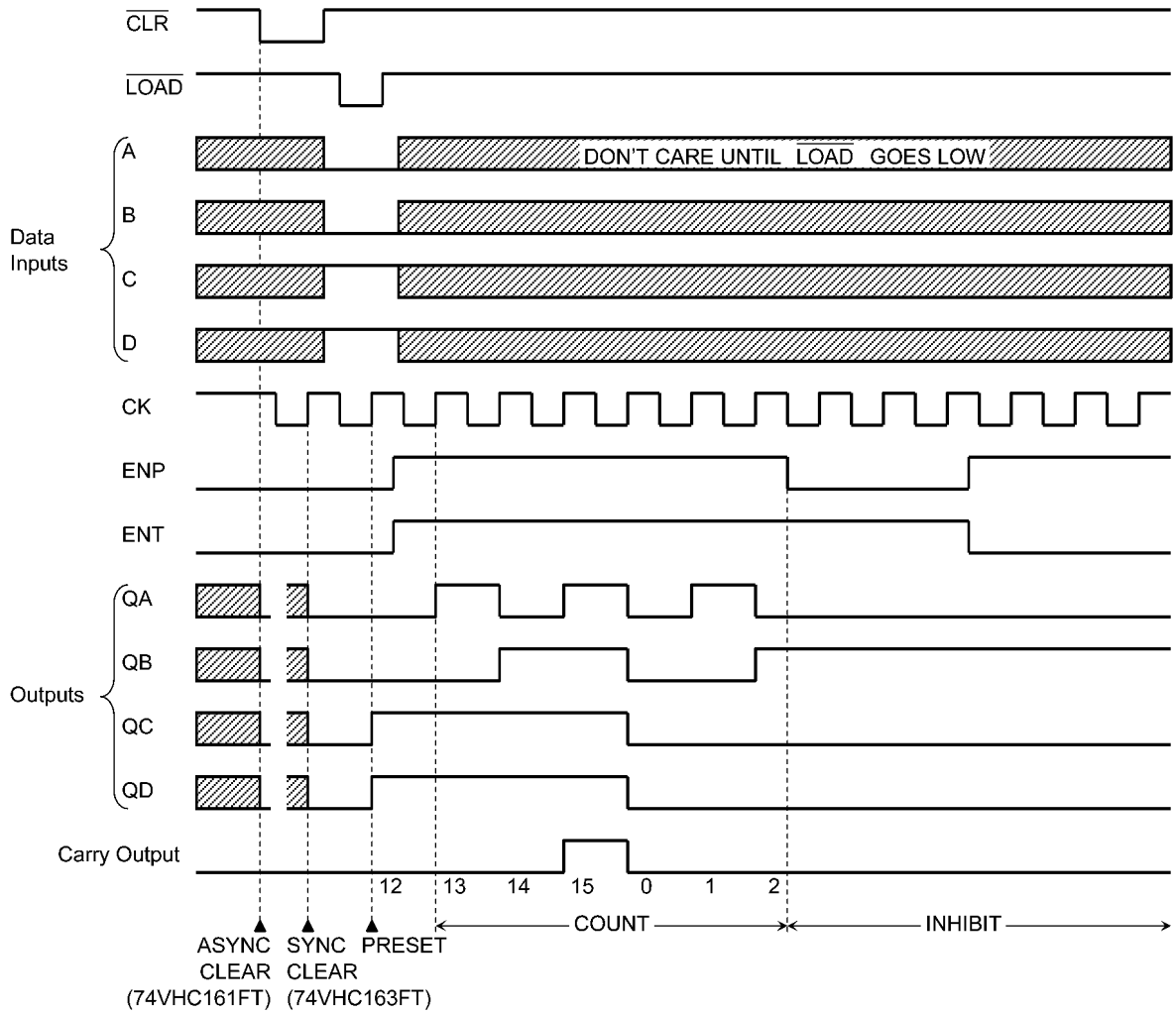
74VHC161FT					74VHC163FT					Outputs				Function
Inputs					Inputs									
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	Reset to “0”
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	↑	H	H	X	L	↑	No Change				No Count
H	H	L	X	↑	H	H	L	X	↑	No Change				No Count
H	H	H	H	↑	H	H	H	H	↑	Count Up				Count
H	X	X	X	↓	X	X	X	X	↓	No Change				No Count

X: Don't care

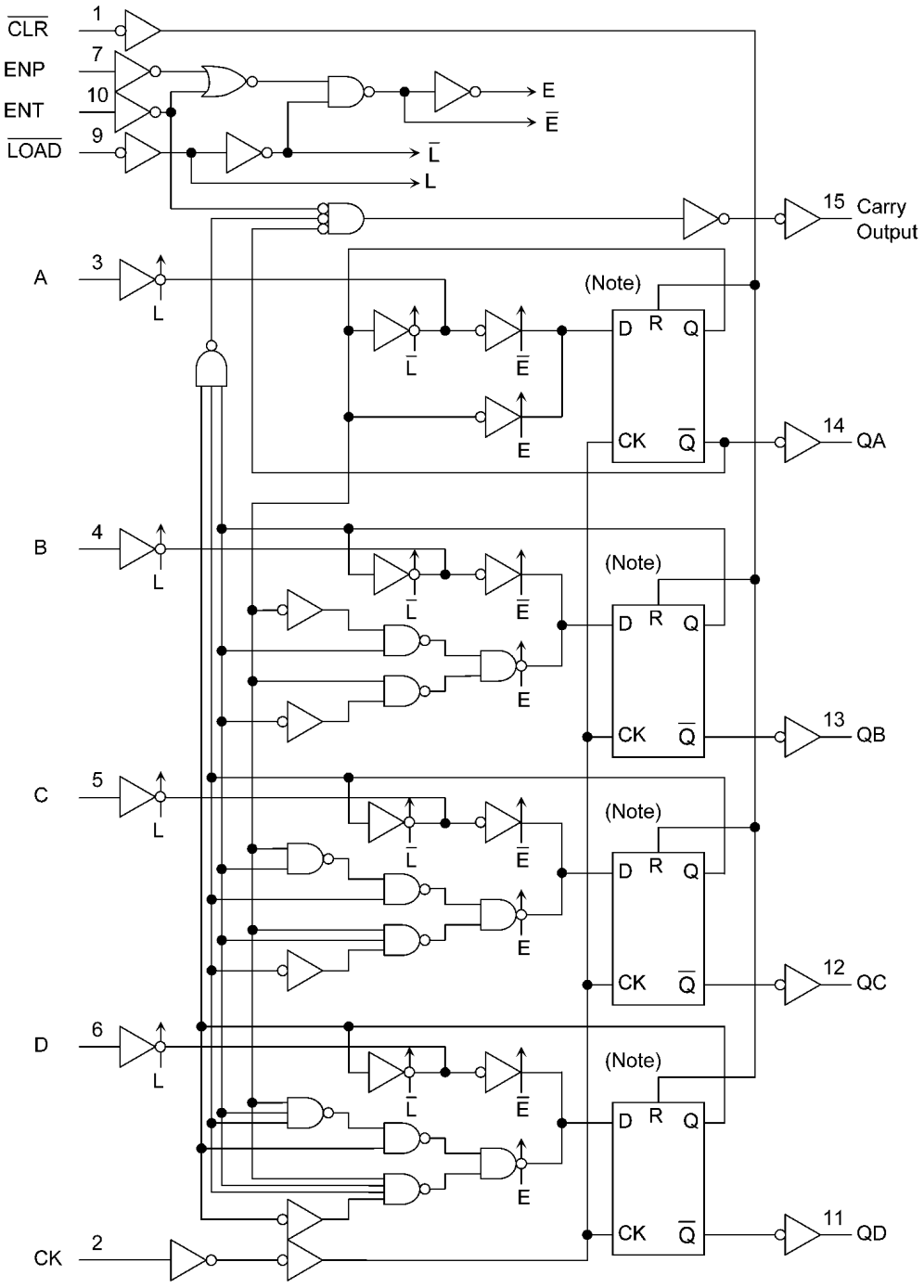
A, B, C, D: Logic level of data inputs

Carry: Carry = ENT · QA · QB · QC · QD

9. Timing Diagrams



10. System Diagram



Note: Truth table of internal F/F

74VHC161FT					74VHC163FT				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	H	↑	L	H	L
X	↓	L	No Change		X	↓	X	No Change	

X: Don't care

11. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Note	Rating	Unit
Supply voltage	V_{CC}		-0.5 to 7.0	V
Input voltage	V_{IN}		-0.5 to 7.0	V
Output voltage	V_{OUT}		-0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}		-20	mA
Output diode current	I_{OK}		±20	mA
Output current	I_{OUT}		±25	mA
V_{CC}/ground current	I_{CC}		±50	mA
Power dissipation	P_D	(Note 1)	180	mW
Storage temperature	T_{stg}		-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 180 mW in the range of T_a = -40 to 85 °C. From T_a = 85 to 125 °C a derating factor of -3.25 mW/°C shall be applied until 50 mW.

12. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	V
Output voltage	V_{OUT}		0 to V_{CC}	V
Operating temperature	T_{opr}		-40 to 125	°C
Input rise and fall times	dt/dv	V_{CC} = 3.3 ± 0.3 V	0 to 100	ns/V
		V_{CC} = 5 ± 0.5 V	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

13. Electrical Characteristics

13.1. DC Characteristics (Unless otherwise specified, T_a = 25 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Typ.	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	V
				3.0 to 5.5	—	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			I_{OH} = -4 mA	3.0	2.58	—	—	
			I_{OH} = -8 mA	4.5	3.94	—	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			I_{OL} = 4 mA	3.0	—	—	0.36	
			I_{OL} = 8 mA	4.5	—	—	0.36	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	—	±0.1	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	μA

13.2. DC Characteristics (Unless otherwise specified, T_a = -40 to 85 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.48	—	
			I_{OH} = -8 mA	4.5	3.80	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.44	
			I_{OL} = 8 mA	4.5	—	0.44	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	40.0	μA

13.3. DC Characteristics (Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	V
				3.0 to 5.5	V_{CC} × 0.7	—	
Low-level input voltage	V_{IL}	—		2.0	—	0.50	V
				3.0 to 5.5	—	V_{CC} × 0.3	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50 μA	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			I_{OH} = -4 mA	3.0	2.40	—	
			I_{OH} = -8 mA	4.5	3.70	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			I_{OL} = 4 mA	3.0	—	0.55	
			I_{OL} = 8 mA	4.5	—	0.55	
Input leakage current	I_{IN}	V_{IN} = 5.5 V or GND		0 to 5.5	—	±2.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	80.0	μA

13.4. Timing Requirements (Unless otherwise specified, T_a = 25 °C, Input: t_r = t_f = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$		Figure 1	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	(Note 1)	Figure 4	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum setup time (A,B,C,D)	t_S		Figure 2	3.3 ± 0.3	5.5	ns
				5.0 ± 0.5	4.5	
Minimum setup time ($\overline{LOAD}$)	t_S		Figure 2	3.3 ± 0.3	8.0	ns
				5.0 ± 0.5	5.0	
Minimum setup time (ENT,ENP)	t_S		Figure 3	3.3 ± 0.3	7.5	ns
				5.0 ± 0.5	5.0	
Minimum setup time ($\overline{CLR}$)	t_S	(Note 2)	Figure 5	3.3 ± 0.3	4.0	ns
				5.0 ± 0.5	3.5	
Minimum hold time	t_h		Figure 2, Figure 3	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.0	
Minimum hold time ($\overline{CLR}$)	t_h	(Note 2)	Figure 5	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	(Note 1)	Figure 4	3.3 ± 0.3	2.5	ns
				5.0 ± 0.5	1.5	

Note 1: For 74VHC161FT only
Note 2: For 74VHC163FT only

13.5. Timing Requirements (Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$		Figure 1	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	(Note 1)	Figure 4	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum setup time (A,B,C,D)	t_S		Figure 2	3.3 ± 0.3	6.5	ns
				5.0 ± 0.5	4.5	
Minimum setup time ($\overline{LOAD}$)	t_S		Figure 2	3.3 ± 0.3	9.5	ns
				5.0 ± 0.5	6.0	
Minimum setup time (ENT,ENP)	t_S		Figure 3	3.3 ± 0.3	9.0	ns
				5.0 ± 0.5	6.0	
Minimum setup time ($\overline{CLR}$)	t_S	(Note 2)	Figure 5	3.3 ± 0.3	4.0	ns
				5.0 ± 0.5	3.5	
Minimum hold time	t_h		Figure 2, Figure 3	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.0	
Minimum hold time ($\overline{CLR}$)	t_h	(Note 2)	Figure 5	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	(Note 1)	Figure 4	3.3 ± 0.3	2.5	ns
				5.0 ± 0.5	1.5	

Note 1: For 74VHC161FT only
Note 2: For 74VHC163FT only

13.6. Timing Requirements (Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	Limit	Unit
Minimum pulse width (CK)	$t_{w(L)}$,$t_{w(H)}$		Figure 1	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum pulse width ($\overline{CLR}$)	$t_{w(L)}$	(Note 1)	Figure 4	3.3 ± 0.3	5.0	ns
				5.0 ± 0.5	5.0	
Minimum setup time (A,B,C,D)	t_S		Figure 2	3.3 ± 0.3	6.5	ns
				5.0 ± 0.5	4.5	
Minimum setup time ($\overline{LOAD}$)	t_S		Figure 2	3.3 ± 0.3	9.5	ns
				5.0 ± 0.5	6.0	
Minimum setup time (ENT,ENP)	t_S		Figure 3	3.3 ± 0.3	9.0	ns
				5.0 ± 0.5	6.0	
Minimum setup time ($\overline{CLR}$)	t_S	(Note 2)	Figure 5	3.3 ± 0.3	4.0	ns
				5.0 ± 0.5	3.5	
Minimum hold time	t_h		Figure 2, Figure 3	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.0	
Minimum hold time ($\overline{CLR}$)	t_h	(Note 2)	Figure 5	3.3 ± 0.3	1.0	ns
				5.0 ± 0.5	1.5	
Minimum removal time ($\overline{CLR}$)	t_{rem}	(Note 1)	Figure 4	3.3 ± 0.3	3.5	ns
				5.0 ± 0.5	2.0	

Note 1: For 74VHC161FT only
Note 2: For 74VHC163FT only

13.7. AC Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time (CK - Q)	t_{PLH},t_{PHL}		Figure 1, Figure 2	3.3 ± 0.3	15	—	8.3	12.8	ns
					50	—	10.8	16.3	
				5.0 ± 0.5	15	—	4.9	8.1	
					50	—	6.4	10.1	
Propagation delay time (CK - CARRY , count-mode)	t_{PLH},t_{PHL}		Figure 1	3.3 ± 0.3	15	—	8.7	13.6	ns
					50	—	11.2	17.1	
				5.0 ± 0.5	15	—	4.9	8.1	
					50	—	6.4	10.1	
Propagation delay time (CK - CARRY , preset-mode)	t_{PLH},t_{PHL}		Figure 2	3.3 ± 0.3	15	—	11.0	17.2	ns
					50	—	13.5	20.7	
				5.0 ± 0.5	15	—	6.2	10.3	
					50	—	7.7	12.3	
Propagation delay time (ENT - CARRY)	t_{PLH},t_{PHL}		Figure 6	3.3 ± 0.3	15	—	7.5	12.3	ns
					50	—	10.5	15.8	
				5.0 ± 0.5	15	—	4.9	8.1	
					50	—	6.4	10.1	
Propagation delay time ($\overline{CLR}$ - Q)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	—	8.9	13.6	ns
					50	—	11.2	17.1	
				5.0 ± 0.5	15	—	5.5	9.0	
					50	—	7.0	11.0	
Propagation delay time ($\overline{CLR}$ - CARRY)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	—	8.4	13.2	ns
					50	—	10.9	16.7	
				5.0 ± 0.5	15	—	5.0	8.6	
					50	—	6.5	10.6	
Maximum clock frequency	f_{MAX}		—	3.3 ± 0.3	15	80	130	—	MHz
					50	55	85	—	
				5.0 ± 0.5	15	135	185	—	
					50	95	125	—	
Input capacitance	C_{IN}		—			—	4	10	pF
Power dissipation capacitance	C_{PD}	(Note 2)	—			—	23	—	pF

Note 1: For 74VHC161FT only

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of $I_{CC(opr)}$ and ΔI_{CC} which is obtained from the following formula:

$$\Delta I_{CC} = f_{CK} \times V_{CC} \times (C_{QA}/2 + C_{QB}/4 + C_{QC}/8 + C_{QD}/16 + C_{CO}/16)$$

C_{QA} to C_{QD} and C_{CO} are the capacitances at QA to QD and Carry out, respectively.
f_{CK} is the input frequency of the CK.

13.8. AC Characteristics
(Unless otherwise specified, T_a = -40 to 85 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK - Q)	t_{PLH},t_{PHL}		Figure 1, Figure 2	3.3 ± 0.3	15	1.0	15.0	ns
					50	1.0	18.5	
				5.0 ± 0.5	15	1.0	9.5	
					50	1.0	11.5	
Propagation delay time (CK - CARRY , count-mode)	t_{PLH},t_{PHL}		Figure 1	3.3 ± 0.3	15	1.0	16.0	ns
					50	1.0	19.5	
				5.0 ± 0.5	15	1.0	9.5	
					50	1.0	11.5	
Propagation delay time (CK - CARRY , preset-mode)	t_{PLH},t_{PHL}		Figure 2	3.3 ± 0.3	15	1.0	20.0	ns
					50	1.0	23.5	
				5.0 ± 0.5	15	1.0	12.0	
					50	1.0	14.0	
Propagation delay time (ENT - CARRY)	t_{PLH},t_{PHL}		Figure 6	3.3 ± 0.3	15	1.0	14.5	ns
					50	1.0	18.0	
				5.0 ± 0.5	15	1.0	9.5	
					50	1.0	11.5	
Propagation delay time ($\overline{CLR}$ - Q)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	1.0	16.0	ns
					50	1.0	19.5	
				5.0 ± 0.5	15	1.0	10.5	
					50	1.0	12.5	
Propagation delay time ($\overline{CLR}$ - CARRY)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	1.0	15.5	ns
					50	1.0	19.0	
				5.0 ± 0.5	15	1.0	10.0	
					50	1.0	12.0	
Maximum clock frequency	f_{MAX}		—	3.3 ± 0.3	15	70	—	MHz
					50	50	—	
				5.0 ± 0.5	15	115	—	
					50	85	—	
Input capacitance	C_{IN}		—			—	10	pF

Note 1: For 74VHC161FT only

13.9. AC Characteristics
(Unless otherwise specified, T_a = -40 to 125 °C, Input: $t_r = t_f$ = 3 ns)

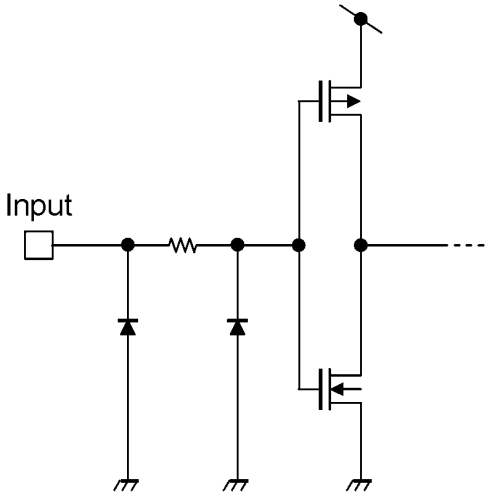
Characteristics	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time (CK - Q)	t_{PLH},t_{PHL}		Figure 1, Figure 2	3.3 ± 0.3	15	1.0	17.0	ns
					50	1.0	20.5	
				5.0 ± 0.5	15	1.0	11.0	
					50	1.0	13.0	
Propagation delay time (CK - CARRY , count-mode)	t_{PLH},t_{PHL}		Figure 1	3.3 ± 0.3	15	1.0	18.0	ns
					50	1.0	21.5	
				5.0 ± 0.5	15	1.0	11.0	
					50	1.0	13.0	
Propagation delay time (CK - CARRY , preset-mode)	t_{PLH},t_{PHL}		Figure 2	3.3 ± 0.3	15	1.0	22.5	ns
					50	1.0	26.0	
				5.0 ± 0.5	15	1.0	13.5	
					50	1.0	15.5	
Propagation delay time (ENT - CARRY)	t_{PLH},t_{PHL}		Figure 6	3.3 ± 0.3	15	1.0	16.5	ns
					50	1.0	20.0	
				5.0 ± 0.5	15	1.0	11.0	
					50	1.0	13.0	
Propagation delay time ($\overline{CLR}$ - Q)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	1.0	18.0	ns
					50	1.0	21.5	
				5.0 ± 0.5	15	1.0	12.0	
					50	1.0	14.0	
Propagation delay time ($\overline{CLR}$ - CARRY)	t_{PHL}	(Note 1)	Figure 4	3.3 ± 0.3	15	1.0	17.5	ns
					50	1.0	21.0	
				5.0 ± 0.5	15	1.0	11.5	
					50	1.0	13.5	
Maximum clock frequency	f_{MAX}		—	3.3 ± 0.3	15	60	—	MHz
					50	40	—	
				5.0 ± 0.5	15	105	—	
					50	75	—	
Input capacitance	C_{IN}		—			—	10	pF

Note 1: For 74VHC161FT only

14. Noise Characteristics (Unless otherwise specified, T_a = 25 °C, Input: $t_r = t_f$ = 3 ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	C_L = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	C_L = 50 pF	5.0	-0.4	-0.8	V
Minimum high-level dynamic input voltage	V_{IHD}	C_L = 50 pF	5.0	—	3.5	V
Maximum low-level dynamic input voltage	V_{ILD}	C_L = 50 pF	5.0	—	1.5	V

15. Internal Equivalent Circuit



16. AC Characteristics Test Waveform

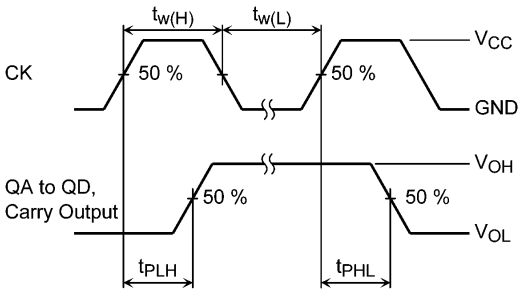


Figure 1 Count Mode

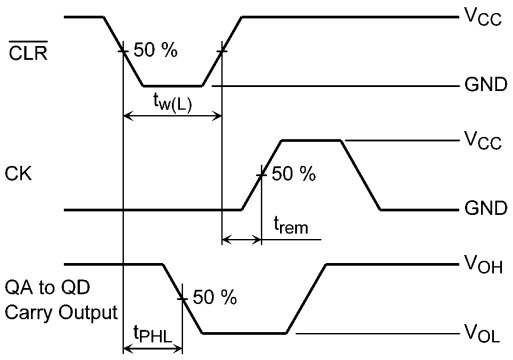


Figure 4 Clear Mode (74VHC161FT)

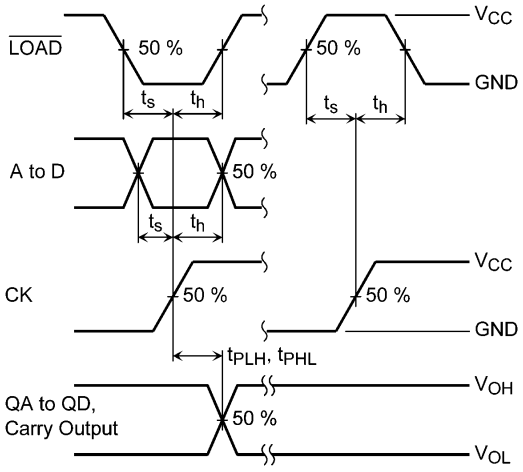


Figure 2 Preset Mode

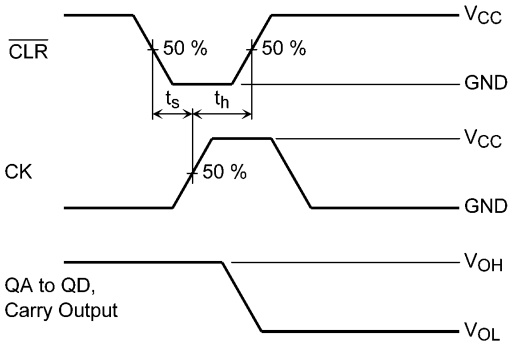


Figure 5 Clear Mode (74VHC163FT)

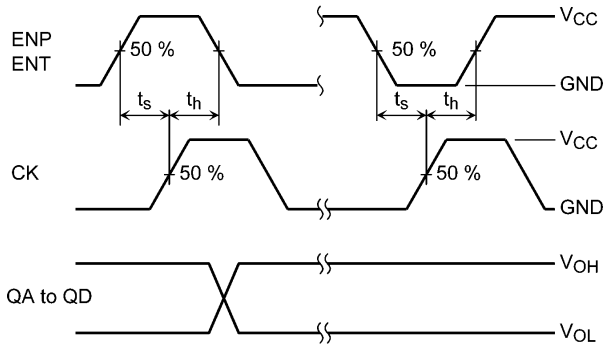


Figure 3 Count Enable Mode

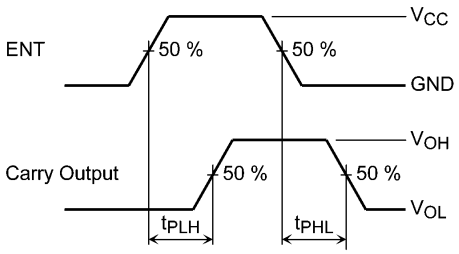
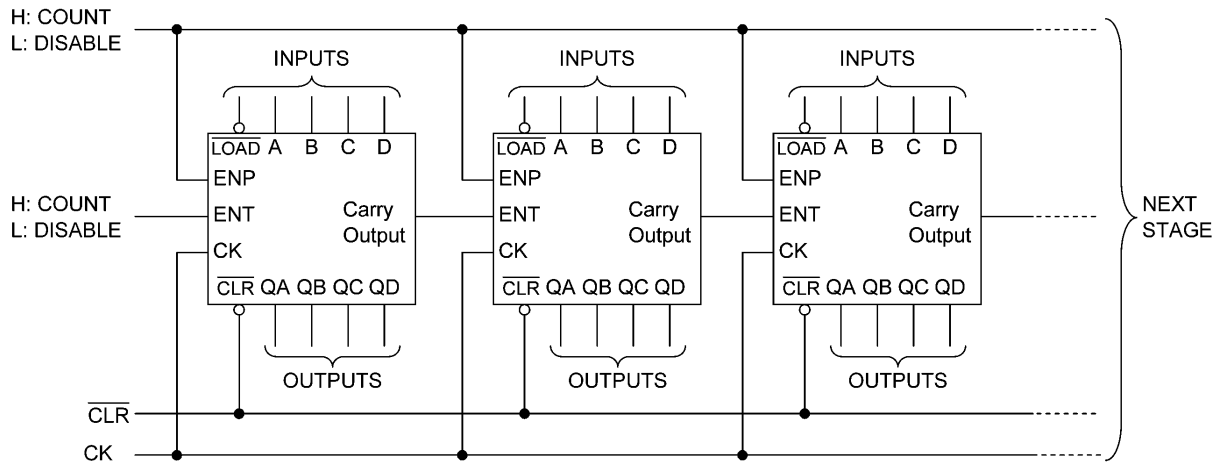


Figure 6 Cascade Mode (fix maximum count)

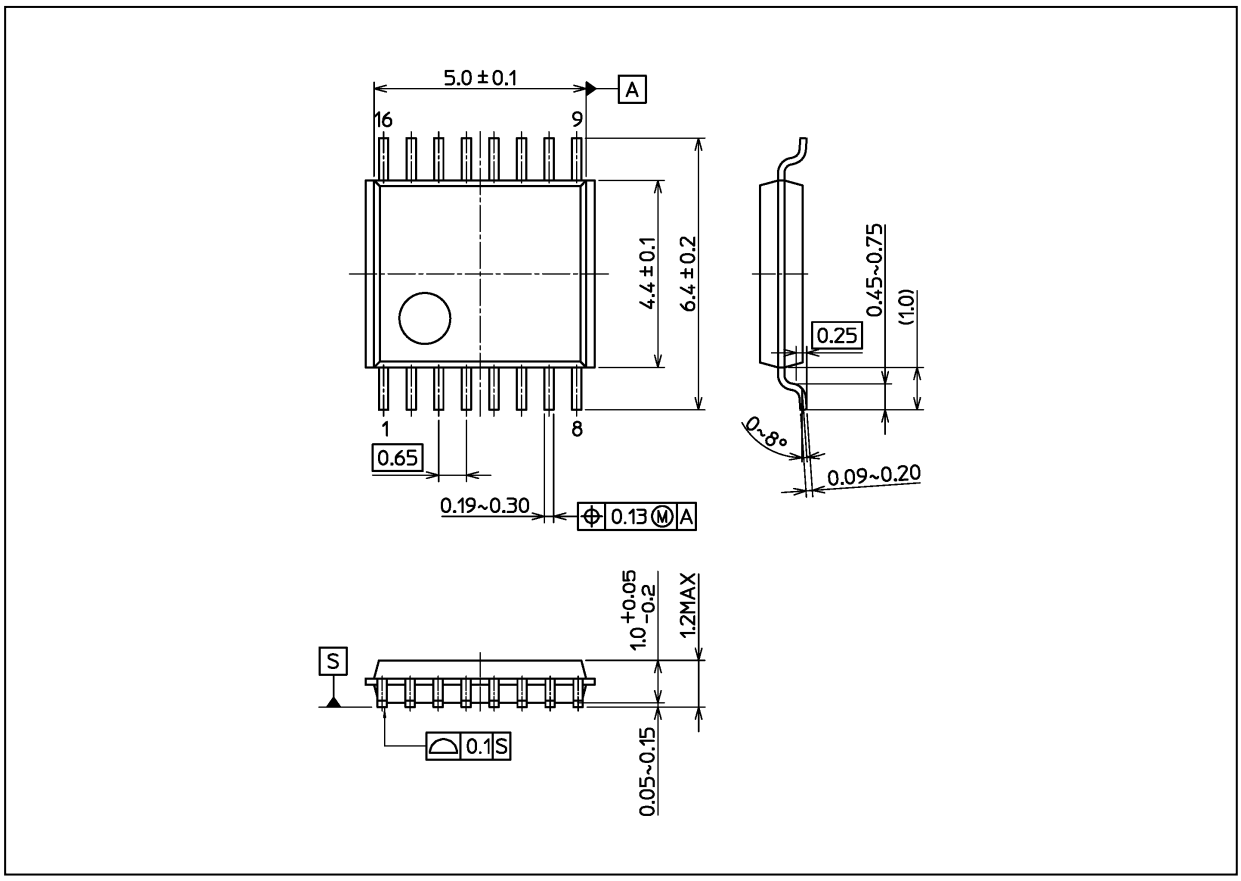
17. Typical Application



Parallel Carry N-Bit Counter

Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

Package Name(s)
Nickname: TSSOP16B

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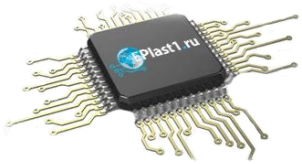
- Защита от снятия компонента с производства.



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