RF Diversity and 1.2 GHz Bandwidth Observation Receiver

Data Sheet **AD6688**

FEATURES

- JESD204B (Subclass 1) coded serial digital outputs
  - Support for lane rates up to 16 Gbps per lane
- 1.7 W total power per channel at 3 GSPS (default settings)
- Performance at −2 dBFS amplitude, 2.6 GHz input
  - SFDR = 70 dBFS
  - NSD = −148.0 dBFS/Hz
- Performance at −9 dBFS amplitude, 2.6 GHz input
  - SFDR = 75 dBFS
  - NSD = −151.4 dBFS/Hz
- Integrated input buffer
- Noise density = −152.0 dBFS/Hz
- 0.975 V, 1.9 V, and 2.5 V dc supply operation
- 9 GHz analog input full power bandwidth (−3 dB)
- Amplitude detect bits for efficient AGC implementation
- Two Integrated wideband digital processors per channel
  - 48-bit NCO
  - 4 cascaded half band filters
- Phase coherent NCO switching
  - Up to 4 channels available
- Serial port control
  - Integer clock divide by 2 and divide by 4
  - Flexible JESD204B lane configurations
- On-chip dither

APPLICATIONS

- Diversity multiband, multimode digital receivers
- 3G/4G, TD-SCDMA, W-CDMA, GSM, LTE, LTE-A
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers

FUNCTIONAL BLOCK DIAGRAM

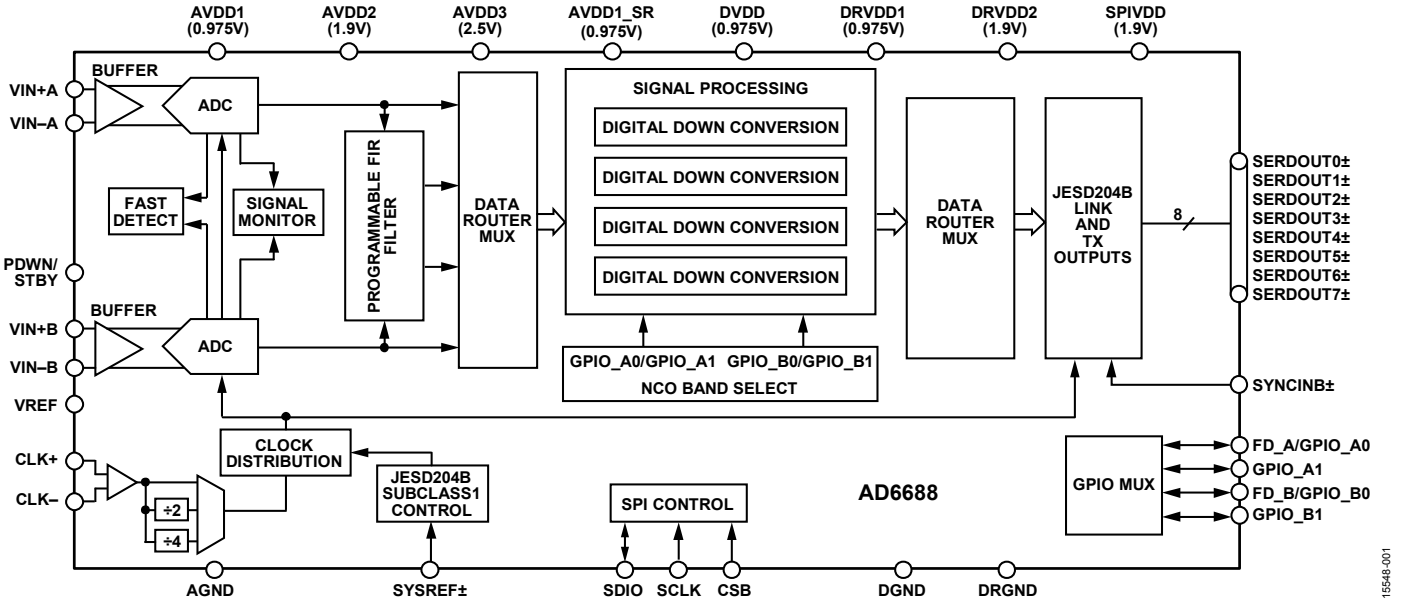

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

4/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD6688 is a 1.2 GHz bandwidth, mixed-signal, direct radio frequency (RF) sampling receiver. It consists of two 14-bit, 3.0 GSPS analog-to-digital converters (ADCs) and various digital signal processing blocks consisting of four wideband digital downconverters (DDCs). The AD6688 has an on-chip buffer and a sample-and-hold circuit designed for low power, small size, and ease of use. This product is designed to support communications applications capable of direct sampling wide bandwidth analog signals of up to 5 GHz. The 3 dB bandwidth of the ADC input is greater than 9 GHz. The AD6688 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. The analog input and clock signals are differential inputs. The ADC data outputs are internally connected to four DDCs through a crossbar mux. Each DDC consists of up to five cascaded signal processing stages: a 48-bit numerically controlled oscillator (NCO) and up to four half-band decimation filters. The NCO has the option to select preset bands over the general-purpose input/output (GPIO) pins, which enables selection of up to three bands. Operation of the AD6688 between the DDC modes is selectable via SPI-programmable profiles.

In addition to the DDC blocks, the AD6688 has several functions that simplify the automatic gain control (AGC) function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect control bits in Register 0x0245 of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input. Besides the fast detect outputs, the AD6688 also offers signal monitoring capability. The signal monitoring block provides additional information about the signal being digitized by the ADC.

The user can configure the Subclass 1 JESD204B-based high speed serialized output in a variety of one-lane, two-lane, four-lane, six-lane, and eight-lane configurations, depending on the DDC configuration and the acceptable lane rate of the receiving logic device. Multidevice synchronization is supported through the SYSREF± and SYNCINB± input pins.

The AD6688 has flexible power-down options that allow significant power savings when desired. All of these features can be programmed using a 3-wire serial port interface (SPI).

The AD6688 is available in a Pb-free, 196-ball BGA specified over the −40°C to +85°C ambient temperature range. This product is protected by a U.S. patent.

PRODUCT HIGHLIGHTS

1. Wide full power bandwidth supports IF sampling of signals up to 9 GHz (−3 dB point).
2. Four integrated wide-band decimation filter and NCO blocks supporting multiband receivers.
3. Fast NCO switching enabled through GPIO pins.
4. Flexible SPI controls various product features and functions to meet specific system requirements.
5. Programmable fast overrange detection and signal monitoring.
6. On-chip temperature diode for system thermal management.
7. 12 mm × 12 mm, 196-ball BGA.

SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, input amplitude (A_{IN}) = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
ACCURACY				
No Missing Codes		Guaranteed		
Offset Error		0		%FSR
Offset Matching		0		%FSR
Gain Error	−5.89	±1	+5.89	%FSR
Gain Matching	−2.9	±0.2	+2.9	%FSR
Differential Nonlinearity (DNL)	−0.63	±0.4	+0.74	LSB
Integral Nonlinearity (INL)	−26	±6	+21	LSB
TEMPERATURE DRIFT				
Offset Error		±15		ppm/°C
Gain Error		440		ppm/°C
INTERNAL VOLTAGE REFERENCE		0.5		V
ANALOG INPUTS				
Differential Input Voltage Range		1.7		V p-p
Common-Mode Voltage (V_{CM})	1.32	1.35	1.52	V
Differential Input Resistance		200		Ω
Differential Input Capacitance		0.25		pF
Differential Input Return Loss at 2.1 GHz[2]		−7		dB
−3 dB Bandwidth		9		GHz
POWER SUPPLY				
AVDD1	0.95	0.975	1.0	V
AVDD2	1.85	1.9	1.95	V
AVDD3	2.44	2.5	2.56	V
AVDD1_SR	0.95	0.975	1.0	V
DVDD	0.95	0.975	1.0	V
DRVDD1	0.95	0.975	1.0	V
DRVDD2	1.85	1.9	1.95	V
SPIVDD	1.85	1.9	1.95	V
I_{AVDD1}		640	765	mA
I_{AVDD2}		790	885	mA
I_{AVDD3}		110	120	mA
I_{AVDD1_SR}		24	50	mA
I_{DVDD}		480	1020	mA
I_{DRVDD1}[3]		320	590	mA
I_{DRVDD2}		30	35	mA
I_{SPIVDD}		1	5	mA

Parameter	Min	Typ	Max	Unit
POWER CONSUMPTION				
Total Power Dissipation (Including Output Drivers)[4]		3.3		W
Power-Down Dissipation		300		mW
Standby[5]		1.65		mW

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] For more information, see the Analog Input Considerations section.
[3] All lanes running. Power dissipation on DRVDD1 changes with lane rate and number of lanes used.
[4] Default mode. No DDCs used.
[5] Can be controlled by SPI.

AC SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, DDC decimation ratio = 8, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 2.

	A_{IN} = −2 dBFS			A_{IN} = −9 dBFS			
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
ANALOG INPUT FULL SCALE (DIFFERENTIAL)	1.1	1.7	2.04	1.1	1.7	2.04	V p-p
NOISE FIGURE		24.5			24.5		dB
NOISE SPECTRAL DENSITY (NSD)							
Input Frequency (f_{IN}) = 10 MHz, A_{IN} = −30 dBFS (2.04 V p-p)		−153.6			−153.6		dBFS/Hz
f_{IN} = 10 MHz, A_{IN} = −30 dBFS		−152.0			−152.0		dBFS/Hz
f_{IN} = 255 MHz		−151.5			−152.0		dBFS/Hz
f_{IN} = 950 MHz		−150.5			−151.9		dBFS/Hz
f_{IN} = 1870 MHz		−149.9			−151.9		dBFS/Hz
f_{IN} = 2170 MHz		−149.7			−151.8		dBFS/Hz
f_{IN} = 2600 MHz		−148.0	−143.9		−151.4		dBFS/Hz
IN-BAND SIGNAL-TO-NOISE RATIO (SNR)[3]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		65.8			67.7		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		65.2			67.2		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		65.0			67.1		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		63.4			66.7		dBFS
IN-BAND SIGNAL-TO-NOISE-AND-DISTORTION RATIO (SINAD)[3]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		65.6			67.7		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		65.1			67.1		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		64.8			67.0		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		63.2			66.5		dBFS
SPURIOUS FREE DYNAMIC RANGE (SFDR), SECOND OR THIRD HARMONIC[4]							
f_{IN} = 950 MHz		71			78		dBFS
f_{IN} = 1870 MHz		69			76		dBFS
f_{IN} = 2170 MHz		67			73		dBFS
f_{IN} = 2600 MHz	51	70			75		dBFS
IN-BAND SPURIOUS FREE DYNAMIC RANGE (SFDR), WORST HARMONIC[5]							
f_{IN} = 950 MHz, NCO Tuning Frequency = 942.5 MHz		71			91		dBFS
f_{IN} = 1870 MHz, NCO Tuning Frequency = 1842.0 MHz		90			96		dBFS
f_{IN} = 2170 MHz, NCO Tuning Frequency = 2140.0 MHz		88			92		dBFS
f_{IN} = 2600 MHz, NCO Tuning Frequency = 2655.0 MHz		89			92		dBFS
WORST OTHER, EXCLUDING SECOND OR THIRD HARMONIC[6]							
f_{IN} = 950 MHz		−86			−95		dBFS
f_{IN} = 1870 MHz		−84			−94		dBFS
f_{IN} = 2170 MHz		−83			−94		dBFS
f_{IN} = 2600 MHz		−79	−66		−90		dBFS

Parameter[2]	A_{IN} = −2 dBFS Min	Typ	Max	A_{IN} = −9 dBFS Min	Typ	Max	Unit
TWO-TONE INTERMODULATION DISTORTION (IMD), A_{IN1} AND A_{IN2} = −15.0 dBFS f_{IN1} = 1.841 GHz, f_{IN2} = 1.846 GHz; NCO Frequency = 1874.28 MHz		N/A[7]			96		dBFS
CROSSTALK[8]		>90			>90		dB
ANALOG INPUT BANDWIDTH, FULL POWER[9]		5			5		GHz

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to +85°C.
[2] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[3] In-band SNR is dependent on the DDC decimation ratio (DCM) and is calculated by |NSD| = |SNR| + 10 × log(f_S/(2 × DCM)), where f_S = ADC sample clock rate.
[4] SFDR is specified with DDCs bypassed.
[5] In-band SFDR is defined as the worst spur within the alias protected bandwidth of the DDC outputs. When DDCs are enabled, SFDR changes with DDC decimation settings, NCO frequency, and overall frequency plan.
[6] Worst other harmonic is specified with DDCs bypassed.
[7] N/A means not applicable.
[8] Crosstalk is measured at 950 MHz with a −2.0 dBFS analog input on one channel, and no input on the adjacent channel.
[9] Full power bandwidth is the bandwidth of operation in which proper ADC performance can be achieved.

DIGITAL SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, A_{IN} = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 3.

Parameter	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	300	800	1800	mV p-p
Input Common-Mode Voltage		0.675		V
Input Resistance (Differential)		106		Ω
Input Capacitance		0.9		pF
Differential Input Return Loss at 3 GHz[2]		−9.4		dB
SYSREF INPUTS (SYSREF+, SYSREF−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance (Differential)		1		pF
LOGIC INPUT (SDIO, SCLK, CSB, PDWN/STBY, FD_A/GPIO_A0, FD_B/GPIO_B0, GPIO_A1, GPIO_B1)				
Logic Compliance		CMOS		
Logic 1 Voltage	0.65 × SPIVDD			V
Logic 0 Voltage	0		0.35 × SPIVDD	V
Input Resistance		30		kΩ
LOGIC OUTPUT (SDIO, FD_A, FD_B)				
Logic Compliance		CMOS		
Logic 1 Voltage (I_{OH} = 4 mA)	SPIVDD − 0.45V			V
Logic 0 Voltage (I_{OL} = 4 mA)	0		0.45	V
SYNCIN INPUT (SYNCINB+/SYNCINB−)				
Logic Compliance		LVDS/LVPECL		
Differential Input Voltage	400	800	1800	mV p-p
Input Common-Mode Voltage		0.675	2.0	V
Input Resistance (Differential)		18		kΩ
Input Capacitance		1		pF
SYNCINB+ INPUT				
Logic Compliance		CMOS		
Logic 1 Voltage	0.9 × DRVDD1		2 × DRVDD1	V
Logic 0 Voltage			0.1 × DRVDD1	V
Input Resistance		2.6		kΩ
DIGITAL OUTPUTS (SERDOUTx±, x = 0 TO 7)				
Logic Compliance		SST		
Differential Output Voltage	360	560	770	mV p-p
Differential Termination Impedance	80	100	120	Ω

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] Reference impedance = 100 Ω.

SWITCHING SPECIFICATIONS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, A_{IN} = −2.0 dBFS, L = 8, M = 2, F = 1, −10°C ≤ T_J ≤ +120°C[1], unless otherwise noted. Typical specifications represent performance at T_J = 70°C (T_A = 25°C).

Table 4.

Parameter	Min	Typ	Max	Unit
CLOCK				
Clock Rate (at CLK+/CLK− Pins)		3	6	GHz
Sample Rate[2]	2500	3000	3100	MSPS
Clock Pulse Width High	161.29	166.67	192.31	ps
Clock Pulse Width Low	161.29	166.67	192.31	ps
OUTPUT PARAMETERS				
Unit Interval (UI)[3]	62.5	66.67	592.6	ps
Rise Time (t_R) (20% to 80% into 100 Ω Load)		26		ps
Fall Time (t_F) (20% to 80% into 100 Ω Load)		26		ps
Phase-Locked Loop (PLL) Lock Time		5		ms
Data Rate per Channel (NRZ)[4]	1.6875	15	16	Gbps
LATENCY[5]				
Pipeline Latency		75		Clock cycles
Fast Detect Latency		26		Clock cycles
WAKE-UP TIME				
Standby		400		µs
Power-Down		15		ms
NCO CHANNEL SELCTION TO OUTPUT			8	Clock cycles
APERTURE				
Aperture Delay (t_A)		250		ps
Aperture Uncertainty (Jitter, t_J)		55		fs rms
Out of Range Recovery Time		1		Clock cycles

[1] Junction temperature (T_J) range of −10°C to +120°C translates to an ambient temperature range of −40°C to+85°C.
[2] The maximum sample rate is the clock rate after the divider.
[3] Baud rate = 1/UI. A subset of this range can be supported.
[4] Default L = 8. This number can be changed based on the sample rate and decimation ratio.
[5] No DDCs used. L = 8, M = 2, F = 1.

TIMING SPECIFICATIONS

Table 5.

Parameter	Description	Min	Typ	Max	Unit
CLK+ to SYSREF+ TIMING REQUIREMENTS					
t_{SU_SR}	Device clock to SYSREF+ setup time		−65		ps
t_{H_SR}	Device clock to SYSREF+ hold time		95		ps
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK must be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK must be in a logic low state	10			ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		6	10	ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

Timing Diagrams

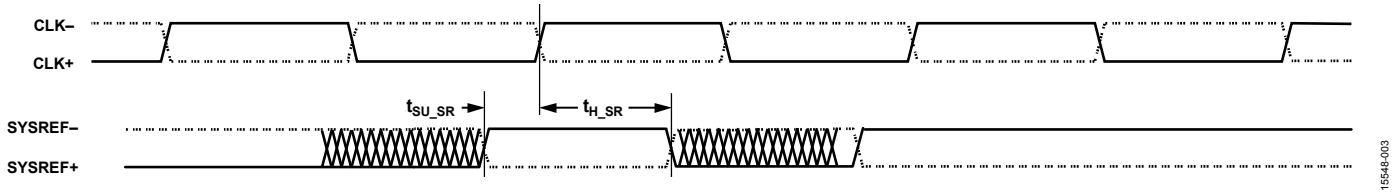


Figure 2. SYSREF± Setup and Hold Timing

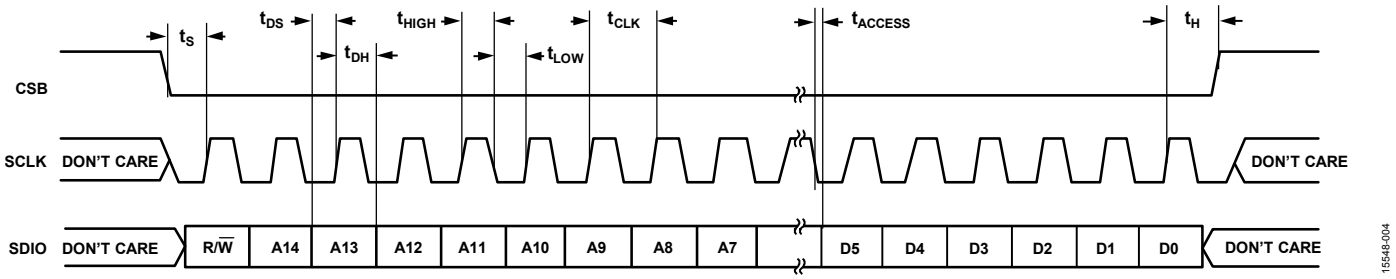


Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	1.05 V
AVDD1_SR to AGND	1.05 V
AVDD2 to AGND	2.0 V
AVDD3 to AGND	2.70 V
DVDD to DGND	1.05 V
DRVDD1 to DRGND	1.05 V
DRVDD2 to DRGND	2.0 V
SPIVDD to DGND	2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to DRGND	−0.3 V to +0.3 V
VIN±x to AGND	AGND − 0.3 V to AVDD3 + 0.3 V
CLK± to AGND	AGND − 0.3 V to AVDD1 + 0.3 V
SCLK, SDIO, CSB to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
PDWN/STBY to DGND	DGND − 0.3 V to SPIVDD + 0.3 V
SYSREF± to AGND	2.5 V
SYNCINB± to DRGND	2.5 V
Junction Temperature Range (T_J)	−40°C to +125°C
Storage Temperature Range, Ambient (T_A)	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC_TOP}	Ψ_{JB}	Ψ_{JT}	Unit
BP-196-4[1]	16.26	1.4	5.44	1.68	°C/W

[1] Test Condition 1: Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 190 thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AVDD2	AVDD2	AVDD1	AVDD1[1]	AVDD1[1]	AGND[1]	CLK+	CLK–	AGND[1]	AVDD1[1]	AVDD1[1]	AVDD1	AVDD2	AVDD2
B	AVDD2	AVDD2	AVDD1	AVDD1[1]	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AVDD1[1]	AVDD1	AVDD2	AVDD2
C	AVDD2	AVDD2	AVDD1	AGND	AGND	AGND[1]	AGND[1]	AGND[1]	AGND[1]	AGND	AGND	AVDD1	AVDD2	AVDD2
D	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND[1]	AGND[1]	AGND	AGND	AGND	AGND	AGND	AVDD3
E	VIN–B	AGND	AGND	AGND	AGND	AGND[2]	AVDD1_SR	AGND[2]	AGND	AGND	AGND	AGND	AGND	VIN–A
F	VIN+B	AGND	AGND	AGND	AGND	AGND	SYSREF+	SYSREF–	AGND	AGND	AGND	AGND	AGND	VIN+A
G	AVDD3	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AVDD3
H	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	VREF	AGND	AGND	AGND	AGND
J	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND
K	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]	AGND[3]
L	DGND	GPIO_B1	SPIVDD	FD_B/ GPIO_B0	CSB	SCLK	SDIO	PDWN/ STBY	FD_A/ GPIO_A0	SPIVDD	GPIO_A1	DGND	DGND	DGND
M	DGND	DGND	DRGND	DRGND	DRVDD1	DRVDD1	DRVDD1	DRVDD1	DRGND	DRGND	DRVDD1	DRGND	DRVDD2	DVDD
N	DVDD	DVDD	DRGND	SERDOUT7+	SERDOUT6+	SERDOUT5+	SERDOUT4+	SERDOUT3+	SERDOUT2+	SERDOUT1+	SERDOUT0+	DRGND	SYNCINB+	DVDD
P	DVDD	DVDD	DRGND	SERDOUT7–	SERDOUT6–	SERDOUT5–	SERDOUT4–	SERDOUT3–	SERDOUT2–	SERDOUT1–	SERDOUT0–	DRGND	SYNCINB–	DVDD

[1]DENOTES CLOCK DOMAIN.
[2]DENOTES SYSREF± DOMAIN.
[3]DENOTES ISOLATION DOMAIN.

15548-005

Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions[1]

Pin No.	Mnemonic	Type	Description
Power Supplies			
A3, A12, B3, B12, C3, C12	AVDD1	Power	Analog Power Supply (0.975 V Nominal).
A4, A5, A10, A11, B4, B11	AVDD1[2]	Power	Analog Power Supply for the Clock Domain (0.975 V Nominal).
A1, A2, A13, A14, B1, B2, B13, B14, C1, C2, C13, C14	AVDD2	Power	Analog Power Supply (1.9 V Nominal).
D1, D14, G1, G14	AVDD3	Power	Analog Power Supply (2.5 V Nominal).
E7	AVDD1_SR	Power	Analog Power Supply for SYSREF± (0.975 V Nominal).
L3, L10	SPIVDD	Power	Digital Power Supply for SPI (1.9 V Nominal).
M14, N1, N2, N14, P1, P2, P14	DVDD	Power	Digital Power Supply (0.975 V Nominal).
M5 to M8, M11	DRVDD1	Power	Digital Driver Power Supply (0.975 V Nominal).
M13	DRVDD2	Power	Digital Driver Power Supply (1.9 V Nominal).
B5, B10, C4, C5, C10, C11, D2 to D6, D9 to D13, E2 to E5, E9 to E13, F2 to F6, F9 to F13, G2 to G13, H1 to H9, H11 to H14, J1 to J14	AGND	Ground	Analog Ground. These pins connect to the analog ground plane.
A6, A9, B6 to B9, C6 to C9, D7, D8	AGND[2]	Ground	Ground Reference for Clock Domain.
E6, E8	AGND[3]	Ground	Ground Reference for SYSREF±.
K1 to K14	AGND[4]	Ground	Isolation Ground.
L1, L12 to L14, M1, M2	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
M3, M4, M9, M10, M12, N3, N12, P3, P12	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
Analog			
E1, F1	VIN−B, VIN+B	Input	ADC B Analog Input Complement/True.
E14, F14	VIN−A, VIN+A	Input	ADC A Analog Input Complement/True.
A7, A8	CLK+, CLK−	Input	Clock Input True/Complement.
H10	VREF	Input/DNC	0.50 V Reference Voltage Input/Do Not Connect. This pin is configurable through the SPI as a no connect or an input. Do not connect this pin if using the internal reference. This pin requires a 0.50 V reference voltage input if using an external voltage reference source.
CMOS Inputs/Outputs			
L2	GPIO_B1	Input/Output	GPIO B1.
L4	FD_B/GPIO_B0	Input/Output	Fast Detect Outputs for Channel B/GPIO B0.
L9	FD_A/GPIO_A0	Input/Output	Fast Detect Outputs for Channel A/GPIO A0.
L11	GPIO_A1	Input/Output	GPIO A1.
Digital Inputs			
F7, F8	SYSREF+, SYSREF−	Input	Active High JESD204B LVDS System Reference Input True/Complement.
N13	SYNCINB+	Input	Active Low JESD204B LVDS/CMOS Sync Input True.
P13	SYNCINB−	Input	Active Low JESD204B LVDS Sync Input Complement.
Data Outputs			
N4, P4	SERDOUT7+, SERDOUT7−	Output	Lane 7 Output Data True/Complement.
N5, P5	SERDOUT6+, SERDOUT6−	Output	Lane 6 Output Data True/Complement.
N6, P6	SERDOUT5+, SERDOUT5−	Output	Lane 5 Output Data True/Complement.
N7, P7	SERDOUT4+, SERDOUT4−	Output	Lane 4 Output Data True/Complement.
N8, P8	SERDOUT3+, SERDOUT3−	Output	Lane 3 Output Data True/Complement.
N9, P9	SERDOUT2+, SERDOUT2−	Output	Lane 2 Output Data True/Complement.
N10, P10	SERDOUT1+, SERDOUT1−	Output	Lane 1 Output Data True/Complement.
N11, P11	SERDOUT0+, SERDOUT0−	Output	Lane 0 Output Data True/Complement.

Pin No.	Mnemonic	Type	Description
Digital Controls			
L8	PDWN/STBY	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby.
L5	CSB	Input	SPI Chip Select (Active Low).
L6	SCLK	Input	SPI Serial Clock.
L7	SDIO	Input/Output	SPI Serial Data Input/Output.

[1] See the Theory of Operation section and Applications Information section for more information on isolating the planes for optimal performance.
[2] Denotes clock domain.
[3] Denotes SYSREF± domain.
[4] Denotes isolation domain.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 0.975 V, AVDD1_SR = 0.975 V, AVDD2 = 1.9 V, AVDD3 = 2.5 V, DVDD = 0.975 V, DRVDD1 = 0.975 V, DRVDD2 = 1.9 V, SPIVDD = 1.9 V, sampling rate = 3000 MHz, 1.7 V p-p full-scale differential input, DDC decimation rate = 8, default buffer current settings, T_A = 25°C, 128,000 FFT sample, unless otherwise noted. See Table 10 for the recommended settings.

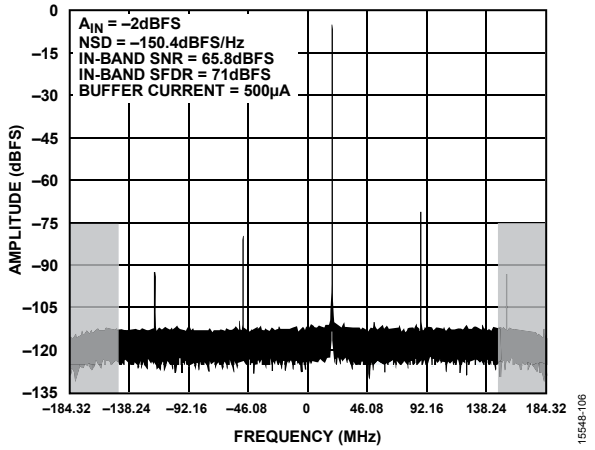


Figure 5. Single-Tone FFT at f_{IN} = 960 MHz, NCO Frequency = 942.5 MHz, A_{IN} = –2 dBFS, f_S = 2.94912 GHz

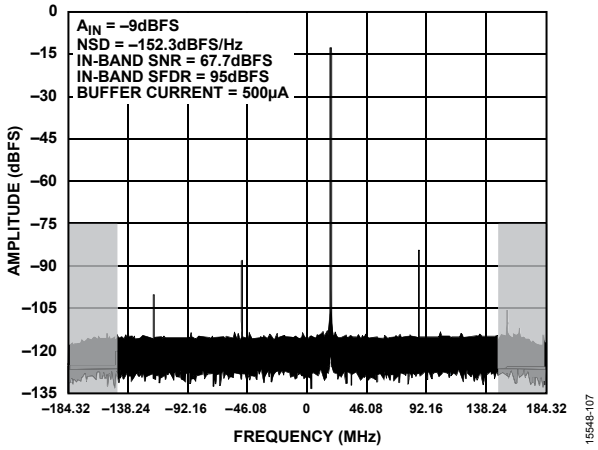


Figure 6. Single-Tone FFT at f_{IN} = 960 MHz, NCO Frequency = 942.5 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

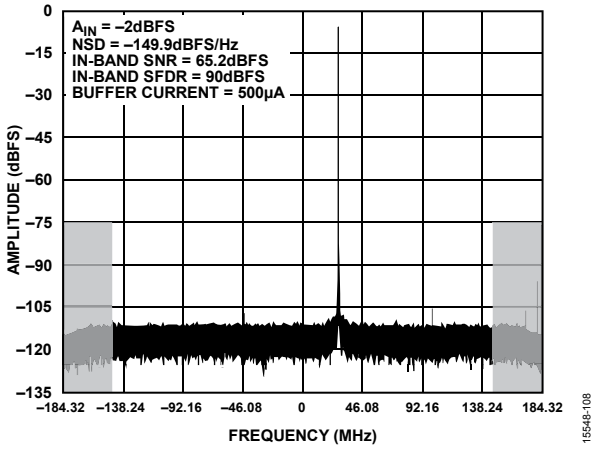


Figure 7. Single-Tone FFT at f_{IN} = 1870 MHz, NCO Frequency = 1842 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

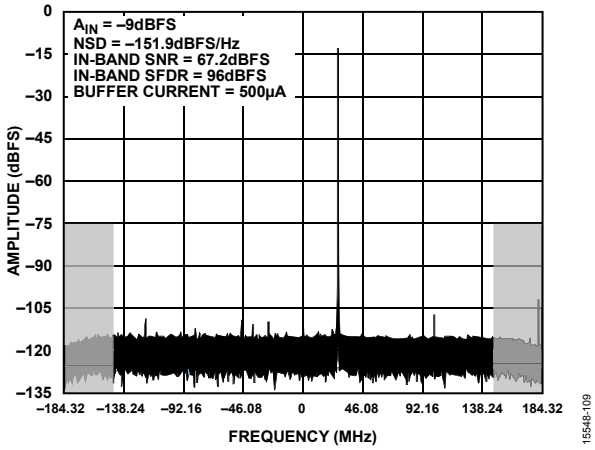


Figure 8. Single-Tone FFT at f_{IN} = 1870 MHz, NCO Frequency = 1842 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

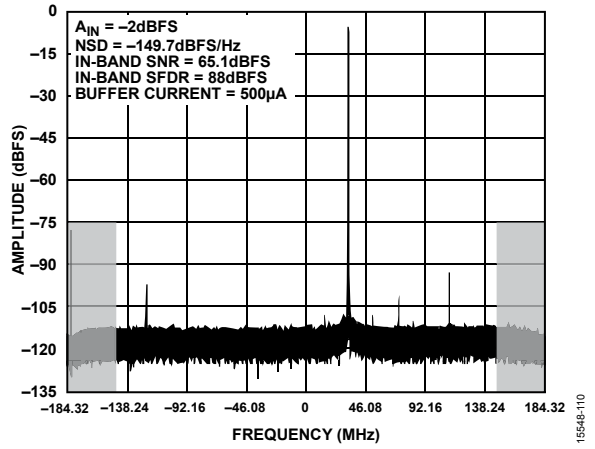


Figure 9. Single-Tone FFT at f_{IN} = 2170 MHz, NCO Frequency = 2140 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

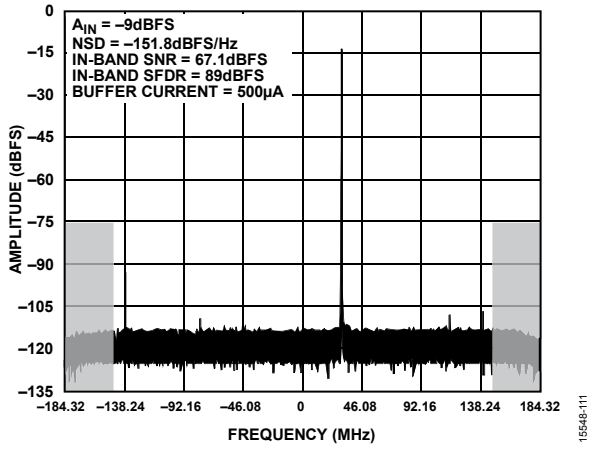


Figure 10. Single-Tone FFT at f_{IN} = 2170 MHz, NCO Frequency = 2140 MHz, A_{IN} = –9 dBFS; f_S = 2.94912 GHz

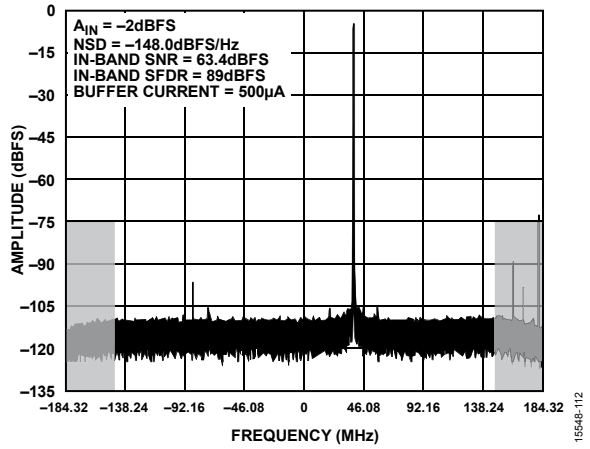


Figure 11. Single-Tone FFT at f_{IN} = 2690 MHz, NCO Frequency = 2655 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

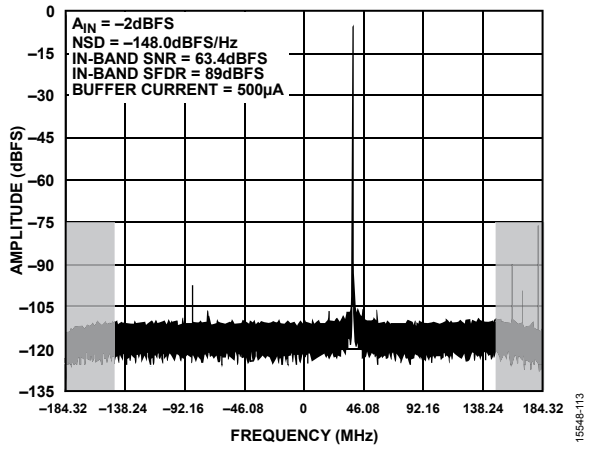


Figure 12. Single-Tone FFT at f_{IN} = 2690 MHz, NCO Frequency = 2655 MHz, A_{IN} = –2 dBFS; f_S = 2.94912 GHz

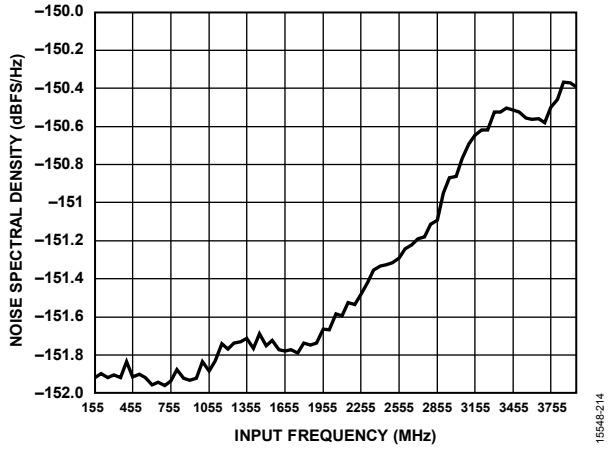


Figure 13. NSD vs. f_{IN}; A_{IN} = –9 dBFS

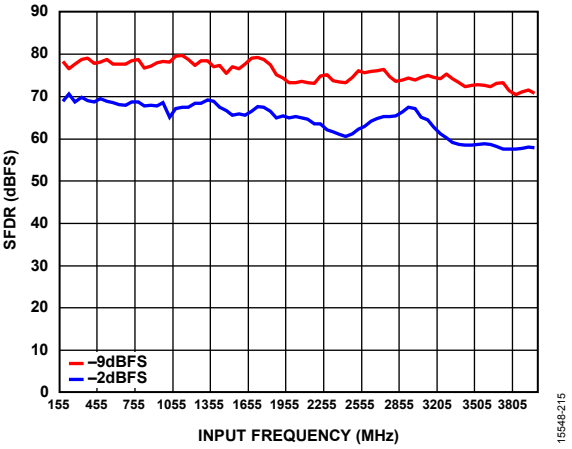


Figure 14. SFDR vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

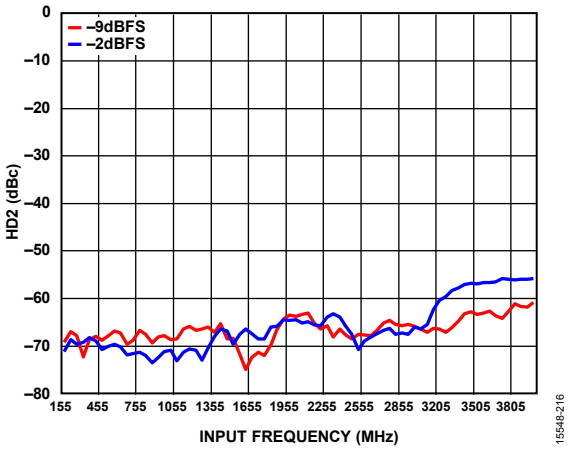


Figure 15. Second Harmonic Distortion (HD2) vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

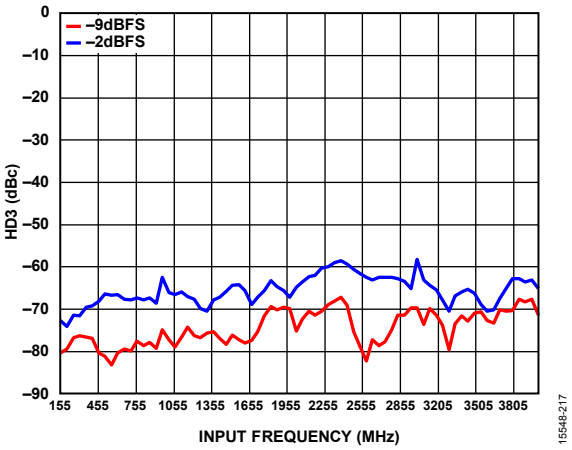


Figure 16. Third Harmonic Distortion (HD3) vs. f_{IN}; A_{IN} = –2 dBFS and –9 dBFS

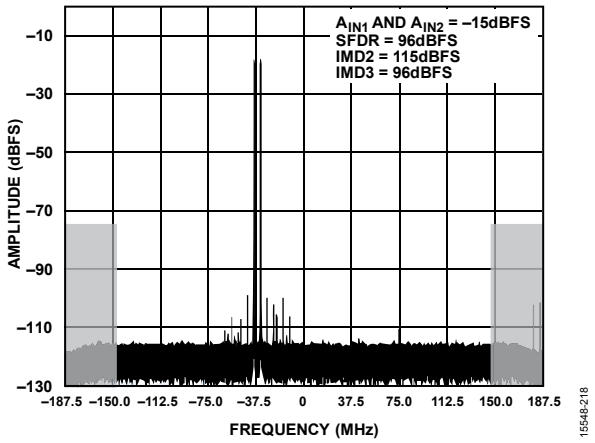


Figure 17. Two-Tone FFT; f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz; NCO Frequency = 1874.28 MHz; f_S = 3 GHz

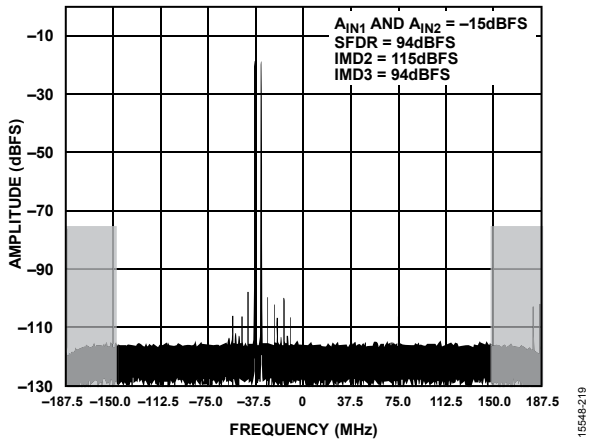


Figure 18. Two-Tone FFT; f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz NCO Frequency = 2176.92 MHz; f_S = 3 GHz

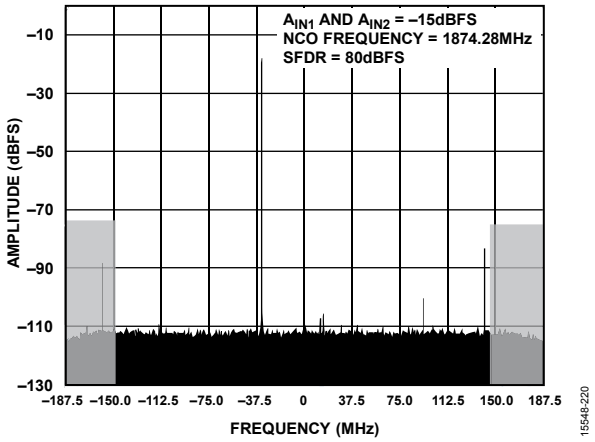


Figure 19. Two-Tone FFT; f_{IN1} = 1800 MHz, f_{IN2} = 2100 MHz NCO Frequency = 1874.28 MHz; f_S = 2.94912 GHz

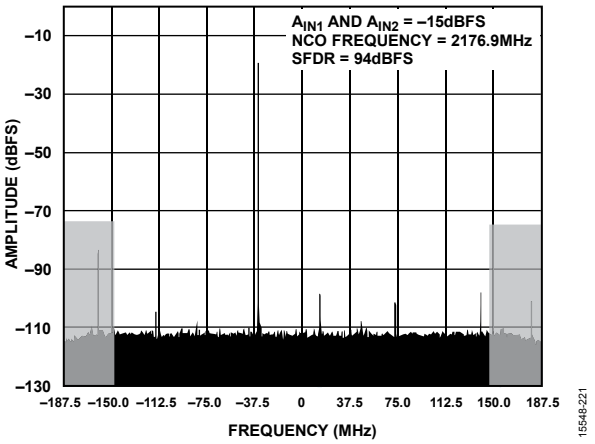


Figure 20. Two-Tone FFT; f_{IN1} = 1800 MHz, f_{IN2} = 2100 MHz NCO Frequency = 2176.92 MHz; f_S = 2.94912 GHz

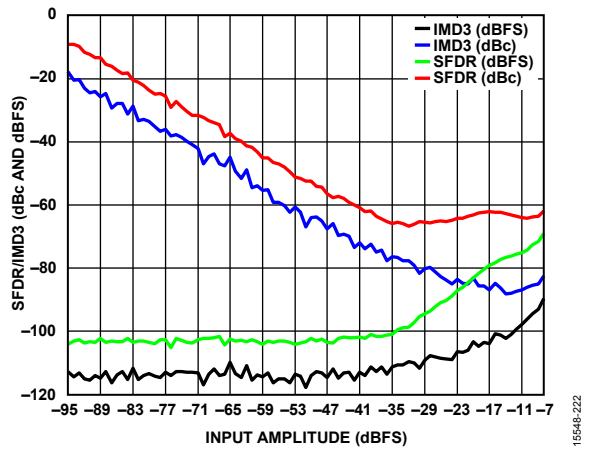


Figure 21. Two-Tone SFDR/IMD3 vs. Input Amplitude with f_{IN1} = 1841.5 MHz, f_{IN2} = 1846.5 MHz

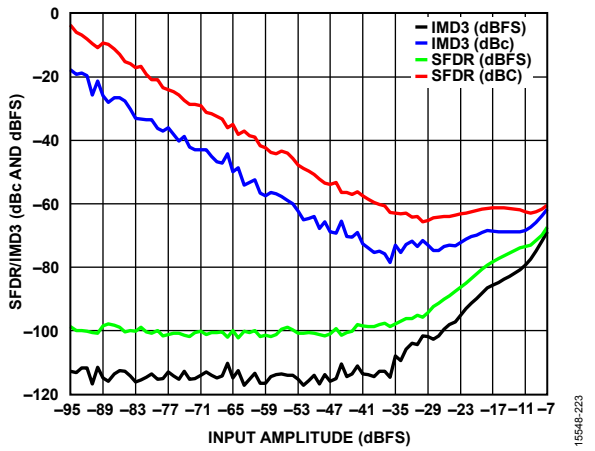


Figure 22. Two-Tone SFDR/IMD3 vs. Input Amplitude with f_{IN1} = 2137.5 MHz, f_{IN2} = 2142.5 MHz

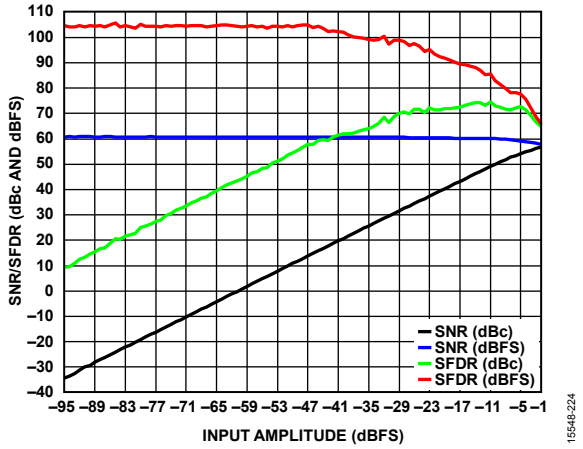


Figure 23. SNR/SFDR vs. Input Amplitude, f_{IN} = 950 MHz

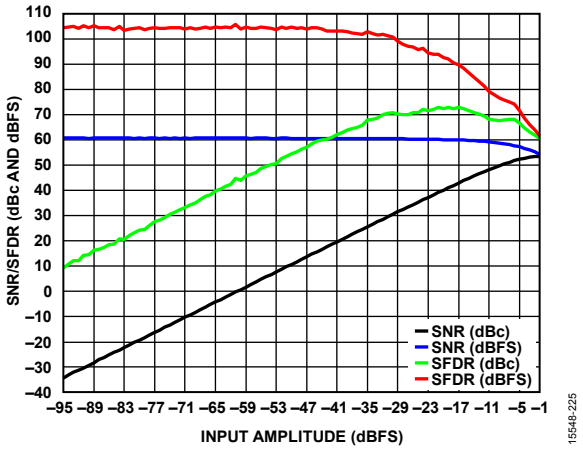


Figure 24. SNR/SFDR vs. Input Amplitude, f_{IN} = 1800 MHz

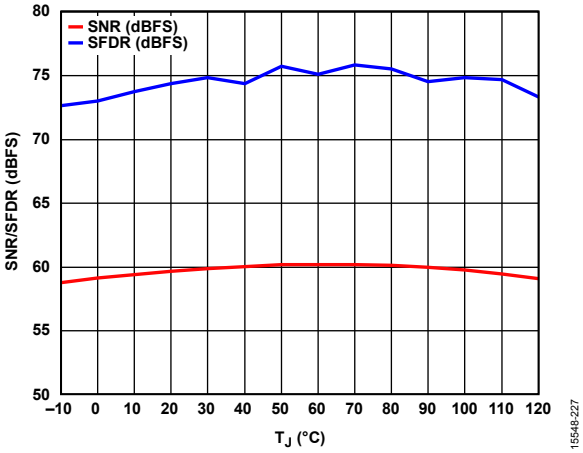


Figure 25. SNR/SFDR vs. Junction Temperature, f_{IN} = 950 MHz, A_{IN} = −9 dBFS

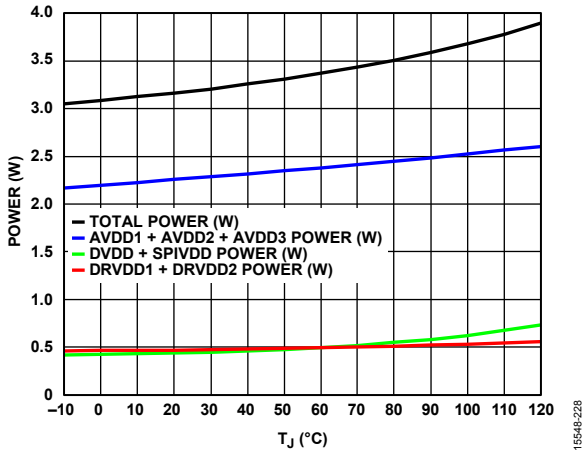


Figure 26. Power vs. Junction Temperature, f_{IN} = 950 MHz

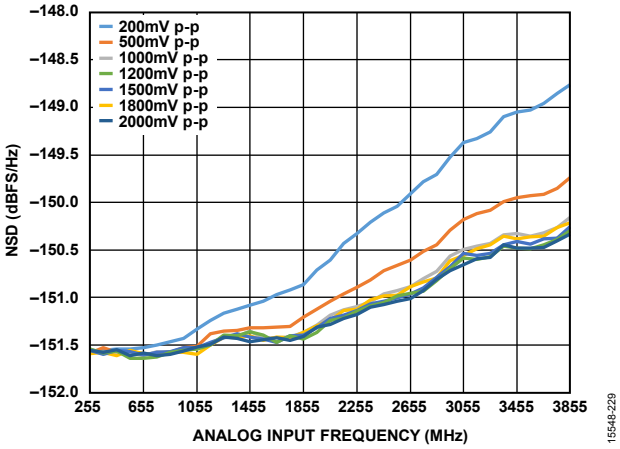


Figure 27. NSD vs. Analog Input Frequency vs. Various Clock Amplitude in Differential Voltages, A_{IN} = −9 dBFS

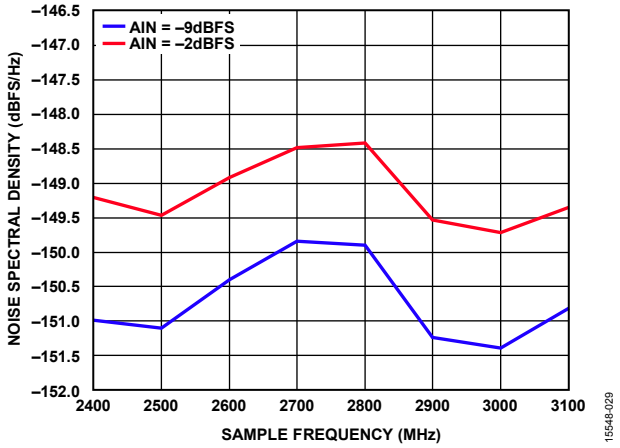


Figure 28. NSD vs. Sample Frequency (f_S)
f_{IN} = 1.8 GHz; A_{IN} = −2 dBFS

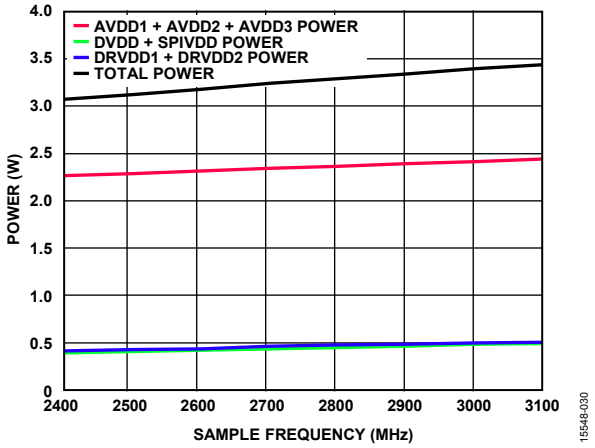


Figure 29. Power Dissipation vs. Sample Frequency (f_S)
f_{IN} = 1.8 GHz; A_{IN} = –2 dBFS

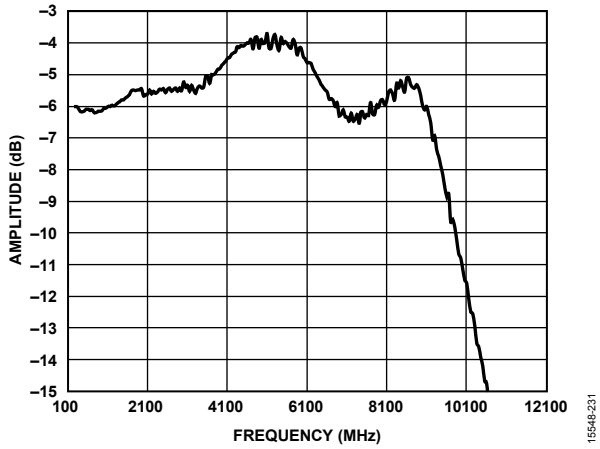


Figure 30. Input Bandwidth (see Figure 46 for Input Configuration)

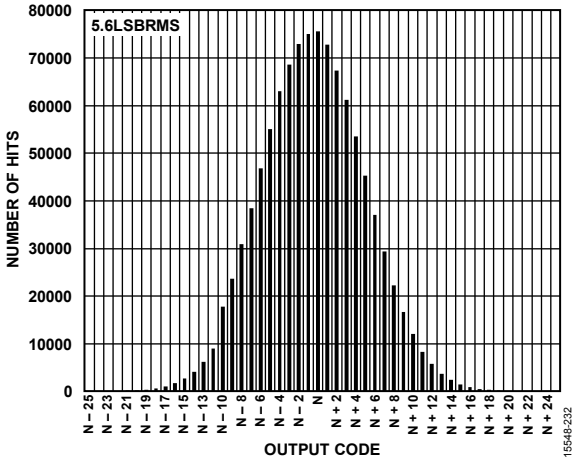


Figure 31. Input Referred Noise Histogram

EQUIVALENT CIRCUITS

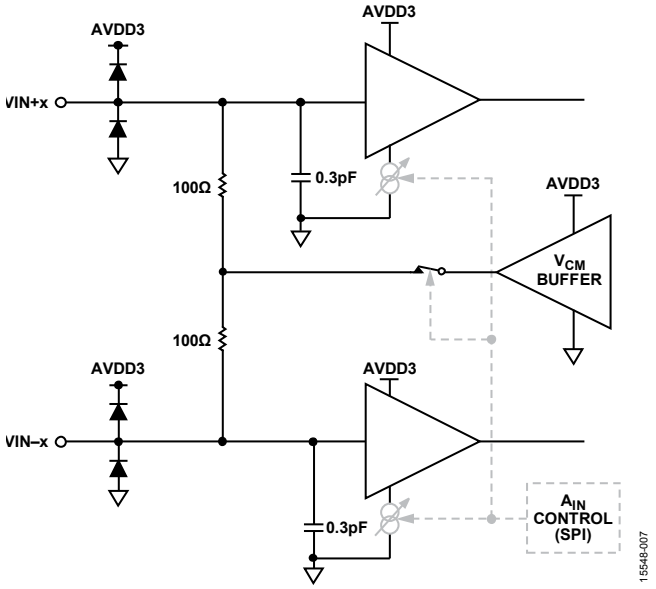


Figure 32. Analog Inputs

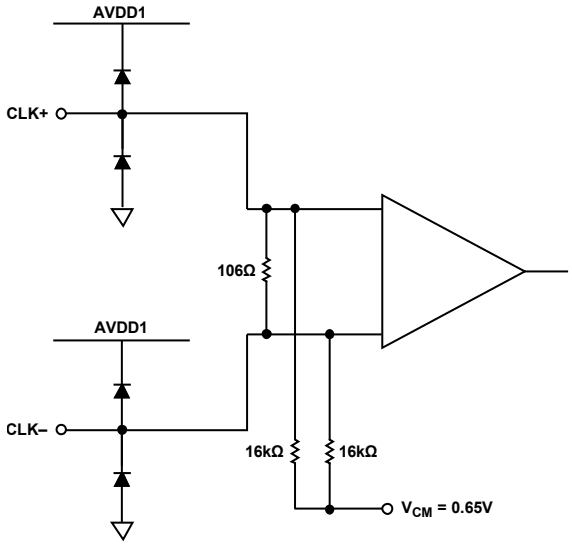


Figure 33. Clock Inputs

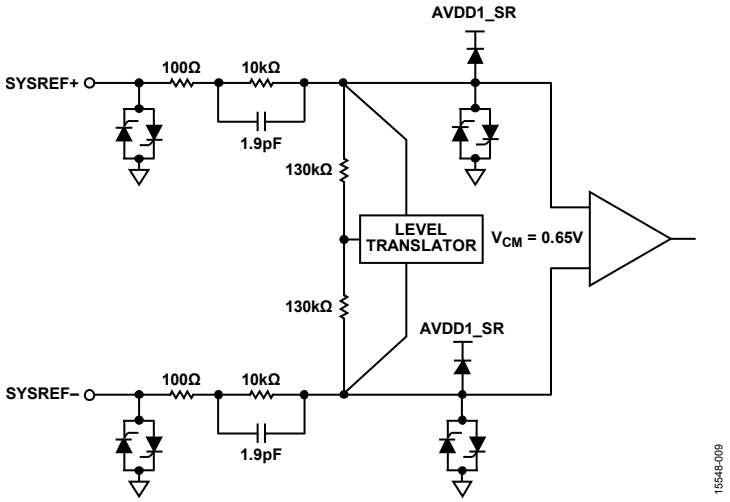


Figure 34. SYSREF± Inputs

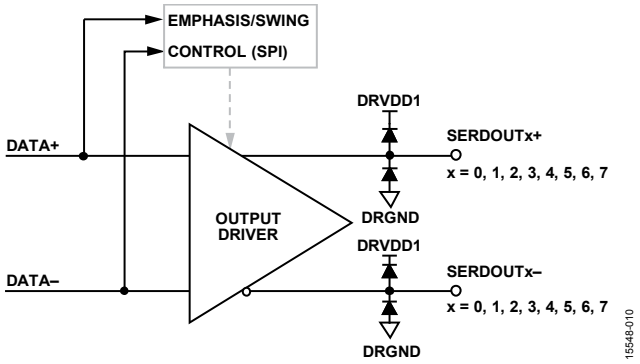


Figure 35. Digital Outputs

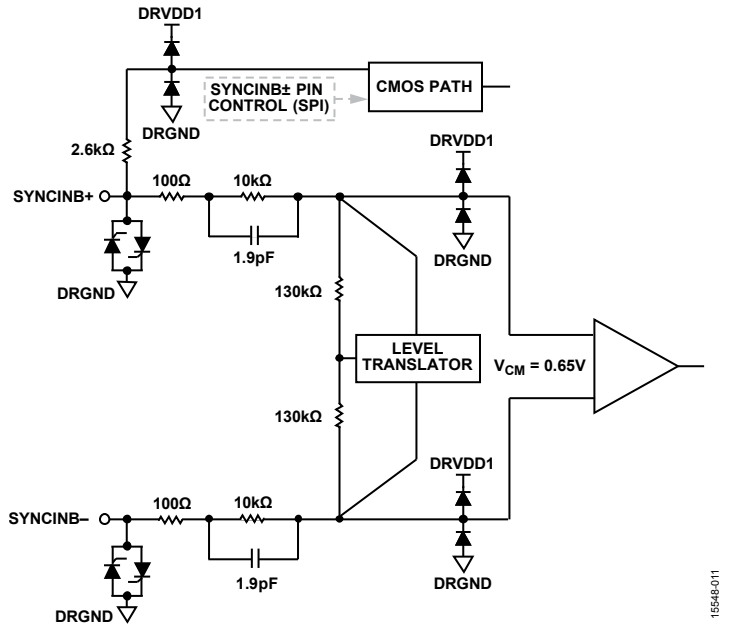


Figure 36. SYNCINB± Inputs

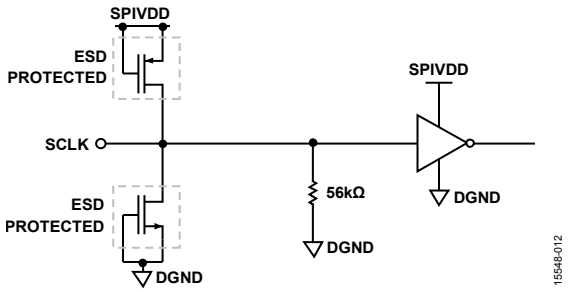


Figure 37. SCLK Input

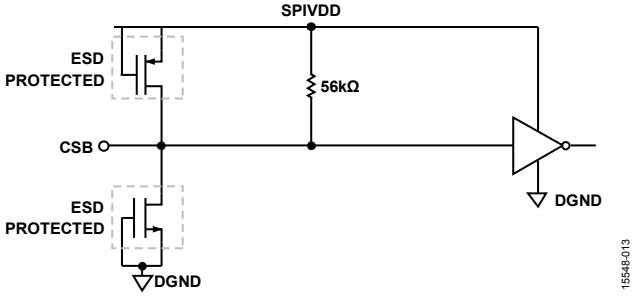


Figure 38. CSB Input

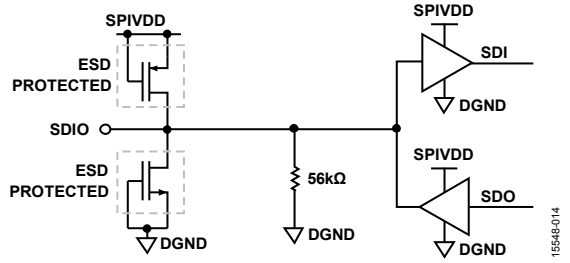


Figure 39. SDIO Input

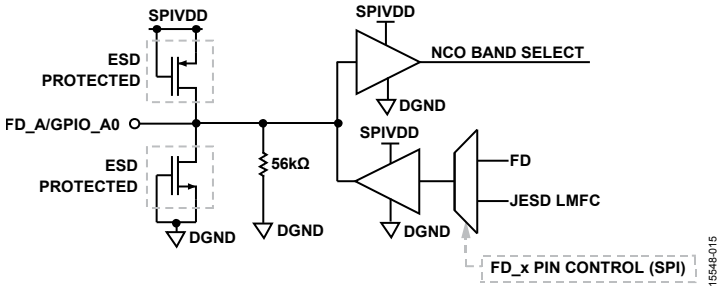


Figure 40. FD_A/GPIO_A0, FD_B/GPIO_B0, Input/Outputs

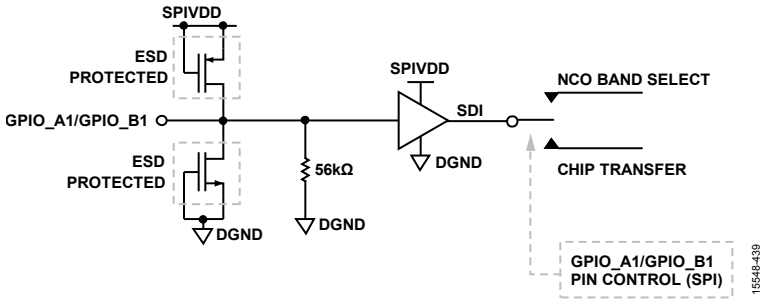


Figure 41. GPIO_A1/GPIO_B1

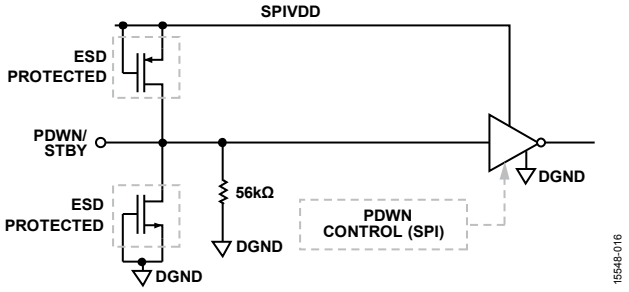


Figure 42. PDWN/STBY Input

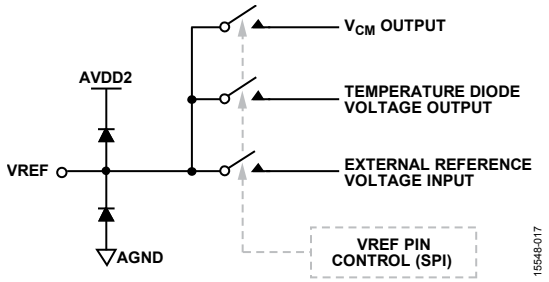


Figure 43. VREF Input/Output

THEORY OF OPERATION

The AD6688 has two analog input channels and up to eight JESD204B output lane pairs. The ADC samples wide bandwidth analog signals of up to 5 GHz. The actual 3 dB roll-off of the analog inputs is greater than 9 GHz. The AD6688 is optimized for wide input bandwidth, high sampling rate, excellent linearity, and low power in a small package.

The dual ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations.

The AD6688 has several functions that simplify the AGC function in a communications receiver. The programmable threshold detector allows monitoring of the incoming signal power using the fast detect output bits of the ADC. If the input signal level exceeds the programmable threshold, the fast detect indicator goes high. Because this threshold indicator has low latency, the user can quickly turn down the system gain to avoid an overrange condition at the ADC input.

The Subclass 1 JESD204B-based high speed serialized output data lanes can be configured in one lane (L = 1), two lane (L = 2), four lane (L = 4), and eight lane (L = 8) configurations, depending on the sample rate and the decimation ratio. Multiple device synchronization is supported through the SYSREF± and SYNCINB± input pins. The SYSREF± pin in the AD6688 can also be used as a timestamp of data as it passes through the ADC and out the JESD204B interface.

ADC ARCHITECTURE

The architecture of the AD6688 consists of an input buffered pipelined ADC. The input buffer provides a termination impedance to the analog input signal. This termination impedance is set to 200 Ω. The equivalent circuit diagram of the analog input termination is shown in Figure 32. The input buffer is optimized for high linearity, low noise, and low power across a wide bandwidth.

The input buffer provides a linear high input impedance (for ease of drive) and reduces kickback from the ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample; at the same time, the remaining stages operate with the preceding samples. Sampling occurs on the rising edge of the clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD6688 is a differential buffer. The internal common-mode voltage of the buffer is 1.35 V. The clock signal alternately switches the input circuit between sample mode and hold mode.

Either a differential capacitor or two single-ended capacitors (or a combination of both) can be placed on the inputs to provide a matching passive network. These capacitors ultimately create a low-pass filter that limits unwanted broadband noise. For more information, refer to the *Analog Dialogue* article "Transformer-Coupled Front-End for Wideband A/D Converters" (Volume 39, April 2005). In general, the precise front-end network component values depend on the application.

Figure 44 shows the differential input return loss curve for the analog inputs across a frequency range of 100 MHz to 10 GHz. The reference impedance is 100 Ω.

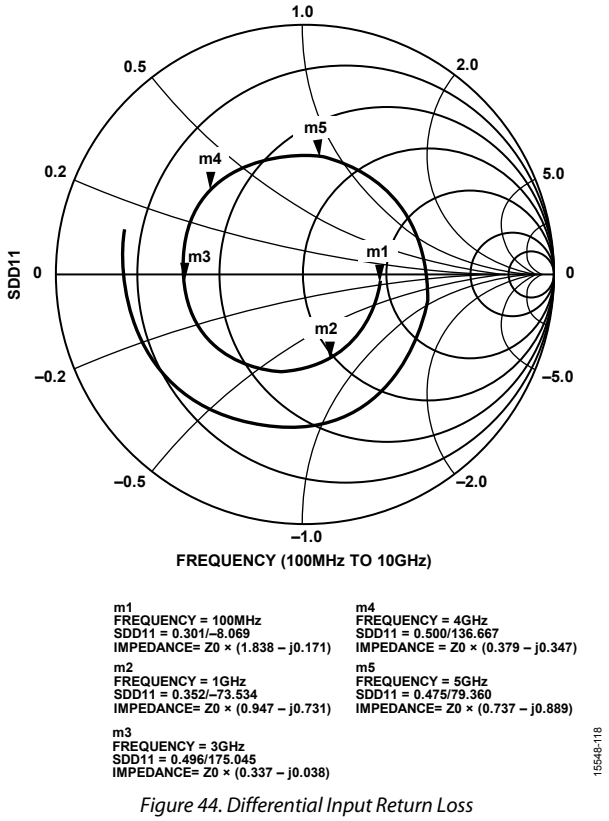


Figure 44. Differential Input Return Loss

For best dynamic performance, the source impedances driving VIN+x and VIN−x must be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC. An internal reference buffer creates a differential reference that defines the span of the ADC core.

Maximum SNR performance is achieved by setting the ADC to the largest span in a differential configuration. For the AD6688, the available span is programmable through the SPI port from 1.1 V p-p to 2.04 V p-p differential, with 1.7 V p-p differential being the default.

Differential Input Configurations

There are several ways to drive the AD6688, either actively or passively. Optimum performance is achieved by driving the analog input differentially.

For applications where SNR and SFDR are key parameters, differential transformer coupling is the recommended input configuration (see Figure 45 and Table 9) because the noise performance of most amplifiers is not adequate to achieve the true performance of the AD6688.

For low to midrange frequencies, a double balun or double transformer network (see Figure 45 and Table 9) is recommended for optimum performance of the AD6688. For higher frequencies in the second or third Nyquist zones, it is recommended to remove some of the front-end passive components to ensure wideband operation (see Figure 45 and Table 9).

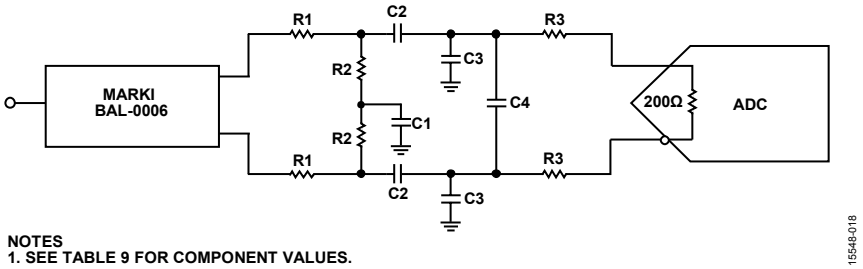


Figure 45. Differential Transformer-Coupled Configuration for AD6688

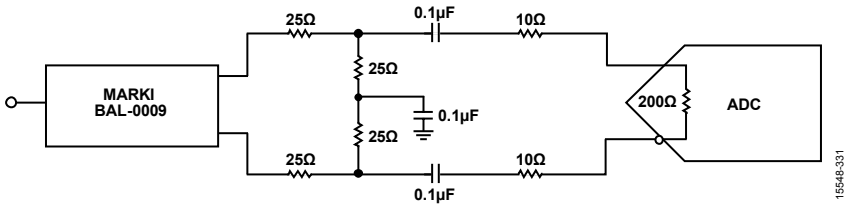


Figure 46. Input Network Configuration for Frequencies >5 GHz

Table 9. Differential Transformer-Coupled Input Configuration Component Values

Device	Frequency Range	Transformer	R1	R2	R3	C1	C2	C3	C4
AD6688	<5000 MHz	BAL-0006	25 Ω	25 Ω	10 Ω	0.1 µF	0.1 µF	0.4 pF	0.4 pF

Input Common Mode

The analog inputs of the AD6688 are internally biased to the common-mode voltage, as shown in Figure 48. The common-mode buffer has a limited range in that the performance suffers greatly if the common-mode voltage drops by more than 50 mV on either side of the nominal value.

For dc-coupled applications, the recommended operation procedure is to export the common-mode voltage to the VREF pin using the SPI writes listed in this section. The common-mode voltage must be set by the exported value to ensure proper ADC operation. Disconnect the internal common-mode buffer from the analog input using Register 0x1908.

When performing SPI writes for dc coupling operation, use the following register settings in order:

1. Set Register 0x1908, Bit 2 to disconnect the internal common-mode buffer from the analog input. Note that this is a local register.
2. Set Register 0x18A6 to 0x00 to turn off the voltage reference.
3. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
4. Set Register 0x18E3, Bit 6 to 1 to turn on the V_{CM} export.
5. Set Register 0x18E3, Bit[5:0] to the buffer current setting (Register 0x1A4C and Register 0x1A4D) to improve the accuracy of the common-mode export.

Figure 47 shows the block diagram representation of a dc-coupled application.

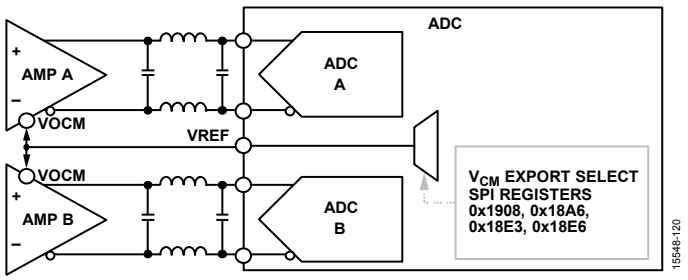


Figure 47. DC-Coupled Application Using AD6688

Analog Input Buffer Controls and SFDR Optimization

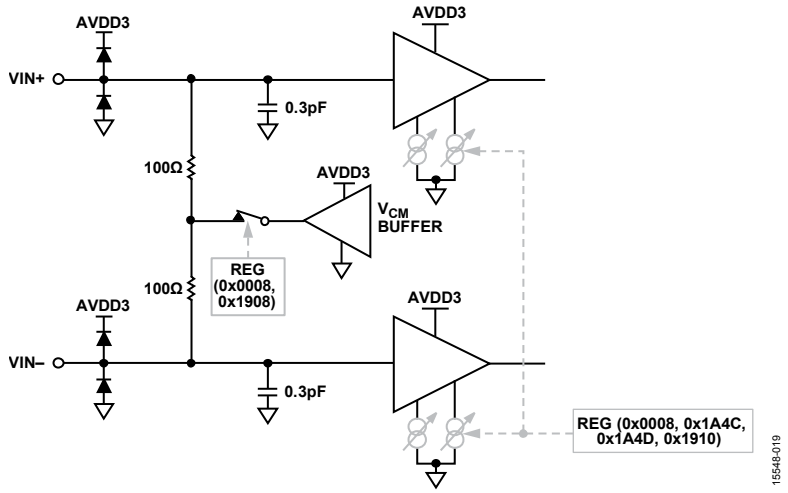


Figure 48. Analog Input Controls

The AD6688 input buffer offers flexible controls for the analog inputs, such as buffer current, dc coupling, and input full-scale adjustment. All the available controls are shown in Figure 48.

Using the 0x1A4C and 0x1A4D registers, the buffer behavior on each channel can be adjusted to optimize the SFDR over various input frequencies and bandwidths of interest. Register 0x1910 can be used to change the internal reference voltage. Changing the internal reference voltage results in a change in the input full-scale voltage.

When the input buffer current in Register 0x1A4C and Register 0x1A4D is set, the amount of current required by the AVDD3 supply changes. This relationship is shown in Figure 49. For a complete list of buffer current settings, see Table 46.

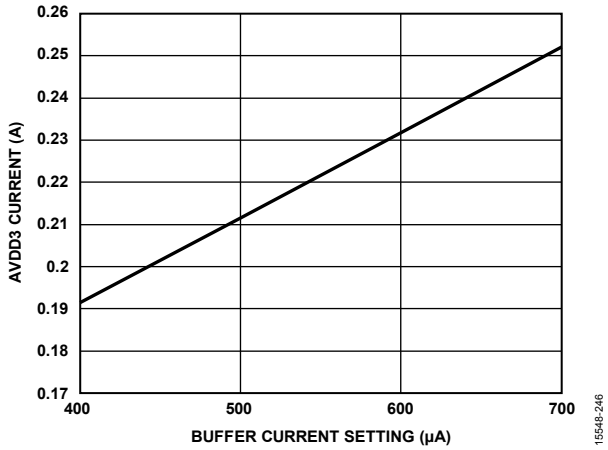


Figure 49. AVDD3 Current (I_{AVDD3}) vs. Buffer Control 1 Setting in Register 0x1A4C and Register 0x1A4D

Table 10 shows the recommended values for the buffer current for various Nyquist zones.

Table 10. SFDR Optimization for Input Frequencies

Product	Frequency	0x1A4C and 0x1A4D
AD6688	DC to 1500 MHz	400 µA/500 µA
	1500 MHz to 3000 MHz	500 µA
	>3000 MHz	500 µA/700 µA

Dither

The AD6688 has internal on-chip dither circuitry that improves the ADC linearity and SFDR, particularly at smaller signal levels. A known but random amount of white noise is injected into the input of the AD6688. This dither improves the small signal linearity within the ADC transfer function and is precisely subtracted out digitally. The dither is turned on by default and does not reduce the ADC input dynamic range. The data sheet specifications and limits are obtained with the dither turned on.

The dither is on by default. It is not recommended to turn it off.

Absolute Maximum Input Swing

The absolute maximum input swing allowed at the inputs of the AD6688 is 5.8 V p-p differential. Signals operating near or at this level can cause permanent damage to the ADC. See Table 6 for more information.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD6688. This internal 0.5 V reference sets the full-scale input range of the ADC. The full-scale input range can be adjusted via the ADC input full-scale control register (Register 0x1910). For more information on adjusting the input swing, see Table 46. Figure 51 shows the block diagram of the internal 0.5 V reference controls.

The SPI Register 0x18A6 enables the user to either use this internal 0.5 V reference or to provide an external 0.5 V reference. When using an external voltage reference, provide a 0.5 V reference. The full-scale adjustment is made using the SPI, irrespective of the reference voltage. For more information on adjusting the full-scale level of the AD6688, refer to the Memory Map section.

The SPI writes required to use the external voltage reference, in order, are as follows:

1. Set Register 0x18E3 to 0x00 to turn off the V_{CM} export.
2. Set Register 0x18E6 to 0x00 to turn off the temperature diode export.
3. Set Register 0x18A6 to 0x01 to turn on the external voltage reference.

The use of an external reference may be necessary in some applications to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. Figure 50 shows the typical drift characteristics of the internal 0.5 V reference.

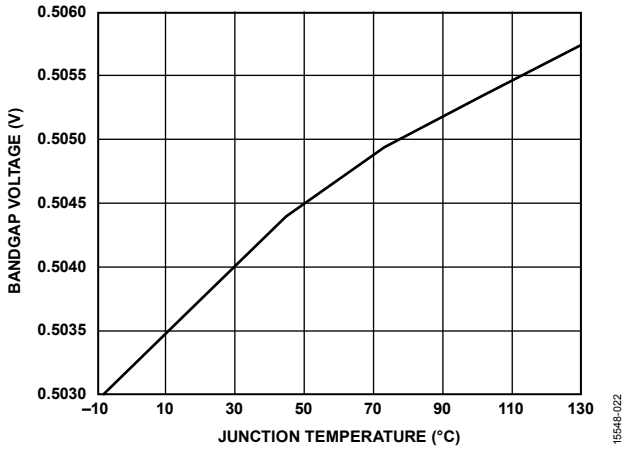


Figure 50. Typical V_{REF} Drift

The external reference must be a stable 0.5 V reference. The ADR130 is a good option for providing the 0.5 V reference. Figure 52 shows how the ADR130 can be used to provide the external 0.5 V reference to the AD6688. The grayed out areas show unused blocks within the AD6688 while using the ADR130 to provide the external reference.

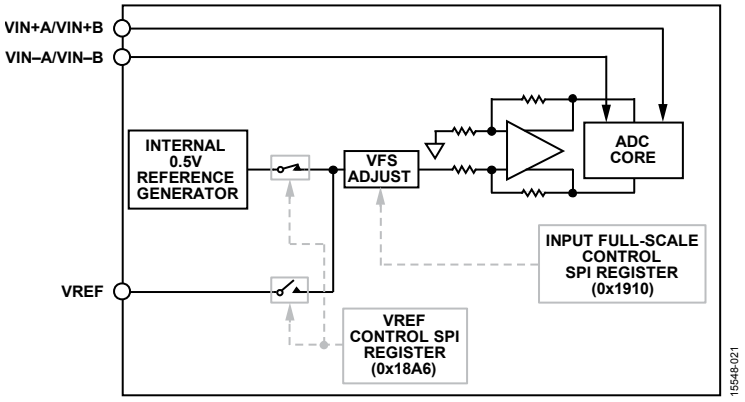


Figure 51. Internal Reference Configuration and Controls

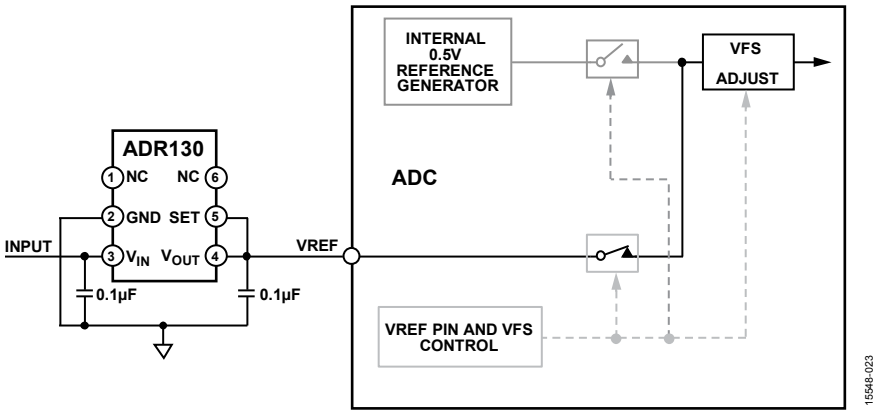


Figure 52. External Reference Using ADR130

DC OFFSET CALIBRATION

The AD6688 contains a digital filter to remove the dc offset from the output of the ADC. For ac-coupled applications, this filter can be enabled by writing 0x86 to Register 0x0701. The filter computes the average dc signal and it is digitally subtracted from the ADC output. As a result, the dc offset is improved to better than 70 dBFS at the output. Since the filter does not distinguish between the source of dc signals, this feature can be used when the signal content at dc is not of interest. The filter corrects dc up to ±512 codes and saturates beyond that.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD6688 sample clock inputs (CLK+ and CLK–) with a differential signal. This signal is ac-coupled to the CLK+ and CLK– pins via a transformer or clock drivers. These pins are biased internally and require no additional biasing.

Figure 53 shows the differential input return loss curve for the clock inputs across a frequency range of 100 MHz to 6 GHz. The reference impedance is 100 Ω.

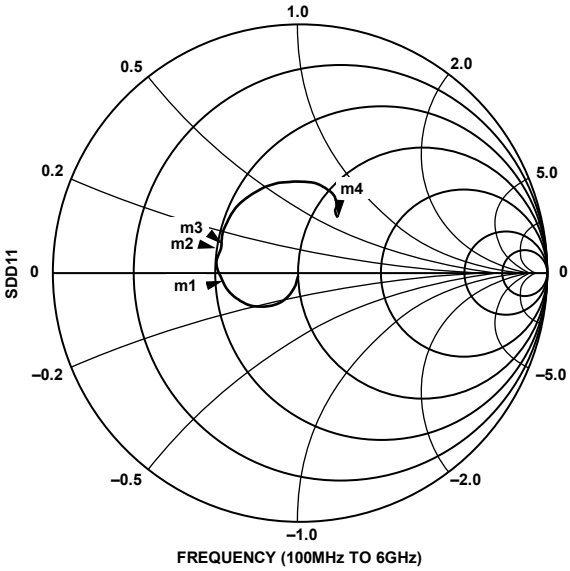


Figure 53. Differential Input Return Loss for the CLK± Inputs

Figure 54 shows a preferred method for clocking the AD6688. The low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer.

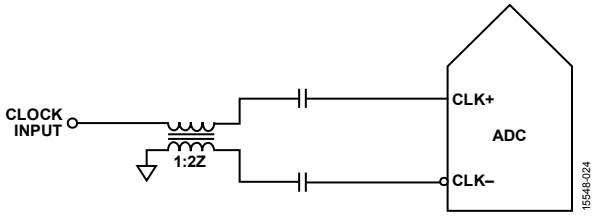


Figure 54. Transformer-Coupled Differential Clock

Another option is to ac couple a differential CML or LVDS signal to the sample clock input pins, as shown in Figure 55.

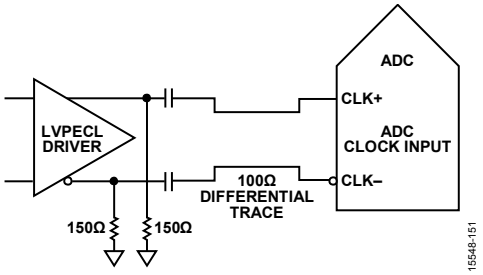


Figure 55. Differential LVPECL Sample Clock

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. The AD6688 contains an internal clock divider and a duty cycle stabilizer (DCS). In the AD6688, the DCS is enabled by default. In applications where the clock duty cycle cannot be guaranteed to be 50%, a higher multiple frequency clock along with the usage of the clock divider is recommended.

When it is not possible to provide a higher frequency clock, it is recommended to turn on the DCS using Register 0x011C and Register 0x011E. Figure 56 shows a block diagram representation showing the different controls to the AD6688 clock inputs. The output of the divider offers a 50% duty cycle, high slew rate (fast edge) clock signal to the internal ADC. See the Memory Map section for more details on using this feature.

Input Clock Divider

The AD6688 contains an input clock divider with the ability to divide the input clock by 1, 2, or 4. The divider ratios can be selected using Register 0x0108, as shown in Figure 56.

The maximum frequency at the CLK± inputs is 6 GHz, which is the limit of the divider. In applications where the clock input is a multiple of the sample clock, take care to program the appropriate divider ratio into the clock divider before applying the clock signal. This ensures that the current transients during device startup are controlled.

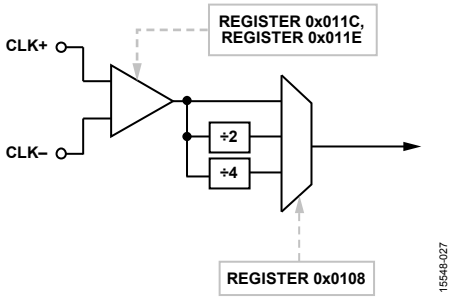


Figure 56. Clock Divider Circuit

The AD6688 clock divider can be synchronized using the external SYSREF± input. A valid SYSREF± causes the clock divider to reset to a programmable state. This synchronization feature allows multiple devices to have their clock dividers aligned to guarantee simultaneous input sampling. See the Memory Map Register Details section for more information.

Input Clock Divider ½ Period Delay Adjust

The input clock divider inside the AD6688 provides phase delay in increments of ½ the input clock cycle. Register 0x0109 can be programmed to enable this delay independently for each channel. Changing this register does not affect the stability of the JESD204B link.

Clock Fine Delay and Super Fine Delay Adjust

The AD6688 sampling edge instant can be adjusted by writing to Register 0x0110, Register 0x0111, and Register 0x0112. Bits[2:0] of Register 0x0110 enable the selection of the fine delay, or the fine delay with super fine delay. The fine delay allows the user to delay the clock edges with 16 step or 192 step delay options. The super fine delay is an unsigned control to adjust the clock delay in super fine steps of 0.25 ps each.

Register 0x0112, Bits[7:0] offer the user the option to delay the clock in 192 delay steps. Register 0x0111, Bits[7:0] offer the user the option to delay the clock in 128 super-fine steps. These values can be programmed individually for each channel. To utilize the super fine delay option, the user must set the clock delay control, Register 0x0110, Bits[2:0], to 0x2 or 0x6. Figure 57 shows the controls available to the clock dividers within the AD6688. It is recommended to apply the same delay settings to the digital delay circuits as are applied to the analog delay circuits to maintain sample accuracy through the pipe.

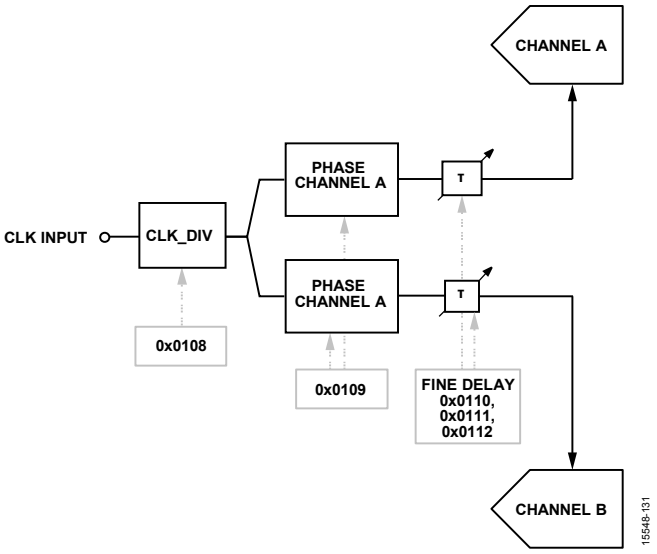


Figure 57. Clock Divider Phase and Delay Controls

The clock delay adjust takes effect immediately when it is enabled via SPI writes. Enabling the clock fine delay adjust in Register 0x0110 causes a datapath reset. However, the contents of Register 0x0111 and Register 0x0112 can be changed without affecting the stability of the JESD204B link.

Clock Coupling Considerations

The AD6688 has many different domains within the analog supply that control various aspects of the data conversion. The clock domain is supplied by the A4, A5, A10, A11, B4, and B11 pins on the analog supply, AVDD1 (0.975 V), and the A6, A9, B6, B7, B8, B9, C6, C7, C8, C9, D7, and D8 pins on the ground (AGND) side. To minimize coupling between the clock supply domain and the other analog domains, it is recommended to add a supply Q factor reduction circuitry for the A4/A11 and B4/B11 pins, as shown in Figure 58.

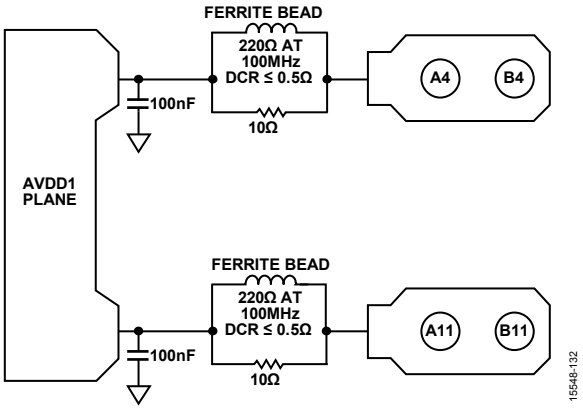


Figure 58. De-Q Network Recommendation for Clock Domain Supply

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR_{JITTER} = -20 \times \log_{10}(2 \times \pi \times f_A \times t_J)$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications.

Treat the clock input as an analog signal in cases where aperture jitter can affect the dynamic range of the AD6688. Separate power supplies for clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. If the clock is generated from another type of source (by gating, dividing, or other methods), retime the clock by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs.

The SNR can be estimated by using the following equation:

$$SNR(\text{dBFS}) = -10\log_{10}\left[10^{\left(\frac{-SNR_{ADC}}{10}\right)} + 10^{\left(\frac{-SNR_{JITTER}}{10}\right)}\right]$$

POWER-DOWN/STANDBY MODE

The AD6688 has a PDWN/STBY pin that can configure the device in power-down or standby mode. The default operation is PDWN. The PDWN/STBY pin is a logic high pin. When in power-down mode, the JESD204B link is disrupted. The power-down option can also be set via Register 0x003F and Register 0x0040.

In standby mode, the JESD204B link is not disrupted and transmits zeros for all converter samples. This can be changed using Register 0x0571, Bit 7 to select /K/ characters.

TEMPERATURE DIODE

The AD6688 contains diode-based temperature sensors. The diodes output voltages commensurate to the temperature of the silicon. There are multiple diodes on the die; however, the results established using the temperature diode at the central location of the die can be regarded as representative of the entire die. However, in applications where only one channel is used (the other being in the power-down state), it is recommended to read the temperature diode corresponding to the channel that is on. Figure 59 shows the locations of the diodes inside the AD6688 whose voltages can be output to the VREF pin. In each location, there is a pair of diodes, one of which is 20× the size of the other. It is recommended to use both diodes in a location to obtain an accurate estimate of the die temperature. For more information, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs*.

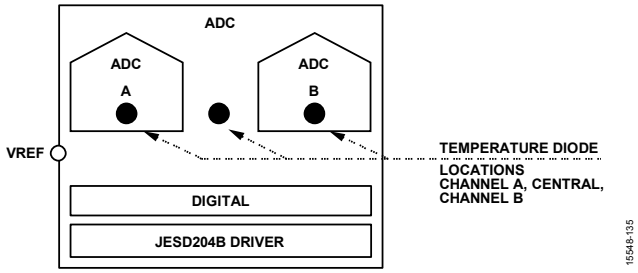


Figure 59. Temperature Diode Locations in the Die

The temperature diode voltages can be exported to the VREF pin using the SPI. Use Register 0x18E6 to enable or disable the diodes. It is important to note that other voltages can be exported to the VREF pin at the same time, which can result in undefined behavior. To ensure a proper readout, switch off all other voltage exporting circuits as detailed in this section. Figure 60 shows the block diagram representation of the controls that are required to enable the diode voltage readout.

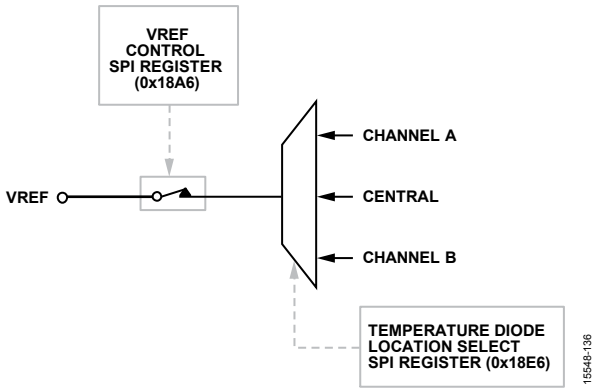


Figure 60. Register Controls to Output Temperature Diode Voltage on VREF Pin

The SPI writes required to export the central temperature diode are as follows (see the Memory Map Register Details for more information):

1. Set Register 0x0008 to 0x03 to select both channels.
2. Set Register 0x18E3 to 0x00 to turn off the V_{CM} export.
3. Set Register 0x18A6 to 0x00 to turn off the voltage reference export.
4. Set Register 0x18E6 to 0x01 to turn on voltage export of the central 1× temperature diode. The typical voltage response of the temperature diode is shown in Figure 61. Even though this voltage does represent the die temperature, it is recommended to take measurements from a pair of diodes for improved accuracy. The following step explains how to enable the 20× diode.
5. Set Register 0x18E6 to 0x02 to turn on the second central temperature diode of the pair, which is 20× the size of the first. For the method utilizing two diodes simultaneously giving a more accurate result, see the AN-1432 Application Note, *Practical Thermal Modeling and Measurements in High Power ICs*.

The relationship between the measured ΔV and the junction temperature in degrees Celsius is shown in Figure 62.

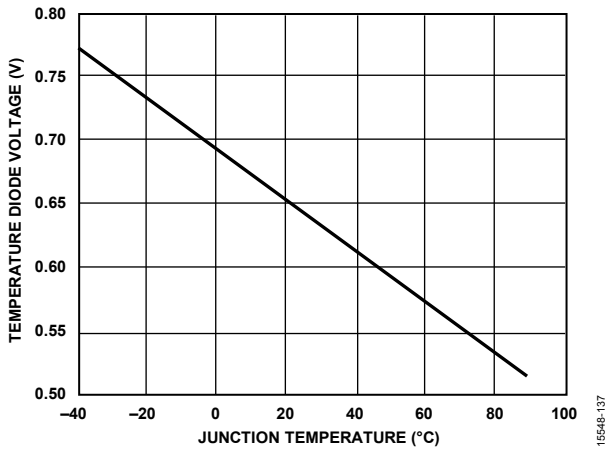


Figure 61. Typical Voltage Response of 1× Temperature Diode

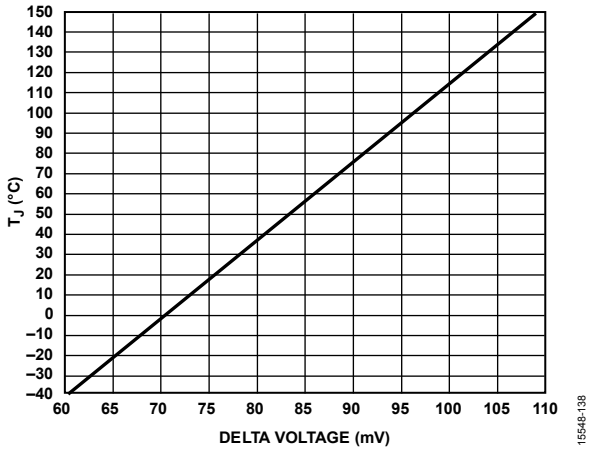


Figure 62. Junction Temperature (°C) vs. ΔV (mV)

ADC OVERRANGE AND FAST DETECT

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overrange bit in the JESD204B outputs provides information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, the latency of this function is of major concern. Highly pipelined converters can have significant latency. The AD6688 contains fast detect circuitry for individual channels to monitor the threshold and assert the FD_A and FD_B pins.

ADC OVERRANGE

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange indicator can be embedded within the JESD204B link as a control bit (when CSB > 0). The latency of this overrange indicator matches the sample latency.

The AD6688 also records any overrange condition in any of the eight virtual converters. For more information on the virtual converters, refer to Figure 71. The overrange status of each virtual converter is registered as a sticky bit in Register 0x0563. The contents of Register 0x0563 can be cleared using Register 0x0562, by toggling the bits corresponding to the virtual converter to the set and reset positions.

FAST THRESHOLD DETECTION (FD_A AND FD_B)

The FD_A or FD_B pin is immediately set whenever the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit is only cleared when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time. This feature provides hysteresis and prevents the FD bit from excessively toggling.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 63.

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located at Register 0x0247 and Register 0x0248. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 28 clock cycles (maximum). The approximate upper threshold magnitude is defined by

$$\textit{Upper Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x0249 and Register 0x024A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency, but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

$$\textit{Lower Threshold Magnitude}\ (\text{dBFS}) = 20\log(\textit{Threshold Magnitude}/2^{13})$$

For example, to set an upper threshold of −6 dBFS, write 0xFFF to Register 0x0247 and Register 0x0248. To set a lower threshold of −10 dBFS, write 0xA1D to Register 0x0249 and Register 0x024A.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located at Register 0x024B and Register 0x024C. See the Memory Map section (Register 0x0040, and Register 0x0245 to Register 0x024C in Table 46) for more details.

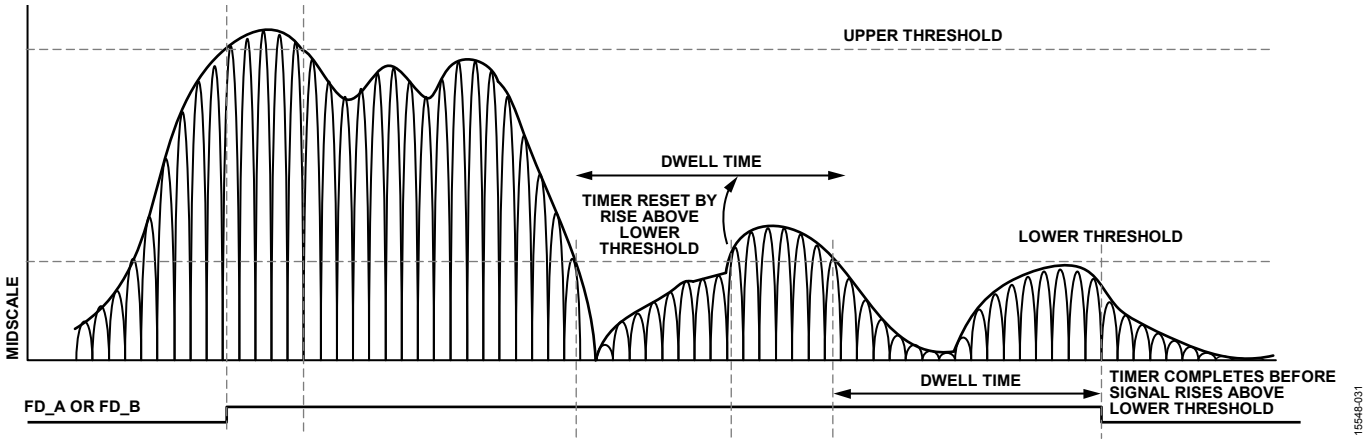


Figure 63. Threshold Settings for FD_A and FD_B Signals

ADC APPLICATION MODES AND JESD204B Tx CONVERTER MAPPING

The AD6688 contains a configurable signal path that allows different features to be enabled for different applications. These features are controlled through the chip application mode register (0x0200). The chip operating mode is controlled by Bits[3:0] and the chip Q ignore is controlled by Bit 5.

The AD6688 contains the following modes:

- Full bandwidth mode: two 7-bit ADC cores running at full sample rate.
- DDC mode: up to four DDC channels.

When the chip application mode has been selected, the output decimation ratio is set using the chip decimation ratio in Register 0x0201, Bits[3:0]. The output sample rate = ADC sample rate/the chip decimation ratio.

To support the different application layer modes, the AD6688 treats each sample stream (real or I or Q) as originating from separate virtual converters. Table 11 shows the number of virtual converters required and the transport layer mapping when channel swapping is disabled. Figure 64 shows the virtual converters and their relationship to the DDC outputs when using complex outputs.

Each DDC channel outputs either two sample streams (I/Q) for the complex data components (real and imaginary) or one sample stream for real (I) data. The AD6688 can be configured to use up to eight virtual converters depending on the DDC configuration.

The I/Q samples are always mapped in pairs with the I samples mapped to the first virtual converter and the Q samples mapped to the second virtual converter. With this transport layer mapping, the number of virtual converters are the same whether

- A single real converter is used along with a digital downconverter block producing I/Q outputs, or
- An analog downconversion is used with two real converters producing I/Q outputs.

Figure 65 shows a block diagram of the two scenarios described for I/Q transport layer mapping.

Table 11. Virtual Converter Mapping

Number of Virtual Converters Supported	Chip Application Mode (0x0200, Bits[3:0])	Chip Q Ignore (0x0200, Bit 5)	Virtual Converter Mapping							
			0	1	2	3	4	5	6	7
1 to 2	Full bandwidth mode (0x0)	Real or complex (0x0)	ADC A samples	ADC B samples	Unused	Unused	Unused	Unused	Unused	Unused
1	One DDC mode (0x1)	Real (I only) (0x1)	DDC0 I samples	Unused	Unused	Unused	Unused	Unused	Unused	Unused
2	One DDC mode (0x1)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	Unused	Unused	Unused	Unused	Unused	Unused
2	Two DDC mode (0x2)	Real (I only) (0x1)	DDC0 I samples	DDC1 I samples	Unused	Unused	Unused	Unused	Unused	Unused
4	Two DDC mode (0x2)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	DDC1 I samples	DDC1 Q samples	Unused	Unused	Unused	Unused
4	Four DDC mode (0x3)	Real (I only) (0x1)	DDC0 I samples	DDC1 I samples	DDC2 I samples	DDC3 I samples	Unused	Unused	Unused	Unused
8	Four DDC mode (0x3)	Complex (I/Q) (0x0)	DDC0 I samples	DDC0 Q samples	DDC1 I samples	DDC1 Q samples	DDC2 I samples	DDC2 Q samples	DDC3 I samples	DDC3 Q samples

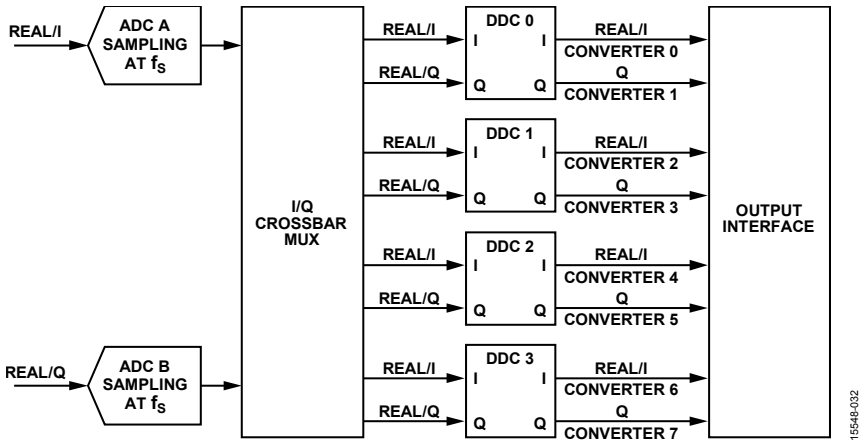


Figure 64. DDCs and Virtual Converter Mapping

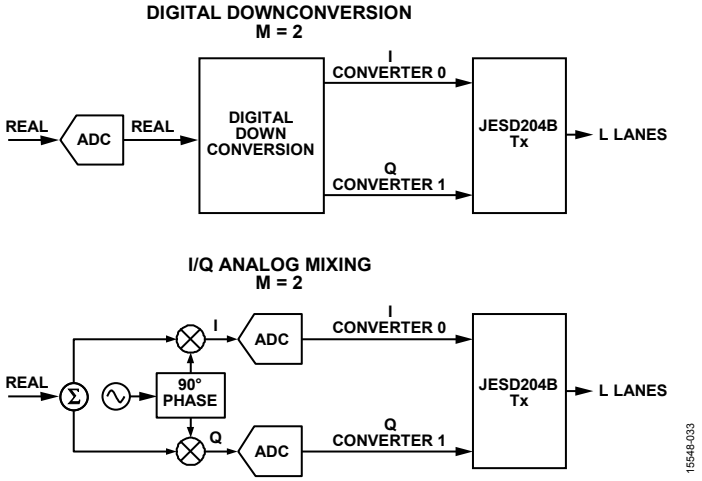


Figure 65. I/Q Transport Layer Mapping

PROGRAMMABLE FIR FILTERS

SUPPORTED MODES

The AD6688 supports the following modes of operation:

- Real 48-tap filter for each I/Q channel (see Figure 66)
  - dout_i[n] = din_i[n] * xy_i[n]
  - dout_q[n] = din_q[n] * xy_q[n]
- Real 96-tap filter for on either I or Q channel (see Figure 67)
  - dout_i[n] = din_i[n] * xy_i[n]
  - dout_q[n] = din_q[n] * xy_q[n]
- Real set of two cascaded 24-tap filters for each I/Q channel (see Figure 68)
  - dout_i[n] = din_i[n] * x_i[n] * y_i[n]
  - dout_q[n] = din_q[n] * x_q[n] * y_q[n]
- Half complex filter using two real 48-tap filters for the I/Q channels (see Figure 69)
  - dout_i[n] = din_i[n]
  - dout_q[n] = din_q[n] * xy_q[n] + din_i[n] * xy_i[n]
- Full complex filter using four real 24-tap filters for the I/Q channels (see Figure 70)
  - dout_i[n] = din_i[n] * x_i[n] + din_q[n] * y_q[n]
  - dout_q[n] = din_q[n] * x_q[n] + din_i[n] * y_i[n]

The asterisk symbol (*) denotes convolution.

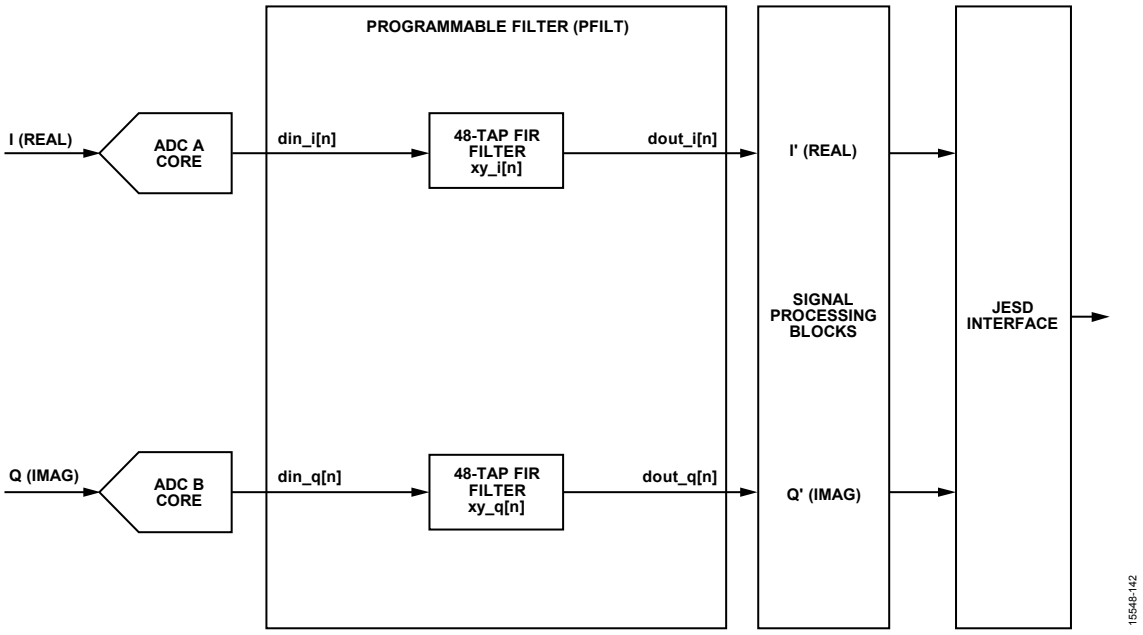


Figure 66. Real 48-Tap Filter Configuration

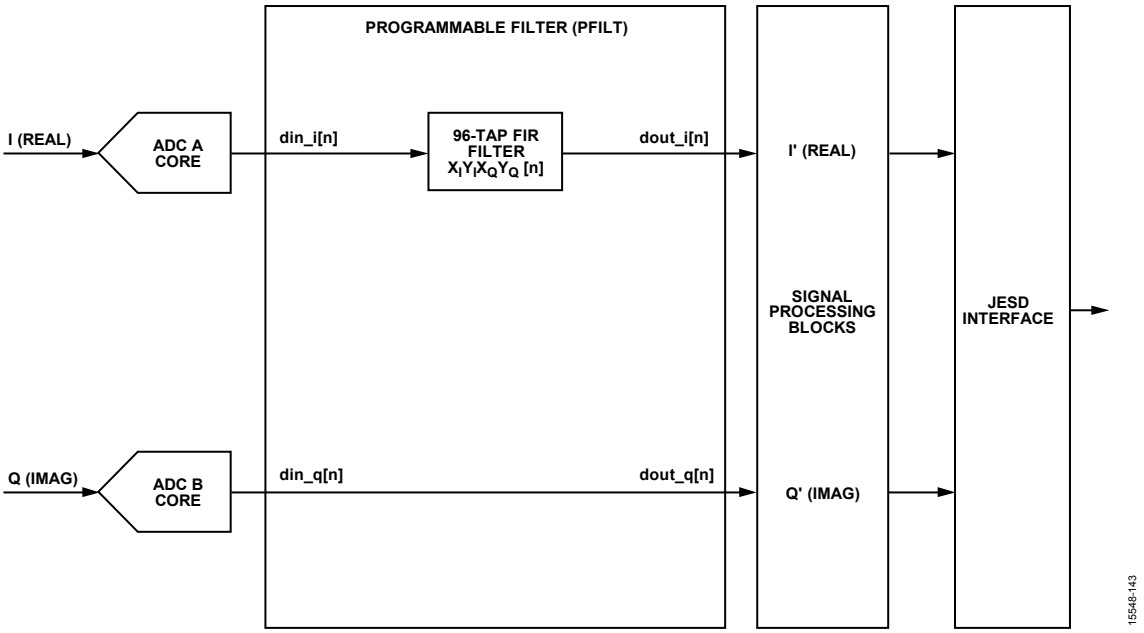


Figure 67. Real 96-Tap Filter Configuration

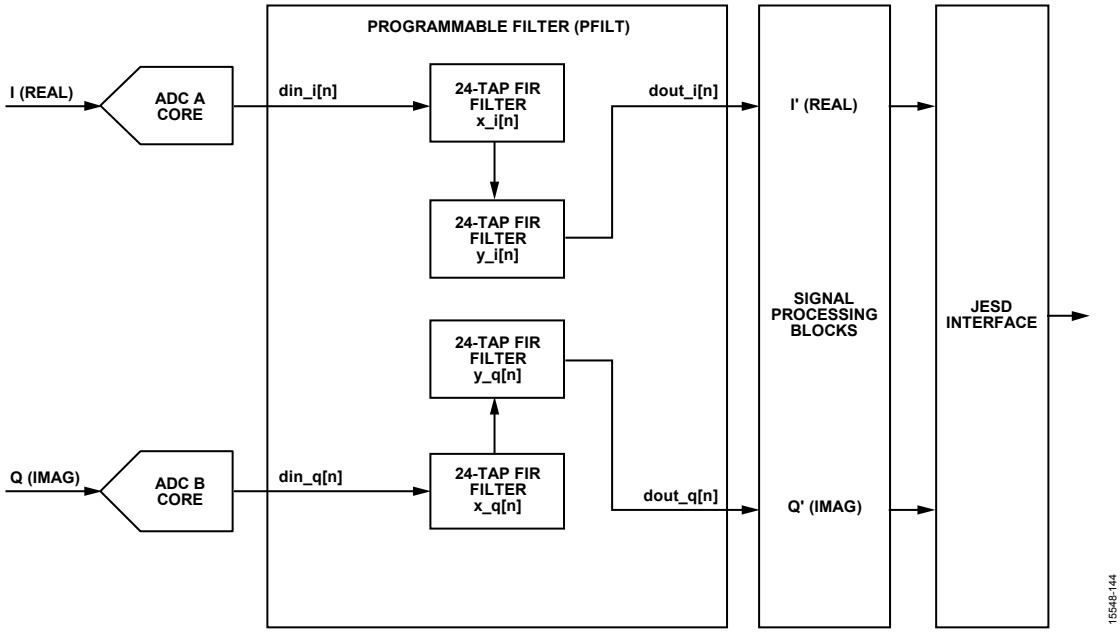


Figure 68. Real Two Cascaded 24-Tap Filter Configuration

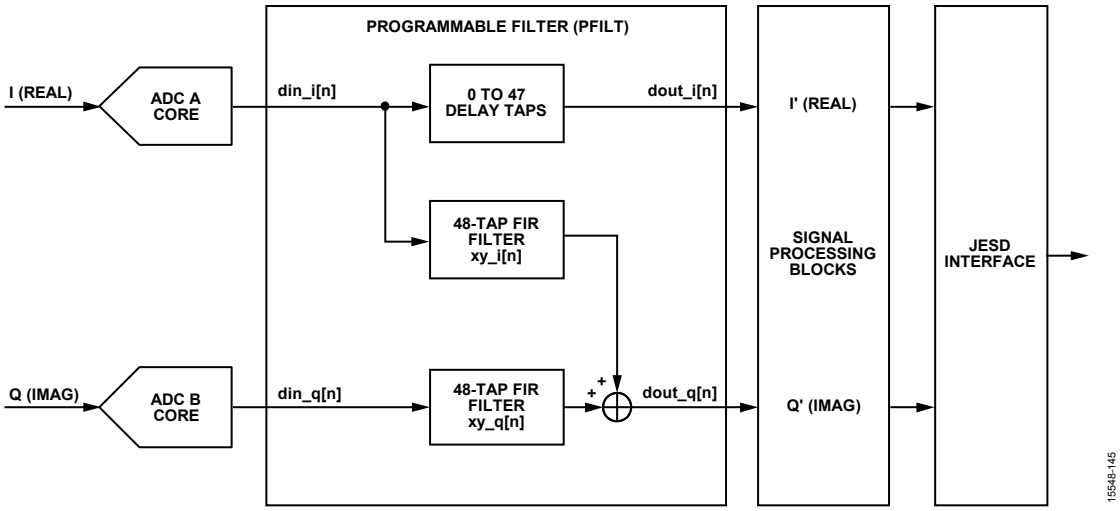


Figure 69. 48 Half Complex Filter Configuration

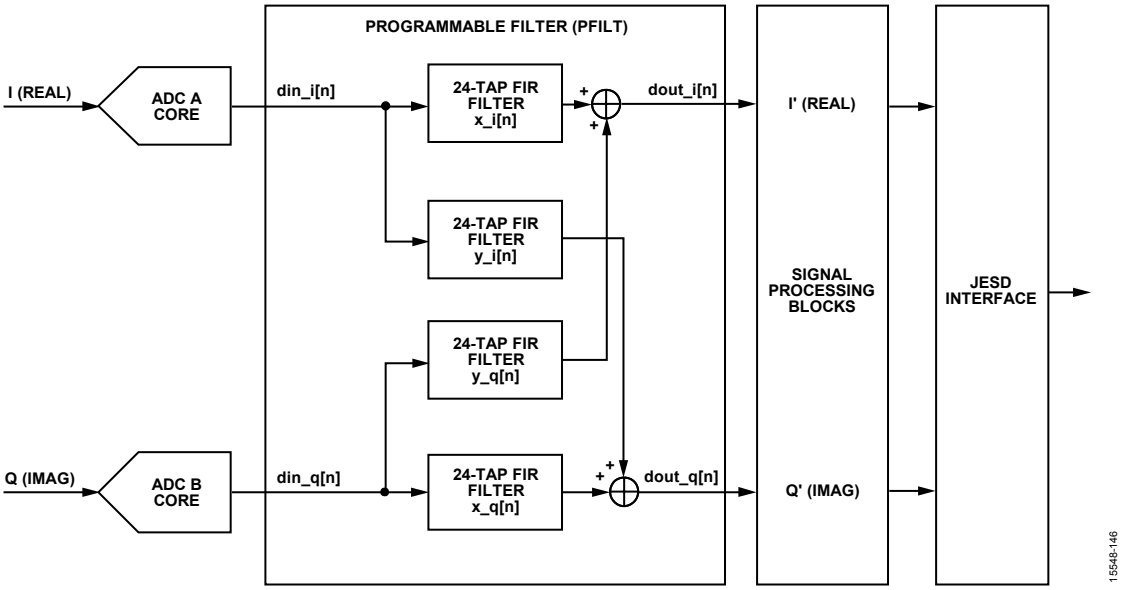


Figure 70. 24-Tap Full Complex Filter Configuration

PROGRAMMING INSTRUCTIONS

Follow this sequence to set up the programmable finite impulse response (FIR) filter:

1. Enable sample CLK to the device.
2. Configure the mode registers.
   a. Set device index to Channel A (I path) (Register 0x0008 = 0x01).
   b. Set I path mode (IMODE) and gain in Register 0x0DF8 and Register 0x0DF9 (see Table 12 and Table 13).
   c. Set device index to Channel B (Q path) (Register 0x0008 = 0x02).
   d. Set Q path mode (QMODE) and gain in Register 0x0DF8 and Register 0x0DF9.
3. Wait for at least 5 µs to allow the programmable filter to power up.
4. Program the I path coefficients to the internal shadow registers.
   a. Set device index to Channel A (I path) (Register 0x0008 = 0x01).
   b. Program the I path X coefficients (XI) in Register 0x0E00 to Register 0x0E2F (see Table 14 and Table 15).
   c. Program the I path Y coefficients (YI) in Register 0x0F00 to Register 0x0F7F (see Table 14 and Table 15).
   d. Program tapped delay in Register 0x0F30 (optional).
5. Program the Q path coefficients to the internal shadow registers:
   a. Set device index to Channel B (Q path) (Register 0x0008 = 0x02).
   b. Set Q path mode and gain in Register 0x0DF8 and Register 0x0DF9 (see Table 12 and Table 13).
   c. Program the Q path X coefficients (XQ) in Register 0x0E00 to Register 0x0E2F (see Table 14 and Table 15).
   d. Program Q path Y coefficients (YQ) in Register 0x0F00 to Register 0x0F7F (see Table 14 and Table 15).
   e. Program tapped delay in Register 0x0F30 (see Table 14 and Table 15) (optional).
6. Set the chip transfer bit using one of the following methods (note that setting the chip transfer bit applies the programmed shadow coefficients to the filter).
   - Register map.
   - Write the chip transfer bit (Register 0x000F = 0x01).
   - GPIO pin.
     i. Configure one of the GPIO pins as the chip transfer bit in Register 0x0040 to Register 0x0042.
     ii. Toggle the GPIO pin to initiate the chip transfer (rising edge triggered).
7. Whenever the I or Q path mode register changes in Register 0x0DF8, all coefficients must be reprogrammed.

Table 12. Register 0x0DF8 Definition

Bit(s)	Description
[7:3]	Reserved
[2:0]	Filter mode (IMODE or QMODE) 000: filters bypassed 001: real 24-tap filter (X only) 010: real 48-tap filter (X and Y together) 100: real set of two cascaded 24-tap filters (X then Y cascaded) 101: full complex filter using four real 24-tap filters for the A and B channels (opposite channel must also be set to 101) 110: half complex filter using two real 48-tap filters + 48-tap delay line (X and Y together) (opposite channel must also be set to 010) 111: real 96-tap filter (XI, YI, XQ, and YQ together) (opposite channel must be set to 000)

Table 13. Register 0x0DF9 Definition

Bit(s)	Description
7	Reserved
[6:4]	Y filter gain 110: −12 dB loss 111: −6 dB loss 000: 0 dB gain 001: 6 dB gain 010: 12 dB gain
3	Reserved
[2:0]	X filter gain 110: −12 dB loss 111: −6 dB loss 000: 0 dB gain 001: 6 dB gain 010: 12 dB gain

Table 14 and Table 15 show the coefficient tables in Register 0x0E00 to Register 0x0F30. All coefficients are Q1.15 format (sign bit + 15 fractional bits).

Table 14. I Coefficient Table (Device Selection = 0x1)[1]

Addr.	Single 24-Tap Filter (IMODE[2:0] = 0x1)	Single 48-Tap Filter (IMODE[2:0] = 0x2)	Two Cascaded 24-Tap Filters (IMODE[2:0] = 0x4)	Full Complex 24-Tap Filters (IMODE[2:0] = 0x5 and QMODE[2:0] = 0x5)	Half Complex 48-Tap Filters (IMODE[2:0] = 0x6 and QMODE[2:0] = 0x2)[2]	I Path 96-Tap Filter (IMODE[2:0] = 0x7 and QMODE[2:0] = 0x0)[3]	Q Path 96-Tap Filter (IMODE[2:0] = 0x0 and QMODE[2:0] = 0x7)[3]
0x0E00	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XI C0 [7:0]	XQ C48 [7:0]
0x0E01	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XI C0 [15:8]	XQ C48 [15:8]
0x0E02	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XI C1 [7:0]	XQ C49 [7:0]
0x0E03	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XI C1 [15:8]	XQ C49 [15:8]
...	...	...	...	...	...	...	...
0x0E2E	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XI C23 [7:0]	XQ C71 [7:0]
0x0E2F	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XI C23 [15:0]	XQ C71 [15:0]
0x0F00	Unused	YI C24 [7:0]	YI C0 [7:0]	YI C0 [7:0]	YI C24 [7:0]	YI C24 [7:0]	YQ C72 [7:0]
0x0F01	Unused	YI C24 [15:8]	YI C0 [15:8]	YI C0 [15:8]	YI C24 [15:8]	YI C24 [15:8]	YQ C72 [15:8]
0x0F02	Unused	YI C25 [7:0]	YI C1 [7:0]	YI C1 [7:0]	YI C25 [7:0]	YI C25 [7:0]	YQ C73 [7:0]
0x0F03	Unused	YI C25 [15:8]	YI C1 [15:8]	YI C1 [15:8]	YI C25 [15:8]	YI C25 [15:8]	YQ C73 [15:8]
...	Unused	...	...	...	...	...	...
0x0F2E	Unused	YI C47 [7:0]	YI C23 [7:0]	YI C23 [7:0]	YI C47 [7:0]	YI C47 [7:0]	YQ C95 [7:0]
0x0F2F	Unused	YI C47 [15:0]	YI C23 [15:0]	YI C23 [15:0]	YI C47 [15:0]	YI C47 [15:0]	YQ C95 [15:0]
0x0F30	Unused	Unused	Unused	Unused	I path tapped delay 0: 0 tapped delay (matches C0 in the filter) 1: 1 tapped delays … 47: 47 tapped delays	Unused	Unused

[1] XI Cn means I Path X Coefficient n. YI Cn means I Path Y Coefficient n.
[2] When using the I path in half-complex 48-tap filter mode, the Q path must be in single 48-tap filter mode.
[3] When using the I path in 96-tap filter mode, the Q path must be in bypass mode.

Table 15. Q Coefficient Table (Device Selection = 0x2)[1]

Addr.	Single 24-Tap Filter (QMODE[2:0] = 0x1)	Single 48-Tap Filter (QMODE[2:0] = 0x2)	Two Cascaded 24-Tap Filters (QMODE[2:0] = 0x4)	Full Complex 24-Tap Filters (QMODE[2:0] = 0x5 and IMODE[2:0] = 0x5)	Half Complex 48-Tap Filters (QMODE[2:0] = 0x6 and IMODE[2:0] = 0x2)[2]	I Path 96-Tap Filter (QMODE[2:0] = 0x0 and IMODE[2:0] = 0x7)[3]	Q Path 96-Tap Filter (QMODE[2:0] = 0x7 and IMODE[2:0] = 0x0)[3]
0x0E00	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XQ C0 [7:0]	XI C48 [7:0]	XQ C0 [7:0]
0x0E01	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XQ C0 [15:8]	XI C48 [15:8]	XQ C0 [15:8]
0x0E02	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XQ C1 [7:0]	XI C49 [7:0]	XQ C1 [7:0]
0x0E03	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XQ C1 [15:8]	XI C49 [15:8]	XQ C1 [15:8]
...	...	...	...	...	...	...	...
0x0E2E	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XQ C23 [7:0]	XI C71 [7:0]	XQ C23 [7:0]
0x0E2F	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XQ C23 [15:0]	XI C71 [15:0]	XQ C23 [15:0]
0x0F00	Unused	YQ C24 [7:0]	YQ C0 [7:0]	YQ C0 [7:0]	YQ C24 [7:0]	YI C72 [7:0]	YQ C24 [7:0]
0x0F01	Unused	YQ C24 [15:8]	YQ C0 [15:8]	YQ C0 [15:8]	YQ C24 [15:8]	YI C72 [15:8]	YQ C24 [15:8]
0x0F02	Unused	YQ C25 [7:0]	YQ C1 [7:0]	YQ C1 [7:0]	YQ C25 [7:0]	YI C73 [7:0]	YQ C25 [7:0]
0x0F03	Unused	YQ C25 [15:8]	YQ C1 [15:8]	YQ C1 [15:8]	YQ C25 [15:8]	YI C73 [15:8]	YQ C25 [15:8]
...	Unused	...	...	...	...	...	...
0x0F2E	Unused	YQ C47 [7:0]	YQ C23 [7:0]	YQ C23 [7:0]	YQ C47 [7:0]	YI C95 [7:0]	YQ C47 [7:0]
0x0F2F	Unused	YQ C47 [15:0]	YQ C23 [15:0]	YQ C23 [15:0]	YQ C47 [15:0]	YI C95 [15:0]	YQ C47 [15:0]
0x0F30	Unused	Unused	Unused	Unused	Q Path Tapped Delay 0: 0 tapped delay (matches C0 in the filter) 1: 1 tapped delays … 47: 47 tapped delays	Unused	Unused

[1] XQ Cn means Q Path X Coefficient n. YQ Cn means Q Path Y Coefficient n.
[2] When using the I path in half-complex 48-tap filter mode, the Q path must be in single 48-tap filter mode.
[3] When using the I path in 96-tap filter mode, the Q path must be in bypass mode.

DIGITAL DOWNCONVERTER (DDC)

The AD6688 includes four digital downconverters (DDC0 to DDC3) that provide filtering and reduce the output data rate. This digital processing section includes an NCO, multiple decimating FIR filters, a gain stage, and a complex to real conversion stage. Each of these processing blocks has control lines that allow it to be independently enabled and disabled to provide the desired processing function. The digital downconverter can be configured to output either real data or complex output data.

The DDCs output a 16-bit stream. To enable this operation, the converter number of bits, N, is set to a default value of 16, even though the analog core only outputs 14 bits. In full bandwidth operation, the ADC outputs are the 14-bit word followed by two zeros, unless the tail bits are enabled.

DDC I/Q INPUT SELECTION

The AD6688 has two ADC channels and four DDC channels. Each DDC channel has two input ports that can be paired to support both real and complex inputs through the I/Q crossbar mux. For real signals, both DDC input ports must select the same ADC channel (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel A). For complex signals, each DDC input port must select different ADC channels (that is, DDC Input Port I = ADC Channel A and DDC Input Port Q = ADC Channel B).

The inputs to each DDC are controlled by the DDC input selection registers (Register 0x0311, Register 0x0331, Register 0x0351, and Register 0x0371). See Table 46 for information on how to configure the DDCs.

DDC I/Q OUTPUT SELECTION

Each DDC channel has two output ports that can be paired to support both real and complex outputs. For real output signals, only the DDC Output Port I is used (the DDC Output Port Q is invalid). For complex I/Q output signals, both DDC Output Port I and DDC Output Port Q are used.

The I/Q outputs to each DDC channel are controlled by the DDC complex to real enable bit, Bit 3, in the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350, and Register 0x0370).

The chip Q ignore bit in the chip mode register (Register 0x0200, Bit 5) controls the chip output muxing of all the DDC channels. When all DDC channels use real outputs, set this bit high to ignore all DDC Q output ports. When any of the DDC channels are set to use complex I/Q outputs, the user must clear this bit to use both DDC Output Port I and DDC Output Port Q. For more information, see Figure 88.

DDC GENERAL DESCRIPTION

The four DDC blocks are used to extract a portion of the full digital spectrum captured by the ADC(s). They are intended for IF sampling or oversampled baseband radios requiring wide bandwidth input signals.

Each DDC block contains the following signal processing stages:

- Frequency translation stage (optional)
- Filtering stage
- Gain stage (optional)
- Complex to real conversion stage (optional)

Frequency Translation Stage (Optional)

This stage consists of a phase coherent, numerically controlled oscillator (NCO) and quadrature mixers that can be used for frequency translation of both real or complex input signals. The phase-coherent NCO allows an infinite number of frequency hops that are all referenced back to a single synchronization event. It also includes 16 shadow registers for fast-switching applications. This stage shifts a portion of the available digital spectrum down to baseband.

Filtering Stage

After shifting down to baseband, this stage decimates the frequency spectrum using multiple low pass FIR filters for rate conversion. The decimation process lowers the output data rate, which in turn reduces the output interface rate.

Gain Stage (Optional)

Because of losses associated with mixing a real input signal down to baseband, this stage compensates by adding an additional 0 dB or 6 dB of gain.

Complex to Real Conversion Stage (Optional)

When real outputs are necessary, this stage converts the complex outputs back to real by performing an $f_S/4$ mixing operation plus a filter to remove the complex component of the signal.

Figure 71 shows the detailed block diagram of the DDCs implemented in the AD6688.

Figure 72 shows an example usage of one of the four DDC channels with a real input signal and four half-band filters (HB4 + HB3 + HB2 + HB1) used. It shows both complex (decimate by 16) and real (decimate by 8) output options.

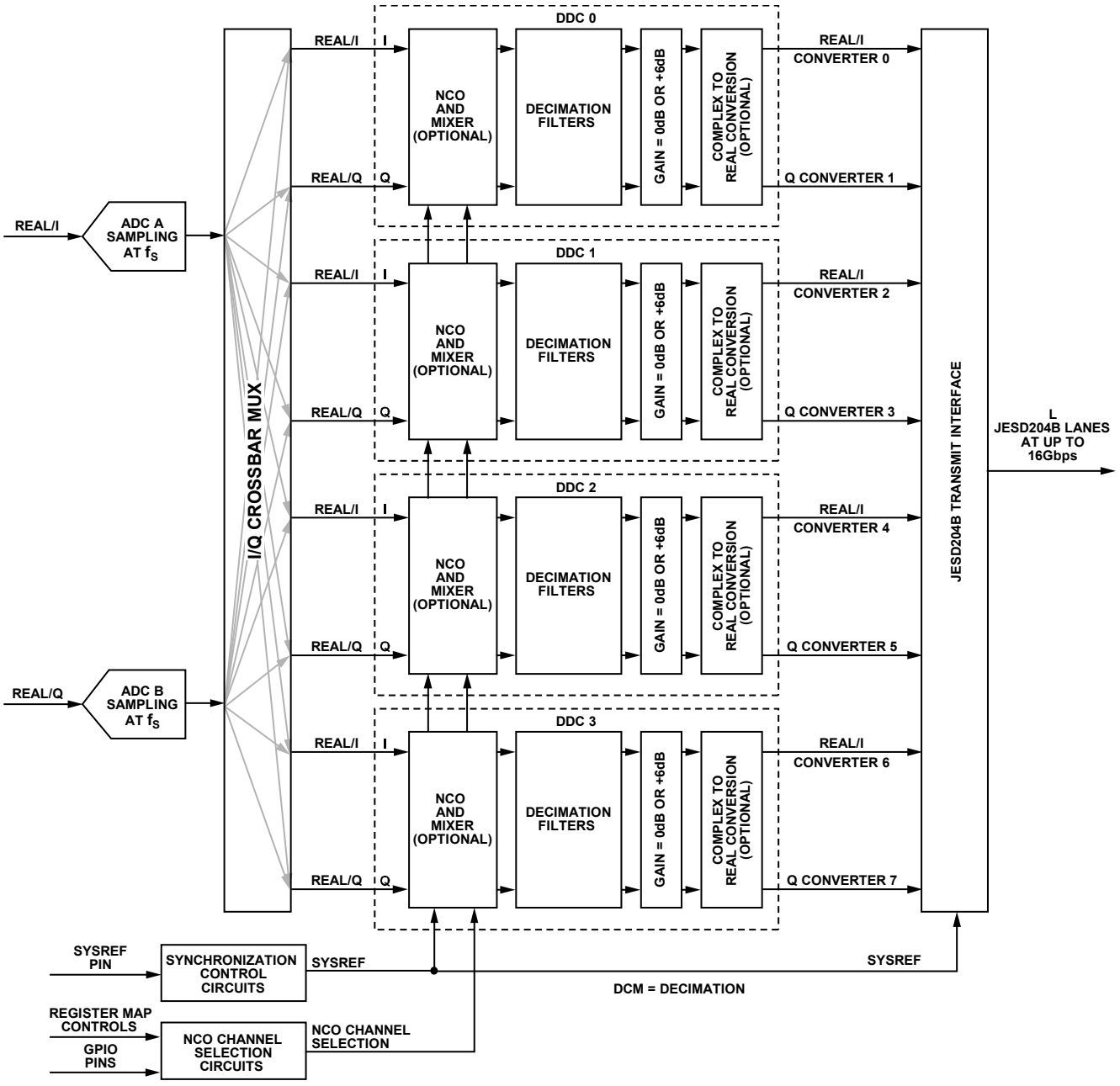


Figure 71. DDC Detailed Block Diagram

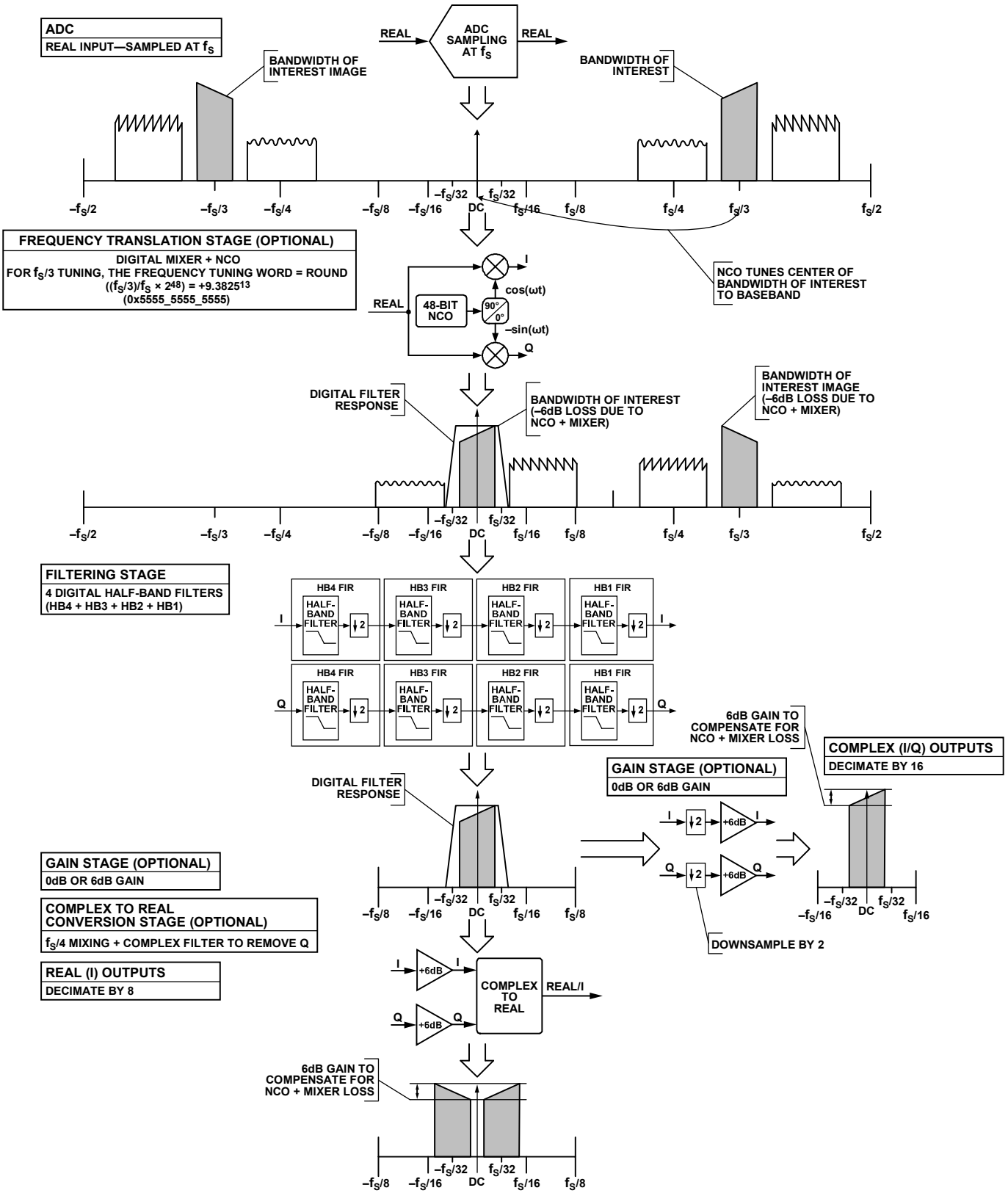


Figure 72. DDC Theory of Operation Example (Real Input)

DDC FREQUENCY TRANSLATION

DDC Frequency Translation General Description

Frequency translation is accomplished by using a 48-bit complex NCO with a digital quadrature mixer. This stage translates either a real or complex input signal from an IF to a baseband complex digital output (carrier frequency = 0 Hz).

The frequency translation stage of each DDC can be controlled individually and supports four different IF modes using Bits[5:4] of the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350, and Register 0x0370). These IF modes are

- Variable IF mode
- 0 Hz IF or zero IF (ZIF) mode
- $f_S/4$ Hz IF mode
- Test mode

Variable IF Mode

In this mode, the NCO and mixers are enabled. NCO output frequency can be used to digitally tune the IF frequency.

0 Hz IF (ZIF) Mode

In this mode, the mixers are bypassed, and the NCO is disabled.

$f_S/4$ Hz IF Mode

In this mode, the mixers and the NCO are enabled in special downmixing by $f_S/4$ mode to save power.

Test Mode

In this mode, input samples are forced to 0.999 to positive full scale. The NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters.

Figure 73 and Figure 74 show examples of the frequency translation stage for both real and complex inputs.

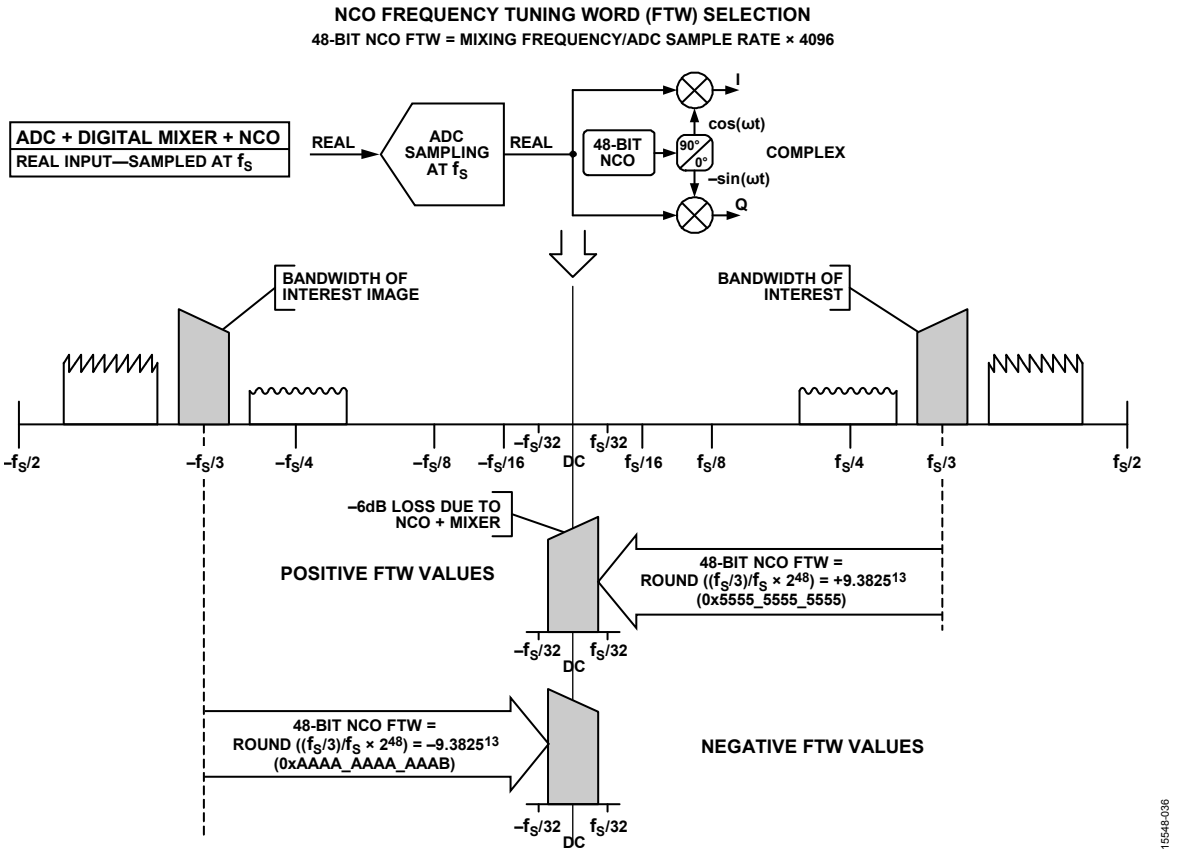


Figure 73. DDC NCO Frequency Tuning Word Selection—Real Inputs

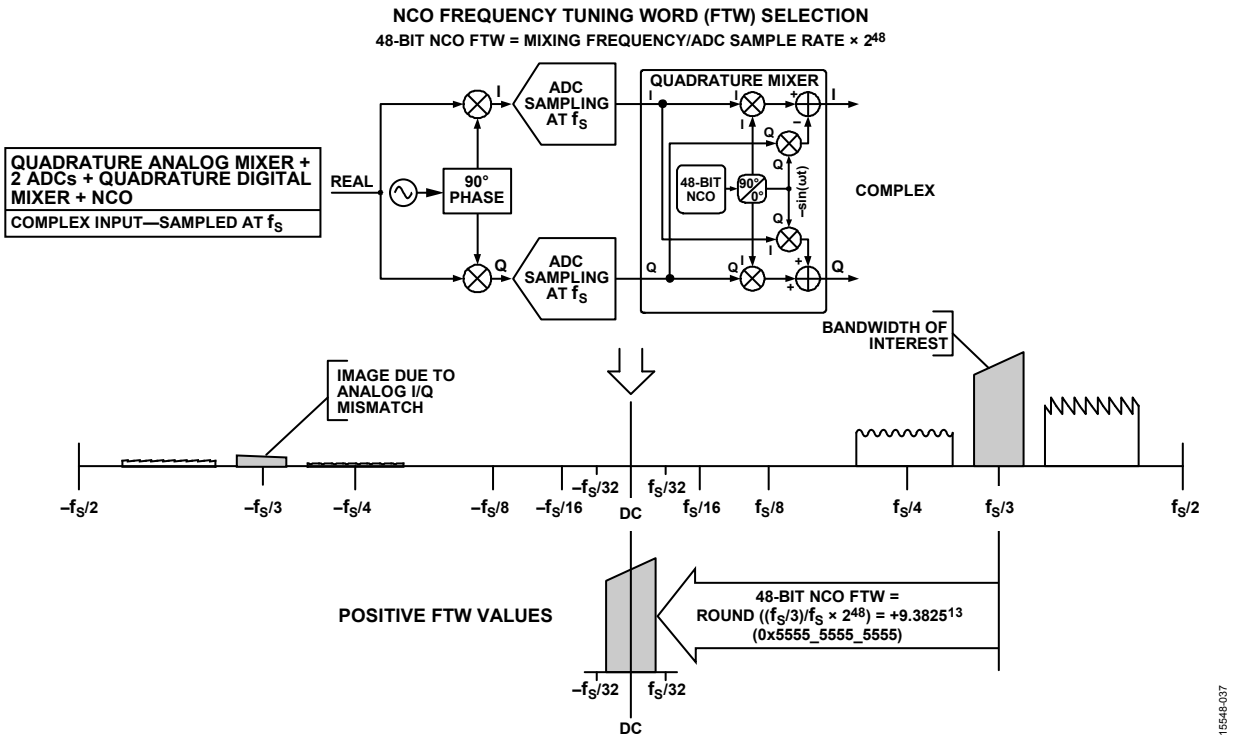


Figure 74. DDC NCO Frequency Tuning Word Selection—Complex Inputs

DDC NCO Description

Each DDC contains one NCO. Each NCO enables the frequency translation process by creating a complex exponential frequency ($e^{-j\omega ct}$), which can be mixed with the input spectrum to translate the desired frequency band of interest to dc, where it can be filtered by the subsequent low-pass filter blocks to prevent aliasing.

When placed in variable IF mode, the NCO supports two different additional modes.

DDC NCO Programmable Modulus Mode

This mode supports >48-bit frequency tuning accuracy for applications that require exact rational (M/N) frequency synthesis at a single carrier frequency. In this mode, the NCO is set up by providing the following:

- 48-bit frequency tuning word (FTW)
- 48-bit Modulus A word (MAW)
- 48-bit Modulus B word (MBW)
- 48-bit phase offset word (POW)

DDC NCO Coherent Mode

This mode allows an infinite number of frequency hops where the phase is referenced to a single synchronization event at Time 0. This mode is useful when phase coherency must be maintained when switching between different frequency bands. In this mode, the user can switch to any tuning frequency without the need to reset the NCO. Although only one FTW is required, the NCO contains 16 shadow registers for fast switching applications. Selection of the shadow registers is controlled by the CMOS GPIO pins or through the register map of the SPI. In this mode, the NCO can be set up by providing the following:

- Up to 16, 48-bit FTWs.
- Up to 16, 48-bit POWs.
- The 48-bit MAW must be set to 0 in coherent mode.

Figure 75 shows a block diagram of one NCO and its connection to the rest of the design. The coherent phase accumulator block contains the logic that allows an infinite number of frequency hops. The gray lines in Figure 75 represent SPI control lines.

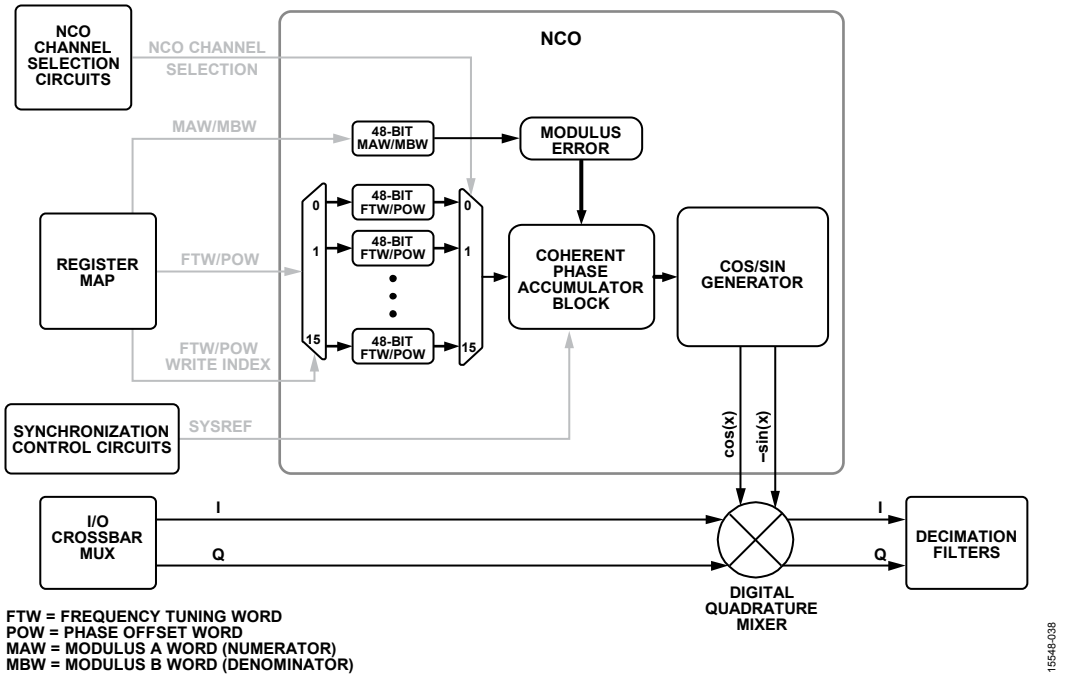


Figure 75. NCO + Mixer Block Diagram

NCO FTW/POW/MAW/MAB Description

The NCO frequency value is determined by the following settings:

- A 48-bit twos complement number entered in the FTW.
- A 48-bit unsigned number entered in the MAW.
- A 48-bit unsigned number entered in the MBW.

Frequencies between $-f_S/2$ and $+f_S/2$ ($f_S/2$ excluded) are represented using the following values:

- FTW = 0x8000_0000_0000 and MAW = 0x0000_0000_0000 represents a frequency of $-f_S/2$.
- FTW = 0x0000_0000_0000 and MAW = 0x0000_0000_0000 represents dc (frequency is 0 Hz).
- FTW = 0x7FFF_FFFF_FFFF and MAW = 0x0000_0000_0000 represents a frequency of $+f_S/2$.

NCO FTW/POW/MAW/MAB Programmable Modulus Mode

For programmable modulus mode, the MAW must be set to a nonzero value (not equal to 0x0000_0000_0000). This mode is only needed when frequency accuracy of >48 bits is required. One example of a rational frequency synthesis requirement that requires >48 bits of accuracy is a carrier frequency of 1/3 the sample rate. When frequency accuracy of ≤48 bits is required, coherent mode must be used (see the NCO FTW/POW/MAW/MAB Coherent Mode section).

In programmable modulus mode, the FTW, MAW, and MBW must satisfy the following four equations (for a detailed description of the programmable modulus feature, see the DDS architecture described in the AN-953 Application Note):

$$\frac{\mathrm{mod}(f_c, f_s)}{f_s} = \frac{M}{N} = \frac{FTW + \frac{MAW}{MBW}}{2^{48}} \quad (1)$$

$$FTW = \mathrm{floor}\left(2^{48}\frac{\mathrm{mod}(f_c, f_s)}{f_s}\right) \quad (2)$$

$$MAW = \mathrm{mod}(2^{48} \times M, N) \quad (3)$$

$$MBW = N \quad (4)$$

where:
f_C is the desired carrier frequency.
f_S is the ADC sampling frequency.
M is the integer representing the rational numerator of the frequency ratio.
N is the integer representing the rational denominator of the frequency ratio.
FTW is the 48-bit twos complement number representing the NCO FTW.
MAW is the 48-bit unsigned number representing the NCO MAW (must be $<2^{47}$).
MBW is the 48-bit unsigned number representing the NCO MBW.
mod(x) is a remainder function. For example mod(110,100) = 10 and for negative numbers, mod(−32,10)= −2.
floor(x) is defined as the largest integer less than or equal to x. For example, floor(3.6) = 3.

Note that Equation 1 to Equation 4 apply to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals).

M and N are integers reduced to their lowest terms. MAW and MBW are integers reduced to their lowest terms. When MAW is set to zero, the programmable modulus logic is automatically disabled.

For example, if the ADC sampling frequency (f_S) is 3000 MSPS and the carrier frequency (f_C) is 1001.5 MHz, then,

$$\frac{\mathrm{mod}(1001.5, 3000)}{3000} = \frac{M}{N} = \frac{2003}{6000}$$

$$FTW = \mathrm{floor}\left(2^{48}\frac{\mathrm{mod}(1001.5, 3000)}{3000}\right) = 0\text{x}5576_19F0_FB38$$

$$MAW = \mathrm{mod}(2^{48} \times 2003, 6000) = 0\text{x}0000_0000_0F80$$

$$MBW = 0\text{x}0000_0000_1770$$

The actual carrier frequency can be calculated based on the following equation:

$$f_{C_ACTUAL} = \frac{FTW + \frac{MAW}{MBW} \times f_S}{2^{48}}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is

$$f_{C_ACTUAL} = \frac{0\text{x}5576_19F0_FB38 \times \frac{0\text{x}0000_0000_0F80}{0\text{x}0000_0000_1770}}{2^{48}} = 1001.5\ \mathrm{MHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

While in programmable modulus mode, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the NCO. However, the following procedure must be followed to update the MAW and/or MBW registers to ensure proper operation of the NCO:

1. Write to the MAW and MBW registers for all the DDCs.
2. Synchronize the NCOs either through the DDC soft reset bit accessible through the SPI or through the assertion of the SYSREF± pin (see the Memory Map section).

NCO FTW/POW/MAW/MAB Coherent Mode

For coherent mode, the NCO MAW must be set to zero (0x0000_0000_0000). In this mode, the NCO FTW can be calculated by the following equation:

$$FTW = \text{round}(2^{48} \frac{\text{mod}(f_c, f_s)}{f_s}) \quad (5)$$

where:
FTW is the 48-bit twos complement number representing the NCO FTW.
f_S is the ADC sampling frequency.
f_C is the desired carrier frequency.
mod(*x*) is a remainder function. For example mod(110,100) = 10 and for negative numbers, mod(−32,10) = −2.
round(*x*) is a rounding function. For example round(3.6) = 4 and for negative numbers, round(−3.4)= −3.

Note that Equation 5 applies to the aliasing of signals in the digital domain (that is, aliasing introduced when digitizing analog signals). The MAW must be set to zero to use coherent mode. When MAW is zero, the programmable modulus logic is automatically disabled.

For example, if the ADC sampling frequency (f_S) is 3000 MSPS and the carrier frequency (f_C) is 416.667 MHz, then,

$$NCO_FTW = \text{round}(2^{48} \frac{\text{mod}(416.667,3000)}{3000}) = 0x2EC6_C03A_8E23$$

The actual carrier frequency can be calculated based on the following equation:

$$f_{C_ACTUAL} = \frac{FTW \times f_S}{2^{48}}$$

For the previous example, the actual carrier frequency (f_{C_ACTUAL}) is

$$f_{C_ACTUAL} = \frac{416.667 \times 3000}{2^{48}} = 416.66699\,\text{MHz}$$

A 48-bit POW is available for each NCO to create a known phase relationship between multiple chips or individual DDC channels inside the chip.

While in coherent mode, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the NCO.

NCO Channel Selection

When configured in coherent mode, only one FTW is required in the NCO. In this mode, the user can switch to any tuning frequency without the need to reset the NCO by writing to the FTW directly. However, for fast switching applications, where either all FTWs are known beforehand or it is possible to queue up the next set of FTWs, the NCO contains 16 additional shadow registers (see Figure 75). These shadow registers are hereafter referred to as the NCO channels.

Figure 76 shows a simplified block diagram of the NCO channel selection block. The gray lines in Figure 76 represent SPI control lines.

Only one NCO channel is active at a time, and NCO channel selection is controlled either by the CMOS GPIO pins or through the register map.

Each NCO channel selector supports three different modes, as described in the following sections.

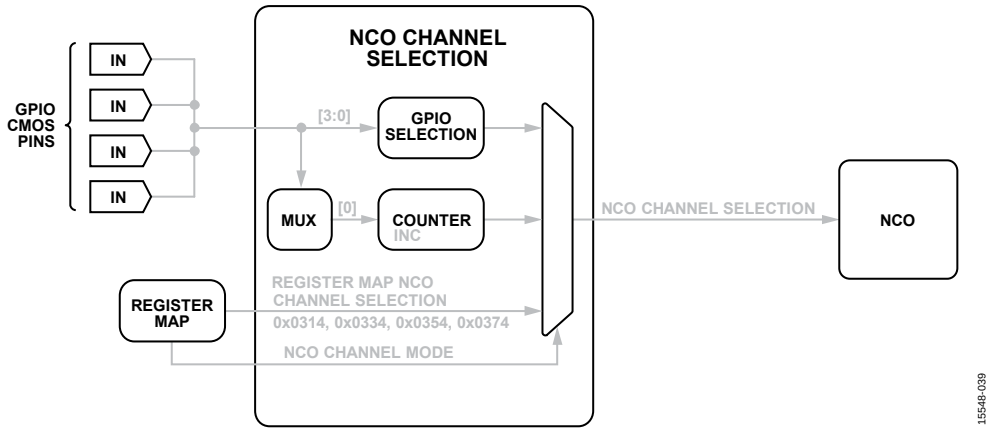


Figure 76. NCO Channel Selection Block

GPIO Level Control Mode

The GPIO pins determine the exact NCO channel selected.

The following procedure must be followed to use GPIO level control for NCO channel selection:

1. Configure one or more GPIO pins as NCO channel selection inputs. GPIO pins not configured as NCO channel selection are internally tied low.
   a. To use GPIO_A0, write Bits[2:0] in Register 0x0040 to 0x6 and Bits[3:0] in Register 0x0041 to 0x0.
   b. To use GPIO_B0, write Bits[5:3] in Register 0x0040 to 0x6 and Bits[7:4] in Register 0x0041 to 0x0.
   c. To use GPIO_A1, write Bits[3:0] in Register 0x0042 to 0x0.
   d. To use GPIO_B1, write Bits[7:4] in Register 0x0042 to 0x0.
2. Configure the NCO channel selector in GPIO level control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374) to 0x1 through 0x6, depending on the desired GPIO pin ordering.
3. Select the desired NCO channel through the GPIO pins.

GPIO Edge Control Mode

Low to high transition on a single GPIO pin determines the exact NCO channel selected. The internal channel selection counter is reset by either SYSREF± or the DDC soft reset.

The following procedure must be followed to use GPIO edge control for NCO channel selection:

1. Configure one or more GPIO pins as NCO channel selection inputs.
   a. To use GPIO_A0, write Bits[2:0] in Register 0x0040 to 0x6 and Bits[3:0] in Register 0x0041 to 0x0.
   b. To use GPIO_B0, write Bits[5:3] in Register 0x0040 to 0x6 and Bits[7:4] in Register 0x0041 to 0x0.
   c. To use GPIO_A1, write Bits[3:0] in Register 0x0042 to 0x0.
   d. To use GPIO_B1, write Bits[7:4] in Register 0x0042 to 0x0.
2. Configure the NCO channel selector in GPIO edge control mode by setting Bits[7:4] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374) to 0x8 through 0xB, depending on the desired GPIO Pin.
3. Configure the wrap point for the NCO channel selection by setting Bits[3:0] in the NCO control registers (Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374). A value of 4 causes the channel selection to wrap at Channel 4 (0, 1, 2, 3, 4, 0, 1, 2, 3, 4, and so on).
4. Transition the selected GPIO pin from low to high to increment the NCO channel selection.

Register Map Mode

NCO channel selection is controlled directly through the register map.

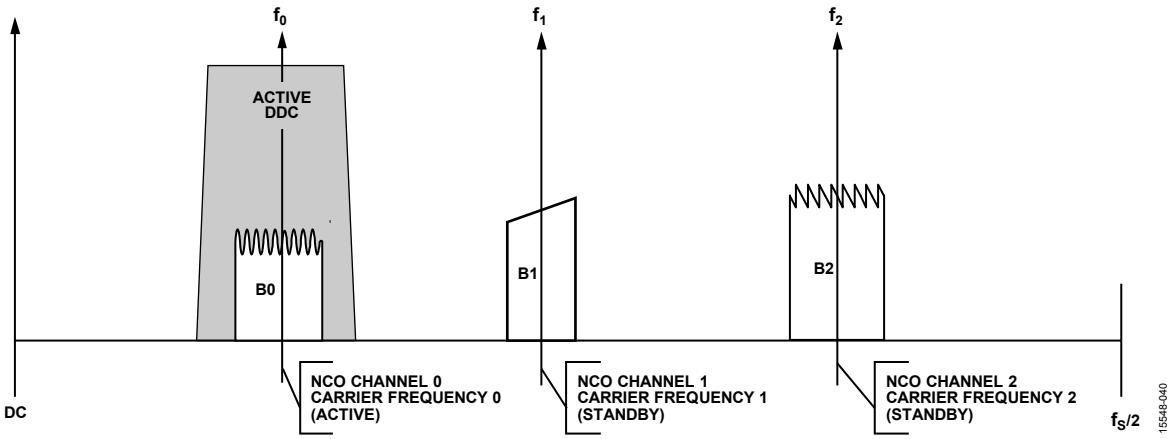


Figure 77. NCO Coherent Mode with Three NCO Channels (B0 Selected)

Figure 77 shows an example use case for coherent mode utilizing three NCO channels. In this example, NCO Channel 0 is actively downconverting bandwidth 0 (B0) while NCO Channel 1 and Channel 2 are in standby and tuned to Bandwidth 1 and Bandwidth 2 (B1 and B2), respectively.

The phase coherent NCO switching feature allows infinite number of frequency hops that are all phase coherent. The initial phase of the NCO is established at Time t_0 from SYSREF synchronization. Switching the NCO FTW does not affect the phase. With this feature, only one FTW is required; however, the user may want to use all 16 channels to queue up the next hop.

After SYSREF synchronization at start-up, all NCOs across multiple chips are inherently synchronized.

Setting Up the Multichannel NCO Feature

The first step to configure the multichannel NCO is to program the FTWs. The AD6688 memory map has a FTW index register for each DDC. This index determines which NCO channel receives the FTW from the register map. The following sequence describes the method for programming the FTWs.

1. Write the FTW index register with the desired DDC channel.
2. Write the FTW with the desired value. This value is applied to the NCO channel index mentioned in Step 1.
3. Repeat Step 1 and Step 2 for other NCO channels.

After setting the FTWs, the user must then select an active NCO channel. This selection can be done either through the SPI registers or through the external GPIO pins. The following sequence describes the method for selecting the active NCO channel using SPI.

1. Set the NCO channel selection mode (Bits[7:4]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374 to 0x0 to enable SPI selection.
2. Choose the active NCO channel (Bits[3:0]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374.

The following sequence describes the method for selecting the active NCO channel using GPIO CMOS pins.

1. Set NCO channel selection mode (Bits[7:4]) in Register 0x0314, Register 0x0334, Register 0x0354, and Register 0x0374 to a nonzero value to enable GPIO pin selection.
2. Configure the GPIO pins as NCO channel selection inputs by writing to Register 0x0040, Register 0x0041, and Register 0x0042.
3. NCO switching is done by externally controlling the GPIO CMOS pins.

NCO Synchronization

Each NCO contains a separate phase accumulator word (PAW). The initial reset value of each PAW is set to zero and incremented every clock cycle. The instantaneous phase of the NCO is calculated using the PAW, FTW, MAW, MBW, and POW. Because of this architecture, the FTW and POW registers can be updated at any time while still maintaining deterministic phase results in the PAW of the NCO.

Two methods can be used to synchronize multiple PAWs within the chip:

- Using the SPI. Use The DDC soft reset bit in the DDC synchronization control register (Register 0x0300, Bit 4) to reset all the PAWs in the chip. This is accomplished by setting the DDC soft reset high and then setting this bit low. Note that this method can only be used to synchronize DDC channels within the same chip.
- Using the SYSREF± pin. When the SYSREF± pin is enabled in the SYSREF± control registers (Register 0x0120 and Register 0x0121) and the DDC synchronization is enabled in the DDC synchronization control register (Register 0x0300, Bits[1:0]); any subsequent SYSREF event resets all the PAWs in the chip. Note that this method can be used to synchronize DDC channels within the same chip or DDC channels within separate chips.

NCO Multichip Synchronization

In some applications, it is necessary to synchronize all the NCOs and LMFCs within multiple devices in a system. For applications needing multiple NCO tuning frequencies in the system, a designer likely needs to generate a single SYSREF pulse at all devices simultaneously. For many systems, generating/receiving a single-shot SYSREF at all devices is challenging because enabling/disabling the SYSREF is often an asynchronous event, and not all clock generation chips support this feature.

For this reason, the AD6688 contains a synchronization triggering mechanism that allows the following:

- At system startup, multichip synchronization of all NCOs and LMFCs.
- During normal operation, multichip synchronization of all NCOs after applying new tuning frequencies.

The synchronization triggering mechanism uses a master/slave arrangement, as shown in Figure 78.

Each device has an internal next synchronization trigger enable (NSTE) signal that controls whether the next SYSREF causes a synchronization event. Slave ADC devices must source their NSTE from an external slave next trigger input (SNTI) pin. Master devices can either use their external master next trigger output (MNTO) pin (default setting) or use an external SNTI pin.

See Register 0x0041 and Register 0x0042 in Table 46 to configure the FD/GPIO pins for this operation.

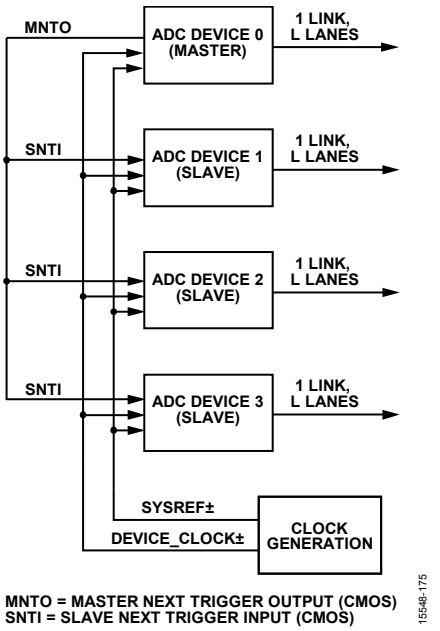


Figure 78. System using Master/Slave Synchronization Triggering

NCO Multichip Synchronization at Startup

Figure 79 shows a timing diagram along with the required sequence of events for NCO multichip synchronization using triggering and SYSREF at startup. Using this startup sequence synchronizes all the NCOs and LMFCs in the system at once.

NCO Multichip Synchronization During Normal Operation

See the Setting Up the Multichannel NCO Feature section.

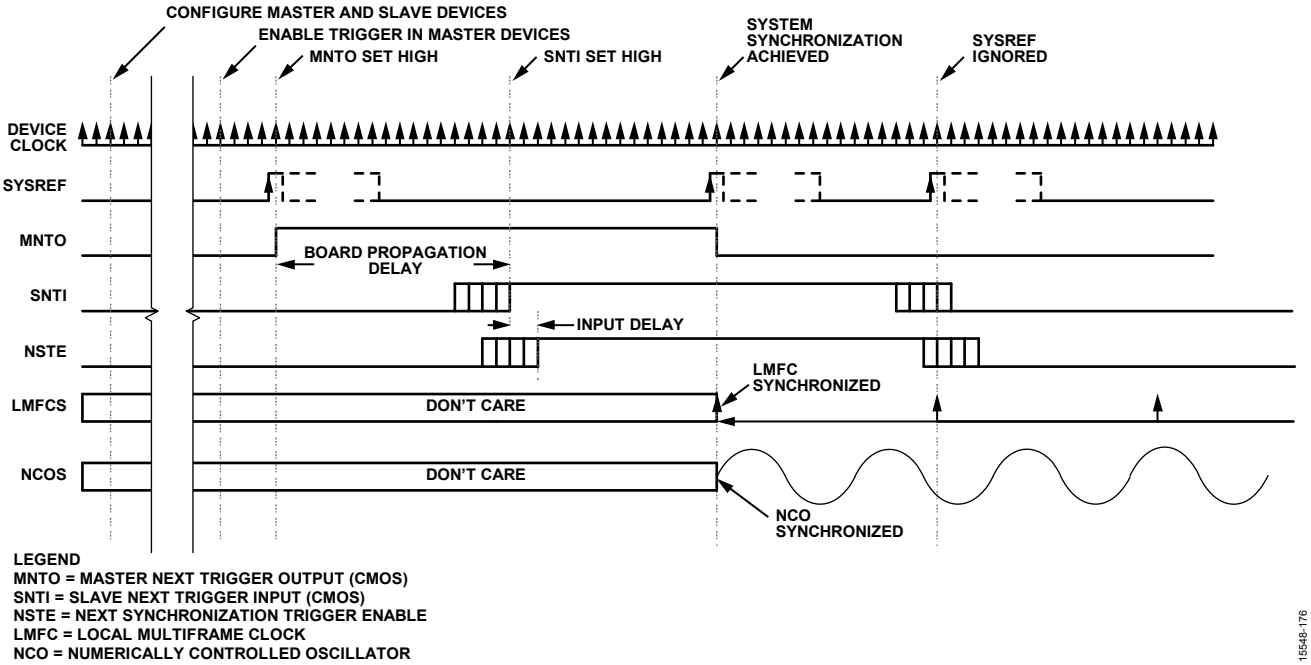


Figure 79. NCO Multichip Synchronization at Startup (Using Triggering and SYSREF)

DDC Mixer Description

When not bypassed (Register 0x0200 ≠ 0x00), the digital quadrature mixer performs a similar operation to an analog quadrature mixer. It performs the downconversion of input signals (real or complex) by using the NCO frequency as a local oscillator. For real input signals, a real mixer operation (with two multipliers) is performed. For complex input signals, a complex mixer operation (with four multipliers and two adders) is performed. The selection of real or complex inputs can be controlled individually for each DDC block using Bit 7 of the DDC control registers (Register 0x0310, Register 0x0330, Register 0x0350, and Register 0x0370).

DDC NCO + Mixer Loss and SFDR

When mixing a real input signal down to baseband, −6 dB of loss is introduced in the signal due to filtering of the negative image. An additional −0.05 dB of loss is introduced by the NCO. The total loss of a real input signal mixed down to baseband is −6.05 dB. For this reason, it is recommended that the user compensate for this loss by enabling the 6 dB of gain in the gain stage of the DDC to recenter the dynamic range of the signal within the full scale of the output bits (see the DDC Gain Stage section for more information).

When mixing a complex input signal (where I and Q DDC inputs come from the different ADCs) down to baseband, the maximum value each I/Q sample can reach is 1.414 × full-scale after it passes through the complex mixer. To avoid overrange of the I/Q samples and to keep the data bit widths aligned with real mixing, −3.06 dB of loss is introduced in the mixer for complex signals. An additional −0.05 dB of loss is introduced by the NCO. The total loss of a complex input signal mixed down to baseband is −3.11 dB.

The worst case spurious signal from the NCO is greater than 102 dBc SFDR for all output frequencies.

DDC DECIMATION FILTERS

After the frequency translation stage, there are multiple decimation filter stages used to reduce the output data rate. After the carrier of interest is tuned down to dc (carrier frequency = 0 Hz), these filters efficiently lower the sample rate, while providing sufficient alias rejection from unwanted adjacent carriers around the bandwidth of interest.

Figure 80 shows a simplified block diagram of the decimation filter stage, and Table 16 describes the filter characteristics of the different finite impulse response (FIR) filter blocks.

Table 17 and Table 18 show the different filter configurations selectable by including different filters. In all cases, the DDC filtering stage provides 80% of the available output bandwidth, <±0.005 dB of passband ripple, and >100 dB of stop band alias rejection.

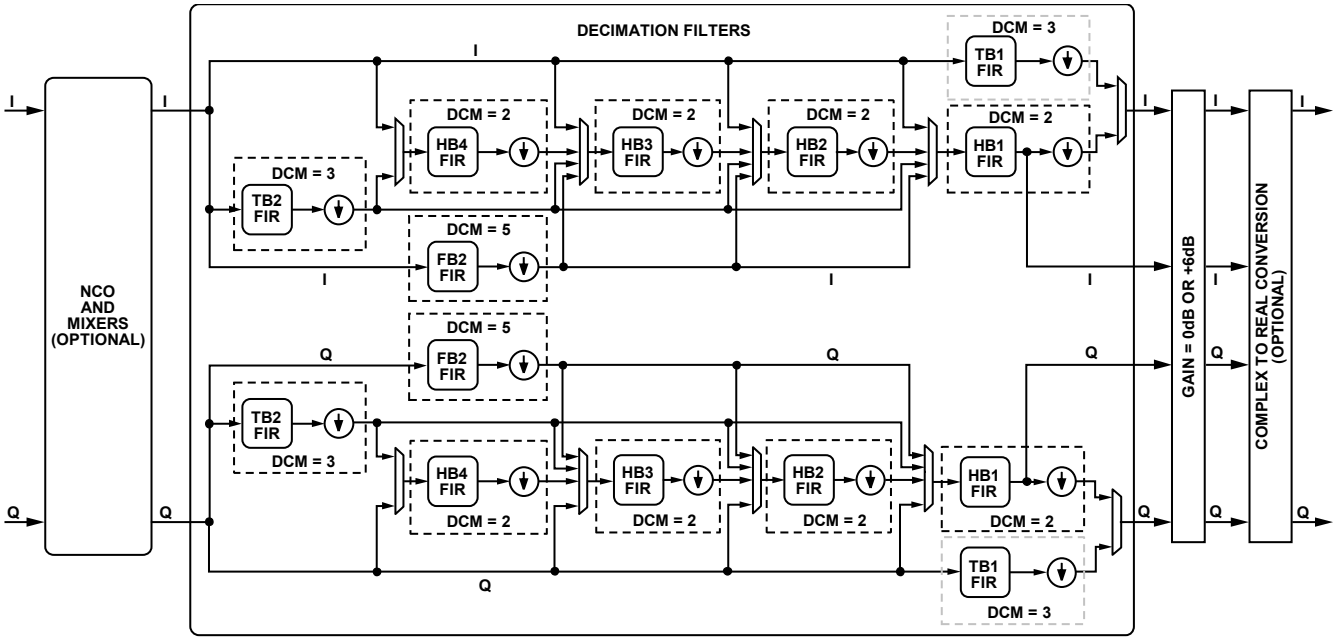


Figure 80. DDC Decimation Filter Block Diagram

Table 16. DDC Decimation Filter Characteristics

Filter Name	Filter Type	Decimation Ratio	Pass Band (rad/sec)	Stop Band (rad/sec)	Pass-Band Ripple (dB)	Stop-Band Attenuation (dB)
HB4	FIR low-pass	2	0.1 x π/2	1.9 x π/2	<±0.001	>100
HB3	FIR low-pass	2	0.2 x π/2	1.8 x π/2	<±0.001	>100
HB2	FIR low-pass	2	0.4 x π/2	1.6 x π/2	<±0.001	>100
HB1	FIR low-pass	2	0.8 x π/2	1.2 x π/2	<±0.001	>100
TB2	FIR low-pass	3	0.4 x π/3	1.6 x π/3	<±0.002	>100
TB1[1]	FIR low-pass	3	0.8 x π/3	1.2 x π/3	<±0.005	>100
FB2	FIR low-pass	5	0.4 x π/5	1.6 x π/5	<±0.001	>100

[1] TB1 is only supported in DDC0 and DDC1.

Table 17. DDC Filter Configurations[1]

ADC Sample Rate	DDC Filter Configuration	Real (I) Output		Complex (I/Q) Outputs		Alias-Protected Bandwidth	Ideal SNR Improvement (dB)[2]
		Decimation Ratio	Sample Rate	Decimation Ratio	Sample Rate		
f_S	HB1	1	f_S	2	$f_S/2$ (I) + $f_S/2$ (Q)	$f_S/2 \times 80\%$	1
f_S	TB1[3]	N/A	N/A	3	f $f_S/3$ (I) + $f_S/3$ (Q)	$f_S/3 \times 80\%$	2.7
f_S	HB2 + HB1	2	$f_S/2$	4	$f_S/4$ (I) + $f_S/4$ (Q)	$f_S/4 \times 80\%$	4
f_S	TB2 + HB1	3	$f_S/3$	6	$f_S/6$ (I) + $f_S/6$ (Q)	$f_S/6 \times 80\%$	5.7
f_S	HB3 + HB2 + HB1	4	$f_S/4$	8	$f_S/8$ (I) + $f_S/8$ (Q)	$f_S/8 \times 80\%$	7
f_S	FB2 + HB1	5	$f_S/5$	10	$f_S/10$ (I) + $f_S/10$ (Q)	$f_S/10 \times 80\%$	8
f_S	TB2 + HB2 + HB1	6	$f_S/6$	12	$f_S/12$ (I) + $f_S/12$ (Q)	$f_S/12 \times 80\%$	8.8
f_S	FB2 + TB1[3]	N/A	N/A	15	$f_S/15$ (I) + $f_S/15$ (Q)	$f_S/15 \times 80\%$	9.7
f_S	HB4 + HB3 + HB2 + HB1	8	$f_S/8$	16	$f_S/16$ (I) + $f_S/16$ (Q)	$f_S/16 \times 80\%$	10
f_S	FB2 + HB2 + HB1	10	$f_S/10$	20	$f_S/20$ (I) + $f_S/20$ (Q)	$f_S/20 \times 80\%$	11
f_S	TB2 + HB3 + HB2 + HB1	12	$f_S/12$	24	$f_S/24$ (I) + $f_S/24$ (Q)	$f_S/24 \times 80\%$	11.8
f_S	HB2 + FB2 + TB1[3]	N/A	N/A	30	$f_S/30$ (I) + $f_S/30$ (Q)	$f_S/30 \times 80\%$	12.7
f_S	FB2 + HB3 + HB2 + HB1	20	$f_S/20$	40	$f_S/40$ (I) + $f_S/40$ (Q)	$f_S/40 \times 80\%$	14
f_S	TB2 + HB4 + HB3 + HB2 + HB1	24	$f_S/24$	48	$f_S/48$ (I) + $f_S/48$ (Q)	$f_S/48 \times 80\%$	14.8

[1] N/A means not applicable.
[2] Ideal SNR improvement due to oversampling + filtering > 10log(bandwidth/$f_S/2$).
[3] TB1 is only supported in DDC0 and DDC1.

Table 18. DDC Filter Configurations (f_S = 3000 MSPS)[1]

ADC Sample Rate (MSPS)	DDC Filter Configuration	Real (I) Output		Complex (I/Q) Outputs		Alias-Protected Bandwidth (MHz)
		Decimation Ratio	Sample Rate (MSPS)	Decimation Ratio	Sample Rate (MSPS)	
3000	HB1	1	3000	2	1500 (I) + 1500 (Q)	1200
3000	TB1[2]	N/A	N/A	3	1000 (I) + 1000 (Q)	800
3000	HB2 + HB1	2	1500	4	750 (I) + 750 (Q)	600
3000	TB2 + HB1	3	1000	6	500 (I) + 500 (Q)	400
3000	HB3 + HB2 + HB1	4	750	8	375 (I) + 375 (Q)	300
3000	FB2 + HB1	5	600	10	300 (I) + 300 (Q)	240
3000	TB2 + HB2 + HB1	6	500	12	250 (I) + 250 (Q)	200
3000	FB2 + TB12	N/A	N/A	15	200 (I) + 200 (Q)	160
3000	HB4 + HB3 + HB2 + HB1	8	375	16	187.5 (I) + 187.5 (Q)	150
3000	FB2 + HB2 + HB1	10	300	20	150 (I) + 150 (Q)	120
3000	TB2 + HB3 + HB2 + HB1	12	250	24	125 (I) + 125 (Q)	100
3000	HB2 + FB2 + TB12	N/A	N/A	30	100 (I) + 100 (Q)	80
3000	FB2 + HB3 + HB2 + HB1	20	150	40	75 (I) + 75 (Q)	60
3000	TB2 + HB4 + HB3 + HB2 + HB1	24	125	48	62.5 (I) + 62.5 (Q)	50

[1] N/A means not applicable.
[2] TB1 is only supported in DDC0 and DDC1.

HB4 Filter Description

The first decimate by 2, half-band, low-pass, FIR filter (HB4) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB4 filter is only used when complex outputs (decimate by 16) or real outputs (decimate by 8) are enabled; otherwise, it is bypassed. Table 19 and Figure 81 show the coefficients and response of the HB4 filter.

Table 19. HB4 Filter Coefficients

HB4 Coefficient Number	Normalized Coefficient	Decimal Coefficient (15-Bit)
C1, C11	0.006042	99
C2, C10	0	0
C3, C9	−0.049377	−809
C4, C8	0	0
C5, C7	0.293304	4806
C6	0.5	8192

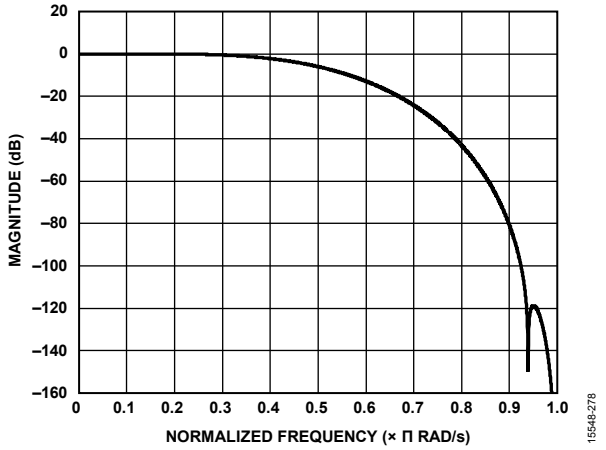


Figure 81. HB4 Filter Response

HB3 Filter Description

The second decimate by 2, half-band, low-pass, FIR filter (HB3) uses an 11-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB3 filter is only used when complex outputs (decimate by 8 or 16) or real outputs (decimate by 4 or 8) are enabled; otherwise, it is bypassed. Table 20 and Figure 82 show the coefficients and response of the HB3 filter.

Table 20. HB3 Filter Coefficients

HB3 Coefficient Number	Normalized Coefficient	Decimal Coefficient (17-Bit)
C1, C11	0.006637	435
C2, C10	0	0
C3, C9	−0.051055	−3346
C4, C8	0	0
C5, C7	0.294418	19295
C6	0.500000	65,536

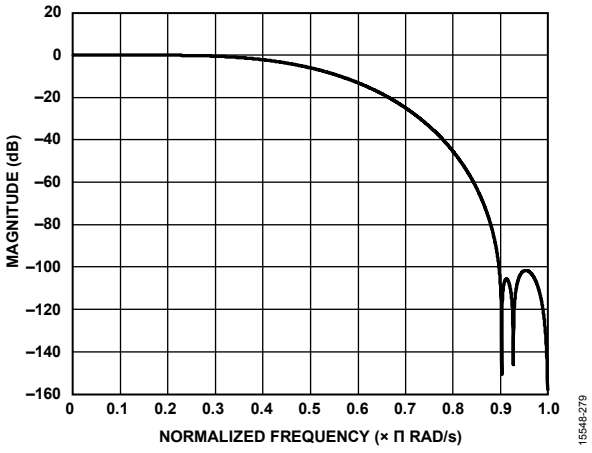


Figure 82. HB3 Filter Response

HB2 Filter Description

The third decimate by 2, half-band, low-pass, FIR filter (HB2) uses a 19-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption.

The HB2 filter is only used when complex or real outputs (decimate by 4, 8, or 16) is enabled; otherwise, it is bypassed.

Table 21 and Figure 83 show the coefficients and response of the HB2 filter.

Table 21. HB2 Filter Coefficients

HB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (18-Bit)
C1, C19	0.000671	88
C2, C18	0	0
C3, C17	−0.005325	−698
C4, C16	0	0
C5, C15	0.022743	2981
C6, C14	0	0
C7, C13	−0.074180	−9723
C8, C12	0	0
C9, C11	0.306091	40120
C10	0.5	65536

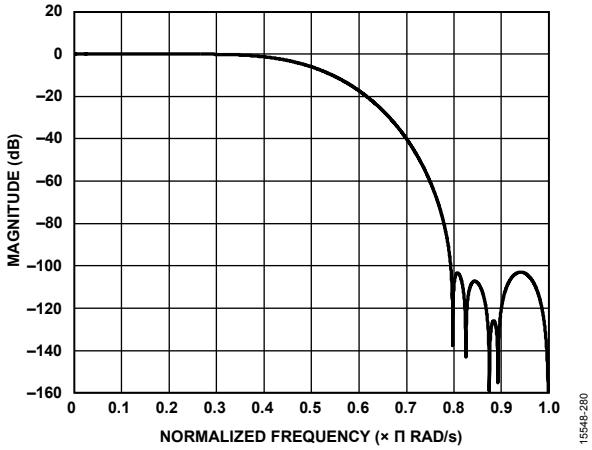


Figure 83. HB2 Filter Response

HB1 Filter Description

The fourth and final decimate by 2, half-band, low-pass, FIR filter (HB1) uses a 63-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The HB1 filter is always enabled and cannot be bypassed. Table 22 and Figure 84 show the coefficients and response of the HB1 filter.

Table 22. HB1 Filter Coefficients

HB1 Coefficient Number	Normalized Coefficient	Decimal Coefficient (20-Bit)
C1, C63	−0.000019	−10
C2, C62	0	0
C3, C61	0.000072	38
C4, C60	0	0
C5, C59	−0.000195	−102
C6, C58	0	0
C7, C57	0.000443	232
C8, C56	0	0
C9, C55	−0.000891	−467
C10, C54	0	0
C11, C53	0.001644	862
C12, C52	0	0
C13, C51	−0.00284	−1489
C14, C50	0	0
C15, C49	0.004654	2440
C16, C48	0	0
C17, C47	−0.007311	−3833
C18, C46	0	0
C19, C45	0.011122	5831
C20, C44	0	0
C21, C43	−0.016554	−8679
C22, C42	0	0
C23, C41	0.02442	12803
C24, C40	0	0
C25, C39	−0.036404	−19086
C26, C38	0	0
C27, C37	0.056866	29814
C28, C36	0	0
C29, C35	−0.101892	−53421
C30, C34	0	0
C31, C33	0.316883	166138
C32	0.5	262144

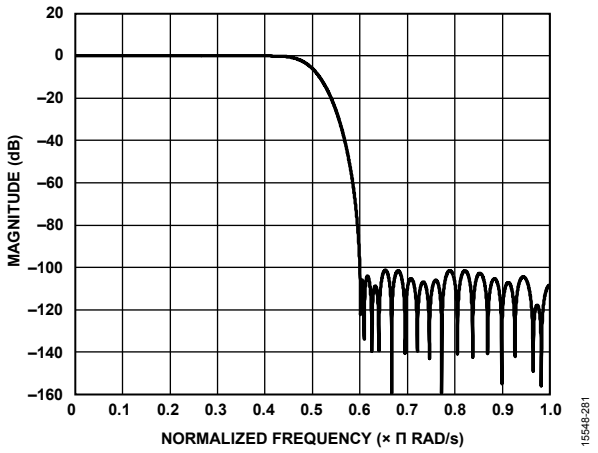


Figure 84. HB1 Filter Response

TB2 Filter Description

The TB2 uses a 26-tap, symmetrical, fixed coefficient filter implementation that is optimized for low power consumption. The TB2 filter is only used when decimation ratios of 6, 12, or 24 are required. Table 23 and Figure 85 show the coefficients and response of the TB2 filter.

Table 23. TB2 Filter Coefficients

TB2 Coefficient Number	Normalized Coefficient	Decimal Coefficient (19-Bit)
C1, C26	−0.000190	−50
C2, C25	−0.000793	−208
C3, C24	−0.00113	−298
C4, C23	0.000915	240
C5, C22	0.006290	1649
C6, C21	0.009822	2575
C7, C20	0.000915	240
C8, C19	−0.023483	−6156
C9, C18	−0.043151	−11312
C10, C17	−0.019317	−5064
C11, C16	0.071327	18698
C12, C15	0.201171	52736
C13, C14	0.297756	78055

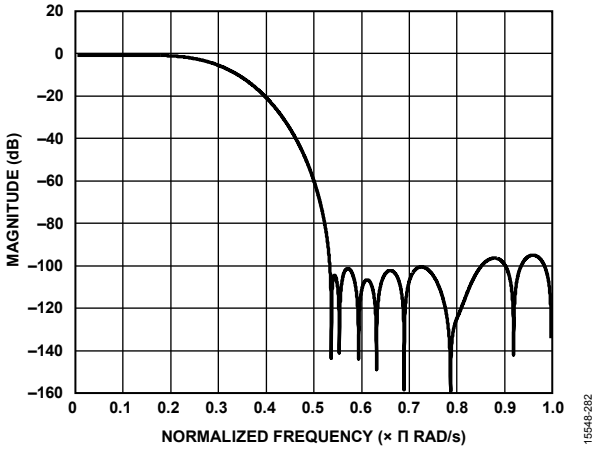


Figure 85. TB2 Filter Response

TB1 Filter Description

The TB1 decimate by 3, low-pass, FIR filter uses a 76-tap, symmetrical, fixed-coefficient filter implementation. Table 24 shows the TB1 filter coefficients and Figure 86 shows the TB1 filter response. TB1 is only supported in DDC0 and DDC1.

Table 24. TB1 Filter Coefficients

TB1 Coefficient Number	Decimal Coefficient	Quantized Coefficient (22-Bit)
1, 96	−0.000023	−96
2, 75	−0.000053	−224
3, 74	−0.000037	−156
4, 73	0.000090	379
5, 72	0.000291	1220
6, 71	0.000366	1534
7, 70	0.000095	398
8, 69	−0.000463	−1940
9, 68	−0.000822	−3448
10, 67	−0.000412	−1729
11, 66	0.000739	3100
12, 65	0.001665	6984
13, 64	0.001132	4748
14, 63	−0.000981	−4114
15, 62	−0.002961	−12418
16, 61	−0.002438	−10226
17, 60	0.001087	4560
18, 59	0.004833	20272
19, 58	0.004614	19352
20, 57	−0.000871	−3652
21, 56	−0.007410	−31080
22, 55	−0.008039	−33718
23, 54	0.000053	222
24, 53	0.010874	45608
25, 52	0.013313	55840
26, 51	0.001817	7620
27, 50	−0.015579	−65344
28, 49	−0.021590	−90556
29, 48	−0.005603	−23502
30, 47	0.022451	94167
31, 46	0.035774	150046
32, 45	0.013541	56796
33, 44	−0.034655	−145352
34, 43	−0.066549	−279128
35, 42	−0.035213	−147694
36, 41	0.071220	298720
37, 40	0.210777	884064
38, 39	0.309200	1296880

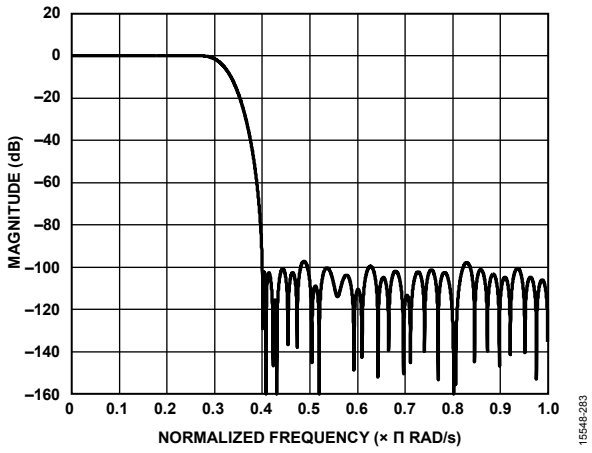


Figure 86. TB1 Filter Response

FB2 Filter Description

The FB2 decimate by 5, low-pass, FIR filter uses a 48-tap, symmetrical, fixed coefficient filter implementation. Table 25 shows the FB2 filter coefficients and Figure 87 shows the FB2 filter response.

Table 25. FB2 Filter Coefficients

FB2 Coefficient Number	Decimal Coefficient	Quantized Coefficient (21-Bit)
1, 48	0.000007	7
2, 47	−0.000004	−4
3, 46	−0.000069	−72
4, 45	−0.000244	−256
5, 44	−0.000544	−570
6, 43	−0.000870	−912
7, 42	−0.000962	−1009
8, 41	−0.000448	−470
9, 40	0.000977	1024
10, 39	0.003237	3394
11, 38	0.005614	5887
12, 37	0.006714	7040
13, 36	0.004871	5108
14, 35	−0.001011	−1060
15, 34	−0.010456	−10964
16, 33	−0.020729	−21736
17, 32	−0.026978	−28288
18, 31	−0.023453	−24592
19, 30	−0.005608	−5880
20, 29	0.027681	29026
21, 28	0.072720	76252
22, 27	0.121223	127112
23, 26	0.162346	170232
24, 25	0.185959	194992

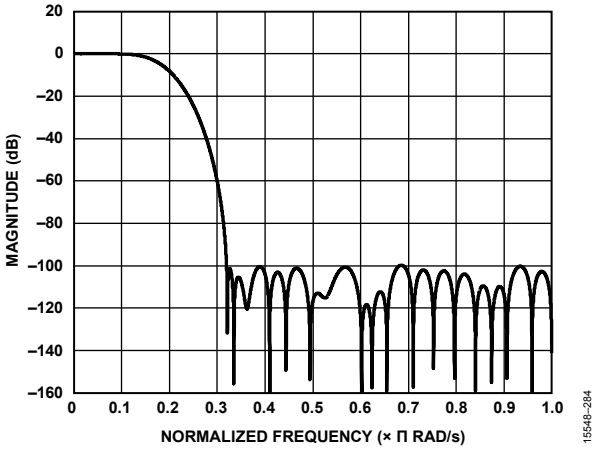


Figure 87. FB2 Filter Response

DDC GAIN STAGE

Each DDC contains an independently controlled gain stage. The gain is selectable as either 0 dB or 6 dB. When mixing a real input signal down to baseband, it is recommended that the user enable the 6 dB of gain to recenter the dynamic range of the signal within the full scale of the output bits.

When mixing a complex input signal down to baseband, the mixer has already recentered the dynamic range of the signal within the full scale of the output bits, and no additional gain is necessary. However, the optional 6 dB gain compensates for low signal strengths. The downsample by 2 portion of the HB1 FIR filter is bypassed when using the complex to real conversion stage. The TB1 filter does not have the 6 dB gain stage.

DDC COMPLEX TO REAL CONVERSION

Each DDC contains an independently controlled complex to real conversion block. The complex to real conversion block reuses the last filter (HB1 FIR) in the filtering stage along with an $f_S/4$ complex mixer to upconvert the signal. After upconverting the signal, the Q portion of the complex mixer is no longer needed and is dropped. The TB1 filter does not support complex to real conversion.

Figure 88 shows a simplified block diagram of the complex to real conversion.

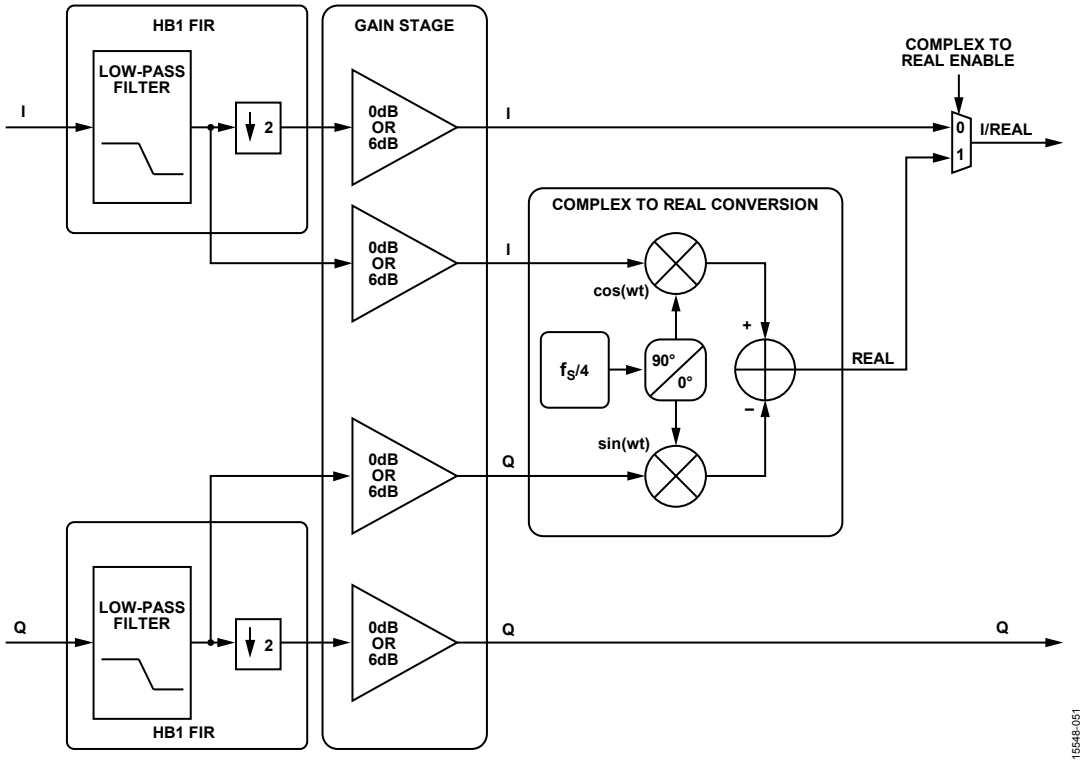


Figure 88. Complex to Real Conversion Block

DDC MIXED DECIMATION SETTINGS

The AD6688 also supports DDCs with different decimation rates. In this scenario, the chip decimation ratio must be set to the lowest decimation ratio of all the DDC channels. Samples of higher decimation ratio DDCs are repeated to match the chip decimation ratio sample rate. Only mixed decimation ratios that are integer multiples of 2 are supported. For example, decimate by 1, 2, 4, 8, or 16 can be mixed together, decimate by 3, 6, 12, 24, or 48 can be mixed together, or decimate by 5, 10, 20, or 40 can be mixed together.

Table 26 shows the DDC sample mapping when the chip decimation ratio is different than the DDC decimation ratio.

For example, if the chip decimation ratio is set to decimate by 4, DDC0 is set to use the HB2 + HB1 filters (complex outputs, decimate by 4) and DDC1 is set to use the HB4 + HB3 + HB2 + HB1 filters (real outputs, decimate by 8), then DDC1 repeats its output data 2 times for every one DDC0 output. The resulting output samples are shown in Table 27.

Table 26. Sample Mapping when Chip Decimation Ratio (DCM) Does Not Match DDC DCM

Sample Index	DDC DCM = Chip DCM	DDC DCM = 2 × Chip DCM	DDC DCM = 4 × Chip DCM	DDC DCM = 8 × Chip DCM
0	N	N	N	N
1	N + 1	N	N	N
2	N + 2	N + 1	N	N
3	N + 3	N + 1	N	N
4	N + 4	N + 2	N + 1	N
5	N + 5	N + 2	N + 1	N
6	N + 6	N + 3	N + 1	N
7	N + 7	N + 3	N + 1	N
8	N + 8	N + 4	N + 2	N + 1
9	N + 9	N + 4	N + 2	N + 1
10	N + 10	N + 5	N + 2	N + 1
11	N + 11	N + 5	N + 2	N + 1
12	N + 12	N + 6	N + 3	N + 1
13	N + 13	N + 6	N + 3	N + 1
14	N + 14	N + 7	N + 3	N + 1
15	N + 15	N + 7	N + 3	N + 1
16	N + 16	N + 8	N + 4	N + 2
17	N + 17	N + 8	N + 4	N + 2
18	N + 18	N + 9	N + 4	N + 2
19	N + 19	N + 9	N + 4	N + 2
20	N + 20	N + 10	N + 5	N + 2
21	N + 21	N + 10	N + 5	N + 2
22	N + 22	N + 11	N + 5	N + 2
23	N + 23	N + 11	N + 5	N + 2
24	N + 24	N + 12	N + 6	N + 3
25	N + 25	N + 12	N + 6	N + 3
26	N + 26	N + 13	N + 6	N + 3
27	N + 27	N + 13	N + 6	N + 3
28	N + 28	N + 14	N + 7	N + 3
29	N + 29	N + 14	N + 7	N + 3
30	N + 30	N + 15	N + 7	N + 3
31	N + 31	N + 15	N + 7	N + 3

Table 27. Chip DCM = 4, DDC0 DCM = 4 (Complex), and DDC1 DCM = 8 (Real)[1]

	DDC0		DDC1	
DDC Input Samples	**Output Port I**	**Output Port Q**	**Output Port I**	**Output Port Q**
N	I0[N]	Q0[N]	I1[N]	Not applicable
N + 1	I0[N]	Q0[N]	I1[N]	Not applicable
N + 2	I0[N]	Q0[N]	I1[N]	Not applicable
N + 3	I0[N]	Q0[N]	I1[N]	Not applicable
N + 4	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 5	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 6	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 7	I0[N + 1]	Q0[N + 1]	I1[N]	Not applicable
N + 8	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 9	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 10	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 11	I0[N + 2]	Q0[N + 2]	I1[N + 1]	Not applicable
N + 12	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 13	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 14	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable
N + 15	I0[N + 3]	Q0[N + 3]	I1[N + 1]	Not applicable

[1] DCM means decimation.

DDC EXAMPLE CONFIGURATIONS

Table 28 describes the register settings for multiple DDC example configurations. Bandwidths listed are with <−0.005 dB of pass-band ripple and >100 dB of stop band alias rejection.

Table 28. DDC Example Configurations (per ADC Channel Pair)

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
One DDC	2	Complex	Complex	40% × f_S	2	0x0200 = 0x01 (one DDC; I/Q selected) 0x0201 = 0x01 (chip decimate by 2) 0x0310 = 0x83 (complex mixer; 0 dB gain; variable IF; complex outputs; HB1 filter) 0x0311 = 0x04 (DDC I Input = ADC Channel A; DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0
Two DDCs	4	Complex	Complex	20% × f_S	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x80 (complex mixer; 0 dB gain; variable IF; complex outputs; HB2+HB1 filters) 0x0311,0x0331 = 0x04 (DDC I input = ADC Channel A; DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	4	Complex	Real	10% × f_S	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x89 (complex mixer; 0 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311,0x0331 = 0x04 (DDC I Input = ADC Channel A; DDC Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	4	Real	Real	10% × f_S	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x49 (real mixer; 6 dB gain; variable IF; real output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Two DDCs	4	Real	Complex	20% × f_S	4	0x0200 = 0x02 (two DDCs; I/Q selected) 0x0201 = 0x02 (chip decimate by 4) 0x0310, 0x0330 = 0x40 (real mixer; 6 dB gain; variable IF; complex output; HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Two DDCs	8	Real	Real	5% × f_S	2	0x0200 = 0x22 (two DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x05 (DDC1 I input = ADC Channel B; DDC1 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1
Four DDCs	8	Real	Complex	10% × f_S	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x41 (real mixer; 6 dB gain; variable IF; complex output; HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3

Chip Application Layer	Chip Decimation Ratio	DDC Input Type	DDC Output Type	Bandwidth Per DDC[1]	No. of Virtual Converters Required	Register Settings
Four DDCs	8	Real	Real	5% × f_S	4	0x0200 = 0x23 (four DDCs; I only selected) 0x0201 = 0x03 (chip decimate by 8) 0x0310, 0x0330, 0x0350, 0x0370 = 0x4A (real mixer; 6 dB gain; variable IF; real output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3
Four DDCs	16	Real	Complex	5% × f_S	8	0x0200 = 0x03 (four DDCs; I/Q selected) 0x0201 = 0x04 (chip decimate by 16) 0x0310, 0x0330, 0x0350, 0x0370 = 0x42 (real mixer; 6 dB gain; variable IF; complex output; HB4 + HB3 + HB2 + HB1 filters) 0x0311 = 0x00 (DDC0 I input = ADC Channel A; DDC0 Q input = ADC Channel A) 0x0331 = 0x00 (DDC1 I input = ADC Channel A; DDC1 Q input = ADC Channel A) 0x0351 = 0x05 (DDC2 I input = ADC Channel B; DDC2 Q input = ADC Channel B) 0x0371 = 0x05 (DDC3 I input = ADC Channel B; DDC3 Q input = ADC Channel B) 0x0316, 0x0317, 0x0318, 0x0319, 0x031A, 0x031B, 0x031D, 0x031E, 0x031F, 0x0320, 0x0321, 0x0322 = FTW and POW set as required by application for DDC0 0x0336, 0x0337, 0x0338, 0x0339, 0x033A, 0x033B, 0x033D, 0x033E, 0x033F, 0x0340, 0x0341, 0x0342 = FTW and POW set as required by application for DDC1 0x0356, 0x0357, 0x0358, 0x0359, 0x035A, 0x035B, 0x035D, 0x035E, 0x035F, 0x0360, 0x0361, 0x0362 = FTW and POW set as required by application for DDC2 0x0376, 0x0377, 0x0378, 0x0379, 0x037A, 0x037B, 0x037D, 0x037E, 0x037F, 0x0380, 0x0381, 0x0382 = FTW and POW set as required by application for DDC3

[1] f_S is the ADC sample rate.

DDC POWER CONSUMPTION

Table 28 describes the typical and maximum DVDD and DRVDD1 power for certain DDC modes. f_S = 3 GHz in all cases.

Table 29. DDC Power Consumption for Example Configurations

Number of DDCs	DDC Decimation Ratio[1]	Number of Lanes (L)	Number of Virtual Converters (M)	Number of Octets per frame (F)	DVDD Power (mW)		DRVDD1 Power (mW)	
					Typ	Max	Typ	Max
2	2	8	4	1	615	1190	415	565
2	3	8	4	1	675	1250	310	435
2	4	8	4	1	585	1150	250	370
2	6	4	4	2	590	1145	175	275
2	8	4	4	2	570	1120	145	245
2	12	2	4	4	585	1135	105	205
4	4	8	8	2	745	1350	415	570
4	6	8	8	2	755	1365	305	440
4	8	8	8	2	715	1320	250	370

[1] See Table 17 and Table 18 for details on decimation filter selection and associated alias protected bandwidths and SNR improvements.

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the peak magnitude of the digitized signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The results of the signal monitor block can be obtained either by reading back the internal values from the SPI port or by embedding the signal monitoring information into the JESD204B interface as special control bits. A global, 24-bit programmable period controls the duration of the measurement. Figure 89 shows the simplified block diagram of the signal monitor block.

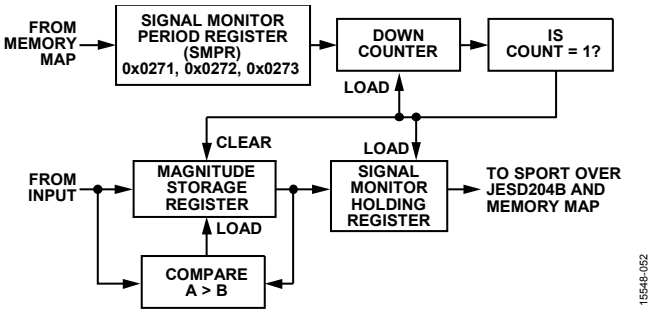


Figure 89. Signal Monitor Block

The peak detector captures the largest signal within the observation period. The detector only observes the magnitude of the signal. The resolution of the peak detector is a 13-bit value, and the observation period is 24 bits and represents converter output samples. The peak magnitude can be derived by using the following equation:

$$Peak\ Magnitude\ (\text{dBFS}) = 20\log(Peak\ Detector\ Value/2^{13})$$

The magnitude of the input port signal is monitored over a programmable time period, which is determined by the signal monitor period register (SMPR). The peak detector function is enabled by setting Bit 1 of Register 0x0270 in the signal monitor control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling peak detection mode, the value in the SMPR is loaded into a monitor period timer, which decrements at the decimated clock rate. The magnitude of the input signal is compared with the value in the internal magnitude storage register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the magnitude storage register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register, which can be read through the memory map or output through the SPORT over the JESD204B interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown restarts. In addition, the magnitude of the first input sample is updated in the magnitude storage register, and the comparison and update procedure, as explained previously, continues.

SPORT OVER JESD204B

The signal monitor data can also be serialized and sent over the JESD204B interface as control bits. These control bits must be deserialized from the samples to reconstruct the statistical data. The signal control monitor function is enabled by setting Bits[1:0] of Register 0x0279 and Bit 1 of Register 0x027A. Figure 90 shows two different example configurations for the signal monitor control bit locations inside the JESD204B samples. A maximum of three control bits can be inserted into the JESD204B samples; however, only one control bit is required for the signal monitor. Control bits are inserted from MSB to LSB. If only one control bit is to be inserted (CS = 1), only the most significant control bit is used (see Example Configuration 1 and Example Configuration 2 in Figure 90). To select the SPORT over JESD204B option, program Register 0x0559, Register 0x055A, and Register 0x058F. See Table 46 for more information on setting these bits.

Figure 91 shows the 25-bit frame data that encapsulates the peak detector value. The frame data is transmitted MSB first with five 5-bit subframes. Each subframe contains a start bit that can be used by a receiver to validate the deserialized data. Figure 92 shows the SPORT over JESD204B signal monitor data with a monitor period timer set to 80 samples.

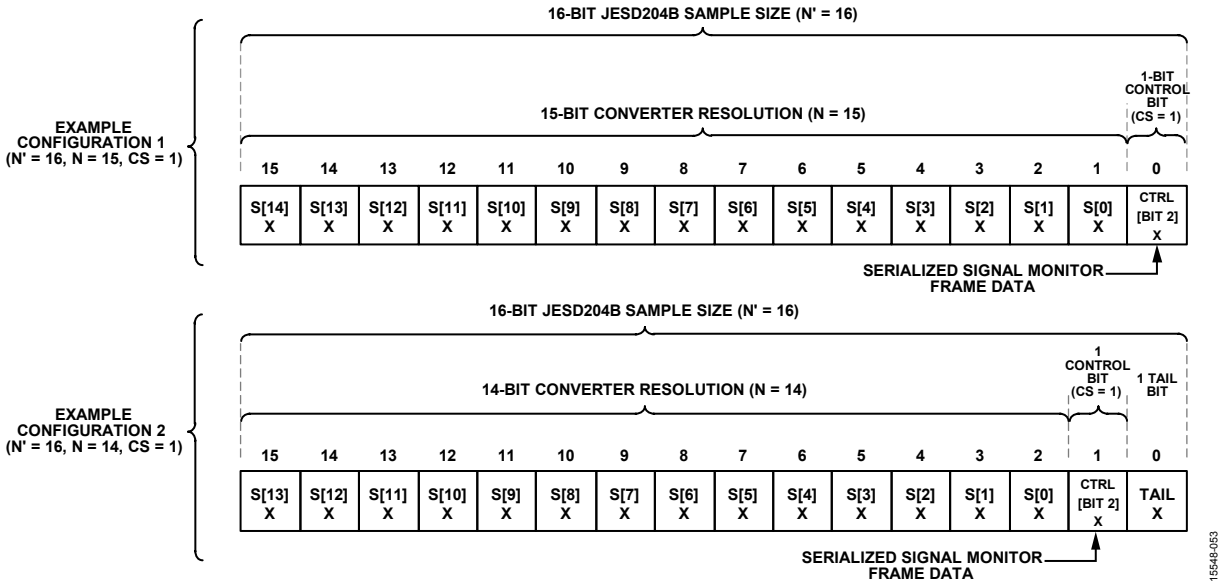


Figure 90. Signal Monitor Control Bit Locations

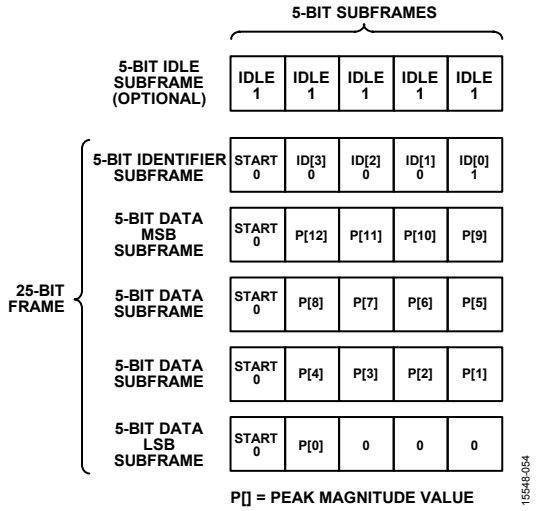


Figure 91. SPORT over JESD204B Signal Monitor Frame Data

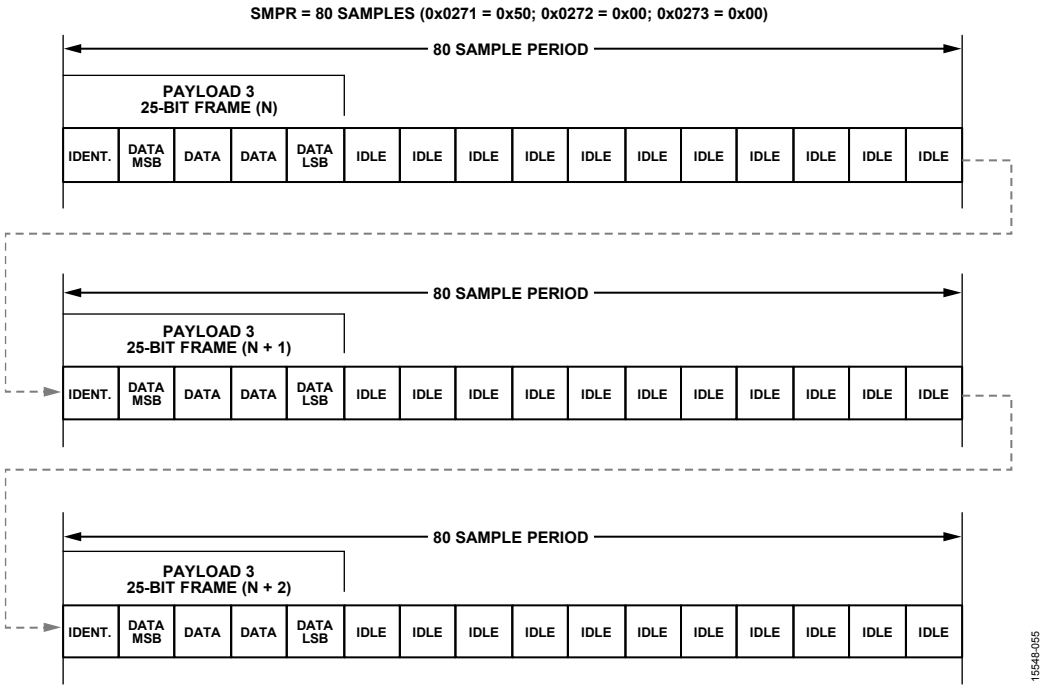


Figure 92. SPORT over JESD204B Signal Monitor Example with Period = 80 Samples

DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD6688 digital outputs are designed to the JEDEC standard JESD204B, serial interface for data converters. JESD204B is a protocol to link the AD6688 to a digital processing device over a serial interface with lane rates of up to 16 Gbps. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and an ability to enable smaller packages for converter and logic devices.

JESD204B OVERVIEW

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported through the use of special control characters during the initial establishment of the link. Additional control characters are embedded in the data stream to maintain synchronization thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD6688 JESD204B data transmit block maps up to two physical ADCs or up to eight virtual converters (when DDCs are enabled) over a link. A link can be configured to use one, two, four, or eight JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (the AD6688 output) and the JESD204B receiver (the logic device input).

The JESD204B link is described according to the following parameters:

- L is the number of lanes per converter device (lanes per link); AD6688 value = 1, 2, 4, or 8.
- M is the number of converters per converter device (virtual converters per link); AD6688 value = 1, 2, 4, or 8.
- F is the octets per frame; AD6688 value = 1, 2, 4, 8, or 16.
- N′ is the number of bits per sample (JESD204B word size); AD6688 value = 8 or 16.
- N is the converter resolution; AD6688 value = 7 to 16.
- CS is the number of control bits per sample; AD6688 value = 0, 1, 2, or 3.
- K is the number of frames per multiframe; AD6688 value = 4, 8, 12, 16, 20, 24, 28, or 32.
- S is the samples transmitted per single converter per frame cycle; AD6688 value is set automatically based on L, M, F, and N′.
- HD is the high density mode; the AD6688 is set automatically based on L, M, F, and N′.
- CF is the number of control words per frame clock cycle per converter device; AD6688 value = 0.

Figure 93 shows a simplified block diagram of the AD6688 JESD204B link. By default, the AD6688 is configured to use two converters and four lanes. Converter A data is output to SERDOUT0± and/or SERDOUT1±, and Converter B is output to SERDOUT2± and/or SERDOUT3±. The AD6688 allows other configurations such as combining the outputs of both converters onto a single lane, or changing the mapping of the A and B digital output paths. These modes are set up via a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD6688, the 14-bit converter word from each converter is broken into two octets (eight bits of data). Bit 13 (MSB) through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 (LSB) and two tail bits. The tail bits can be configured as zeros or as a pseudorandom number sequence. The tail bits can also be replaced with control bits indicating overrange, SYSREF±, or fast detect output.

The two resulting octets can be scrambled. Scrambling is optional; however, it is recommended to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver is a self synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8-bit/10-bit encoder. The 8-bit/10-bit encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 94 shows how the 14-bit data is taken from the ADC, how the tail bits are added, how the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 94 shows the default data format.

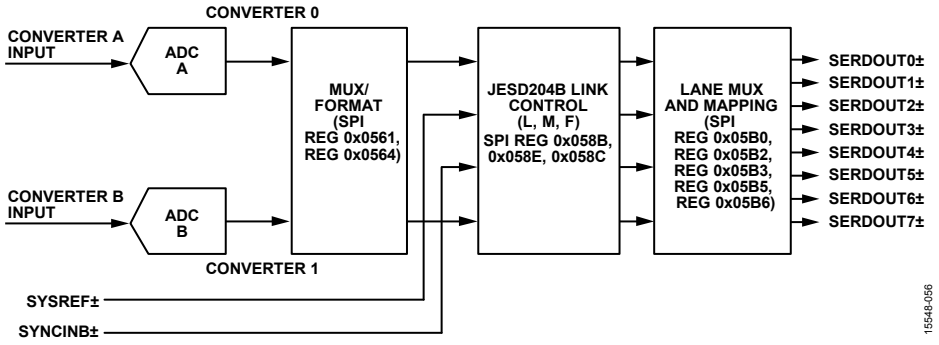


Figure 93. Transmit Link Simplified Block Diagram Showing Full Bandwidth Mode (Register 0x0200 = 0x00)

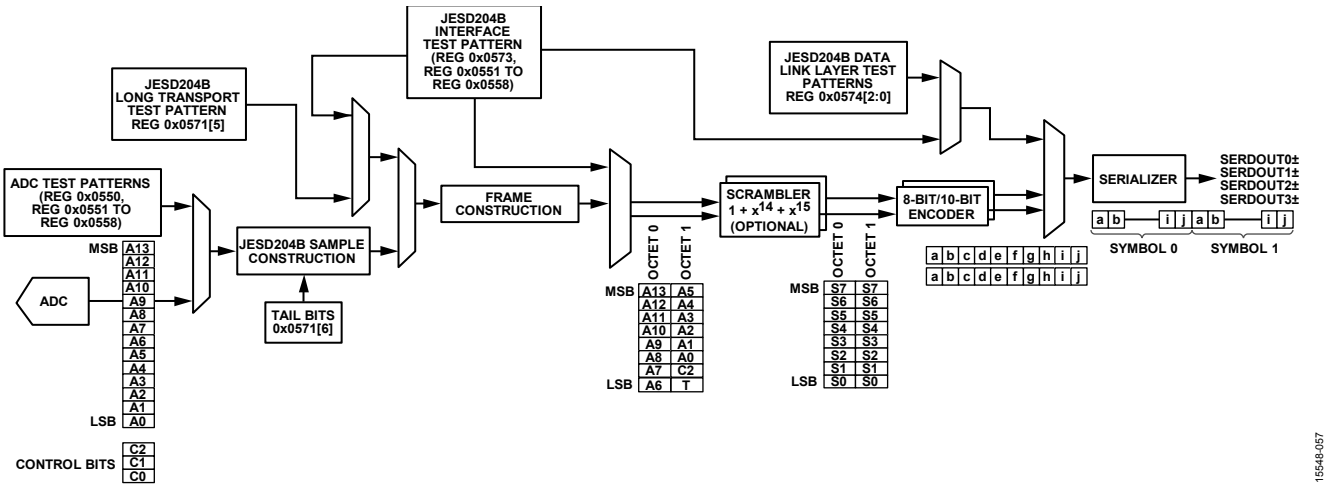


Figure 94. ADC Output Datapath Showing Data Framing

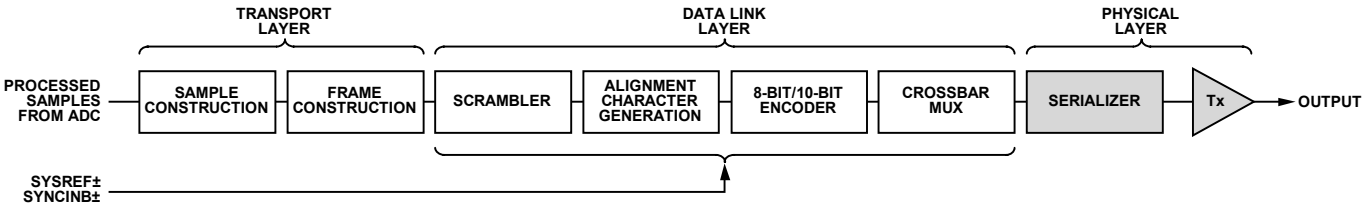


Figure 95. Data Flow

FUNCTIONAL OVERVIEW

The block diagram in Figure 95 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the open source initiative (OSI) model widely used to describe the abstraction layers of communications systems. These layers are the transport layer, data link layer, and physical layer (serializer and output driver).

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into JESD204B frames that are mapped to 8-bit octets. These octets are sent to the data link layer. The transport layer mapping is controlled by rules derived from the link parameters. Tail bits are added to fill gaps where required. The following equation can be used to determine the number of tail bits within a sample (JESD204B word):

$$T = N' - N - CS$$

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These functions include optionally scrambling the data, inserting control characters for multichip synchronization, lane alignment, monitoring and encoding 8-bit octets into 10-bit symbols. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data used by the receiver to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. In this layer, parallel data is converted into one, two, four, or eight lanes of high speed differential serial data.

JESD204B LINK ESTABLISHMENT

The AD6688 JESD204B transmitter (Tx) interface operates in Subclass 1 as defined in the JEDEC Standard JESD204B (July 2011 specification). The link establishment process is divided into the following steps: code group synchronization and SYNCINB±, initial lane alignment sequence, and user data and error correction.

Code Group Synchronization (CGS) and SYNCINB±

The CGS is the process by which the JESD204B receiver finds the boundaries between the 10-bit symbols in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver must locate /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by asserting the SYNCINB± pin of the AD6688 low. The JESD204B Tx then begins sending /K/ characters. After the receiver synchronizes, it waits for the correct reception of at least four consecutive /K/ symbols. It then deasserts SYNCINB±. The AD6688 then transmits an ILAS on the following local multiframe clock (LMFC) boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard JESD204B, July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can also be controlled by the SPI. The SYNCINB± signal is a differential, dc-coupled LVDS mode signal by default, but it can also be driven single-ended. For more information on configuring the SYNCINB± pin operation, refer to Register 0x0572.

The SYNCINB± pins can also be configured to run in CMOS (single-ended) mode by setting Bit[4] in Register 0x0572. When running SYNCINB± in CMOS mode, connect the CMOS SYNCINB± signal to Pin 21 (SYNCINB+) and leave Pin 20 (SYNCINB−) floating.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four multiframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent, starting with the third character. The second character is a /Q/ character to confirm that the link configuration data is to follow. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 96. The four multiframes include the following:

- Multiframe 1: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 2: begins with an /R/ character followed by a /Q/ character (/K28.4/), followed by link configuration parameters over 14 configuration octets (see Table 30) and ends with an /A/ character. Many of the parameter values are of the value − 1 notation.
- Multiframe 3: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).
- Multiframe 4: begins with an /R/ character (/K28.0/) and ends with an /A/ character (/K28.3/).

User Data and Error Detection

After the initial lane alignment sequence is complete, the user data is sent. Normally, within a frame, all characters are considered user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default; however, it can be disabled using the SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced by an /A/. The JESD204B receiver (Rx) checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or asserting the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters can be modified using the SPI. The frame alignment character insertion (FACI) is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x0571.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit symbols and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 30. The 8-bit/10-bit encoding ensures that the signal is dc balanced by using the same number of ones and zeros across multiple symbols.

The 8-bit/10-bit interface has options that can be controlled via the SPI. These operations include bypass and invert. These options are troubleshooting tools for the verification of the digital front end (DFE). See the Memory Map section, Register 0x0572, Bits[2:1] for information on configuring the 8-bit/10-bit encoder.

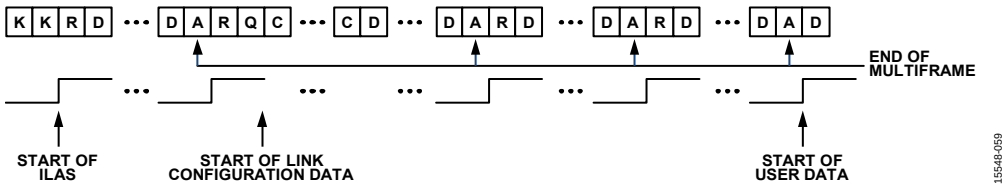


Figure 96. Initial Lane Alignment Sequence

Table 30. AD6688 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value, RD[1] = −1	10-Bit Value, RD[1] = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0100	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

[1] RD means running disparity.

PHYSICAL LAYER (DRIVER) OUTPUTS

Digital Outputs, Timing, and Controls

The AD6688 physical layer consists of drivers that are defined in the JEDEC Standard JESD204B, July 2011. The differential digital outputs are powered up by default. The drivers use a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 0.85 × DRVDD1 V p-p swing at the receiver (see Figure 97). The swing is adjustable through the SPI registers. AC coupling is recommended to connect to the receiver. See the Memory Map section (Register 0x05C0 to Register 0x05C3 in Table 46) for more details.

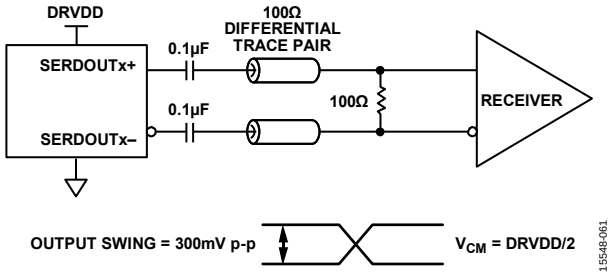


Figure 97. AC-Coupled Digital Output Termination Example

The AD6688 digital outputs can interface with custom application specific ICs (ASICs) and field-programmable gate array (FPGA) receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors can result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 98 to Figure 100 show an example of the digital output data eye, jitter histogram, and bathtub curve for one AD6688 lane running at 16 Gbps. The format of the output data is twos complement by default. To change the output data format, see the Memory Map section (Register 0x0561 in Table 46).

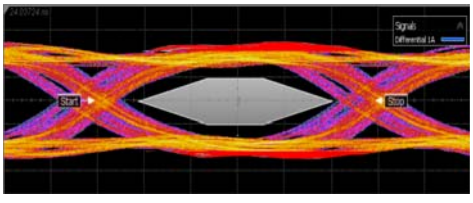


Figure 98. Digital Outputs Data Eye, External 100 Ω Terminations at 16 Gbps

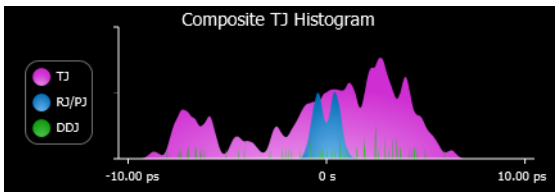


Figure 99. Digital Outputs Jitter Histogram, External 100 Ω Terminations at 16 Gbps

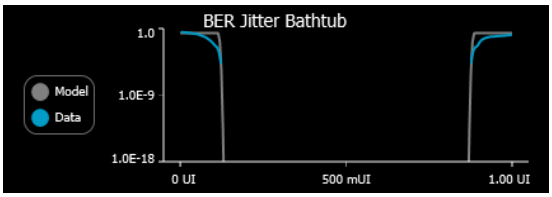


Figure 100. Digital Outputs Bathtub Curve, External 100 Ω Terminations at 16 Gbps

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. Use the de-emphasis feature only when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link can cause the receiver eye diagram to fail. Use the de-emphasis setting with caution because it can increase electromagnetic interference (EMI). See the Memory Map section (Register 0x05C4 to Register 0x05CB in Table 46) for more details.

Phase-Locked Loop

The phase-locked loop (PLL) generates the serializer clock, which operates at the JESD204B lane rate. The status of the PLL lock can be checked in the PLL locked status bit (Register 0x056F, Bit 7). This read only bit notifies the user if the PLL achieved a lock for the specific setup. Register 0x056F also has a loss of lock (LOL) sticky bit (Bit 3) that notifies the user that there was a loss of lock detected. The sticky bit can be reset by issuing a JESD204B link restart (Register 0x0571 = 0x15, followed by Register 0x0571 = 0x14). See Table 32 for the re-initialization of the link following a link power cycle.

The JESD204B lane rate control, Bits[7:4] of Register 0x056E, must be set to correspond with the lane rate. Table 31 shows the lane rates supported by the AD6688 using Register 0x056E.

Table 31. AD6688 Register 0x056E Supported Lane Rates

Value	Lane Rate
0x00	Lane rate = 6.75 Gbps to 13.5 Gbps.
0x10	Lane rate = 3.375 Gbps to 6.75 Gbps.
0x30	Lane rate = 13.5 Gbps to 15.5 Gbps (default for AD6688).
0x50	Lane rate = 1.6875 Gbps to 3.375 Gbps.

$f_S \times 4$ MODE

The $f_S \times 4$ mode adds a special packing mode on top of a JESD204B transmitter/receiver to fix the serial lane rate at four times the sample rate (f_S).

The JESD204B link settings are L = 8; M = 2; F = 2; S = 5; N' = 12; N = 12; CS = 0; CF = 2; and HD = 1.

However, CF = 2 is not supported by the design; therefore, the following link parameters are used along with special packing: L = 8; M = 2; F = 2; S = 4; N' = 16; N = 16; CS = 0; CF = 0; and HD = 0.

In $f_S \times 4$ mode, five 12-bit ADC samples (along with an extra 4 bits) are packed into four 16-bit JESD204B samples to create a 64-bit frame.

The following SPI writes are necessary to place the device in $f_S \times 4$ mode:

- Register 0x0570 = 0xFE. This setting places the device in M = 2, L = 8, $f_S \times 4$ mode.
- Register 0x058B = 0x0F. This setting places the device in CS = 0, N' = 16.
- Register 0x058F = 0x2F. This setting places the device in Subclass 1 mode, N = 16.

The transmit architecture of the $f_S \times 4$ mode is shown in Figure 101, and the receive portion is shown in Figure 102. The $f_S \times 4$ mode only works in full bandwidth mode (Register 0x0200 = 0x00).

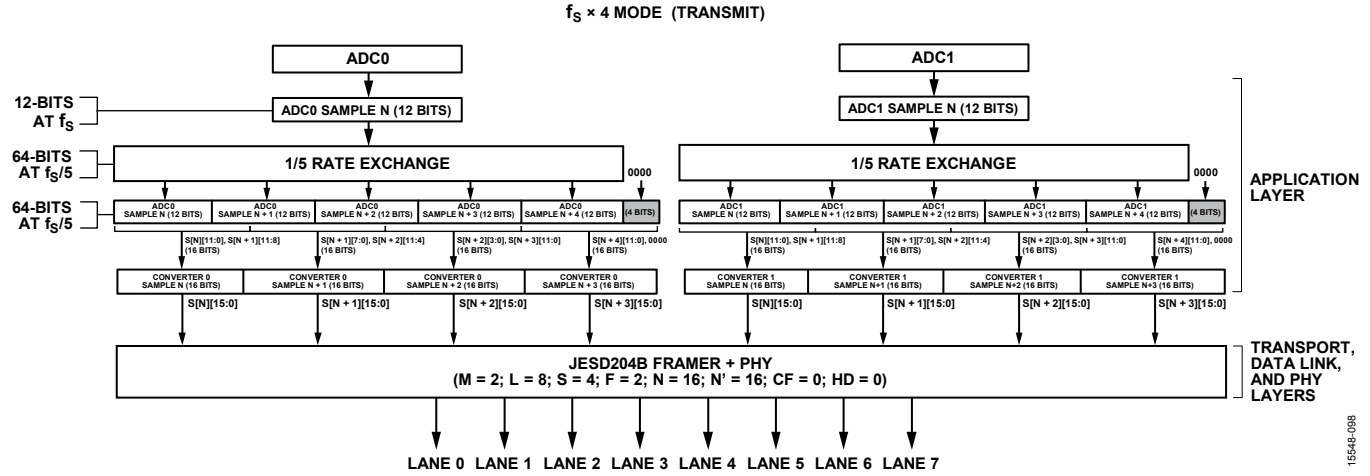


Figure 101. $f_S \times 4$ Mode (Transmit)

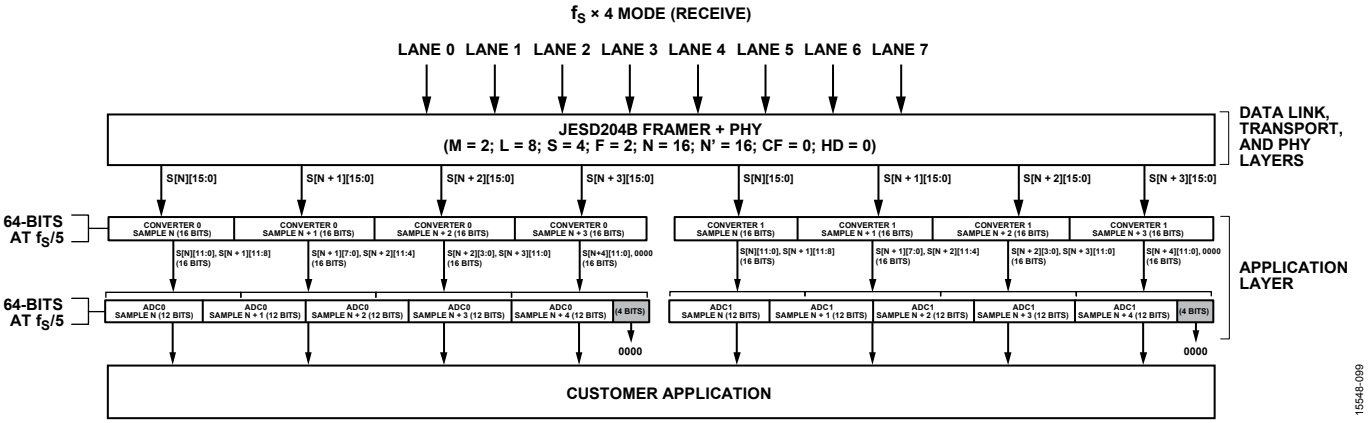


Figure 102. $f_S \times 4$ Mode (Receive)

SETTING UP THE AD6688 DIGITAL INTERFACE

To ensure proper operation of the AD6688 at start-up, some SPI writes are needed to initialize the link. Additionally, these registers must be written every time the ADC is reset. Any one of the following resets warrants the initialization routine for the digital interface:

- Hard reset, as in power-up.
- Power-up using the PDWN pin.
- Power-up using the SPI (Register 0x0002, Bits[1:0]).
- SPI soft reset (Register 0x0000 = 0x81).
- Datapath soft reset (Register 0x0001 = 0x02).
- JESD204B link power cycle (Register 0x0571 = 0x15, then 0x14).

The initialization SPI writes are as shown in Table 32.

Table 32. AD6688 JESD204B Initialization

Register	Value	Comment
0x1228	0x4F	Reset JESD204B start-up circuit
0x1228	0x0F	JESD204B start-up circuit in normal operation
0x1222	0x00	JESD204B PLL force normal operation
0x1222	0x04	Reset JESD204B PLL calibration
0x1222	0x00	JESD204B PLL normal operation
0x1262	0x08	Clear loss of lock bit
0x1262	0x00	Loss of lock bit normal operation

The AD6688 has one JESD204B link. The serial outputs (SERDOUT0± to SERDOUT7±) are considered to be part of one JESD204B link. The basic parameters that determine the link setup are

- Number of lanes per link (L)
- Number of converters per link (M)
- Number of octets per frame (F)

If the internal DDCs are used for on-chip digital processing, M represents the number of virtual converters. The virtual converter mapping setup is shown in Figure 64.

The maximum lane rate allowed by the AD6688 is 16 Gbps. The lane rate is related to the JESD204B parameters using the following equation:

$$Lane\ Rate = \frac{M \times N' \times \left(\frac{10}{8}\right) \times f_{OUT}}{L}$$

where $f_{OUT} = \frac{f_{ADC_CLOCK}}{Decimation\ Ratio}$

The decimation ratio (DCM) is the parameter programmed in Register 0x0201.

Use the following steps to configure the output:

1. Power down the link.
2. Select the JESD204B link configuration options.
3. Configure the detailed options.
4. Set output lane mapping (optional).
5. Set additional driver configuration options (optional).
6. Power up the link.
7. Initialize the JESD204B link by issuing the commands in Table 32.

Table 33 and Table 34 show the JESD204B output configurations supported for both N′ = 16 and N′ = 8 for a given number of virtual converters. Take care to ensure that the serial lane rate for a given configuration is within the supported range of 1.6875 Gbps to 16 Gbps.

See the Example: ADC with DDC Option (Two ADCs Plus Two DDCs section for an example describing which JESD204B transport layer settings are valid for a given chip mode.

Table 33. JESD204B Output Configurations for N′ = 16[1]

No. of Virtual Converters Supported (Same Value as M)	JESD204B Serial Line Rate[2]	Supported Decimation Rates for Lane Rate = 1.7 Gbps to 3.4 Gbps	Supported Decimation Rates for Lane Rate = 3.4 Gbps to 6.8 Gbps	Supported Decimation Rates for Lane Rate = 6.8 Gbps to 13.5 Gbps	Supported Decimation Rates for Lane Rate = 13.5 Gbps to 15.5 Gbps	JESD204B Transport Layer Settings[3]								
						L	M	F	S	HD	N	N'	CS	K
1	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 20, 24	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1	1	2	1	0	8 to 16	16	0 to 3	See Note 4
1	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 20, 24	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1	1	4	2	0	8 to 16	16	0 to 3	See Note 4
1	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	1	1	1	1	8 to 16	16	0 to 3	See Note 4
1	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	1	2	2	0	8 to 16	16	0 to 3	See Note 4
1	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	1	1	2	1	8 to 16	16	0 to 3	See Note 4
1	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	1	2	4	0	8 to 16	16	0 to 3	See Note 4
1	2.5 × f_{OUT}	1, 2, 3, 4	1, 2	1		8	1	1	4	1	8 to 16	16	0 to 3	See Note 4
1	2.5 × f_{OUT}	1, 2, 3, 4	1, 2	1		8	1	2	8	0	8 to 16	16	0 to 3	See Note 4

No. of Virtual Converters Supported (Same Value as M)	JESD204B Serial Line Rate[2]	Supported Decimation Rates for Lane Rate = 1.7 Gbps to 3.4 Gbps	Supported Decimation Rates for Lane Rate = 3.4 Gbps to 6.8 Gbps	Supported Decimation Rates for Lane Rate = 6.8 Gbps to 13.5 Gbps	Supported Decimation Rates for Lane Rate = 13.5 Gbps to 15.5 Gbps	JESD204B Transport Layer Settings[3]								
						L	M	F	S	HD	N	N'	CS	K
2	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30, 40, 48	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1	2	4	1	0	8 to 16	16	0 to 3	See Note 4
2	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30, 40, 48	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1	2	8	2	0	8 to 16	16	0 to 3	See Note 4
2	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	2	2	2	1	0	8 to 16	16	0 to 3	See Note 4
2	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	2	2	4	2	0	8 to 16	16	0 to 3	See Note 4
2	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	4	2	1	1	1	8 to 16	16	0 to 3	See Note 4
2	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	4	2	2	2	0	8 to 16	16	0 to 3	See Note 4
2	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	8	2	1	2	1	8 to 16	16	0 to 3	See Note 4
2	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	8	2	2	4	0	8 to 16	16	0 to 3	See Note 4
4	80 × f_{OUT}	8, 16, 20, 24, 30, 40, 48	4, 8, 10, 12, 16, 20, 24, 30, 40, 48	2, 4, 6, 8, 10, 12, 16, 20, 24, 30	2, 4, 6, 8, 10, 12, 16	1	4	8	1	0	8 to 16	16	0 to 3	See Note 4
4	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30, 40, 48	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	2	4	4	1	0	8 to 16	16	0 to 3	See Note 4
4	40 × f_{OUT}	4, 8, 10, 12, 15, 16, 20, 24, 30, 40, 48	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	2	4	8	2	0	8 to 16	16	0 to 3	See Note 4
4	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	4	4	2	1	0	8 to 16	16	0 to 3	See Note 4
4	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	4	4	4	2	0	8 to 16	16	0 to 3	See Note 4
4	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	8	4	1	1	1	8 to 16	16	0 to 3	See Note 4
4	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	8	4	2	2	0	8 to 16	16	0 to 3	See Note 4
8	160 × f_{OUT}	16, 40, 48	8, 16, 20, 24, 40, 48	4, 8, 12, 16, 20, 24, 40, 48	4, 8, 12, 16, 20, 24	1	8	16	1	0	8 to 16	16	0 to 3	See Note 4
8	80 × f_{OUT}	8, 16, 20, 24, 40, 48	4, 8, 10, 12, 16, 20, 24, 40, 48	2, 4, 6, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2	8	8	1	0	8 to 16	16	0 to 3	See Note 4
8	40 × f_{OUT}	4, 8, 10, 12, 16, 20, 24, 40, 48	2, 4, 6, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	4	8	4	1	0	8 to 16	16	0 to 3	See Note 4
8	40 × f_{OUT}	4, 8, 10, 12, 16, 20, 24, 40, 48	2, 4, 6, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	4	8	8	2	0	8 to 16	16	0 to 3	See Note 4
8	20 × f_{OUT}	2, 4, 6, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	2, 4	8	8	2	1	0	8 to 16	16	0 to 3	See Note 4
8	20 × f_{OUT}	2, 4, 6, 8, 10, 12, 16, 20, 24	2, 4, 6, 8, 10, 12, 16	2, 4, 6, 8	2, 4	8	8	4	2	0	8 to 16	16	0 to 3	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[3] f_{ADC_CLK} is the ADC sample rate; DCM = chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 15.5 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 15500 Mbps and > 13500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Table 34. JESD204B Output Configurations (N' = 12) [1]

No. of Virtual Converters Supported (Same Value as M)	Serial Line Rate[2]	Supported Decimation Rates for Lane Rate = 1.7 Gbps to 3.4 Gbps	Supported Decimation Rates for Lane Rate = 3.4 Gbps to 6.8 Gbps	Supported Decimation Rates for Lane Rate = 6.8 Gbps to 13.5 Gbps	Supported Decimation Rates for Lane Rate = 13.5 Gbps to 15.5 Gbps	JESD204B Transport Layer Settings[3]								
						L	M	F	S	HD	N	N'	L	K
1	15 × f_{OUT}	3, 6, 12	3, 6, 12	3, 6		1	1	3	2	0	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	3, 6	3, 6	3		2	1	3	4	1	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	3, 6	3, 6	3		2	1	6	8	0	8 to 12	12	0 to 3	See Note 4
	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	3	1	1	2	1	8 to 12	12	0 to 3	See Note 4
2	30 × f_{OUT}	3, 6, 12, 24	3, 6, 12, 24	3, 6, 12		1	2	3	1	0	8 to 12	12	0 to 3	See Note 4
	15 × f_{OUT}	3, 6, 12	3, 6, 12	3, 6		2	2	3	2	0	8 to 12	12	0 to 3	See Note 4
	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	3	2	1	1	1	8 to 12	12	0 to 3	See Note 4
	7.5 × f_{OUT}	3, 6	3, 6	3		4	2	3	4	0	8 to 12	12	0 to 3	See Note 4
4	60 × f_{OUT}	6, 12, 24, 48	3, 6, 12, 24, 48	3, 6, 12, 24		1	4	6	1	0	8 to 12	12	0 to 3	See Note 4
	30 × f_{OUT}	3, 6, 12, 24	3, 6, 12, 24	3, 6, 12		2	4	3	1	0	8 to 12	12	0 to 3	See Note 4
	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 16, 20, 24	1, 2, 3, 4, 5, 6, 8, 10, 12, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	3	4	2	1	1	8 to 12	12	0 to 3	See Note 4
	15 × f_{OUT}	3, 6, 12	3, 6, 12	3, 6		4	4	3	2	0	8 to 12	12	0 to 3	See Note 4
8	60 × f_{OUT}	6, 12, 24, 48	6, 12, 24, 48	6, 12, 24		2	8	6	1	0	8 to 12	12	0 to 3	See Note 4
	30 × f_{OUT}	6, 12, 24	6, 12, 24	6, 12		4	8	3	1	0	8 to 12	12	0 to 3	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] f_{ADC_CLK} is the ADC sample rate; DCM is the chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 15.5 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 15500 Mbps and > 13500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[3] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Table 35. JESD204B Output Configurations for N′ = 8[1]

No. of Virtual Converters Supported (Same Value as M)	Serial Lane Rate[2]	Supported Decimation Rates for Lane Rate = 1.7 Gbps to 3.4 Gbps	Supported Decimation Rates for Lane Rate = 3.4 Gbps to 6.8 Gbps	Supported Decimation Rates for Lane Rate = 6.8 Gbps to 13.5 Gbps	Supported Decimation Rates for Lane Rate = 13.5 Gbps to 15.5 Gbps	JESD204B Transport Layer Settings[3]								
						L	M	F	S	HD	N	N'	CS	K
1	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	1	1	1	0	7 to 8	8	0 to 1	See Note 4
1	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	1	2	2	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	2	1	1	2	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	2	1	2	4	0	7 to 8	8	0 to 1	See Note 4
1	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	2	1	4	8	0	7 to 8	8	0 to 1	See Note 4
1	2.5 × f_{OUT}	1, 2, 3, 4	1, 2	1		4	1	1	4	0	7 to 8	8	0 to 1	See Note 4
1	2.5 × f_{OUT}	1, 2, 3, 4	1, 2	1		4	1	2	8	0	7 to 8	8	0 to 1	See Note 4
2	20 × f_{OUT}	2, 4, 5, 6, 8, 10, 12, 15, 16, 20, 24, 30	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1	2	2	1	0	7 to 8	8	0 to 1	See Note 4
2	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	2	1	1	0	7 to 8	8	0 to 1	See Note 4
2	10 × f_{OUT}	1, 2, 3, 4, 5, 6, 8, 10, 12, 15, 16	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	2	2	2	2	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	2	1	2	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	2	2	4	0	7 to 8	8	0 to 1	See Note 4
2	5 × f_{OUT}	1, 2, 3, 4, 5, 6, 8	1, 2, 3, 4	1, 2	1	4	2	4	8	0	7 to 8	8	0 to 1	See Note 4

[1] Due to the internal clock requirements, only certain decimation rates are supported for certain link parameters.

[2] f_{ADC_CLK} is the ADC sample rate; DCM is the chip decimation ratio; f_{OUT} is the output sample rate = f_{ADC_CLK}/DCM; SLR is the JESD204B serial lane rate. The following equations must be met due to internal clock divider requirements: SLR ≥ 1.6875 Gbps and SLR ≤ 15.5 Gbps; SLR/40 ≤ f_{ADC_CLK}; least common multiple (20 × DCM × f_{OUT}/SLR, DCM) ≤ 64. When the SLR is ≤ 15500 Mbps and > 13500 Mbps, Register 0x056E must be set to 0x30. When the SLR is ≤ 13500 Mbps and ≥ 6750 Mbps, Register 0x056E must be set to 0x00. When the SLR is < 6750 Mbps and ≥ 3375 Mbps, Register 0x056E must be set to 0x10. When the SLR is < 3375 Mbps and ≥ 1687.5 Mbps, Register 0x056E must be set to 0x50.

[3] JESD204B transport layer descriptions are as follows: L is the number of lanes per converter device (lanes per link); M is the number of virtual converters per converter device (virtual converters per link); F is the octets per frame; S is the samples transmitted per virtual converter per frame cycle; HD is the high density mode; N is the virtual converter resolution (in bits); N' is the total number of bits per sample (JESD204B word size); CS is the number of control bits per conversion sample; K is the number of frames per multiframe.

[4] Only valid K × F values that are divisible by 4 are supported: for F = 1, K = 20, 24, 28, 32; for F = 2, K = 12, 16, 20, 24, 28, 32; for F = 4, K = 8, 12, 16, 20, 24, 28, 32; for F = 8, K = 4, 8, 12, 16, 20, 24, 28, 32; and for F = 16, K = 4, 8, 12, 16, 20, 24, 28, 32.

Example: ADC with DDC Option (Two ADCs Plus Two DDCs)

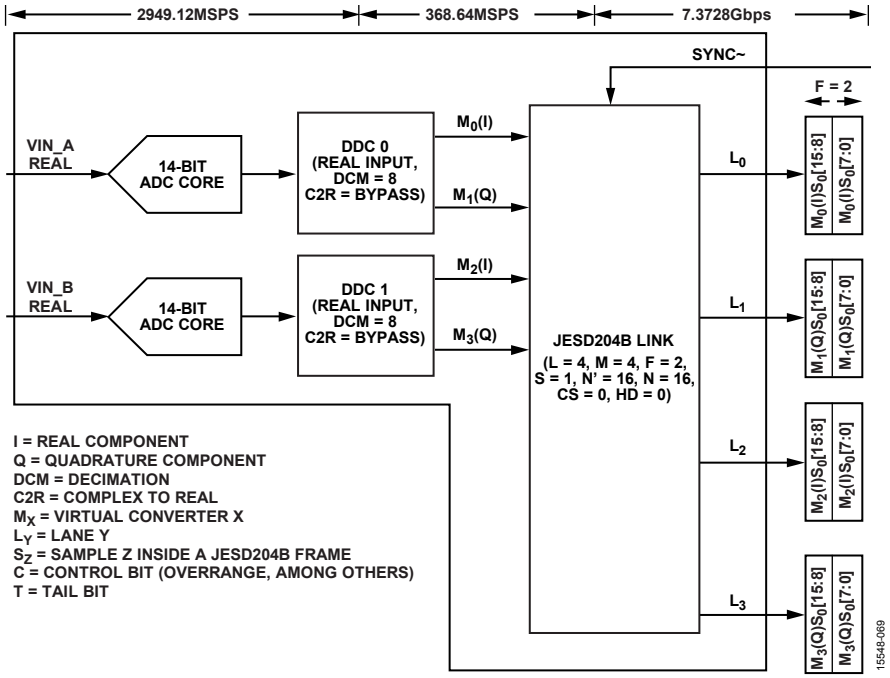


Figure 103. Two ADC Plus Two DDC Mode (L = 4, M = 4, F = 2, S = 1)

The AD6688 is set up as shown in Figure 103, with the following configuration:

- Two 14-bit converters at 2.94912 GSPS.
- Two DDC application layer mode with complex outputs (I/Q).
- Chip decimation ratio = 8.
- DDC decimation ratio = 8 (see Table 46).

The JESD204B output configuration is as follows:

- Virtual converters required = 4 (see Table 33).
- Output sample rate (f_{OUT}) = 2949.12/8 = 368.64 MSPS.

The JESD204B supported output configurations are as follows (see Table 33):

- N′ = 16 bits.
- N = 14 bits.
- L = 2, M = 4, and F = 4, or L = 4, M = 4, and F = 2.
- CS = 0.
- K = 32.
- Output serial lane rate = 14.7456 Gbps per lane (L = 2) or 7.3728 Gbps per lane (L = 4).

For L = 2, the PLL control register (Register 0x056E) must be set to 0x30. For L = 4, the PLL control register (Register 0x056E) must be set to 0x00.

This example shows the flexibility in the digital and lane configurations for the AD6688. The sample rate is 2.94912 GSPS; however, the outputs are all combined in either two or four lanes, depending on the input/output speed capability of the receiving device.

DETERMINISTIC LATENCY

Both ends of the JESD204B link contain various clock domains distributed throughout each system. Data traversing from one clock domain to a different clock domain can lead to ambiguous delays in the JESD204B link. These ambiguities lead to non-repeatable latencies across the link from one power cycle or link reset to the next. Section 6 of the JESD204B specification addresses the issue of deterministic latency with mechanisms defined as Subclass 1 and Subclass 2.

The AD6688 supports JESD204B Subclass 0 and Subclass 1 operation. Register 0x0590, Bit 5 sets the subclass mode for the AD6688 and its default is set for Subclass 1 operating mode (Register 0x0590, Bit 5 = 1). If deterministic latency is not a system requirement, Subclass 0 operation is recommended and the SYSREF signal may not be required. Even in Subclass 0 mode, the SYSREF signal may be required in an application where multiple AD6688 devices must be synchronized with each other. This topic is addressed in the Timestamp Mode section.

SUBCLASS 0 OPERATION

If there is no requirement for multichip synchronization while operating in Subclass 0 mode (Register 0x0590, Bit 5 = 0), the SYSREF input can be left disconnected. In this mode, the relationship of the JESD204B clocks between the JESD204B transmitter and receiver are arbitrary, but does not affect the ability of the receiver to capture and align the lanes within the link.

SUBCLASS 1 OPERATION

The JESD204B protocol organizes data samples into octets, frames, and multiframes as described in the Transport Layer section. The LMFC is synchronous with the beginnings of these multiframes. In Subclass 1 operation, the SYSREF is used to synchronize the LMFCs for each device in a link or across multiple links (within the AD6688, SYSREF also synchronizes the internal sample dividers), as shown in Figure 104. The JESD204B receiver uses the multiframe boundaries and buffering to achieve consistent latency across lanes (or even multiple devices), and also to achieve a fixed latency between power cycles and link reset conditions.

Deterministic Latency Requirements

Several key factors are required for achieving deterministic latency in a JESD204B Subclass 1 system.

- SYSREF± signal distribution skew within the system must be less than the desired uncertainty for the system.
- SYSREF± setup and hold time requirements must be met for each device in the system.
- The total latency variation across all lanes, links, and devices must be ≤1 LMFC periods (see Figure 104). This includes both variable delays and the variation in fixed delays from lane to lane, link to link, and device to device in the system.

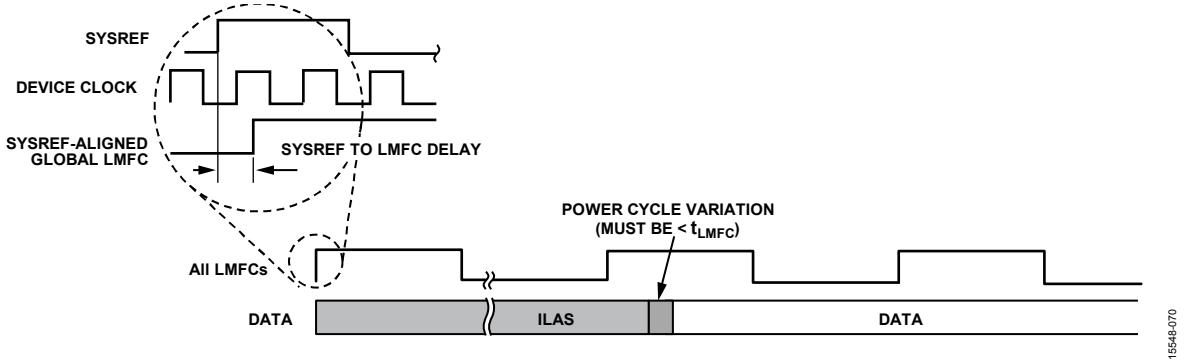


Figure 104. SYSREF and LMFC

Setting Deterministic Latency Registers

The JESD204B receiver in the logic device buffers data starting on the LMFC boundary. If the total link latency in the system is near an integer multiple of the LMFC period, it is possible that from one power cycle to the next, the data arrival time at the receive buffer may straddle an LMFC boundary. To ensure deterministic latency in this case, a phase adjustment of the LMFC at either the transmitter or receiver must be performed. Typically, adjustments to accommodate the receive buffer are made to the LMFC of the receiver. Alternatively, this adjustment can be made in the AD6688 using the LMFC offset register (Register 0x0578, Bits[4:0]). This delays the LMFC in frame clock increments, depending on the F parameter (number of octets per lane per frame). For F = 1, every fourth setting (0, 4, 8, and so on) is valid and results in a four frame clock shift. For F = 2, every other setting (0, 2, 4, and so on) is valid and results in a two frame clock shift. For all other values of F, each setting results in a one frame clock shift. Figure 105 shows that, when the link latency is near an LMFC boundary, the local LMFC of the AD6688 can be adjusted to delay the data arrival time at the receiver. Figure 106 shows how the LMFC of the receiver is delayed to accommodate the receive buffer timing. Consult the applicable JESD204B receiver user guide for details on making this adjustment. If the total latency in the system is not near an integer multiple of the LMFC period or if the appropriate adjustments have been made to the LMFC phase at the clock source, it is still possible to have variable latency from one power cycle to the next. By design, the AD6688 has circuitry in place to minimize this variation from power-up to power-up. In this case, the user must check for the possibility that the setup and hold time requirements for the SYSREF signal are not being met, by reading the SYSREF setup/hold monitor register (Register 0x0128). This function is fully described in the SYSREF± Setup/Hold Window Monitor section.

If reading Register 0x128 indicates that there may be a timing problem, there are a few adjustments that can made in the AD6688. Changing the SYSREF level that is used for alignment is possible using the SYSREF transition select bit (Register 0x0120, Bit 4). Also, changing which edge of CLK is used to capture the SYSREF signal can be done using the CLK edge select bit (Register 0x0120, Bit 3). Both of these options are described in the SYSREF Control Features section. If neither of these measures helps to achieve an acceptable setup and hold time, adjusting the phase of SYSREF and/or the device clock (CLK±) may be required.

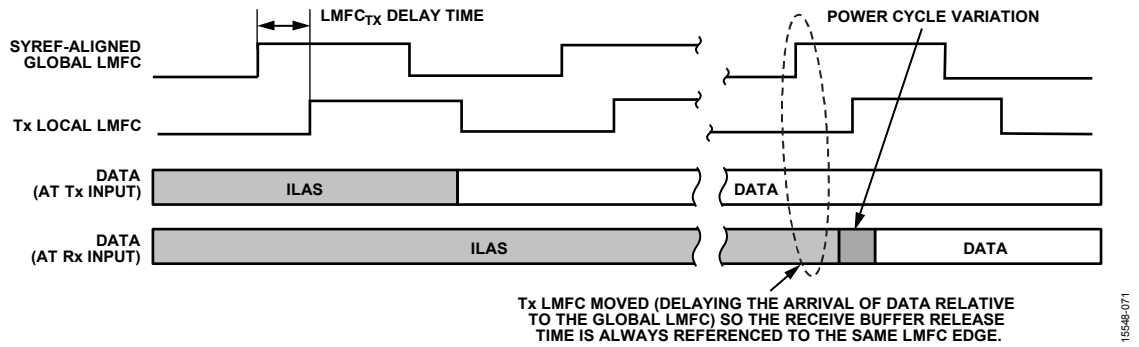


Figure 105. Adjusting the JESD204B Tx LMFC in the AD6688

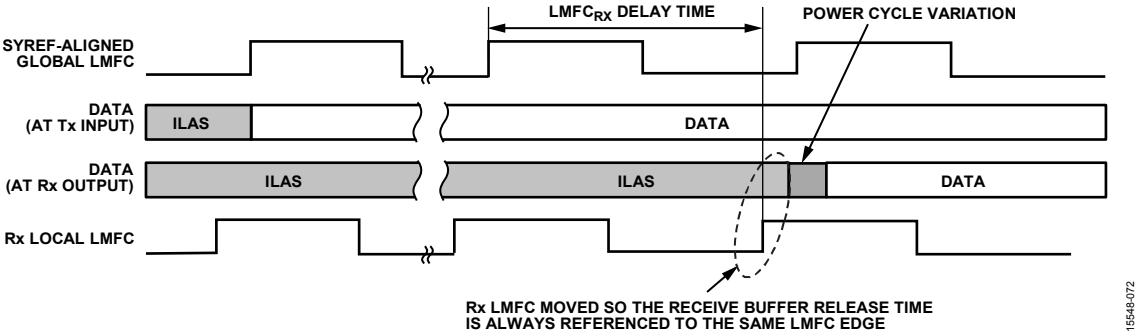


Figure 106. Adjusting the JESD204B Rx LMFC in the Logic Device

MULTICHIP SYNCHRONIZATION

The flowchart in Figure 108 shows the internal mechanism for multichip synchronization in the AD6688. There are two methods by which multichip synchronization can take place, as determined by the chip synchronization mode bit (Register 0x01FF, Bit 0). Each method involves different applications of the SYSREF signal.

NORMAL MODE

The default sate of the chip synchronization mode bit is 0, which configures the AD6688 for normal chip synchronization. The JESD204B standard specifies the use of SYSREF to provide for deterministic latency within a single link. This same concept, when applied to a system with multiple converters and logic devices can also provide multichip synchronization. In Figure 108, this is referred to as normal mode. Following the process in the flowchart ensures that the AD6688 is configured appropriately. The user must also consult the logic devices user IP guide to ensure that the JESD204B receivers are configured appropriately.

TIMESTAMP MODE

For all AD6688 full bandwidth operating modes, the SYSREF input can also be used to timestamp samples. This is another method by which multiple channels and multiple devices can achieve synchronization. This method is especially effective when synchronizing multiple devices to one or more logic devices. The logic devices buffer the data streams, identify the timestamped samples, and align them. When the chip synchronization mode bit (Register 0x01FF, Bit 0) is set to 1, the timestamp method is used for synchronization of multiple channels and/or devices. In this mode, SYSREF resets the sample dividers and the JESD204B clocking. When the chip sync mode is set to 1, the clocks are not reset; instead, the coinciding sample is timestamped using the JESD204B control bits of that sample. To operate in timestamp mode, these additional settings are necessary:

- Continuous or N-shot SYSREF must be enabled (Register 0x0120, Bits[2:1] = 1 or 2).
- At least one control bit must be enabled (Register 0x058F, Bits[7:6] = 1, 2, or 3).
- Set the function for one of the control bits to SYSREF:
  - Register 0x0559, Bits[2:0] = 5 if using Control Bit 0.
  - Register 0x0559, Bits[6:4] = 5 if using Control Bit 1.
  - Register 0x055A, Bits[2:0] = 5 if using Control Bit 2.

Figure 107 shows how the input sample coincident with SYSREF is timestamped and ultimately output from the ADC. In this example, there are two control bits, and Control Bit 0 is the bit indicating which sample was coincident with the SYSREF rising edge. Note that the pipeline latencies for each channel are identical. If so desired, the SYSREF timestamp delay register (Register 0x0123) can be used to adjust the timing of which sample is time stamped.

Note that time stamping is not supported by any AD6688 operating modes that use decimation.

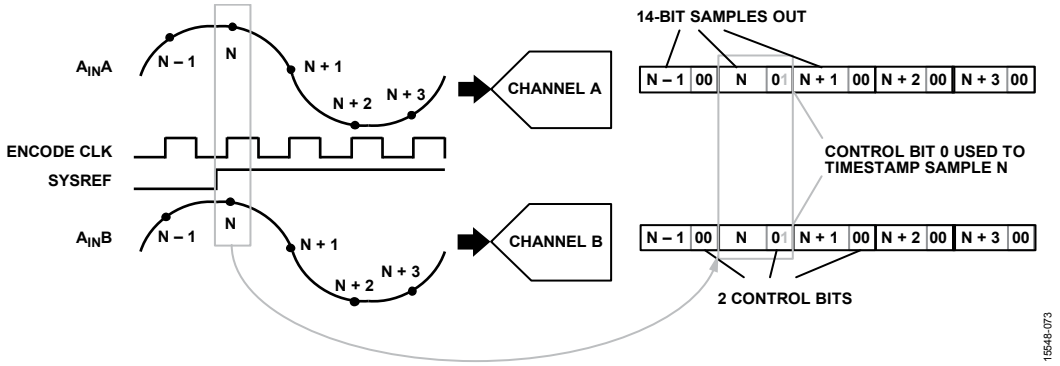


Figure 107. AD6688 Timestamping Example—CS = 2 (Register 0x058F, Bits[7:6] = 2), Control Bit 0 is SYSREF (Register 0x0559, Bits[2:0] = 5)

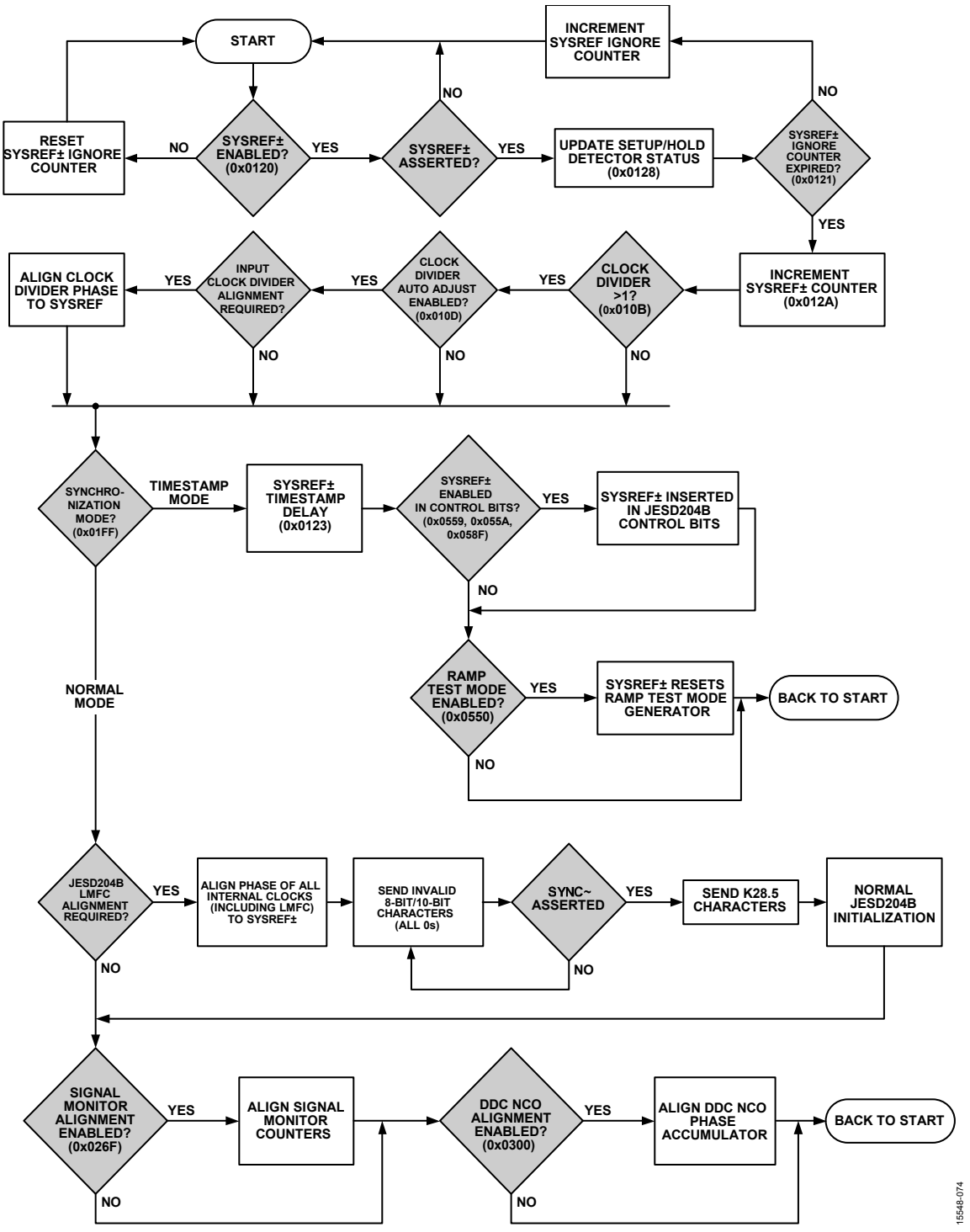


Figure 108. SYSREF Capture Scenarios and Multichip Synchronization

SYSREF INPUT

The SYSREF input signal is used as a high accuracy system reference for deterministic latency and multichip synchronization. The AD6688 accepts a single-shot or periodic input signal. The SYSREF mode select bits (Register 0x0120, Bits[2:1]) select the input signal type and also arm the SYSREF state machine when set. If in single (or N) shot mode (Register 0x0120, Bits[2:1] = 2), the SYSREF mode select bit self clears after the appropriate SYSREF transition is detected. The pulse width must have a minimum width of two CLK± periods. If the clock divider (Register 0x010B, Bits[3:0]) is set to a value other than divide by 1, multiply this minimum pulse width requirement by the divide ratio (that is, if set to divide by 8, the minimum pulse

width is 16 CLK± cycles). When using a continuous SYSREF signal (Register 0x0120, Bits[2:1] = 1), the period of the SYSREF signal must be an integer multiple of the LMFC. Derive LMFC using the following formula:

$$LMFC = ADC\ clock/(S \times K)$$

where:
S is the JESD204B parameter for number of samples per converter.
K is the number of frames per multiframe.

The input clock divider, DDCs, signal monitor block, and JESD204B link are all synchronized using the SYSREF± input when in normal synchronization mode (Register 0x01FF, Bits 0 = 0). The SYSREF± input can also be used to timestamp an ADC sample to provide a mechanism for synchronizing multiple AD6688 devices in a system. For the highest level of timing accuracy, SYSREF± must meet setup and hold requirements relative to the CLK± input. There are several features in the AD6688 that can be used to ensure these requirements are met; these features are described in the SYSREF Control Features section.

SYSREF Control Features

SYSREF is used, along with the input clock (CLK), as part of a source-synchronous timing interface and requires setup and hold timing requirements of −65 ps and 95 ps relative to the input clock (see Figure 109). The AD6688 has several features that aid users in meeting these requirements. First, the SYSREF sample event can be defined as either a synchronous low to high transition or synchronous high to low transition. Second, the AD6688 allows the SYSREF signal to be sampled using either the rising edge or falling edge of the input clock. Figure 109, Figure 110, Figure 111, and Figure 112 show all four possible combinations.

The third SYSREF related feature available is the ability to ignore a programmable number (up to 16) of SYSREF events. The AD6688 is able to ignore N SYSREF events (note that the SYSREF ignore feature is enabled by setting the SYSREF mode register (Register 0x0120, Bits[2:1]) to 2'b10, which is labeled as N-shot mode. This feature is useful for handling periodic SYSREF signals, which need time to settle after startup. Ignoring SYSREF until the clocks in the system have settled can avoid an inaccurate SYSREF trigger. Figure 113 shows an example of the SYSREF ignore feature when ignoring three SYSREF events.

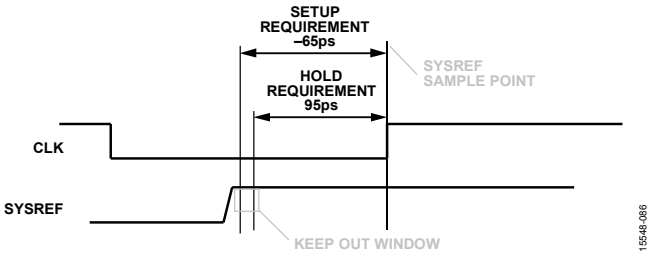


Figure 109. SYSREF Setup and Hold Time Requirements—SYSREF Low to High Transition Using Rising Edge Clock (Default)

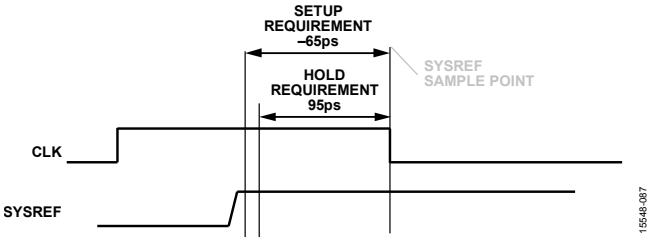


Figure 110. SYSREF Low to High Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1'b0; Register 0x0120, Bit 3 = 1'b1)

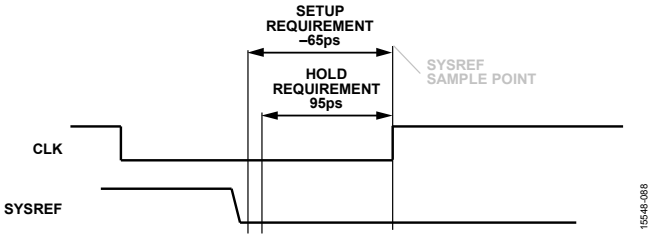


Figure 111. SYSREF High to Low Transition Using Rising Edge Clock Capture (Register 0x0120, Bit 4 = 1'b1; Register 0x0120, Bit 3 = 1'b0)

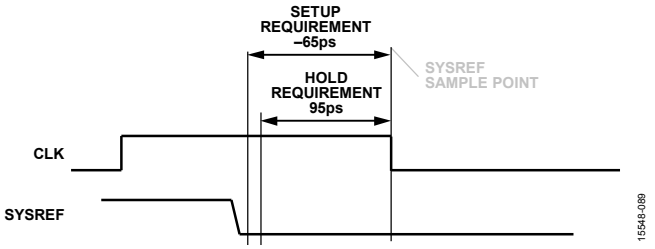


Figure 112. SYSREF High to Low Transition Using Falling Edge Clock Capture (Register 0x0120, Bit 4 = 1'b1; Register 0x0120, Bit 3 = 1'b1)

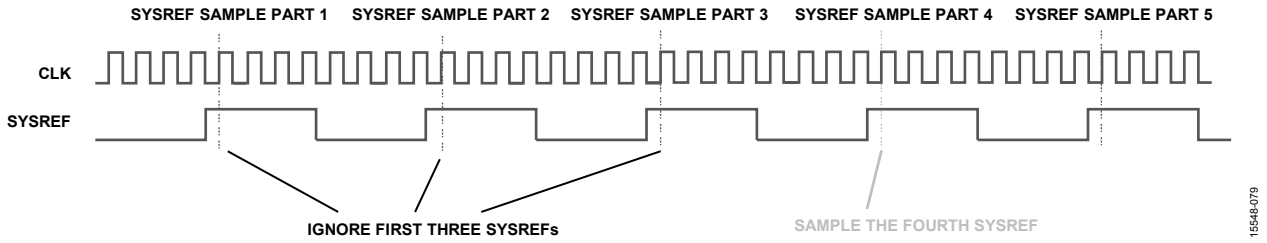


Figure 113. SYSREF Ignore Example (SYSREF Ignore Count, Register 0x0121, Bits[3:0] = 3)

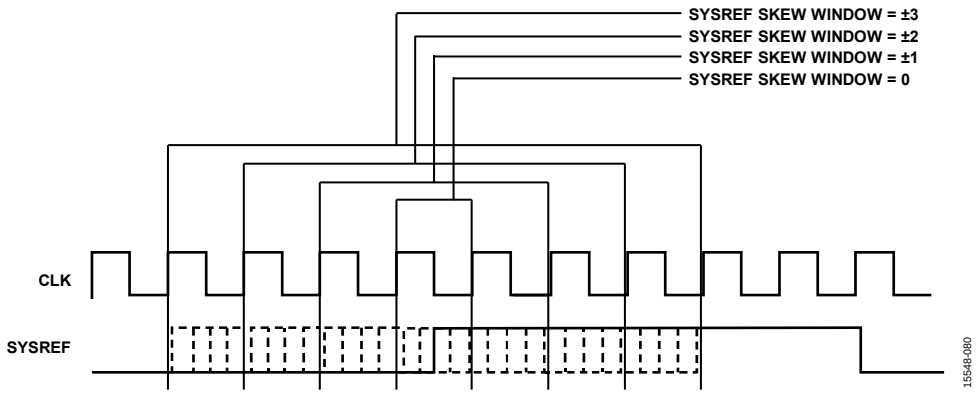


Figure 114. SYSREF Skew Window

When in continuous SYSREF mode (Register 0x0120, Bits[2:1] = 1), the AD6688 monitors the placement of the SYSREF leading edge compared to the internal LMFC. If the SYSREF is captured with a clock edge other than the one that is aligned with LMFC, the AD6688 initiates a resynchronization of the link. Because input clock rates for AD6688 can be up to 4 GHz, the AD6688 provides another SYSREF related feature that makes it possible to accommodate periodic SYSREF signals where cycle accurate capture is not feasible or not required. For these scenarios, the AD6688 has a programmable SYSREF skew window that allows the internal dividers to remain undisturbed unless SYSREF occurs outside the skew window. The resolution of the SYSREF skew window is set in sample clock cycles. If the SYSREF negative skew window is 1 and the positive skew window is 1, the total skew window is ±1 sample clock cycles, meaning that, as long as SYSREF is captured within ±1 sample clock cycle of the clock that is aligned with LMFC, the link continues to operate normally. If the SYSREF has jitter, which can cause a misalignment between SYSREF and LMFC, this feature allows the system to continue running without a resynchronization, while still allowing the device to monitor for larger errors not caused by jitter. For the AD6688, the positive and negative skew window is controlled by the SYSREF window negative register (Register 0x0122, Bits[3:2]) and SYSREF window positive register (Register 0x0122, Bits[1:0]). Figure 114 shows information on the location of the skew window settings relative to Phase 0 of the internal dividers. Negative skew is defined as occurring before the internal dividers reach Phase 0, and positive skew is defined after the internal dividers reach Phase 0.

SYSREF± SETUP/HOLD WINDOW MONITOR

To ensure a valid SYSREF signal capture, the AD6688 has a SYSREF± setup/hold window monitor. This feature allows the system designer to determine the location of the SYSREF± signals relative to the CLK± signals by reading back the amount of setup/hold margin on the interface through the memory map. Figure 115 and Figure 116 show the setup and hold status values for different phases of SYSREF±. The setup detector returns the status of the SYSREF± signal before the CLK± edge, and the hold detector returns the status of the SYSREF signal after the CLK± edge. Register 0x0128 stores the status of SYSREF± and notifies the user if the SYSREF± signal is captured by the ADC.

Table 36 shows the description of the contents of Register 0x0128 and how to interpret them.

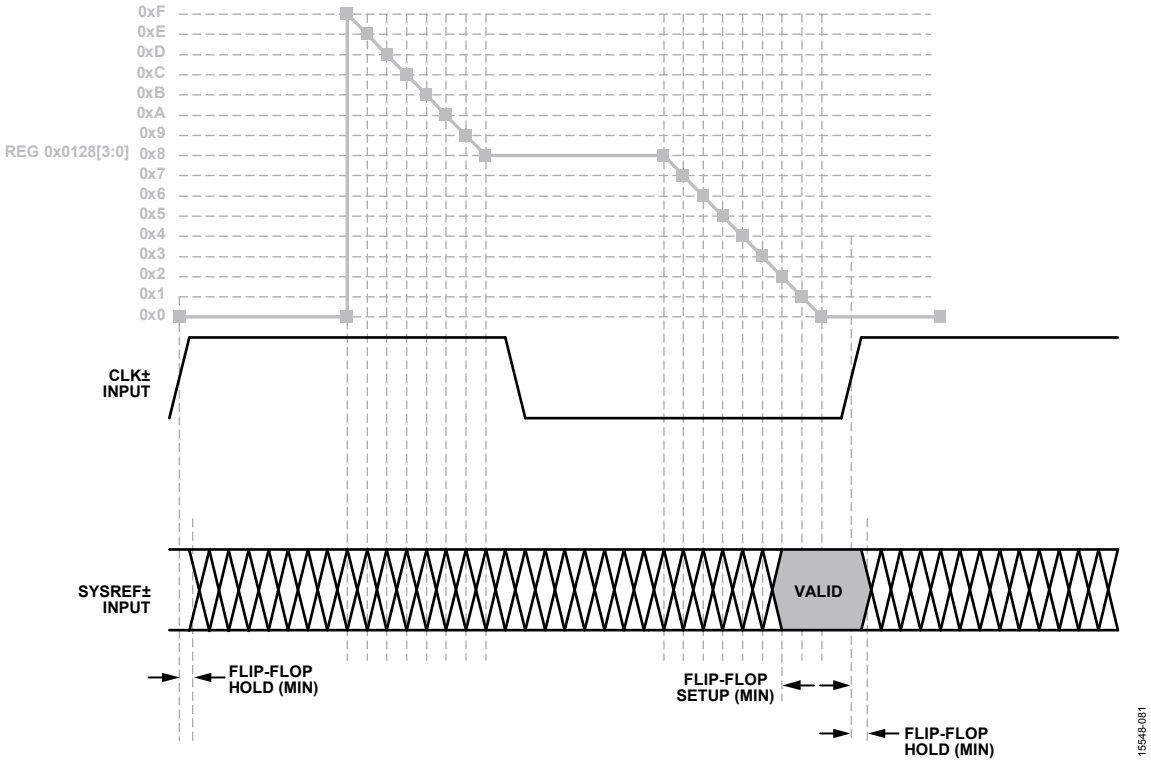


Figure 115. SYSREF± Setup Detector

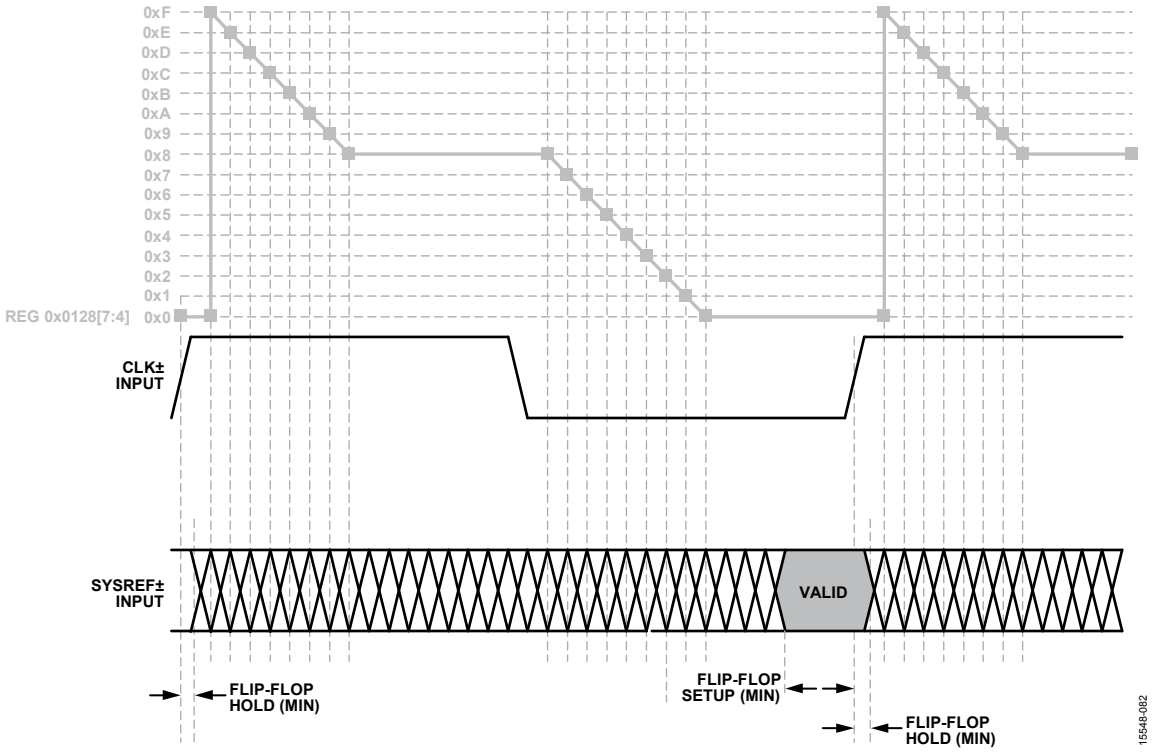


Figure 116. SYSREF± Hold Detector

Table 36. SYSREF± Setup/Hold Monitor, Register 0x0128

Register 0x0128, Bits[7:4] Hold Status	Register 0x0128, Bits[3:0] Setup Status	Description
0x0	0x0 to 0x7	Possible setup error. The smaller this number, the smaller the setup margin.
0x0 to 0x8	0x8	No setup or hold error (best hold margin).
0x8	0x9 to 0xF	No setup or hold error (best setup and hold margin).
0x8	0x0	No setup or hold error (best setup margin).
0x9 to 0xF	0x0	Possible hold error. The larger this number, the smaller the hold margin.
0x0	0x0	Possible setup or hold error.

LATENCY

END TO END TOTAL LATENCY

Total latency in the AD6688 is dependent on the chip application mode and the JESD204B configuration. For any given combination of these parameters, the latency is deterministic; however, the value of this deterministic latency must be calculated as described in the Example Latency Calculations section.

Table 37 shows the combined latency through the ADC and DSP for the different chip application modes supported by the AD6688. Table 38 shows the latency through the JESD204B block for each application mode based on the M/L ratio. For both tables, latency is typical and is in units of the encode clock. The latency through the JESD204B block does not depend on the output data type (real or complex). Therefore, data type is not included in Table 38.

To determine the total latency, select the appropriate ADC + DSP latency from Table 37 and add it to the appropriate JESD204B latency from Table 38. Example calculations are provided in the following section.

EXAMPLE LATENCY CALCULATIONS

Example Configuration 1 is as follows:

- ADC application mode = full bandwidth
- Real outputs
- L = 8, M = 2, F = 1, S = 2 (JESD204B mode)
- 20 × (M/L) = 5
- Latency = 31 + 44 = 75 encode clocks

Example Configuration 2 is as follows:

- ADC application mode = DCM4
- Complex outputs
- L = 4, M = 2, F = 1, S = 1 (JESD204B mode)
- 20 × (M/L) = 10
- Latency = 162 + 88 = 250 encode clocks

LMFC-REFERENCED LATENCY

Some FPGA vendors may require the end user to know LMFC-referenced latency to make appropriate deterministic latency adjustments. If they are required, the latency values in Table 37 and Table 38 can be used for the analog in to LMFC and LMFC to data out latency values.

Table 37. Latency Through the ADC + DSP Blocks (Number of Sample Clocks)[1]

Chip Application Mode	Enabled Filters	ADC + DSP Latency
Full Bandwidth	Not applicable	31
DCM1 (Real)	HB1	90
DCM2 (Complex)	HB1	90
DCM3 (Complex)	TB1	102
DCM2 (Real)	HB2 + HB1	162
DCM4 (Complex)	HB2 + HB1	162
DCM3 (Real)	TB2 + HB1	212
DCM6 (Complex)	TB2 + HB1	212
DCM4 (Real)	HB3 +HB2 + HB1	292
DCM8 (Complex)	HB3 +HB2 + HB1	292
DCM5 (Real)	FB2 + HB1	380
DCM10 (Complex)	FB2 + HB1	380
DCM6 (Real)	TB2 + HB2 + HB1	424
DCM12 (Complex)	TB2 + HB2 + HB1	424
DCM15 (Real)	FB2 + TB1	500
DCM8 (Real)	HB4 + HB3 + HB2 + HB1	552
DCM16 (Complex)	HB4 + HB3 + HB2 + HB1	552
DCM10 (Real)	FB2 + HB2 + HB1	694
DCM20 (Complex)	FB2 + HB2 + HB1	694
DCM12 (Real)	TB2 + HB3 + HB2 + HB1	814
DCM24 (Complex)	TB2 + HB3 + HB2 + HB1	814
DCM30 (Complex)	HB2 + FB2 + TB1	836
DCM20 (Real)	FB2 + HB3 + HB2 + HB1	1420
DCM40 (Complex)	FB2 + HB3 + HB2 + HB1	1420
DCM24 (Real)	TB2 + HB4 + HB3 + HB2 + HB1	1594
DCM48 (Complex)	TB2 + HB4 + HB3 + HB2 + HB1	1594

[1] DCMx indicates the decimation ratio.

Table 38. Latency Through JESD204B Block (Number of Sample Clocks)[1]

Chip Application Mode	M/L Ratio[2]						
	0.125	0.25	0.5	1	2	4	8
Full Bandwidth	82	44	25	14	7	9	3
DCM1	82	44	25	14	7	N/A	N/A
DCM2	160	84	46	27	14	7	N/A
DCM3	237	124	67	39	21	11	N/A
DCM4	315	164	88	50	27	14	9
DCM5	N/A	203[3]	109[3]	62[3]	43[3]	N/A	N/A
DCM6	N/A	243	130	73	39	21	14
DCM8	N/A	323	172	96	50	27	18
DCM10	N/A	N/A	213	119	62	33	22
DCM12	N/A	N/A	255	142	73	39	27
DCM15	N/A	N/A	318[4]	176[4]	90[4]	47[4]	33[4]
DCM16	N/A	N/A	339[4]	188[4]	96[4]	50[4]	35[4]
DCM20	N/A	N/A	N/A	233	119	62	43
DCM24	N/A	N/A	N/A	279	142	73	51
DCM30	N/A	N/A	N/A	348[4]	176[4]	90[4]	62[4]
DCM40	N/A	N/A	N/A	N/A	233[4]	119[4]	82[4]
DCM48	N/A	N/A	N/A	N/A	279[4]	142[4]	97[4]

[1] N/A indicates that the application mode is not supported at the M/L ratio listed.
[2] M/L ratio is the number of converters divided by the number of lanes for the configuration.
[3] The application mode at the M/L ratio listed is only supported in real output mode.
[4] The application mode at the M/L ratio listed is only supported in in complex output mode.

TEST MODES

ADC TEST MODES

The AD6688 has various test options that aid in the system level implementation. The AD6688 has ADC test modes that are available in Register 0x0550. These test modes are described in Table 39. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks, and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The pseudorandom number (PN) generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0550. These tests can be performed with or without an analog signal (if present, the analog signal is ignored); however, they do require an encode clock.

If the application mode is set to select a DDC mode of operation, the test modes must be enabled for each DDC enabled. The test patterns can be enabled via Bit 2 and Bit 0 of Register 0x0327, Register 0x0347, and Register 0x0367, depending on which DDC(s) are selected. The (I) data uses the test patterns selected for Channel A, and the (Q) data uses the test patterns selected for Channel B. For DDC3 only, the (I) data uses the test patterns from Channel A, and the (Q) data does not output test patterns. Bit 0 of Register 0x0387 selects the Channel A test patterns to be used for the (I) data. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 39. ADC Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default/ Seed Value	Sample (N, N + 1, N + 2, …)
0000	Off (default)	Not applicable	Not applicable	Not applicable
0001	Midscale short	0000 0000 0000	Not applicable	Not applicable
0010	Positive full-scale short	01 1111 1111 1111	Not applicable	Not applicable
0011	Negative full-scale short	10 0000 0000 0000	Not applicable	Not applicable
0100	Checkerboard	10 1010 1010 1010	Not applicable	0x1555, 0x2AAA, 0x1555, 0x2AAA, 0x1555
0101	PN sequence long	$x^{23} + x^{18} + 1$	0x3AFF	0x3FD7, 0x0002, 0x26E0, 0x0A3D, 0x1CA6
0110	PN sequence short	$x^9 + x^5 + 1$	0x0092	0x125B, 0x3C9A, 0x2660, 0x0c65, 0x0697
0111	One-/zero-word toggle	11 1111 1111 1111	Not applicable	0x0000, 0x3FFF, 0x0000, 0x3FFF, 0x0000
1000	User input	Register 0x551 to Register 0x558	Not applicable	User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], User Pattern 1[15:2] … for repeat mode. User Pattern 1[15:2], User Pattern 2[15:2], User Pattern 3[15:2], User Pattern 4[15:2], 0x0000 … for single mode.
1111	Ramp Output	(x) % 2^{14}	Not applicable	(x) % 2^{14}, (x +1) % 2^{14}, (x +2) % 2^{14}, (x +3) % 2^{14}

JESD204B BLOCK TEST MODES

In addition to the ADC pipeline test modes, the AD6688 also has flexible test modes in the JESD204B block. These test modes are listed in Register 0x0573 and Register 0x0574. These test patterns can be injected at various points along the output datapath. These test injection points are shown in Figure 94. Table 40 describes the various test modes available in the JESD204B block. For the AD6688, a transition from test modes (Register 0x0573 ≠ 0x00) to normal mode (Register 0x0573 = 0x00) requires an SPI soft reset. This is done by writing 0x81 to Register 0x0000 (self cleared).

Transport Layer Sample Test Mode

The transport layer samples are implemented in the AD6688 as defined by Section 5.1.6.3 in the JEDEC JESD204B specification. These tests are shown in Register 0x0571, Bit 5. The test pattern is equivalent to the raw samples from the ADC.

Interface Test Modes

The interface test modes are described in Register 0x0573, Bits[3:0]. These test modes are also explained in Table 40. The interface tests can be injected at various points along the data. See Figure 94 for more information on the test injection points. Register 0x0573, Bits[5:4] show where these tests are injected.

Table 41, Table 42, and Table 43 show examples of some of the test modes when injected at the JESD204B sample input, PHY 10-bit input, and scrambler 8-bit input. UPx in the tables represent the user pattern control bits from the user register map.

Table 40. JESD204B Interface Test Modes

Output Test Mode Bit Sequence	Pattern Name	Expression	Default
0000	Off (default)	Not applicable	Not applicable
0001	Alternating checker board	0x5555, 0xAAAA, 0x5555, …	Not applicable
0010	1/0 word toggle	0x0000, 0xFFFF, 0x0000, …	Not applicable
0011	31-bit PN sequence	$x^{31} + x^{28} + 1$	0x0003AFFF
0100	23-bit PN sequence	$x^{23} + x^{18} + 1$	0x003AFF
0101	15-bit PN sequence	$x^{15} + x^{14} + 1$	0x03AF
0110	9-bit PN sequence	$x^{9} + x^{5} + 1$	0x092
0111	7-bit PN sequence	$x^{7} + x^{6} + 1$	0x07
1000	Ramp output	$(x) \% 2^{16}$	Ramp size depends on test injection point
1110	Continuous/repeat user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then repeat
1111	Single user test	Register 0x551 to Register 0x558	User Pattern 1 to User Pattern 4, then zeros

Table 41. JESD204B Sample Input for M = 2, S = 2, N' = 16 (Register 0x0573[5:4] = 'b00)

Frame Number	Converter Number	Sample Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	0	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	0	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
0	1	1	0x5555	0x0000	$(x) \% 2^{16}$	0x496F	0xFF5C	UP1[15:0]	UP1[15:0]
1	0	0	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	0	1	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	0	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
1	1	1	0xAAAA	0xFFFF	$(x+1) \% 2^{16}$	0xC9A9	0x0029	UP2[15:0]	UP2[15:0]
2	0	0	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	0	1	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	0	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
2	1	1	0x5555	0x0000	$(x+2) \% 2^{16}$	0x980C	0xB80A	UP3[15:0]	UP3[15:0]
3	0	0	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	0	1	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	0	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
3	1	1	0xAAAA	0xFFFF	$(x+3) \% 2^{16}$	0x651A	0x3D72	UP4[15:0]	UP4[15:0]
4	0	0	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	0	1	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	0	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000
4	1	1	0x5555	0x0000	$(x+4) \% 2^{16}$	0x5FD1	0x9B26	UP1[15:0]	0x0000

Table 42. Physical Layer 10-Bit Input (Register 0x0573, Bits[5:4] = 'b01)

10-Bit Symbol Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x155	0x000	(x) % 2^{10}	0x125	0x3FD	UP1[15:6]	UP1[15:6]
1	0x2AA	0x3FF	(x + 1) % 2^{10}	0x2FC	0x1C0	UP2[15:6]	UP2[15:6]
2	0x155	0x000	(x + 2) % 2^{10}	0x26A	0x00A	UP3[15:6]	UP3[15:6]
3	0x2AA	0x3FF	(x + 3) % 2^{10}	0x198	0x1B8	UP4[15:6]	UP4[15:6]
4	0x155	0x000	(x + 4) % 2^{10}	0x031	0x028	UP1[15:6]	0x000
5	0x2AA	0x3FF	(x + 5) % 2^{10}	0x251	0x3D7	UP2[15:6]	0x000
6	0x155	0x000	(x + 6) % 2^{10}	0x297	0x0A6	UP3[15:6]	0x000
7	0x2AA	0x3FF	(x + 7) % 2^{10}	0x3D1	0x326	UP4[15:6]	0x000
8	0x155	0x000	(x + 8) % 2^{10}	0x18E	0x10F	UP1[15:6]	0x000
9	0x2AA	0x3FF	(x + 9) % 2^{10}	0x2CB	0x3FD	UP2[15:6]	0x000
10	0x155	0x000	(x + 10) % 2^{10}	0x0F1	0x31E	UP3[15:6]	0x000
11	0x2AA	0x3FF	(x + 11) % 2^{10}	0x3DD	0x008	UP4[15:6]	0x000

Table 43. Scrambler 8-Bit Input (Register 0x0573, Bits[5:4] = 'b10)

8-Bit Octet Number	Alternating Checkerboard	1/0 Word Toggle	Ramp	PN9	PN23	User Repeat	User Single
0	0x55	0x00	(x) % 2^{8}	0x49	0xFF	UP1[15:9]	UP1[15:9]
1	0xAA	0xFF	(x + 1) % 2^{8}	0x6F	0x5C	UP2[15:9]	UP2[15:9]
2	0x55	0x00	(x + 2) % 2^{8}	0xC9	0x00	UP3[15:9]	UP3[15:9]
3	0xAA	0xFF	(x + 3) % 2^{8}	0xA9	0x29	UP4[15:9]	UP4[15:9]
4	0x55	0x00	(x + 4) % 2^{8}	0x98	0xB8	UP1[15:9]	0x00
5	0xAA	0xFF	(x + 5) % 2^{8}	0x0C	0x0A	UP2[15:9]	0x00
6	0x55	0x00	(x + 6) % 2^{8}	0x65	0x3D	UP3[15:9]	0x00
7	0xAA	0xFF	(x + 7) % 2^{8}	0x1A	0x72	UP4[15:9]	0x00
8	0x55	0x00	(x + 8) % 2^{8}	0x5F	0x9B	UP1[15:9]	0x00
9	0xAA	0xFF	(x + 9) % 2^{8}	0xD1	0x26	UP2[15:9]	0x00
10	0x55	0x00	(x + 10) % 2^{8}	0x63	0x43	UP3[15:9]	0x00
11	0xAA	0xFF	(x + 11) % 2^{8}	0xAC	0xFF	UP4[15:9]	0x00

Data Link Layer Test Modes

The data link layer test modes are implemented in the AD6688 as defined by Section 5.3.3.8.2 in the JEDEC JESD204B specification. These tests are shown in Register 0x0574, Bits[2:0]. Test patterns inserted at this point are useful for verifying the functionality of the data link layer. When the data link layer test modes are enabled, disable SYNCINB± by writing 0xC0 to Register 0x0572.

SERIAL PORT INTERFACE

The AD6688 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the Serial Control Interface Standard (Rev. 1.0).

CONFIGURATION USING THE SPI

Three pins define the SPI of the AD6688 ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 44). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 44. Serial Port Interface Pins

Pin	Function
SCLK	Serial clock. The serial shift clock input that is used to synchronize serial interface, reads, and writes.
SDIO	Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip select bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 3 and Table 5.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued, which allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the Serial Control Interface Standard (Rev. 1.0).

HARDWARE INTERFACE

The pins described in Table 44 comprise the physical interface between the user programming device and the serial port of the. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD6688 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 45 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the Serial Control Interface Standard (Rev. 1.0). The AD6688 device-specific features are described in the Memory Map section.

Table 45. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode.
Clock	Allows the user to access the clock divider via the SPI.
DDC	Allows the user to set up decimation filters for different applications.
Test Input/Output	Allows the user to set test modes to have known data on output bits.
Output Mode	Allows the user to set up outputs.
SERDES Output Setup	Allows the user to vary SERDES settings such as swing and emphasis.

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each address in the memory map register table has eight bit locations. The memory map is divided into the following sections:

- Analog Devices, Inc., SPI registers (Register 0x0000 to Register 0x000F)
- Clock/SYSREF/chip power-down pin control registers (Register 0x003F to Register 0x01FF)
- Chip operating mode control registers (Register 0x0200 to Register 0x0201)
- Fast detect and signal monitor control registers (Register 0x0245 to Register 0x027A)
- DDC function registers (Register 0x0300 to Register 0x03CD)
- Digital outputs and test modes registers (Register 0x0550 to Register 0x05CB and Register 0x1222 to Register 0x1262)
- Programmable filter control and coefficients registers (Register 0x0DF8 to Register 0x0F7F)
- VREF/analog input control registers (Register 0x0701 and Register 0x18A6 to Register 0x1A4D)

Table 46 (see the Memory Map Register Details section) documents the default hexadecimal value for each hexadecimal address shown. For example, Address 0x0561, the output sample mode register, has a hexadecimal default value of 0x01, which means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see Table 46.

Open and Reserved Locations

All address and bit locations that are not included in Table 46 are not currently supported for this device. Write unused bits of a valid address location with zeros unless the default value is set otherwise. Writing to these locations is required only when part of an address location is unassigned (for example, Bits[7:3] of Address 0x0561). If the entire address location is open (for example, Address 0x0013), do not write to this address location.

Default Values

After the AD6688 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 46.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."
- X denotes a don't care bit.

Channel-Specific Registers

Some channel setup functions, such as the Buffer Control 1 register (Register 0x1A4C), can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 46 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x0008. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, set only Channel A or Channel B to read one of the two registers. If both bits are set during an SPI read cycle, the device returns the value for Channel A. All other registers and bits are considered global, and changes to these registers and bits affect the entire device and the channel features for which independent settings are not allowed between channels. The settings in Register 0x0200 do not affect the global registers and bits.

SPI Soft Reset

After issuing a soft reset by programming 0x81 to Register 0x0000, the AD6688 requires 5 ms to recover. When programming the AD6688 for application setup, ensure that an adequate delay is programmed into the firmware after asserting the soft reset and before starting the device setup.

MEMORY MAP REGISTER DETAILS

All address locations that are not included in Table 46 to Table 53 are not currently supported for this device and must not be written.

Analog Devices SPI Registers

Table 46.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0000	SPI Configuration A	7	Soft reset mirror (self clearing)		Whenever a soft reset is issued, the user must wait 5 ms before writing to any other register. This provides sufficient time for the boot loader to complete.	0x0	R/WC
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
		6	LSB first mirror			0x0	R/W
				1	Least significant bit shifted first for all SPI operations.		
				0	Most significant bit shifted first for all SPI operations.		
		5	Address ascension mirror			0x0	R/W
				0	Multibyte SPI operations cause addresses to auto-decrement.		
				1	Multibyte SPI operations cause addresses to auto-increment.		
		[4:3]	Reserved		Reserved.	0x0	R
		2	Address ascension			0x0	R/W
				0	Multibyte SPI operations cause addresses to auto-decrement.		
				1	Multibyte SPI operations cause addresses to auto-increment.		
		1	LSB first			0x0	R/W
				1	Least significant bit shifted first for all SPI operations.		
				0	Most significant bit shifted first for all SPI operations.		
		0	Soft reset (self clearing)		Whenever a soft reset is issued, the user must wait 5 ms before writing to any other register. This provides sufficient time for the boot loader to complete.	0x0	R/WC
				0	Do nothing.		
				1	Reset the SPI and registers (self clearing).		
0x0001	SPI Configuration B	[7:2]	Reserved		Reserved.	0x0	R
		1	Datapath soft reset (self clearing)			0x0	R/WC
				0	Normal operation.		
				1	Datapath soft reset (self clearing).		
		0	Reserved		Reserved.	0x0	R
0x0002	Chip configuration (local)	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Channel power mode		Channel power modes.	0x0	R/W
				00	Normal mode (power-up).		
				10	Standby mode; digital datapath clocks disabled; JESD204B interface enabled.		
				11	Power-down mode; digital datapath clocks disabled; digital datapath held in reset; JESD204B interface disabled.		
0x0003	Chip type	[7:0]	Chip type		Chip type.	0x03	R
				0x3	High speed ADC.		
0x0004	Chip ID LSB	[7:0]	Chip ID LSB[7:0]		Chip ID.	0xE2	R
				0xE1	AD6688		
0x0005	Chip ID MSB	[7:0]	Chip ID MSB[15:8]		Chip ID.	0x0	R
0x0006	Chip grade	[7:4]	Chip speed grade	0x0	Chip speed grade.	0x0	R
		[3:0]	Reserved		Reserved.	0x0	R
0x0008	Device index	[7:2]	Reserved		Reserved.	0x0	R
		1	Channel B			0x1	R/W
				0	ADC Core B does not receive the next SPI command.		
				1	ADC Core B receives the next SPI command.		
		0	Channel A			0x1	R/W
				0	ADC Core A does not receive the next SPI command.		
				1	ADC Core A receives the next SPI command.		
0x000A	Scratch pad	[7:0]	Scratch pad		Chip scratch pad register. This register is used to provide a consistent memory location for software debug.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x000B	SPI revision	[7:0]	SPI revision		SPI revision register. 0x01: Revision 1.0.	0x1	R
				00000001	Revision 1.0.		
0x000C	Vendor ID LSB	[7:0]	Vendor ID LSB		Vendor ID[7:0].	0x56	R
0x000D	Vendor ID MSB	[7:0]	Vendor ID MSB		Vendor ID[15:8].	0x04	R
0x000F	Transfer	[7:1]	Reserved		Reserved.	0x0	R
		0	Chip transfer		Self clearing chip transfer bit. This bit is used to update the DDC phase increment and phase offset registers when DDC phase update mode (Register 0x0300, Bit 7) = 1. This makes it possible to synchronously update the DDC mixer frequencies. This bit is also used to update the coefficients for the programmable filter (PFILT).	0x0	R/W
				0	Do nothing. Bit is only cleared after transfer is complete.		
				1	Self clearing bit used to synchronize the transfer of data from master to slave registers.		

Clock/SYSREF/Chip Power-Down Pin Control Registers

Table 47.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x003F	Chip PDWN pin (local)	7	Local chip PDWN pin disable		Function is determined by Register 0x0040, Bits[7:6]	0x0	R/W
				0	Power-down pin (PDWN/STBY) enabled (default).		
				1	Power-down pin (PDWN/STBY) disabled/ignored.		
		[6:0]	Reserved		Reserved.	0x0	R
0x0040	Chip Pin Control 1	[7:6]	Chip PDWN pin functionality		External power-down pin functionality. Assertion of the external power-down pin (PDWN/STBY) has higher priority than the channel power mode control bits (Register 0x0002, Bits[1:0]). The PDWN/STBY pin is only used when Register 0x0040, Bits[7:6] = 00 or 01.	0x0	R/W
				00	Power-down pin (default). Assertion of external power-down pin (PDWN/STBY) causes the chip to enter full power-down mode.		
				01	Standby pin. Assertion of external power-down pin (PDWN/STBY) causes the chip to enter standby mode.		
				10	Pin disabled. Power-down pin (PDWN/STBY) is ignored.		
		[5:3]	Chip FD_B/GPIO_B0 pin functionality		Fast Detect B/GPIO B0 pin functionality.	0x7	R/W
				000	Fast Detect B output.		
				001	JESD204B LMFC output.		
				110	Pin functionality determined by Register 0x0041, Bits[7:4].		
				111	Disabled. Configured as input with weak pull-down (default).		
		[2:0]	Chip FD_A/GPIO_A0 pin functionality		Fast Detect A/GPIO A0 pin functionality.	0x7	R/W
				000	Fast Detect A output.		
				001	JESD204B LMFC output.		
				110	Pin functionality determined by Register 0x0041, Bits[3:0].		
				111	Disabled. Configured as an input with weak pull-down (default).		
0x0041	Chip Pin Control 2	[7:4]	Chip FD_B/GPIO_B0 pin secondary functionality		Fast Detect B/GPIO B0 pin secondary functionality (only used when Register 0x0040, Bits[5:3] = 110).	0x0	R/W
				0000	Chip GPIO B0 input (NCO channel selection).		
				0001	Chip transfer input.		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		
		[3:0]	Chip FD_A/GPIO_A0 pin secondary functionality		Fast Detect A/GPIO B0 pin secondary functionality (only used when Register 0x0040, Bits[2:0] = 110).	0x0	R/W
				0000	Chip GPIO A[0] input (NCO channel selection).		
				0001	Chip transfer input.		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0042	Chip Pin Control 3	[7:4]	Chip GPIO_B1 pin functionality		GPIO B1 pin functionality.	0xF	R/W
				0000	Chip GPIO B1 input (NCO channel selection).		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		
				1111	Disabled (configured as input with weak pull-down).		
		[3:0]	Chip GPIO_B1 pin functionality		GPIO A1 pin functionality.	0xF	R/W
				0000	Chip GPIO A1 input (NCO channel selection).		
				1000	Master next trigger output (MNTO).		
				1001	Slave next trigger input (SNTI).		
				1111	Disabled (configured as input with weak pull-down).		
0x0108	Clock divider control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Input clock divider (CLK± pins)			0x0	R/W
				00	Divide by 1.		
				01	Divide by 2.		
				11	Divide by 4.		
0x0109	Clock divider phase (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase offset			0x0	R/W
				0000	0 input clock cycles delayed.		
				0001	½ input clock cycles delayed (invert clock).		
				0010	1 input clock cycles delayed.		
				...	...		
				1110	7 input clock cycles delayed.		
				1111	7½ input clock cycles delayed.		
0x010A	Clock divider and SYSREF control	7	Clock divider auto phase adjust enable		Clock divider auto-phase adjust enable. When enabled, Register 0x0129, Bits[3:0] contain the phase of the divider when SYSREF was captured. The actual divider phase offset = Register 0x0129, Bits[3:0] + Register 0x0109, Bits[3:0].	0x0	R/W
				0	Clock divider phase is not changed by SYSREF (disabled).		
				1	Clock divider phase is automatically adjusted by SYSREF (enabled).		
		[6:4]	Reserved		Reserved.	0x0	R
		[3:2]	Clock divider negative skew window		Clock divider negative skew window (measured in ½ input device clocks). Number of ½ clock cycles before the input device clock by which captured SYSREF transitions are ignored. Only used when Register 0x010A, Bit 7 = 1. Register 0x010A, Bits[3:2] + Register 0x010A, Bits[1:0] < Register 0x0108, Bits[2:0]. This allows some uncertainty in the sampling of SYSREF without disturbing the input clock divider. Also, SYSREF must be disabled (Register 0x0120, Bits[2:1] = 0x0) when changing this control field.	0x0	R/W
				0	No negative skew; SYSREF must be captured accurately.		
				1	½ device clock of negative skew.		
				10	1 device clocks of negative skew.		
				11	1½ device clocks of negative skew.		
		[1:0]	Clock divider positive skew window		Clock divider positive skew window (measured in ½ input device clocks). Number of clock cycles after the input device clock by which captured SYSREF transitions are ignored. Only used when Register 0x010A, Bit 7 = 1. Register 0x010A, Bits[3:2] + Register 0x010A, Bits[1:0] < Register 0x0108, Bits[2:0]. This allows some uncertainty in the sampling of SYSREF without disturbing the input clock divider. Also, SYSREF must be disabled (Register 0x0120, Bits[2:1] = 0x0) when changing this control field.	0x0	R/W
				0	No positive skew; SYSREF must be captured accurately.		
				1	½ device clock of positive skew.		
				10	1 device clocks of positive skew.		
				11	1½ device clocks of positive skew.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x010B	Clock divider SYSREF status	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider SYSREF offset		Clock divider phase status (measured in ½ clock cycles). Internal clock divider phase of the captured SYSREF signal applied to the phase offset. Only used when Register 0x010A, Bit 7 = 1. When Register 0x010A, Bit 7 = 1 and Register 0x010A, Bits[3:2] = 0 and Register 0x010A, Bits[1:0] = 0, clock divider SYSREF offset = 0x0129[3:0].	0x0	R
0x0110	Clock delay control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	Clock delay mode select		Clock delay mode select. Used in conjunction with Register 0x0111 and Register 0x0112.	0x0	R/W
				000	No clock delay.		
				010	Fine delay: only 0 to 16 delay steps are valid.		
				011	Fine delay (lowest jitter): only 0 to 16 delay steps are valid.		
				100	Fine delay: all 192 delay steps are valid.		
				110	Fine delay enabled (all 192 delay steps are valid); super fine delay enabled (all 128 delay steps are valid).		
0x0111	Clock super fine delay (local)	[7:0]	Clock super fine delay adjust		Clock super fine delay adjust. This is an unsigned control to adjust the super fine sample clock delay in 0.25 ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 010 or 110.	0x0	R/W
				0x00	0 delay steps.		
				...	...		
				0x08	8 delay steps.		
				...	...		
				0x80	128 delay steps.		
0x0112	Clock fine delay (local)	[7:0]	Set clock fine delay		Clock fine delay adjust. This is an unsigned control to adjust the fine sample clock skew in 1.725 ps steps. These bits are only used when Register 0x0110, Bits[2:0] = 0x2, 0x3, 0x4, or 0x6. Minimum = 0. Maximum = 192. Increment = 1. Unit is delay steps.	0xC0	R/W
				0x00	0 delay steps.		
				...	...		
				0x08	8 delay steps.		
				...	...		
				0xC0	192 delay steps.		
0x011B	Clock status	[7:1]	Reserved		Reserved.	0x0	R
		0	Input clock detect		Clock detection status.	0x0	R
				0	Input clock not detected.		
				1	Input clock detected/locked.		
0x011C	Clock Duty Cycle Stabilizer 1 control (local)	[7:2]	Reserved		Reserved.	0x0	R/W
		1	DCS1 enable		Clock DCS1 enable.	0x1	R/W
				0	DCS1 bypassed.		
				1	DCS1 enabled.		
		0	DCS1 power up		Clock DCS1 power-up.	0x1	R/W
				0	DCS1 powered down.		
				1	DCS1 powered up.		
0x011E	Clock Duty Cycle Stabilizer 2 control	[7:2]	Reserved		Reserved.	0x0	R/W
		1	DCS2 enable		Clock DCS2 enable.	0x1	R/W
				0	DCS2 bypassed.		
				1	DCS2 enabled.		
		0	DCS2 power up		Clock DCS2 power-up.	0x1	R/W
				0	DCS2 powered down.		
				1	DCS2 powered up.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0120	SYSREF Control 1	7	Reserved		Reserved.	0x0	R
		6	SYSREF± flag reset			0x0	R/W
				0	Normal flag operation.		
				1	SYSREF flags held in reset (setup/hold error flags cleared).		
		5	Reserved		Reserved.	0x0	R
		4	SYSREF± transition select			0x0	R/W
				0	SYSREF is valid on low to high transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
				1	SYSREF is valid on high to low transitions using the selected CLK± edge. When changing this setting, SYSREF± mode select must be set to disabled.		
		3	CLK± edge select			0x0	R/W
				0	Captured on the rising edge of CLK± input.		
				1	Captured on the falling edge of CLK± input.		
		[2:1]	SYSREF± mode select			0x0	R/W
				0	Disabled.		
				1	Continuous.		
				10	N-shot.		
		0	Reserved		Reserved.	0x0	R
0x0121	SYSREF Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	SYSREF N-shot ignore counter select			0x0	R/W
				0000	Next SYSREF± transition only (do not ignore).		
				0001	Ignore the first SYSREF± transition.		
				0010	Ignore the first two SYSREF± transitions.		
				0011	Ignore the first three SYSREF± transitions.		
					…		
				1110	Ignore the first 14 SYSREF± transitions.		
				1111	Ignore the first 15 SYSREF± transitions.		
0x0122	SYSREF Control 3	[7:4]	Reserved		Reserved.	0x0	R
		[3:2]	SYSREF window negative		Negative skew window (measured in sample clocks). Number of clock cycles before the sample clock by which captured SYSREF transitions are ignored.	0x0	R/W
				00	No negative skew; SYSREF must be captured accurately.		
				01	One sample clock of negative skew.		
				10	Two sample clocks of negative skew.		
				11	Three sample clocks of negative skew.		
		[1:0]	SYSREF window positive		Positive skew window (measured in sample clocks). Number of clock cycles before the sample clock by which captured SYSREF transitions are ignored.	0x0	R/W
				00	No positive skew; SYSREF must be captured accurately.		
				01	One sample clock of positive skew.		
				10	Two sample clocks of positive skew.		
				11	Three sample clocks of positive skew.		
0x0123	SYSREF Control 4	7	Reserved		Reserved.	0x0	R
		[6:0]	SYSREF± timestamp delay, Bits[6:0]		SYSREF timestamp delay (in converter sample clock cycles).	0x00	R/W
				0	0 sample clock cycle delay.		
				1	1 sample clock cycle delay.		
				…	…		
				111 1111	127 sample clock cycle delay.		
0x0128	SYSREF Status 1	[7:4]	SYSREF± hold status		SYSREF hold status.	0x0	R
		[3:0]	SYSREF± setup status		SYSREF setup status.	0x0	R

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0129	SYSREF Status 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Clock divider phase when SYSREF± was captured		SYSREF divider phase. Represents the phase of the divider when SYSREF was captured.	0x0	R
				0000	In phase.		
				0001	SYSREF± is ½ cycle delayed from clock.		
				0010	SYSREF± is 1 cycle delayed from clock.		
				0011	SYSREF± is 1½ input clock cycles delayed.		
				0100	SYSREF± is 2 input clock cycles delayed.		
				…	…		
				1111	SYSREF± is 7½ input clock cycles delayed.		
0x012A	SYSREF Status 3	[7:0]	SYSREF counter, Bits[7:0] increments when a SYSREF± is captured		SYSREF count. Running counter that increments whenever a SYSREF event is captured. Reset by Register 0x120, Bit 6. Wraps around at 255. Read these bits only when Register 0x120, Bits[2:1] are set to disabled.	0x0	R
0x01FF	Chip sync mode	[7:1]	Reserved		Reserved.	0x0	R
		0	Synchronization mode			0x0	R/W
				0	JESD204B synchronization mode. The SYSREF signal resets all internal clock dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.		
				1	Timestamp mode. The SYSREF signal does not reset internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF signal. The SYSREF signal timestamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.		

Chip Operating Mode Control Registers

Table 48.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0200	Chip mode	[7:6]	Reserved		Reserved.	0x0	R/W
		5	Chip Q ignore		Chip real (I) only selection.	0x0	R/W
				0	Both real (I) and complex (Q) selected.		
				1	Only real (I) selected; complex (Q) is ignored.		
		4	Reserved		Reserved.	0x0	R
		[3:0]	Chip application mode			0x0	R/W
				0000	Full bandwidth mode (default).		
				0001	One DDC mode (DDC0 only).		
				0010	Two DDC mode (DDC0 and DDC1 only).		
				0011	Four DDC mode (DDC0, DDC1, DDC2, and DDC3).		
0x0201	Chip decimation ratio	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Chip decimation ratio		Chip decimation ratio.	0x0	R/W
				0000	Full sample rate (decimate by 1, DDCs are bypassed).		
				0001	Decimate by 2.		
				1000	Decimate by 3.		
				0010	Decimate by 4.		
				0101	Decimate by 5.		
				1001	Decimate by 6.		
				0011	Decimate by 8.		
				0110	Decimate by 10.		
				1010	Decimate by 12.		
				0111	Decimate by 15.		
				0100	Decimate by 16.		
				1101	Decimate by 20.		
				1011	Decimate by 24.		
				1110	Decimate by 30.		
				1111	Decimate by 40.		
				1100	Decimate by 48.		

Fast Detect and Signal Monitor Control Registers

Table 49.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0245	Fast detect control (local)	[7:4]	Reserved		Reserved.	0x0	R
		3	Force FD_A/FD_B pins			0x0	R/W
				0	Normal operation of the fast detect pin.		
				1	Force a value on the fast detect pin (see Bit 2).		
		2	Force value of FD_A/FD_B pins		The fast detect output pin for this channel is set to this value when the output is forced.	0x0	R/W
		1	Reserved		Reserved.	0x0	R
		0	Enable fast detect output			0x0	R/W
				0	Fast detect disabled.		
				1	Fast detect enabled.		
0x0247	Fast detect up LSB (local)	[7:0]	Fast detect upper threshold		LSBs of fast detect upper threshold. This register contains the 8 LSBs of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0248	Fast detect up MSB (local)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect upper threshold		LSBs of fast detect upper threshold. This register contains the 8 LSBS of the programmable 13-bit upper threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x0249	Fast detect low LSB (local)	[7:0]	Fast detect lower threshold		LSBs of fast detect lower threshold. This register contains the 8 LSBS of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024A	Fast detect low MSB (local)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Fast detect lower threshold		LSBs of fast detect lower threshold. This register contains the 8 LSBs of the programmable 13-bit lower threshold that is compared to the fine ADC magnitude.	0x0	R/W
0x024B	Fast detect dwell LSB (local)	[7:0]	Fast detect dwell time		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x024C	Fast detect dwell MSB (local)	[7:0]	Fast detect dwell time		LSBs of fast detect dwell time counter target. This is a load value for a 16-bit counter that determines how long the ADC data must remain below the lower threshold before the FD_x pins are reset to 0.	0x0	R/W
0x026F	Signal monitor sync control	[7:2]	Reserved		Reserved.	0x0	R
		1	Signal monitor next synchronization mode		Signal monitor next synchronization mode.	0x0	R/W
				0	Continuous mode.		
				1	Next synchronization mode. Only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF has been captured, Register 0x026F, Bit 0 is cleared. The SYSREF± pin must an integer multiple of the signal monitor period for this function to operate correctly in continuous mode.		
		0	Signal monitor synchronization mode		Signal monitor synchronization enable.	0x0	R/W
				0	Synchronization disabled.		
				1	If Register 0x026F, Bit 1 = 1, only the next valid edge of the SYSREF± pin is used to synchronize the signal monitor block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF signal is received, this bit is cleared. The SYSREF± input pin must be enabled to synchronize the signal monitor blocks.		
0x0270	Signal monitor control (local)	[7:2]	Reserved		Reserved.	0x0	R
		1	Peak detector			0x0	R/W
				0	Peak detector disabled.		
				1	Peak detector enabled.		
		0	Reserved		Reserved.	0x0	R

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0271	Signal Monitor Period 0 (local)	[7:0]	Signal monitor period[7:0]		Bits[7:0] of the 24-bit value that sets the number of output clock cycles over which the signal monitor performs its operation. Only even values are supported.	0x80	R/W
0x0272	Signal Monitor Period 1 (local)	[7:0]	Signal monitor period[15:8]		Bits[15:8] of the 24-bit value that sets the number of output clock cycles over which the signal monitor performs its operation. Only even values are supported.	0x0	R/W
0x0273	Signal Monitor Period 2 (local)	[7:0]	Signal monitor period[23:16]		Bits[23:16] of the 24-bit value that sets the number of output clock cycles over which the signal monitor performs its operation. Only even values are supported.	0x0	R/W
0x0274	Signal monitor status control (local)	[7:5]	Reserved		Reserved.	0x0	R
		4	Result update	1	Update signal monitor status registers, Register 0x0275 to Register 0x0278. Self clearing.	0x0	R/WC
		3	Reserved		Reserved.	0x0	R
		[2:0]	Result selection	001	Peak detector placed on status readback signals.	0x1	R/W
0x0275	Signal Monitor Status 0 (local)	[7:0]	Signal monitor result[7:0]		Signal monitor status result. This 20-bit value contains the status result calculated by the signal monitor block.	0x0	R
0x0276	Signal Monitor Status 1 (local)	[7:0]	Signal monitor result[15:8]		Signal monitor status result.	0x0	R
0x0277	Signal Monitor Status 2 (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Signal monitor result[19:16]		Signal monitor status result.	0x0	R
0x0278	Signal monitor status frame counter (local)	[7:0]	Period count result, Bits[7:0]		Signal monitor frame counter status bits. Frame counter increments whenever the period counter expires.	0x0	R
0x0279	Signal monitor serial framer control (local)	[7:2]	Reserved		Reserved.	0x0	R
		[1:0]	Signal monitor SPORT over JESD204B enable	00 11	Disabled. Enabled.	0x0	R/W
0x027A	SPORT over JESD204B input selection (local)	[7:6]	Reserved		Reserved.	0x0	R
		1	SPORT over JESD204B input selection	0 1	Signal monitor serial framer input selection. When each individual bit is a 1, the corresponding signal statistics information is sent within the frame. Disabled. Peak detector data inserted in the serial frame.	0x1	R/W
		0	Reserved		Reserved.	0x0	R

DDC Function Registers (See the Digital Downconverter (DDC) Section)

Table 50.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0300	DDC SYNC control	7	DDC FTW/POW/MAW/ MBW update mode	0 1	Select DDC FTW/POW/MAW/MBW update mode. Instantaneous/continuous update. FTW/POW/MAW/MBW values are updated immediately. FTW/POW/MAW/MBW values are updated synchronously when the chip transfer bit (Register 0x000F, Bit 0) is set.	0x0	R/W
		6:5	Reserved		Reserved.	0x0	R
		4	DDC NCO soft reset	0 1	This bit can be used to synchronize all the NCOs inside the DDC blocks. Normal operation. DDC held in reset.	0x0	R/W
		[3:2]	Reserved		Reserved.	0x0	R

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		1	DDC next sync			0x0	R/W
				0	Continuous mode. The SYSREF frequency must be an integer multiple of the NCO frequency for this function to operate correctly in continuous mode.		
				1	Only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF signal is found, the DDC synchronization enable bit (Register 0x0300, Bit 0) is cleared.		
		0	DDC synchronization mode		The SYSREF input pin must be enabled to synchronize the DDCs.	0x0	R/W
				0	Synchronization disabled.		
				1	If Register 0x0300, Bit 1 = 1, only the next valid edge of the SYSREF± pin is used to synchronize the NCO in the DDC block. Subsequent edges of the SYSREF± pin are ignored. When the next SYSREF signal is received, this bit is cleared.		
0x0310	DDC0 control	7	DDC0 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC0 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC0 intermediate frequency (IF) mode			0x0	R/W
				00	Variable IF mode.		
				01	0 Hz IF mode.		
				10	f_S Hz IF mode.		
				11	Test mode.		
		3	DDC0 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. complex to real enabled. Uses extra f_S mixing to convert to real.		
		[2:0]	DDC0 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0311, Bits[7:4].		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0311	DDC0 input select	[7:4]	DDC0 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
				111	TB1 filter selection: decimate by 3 (decimate by 1.5 not supported).		
				1000	FB2 + TB1 filter selection: decimate by 15 (decimate by 7.5 not supported).		
				1001	HB2 + FB2 + TB1 filter selection: decimate by 30 (decimate by 15 not supported).		
		3	Reserved		Reserved.	0x0	R
		2	DDC0 Q input select			0x0	R/W
				0	Channel A.		
				1	Channel B.		
		1	Reserved		Reserved.	0x0	R
		0	DDC0 I input select			0x0	R/W
				0	Channel A.		
				1	Channel B.		
0x0314	DDC0 NCO control	[7:4]	DDC0 NCO channel select mode		For edge control, the internal counter wraps after the Register 0x0314, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO B0, GPIO A0.		
				10	2'b0, GPIO B1, GPIO A1.		
				11	2'b00, GPIO A1, GPIO A0.		
				100	2'b00, GPIO B1, GPIO B0.		
				101	GPIO B1, GPIO A1, GPIO B0, GPIO A0.		
				110	GPIO B1, GPIO B0, GPIO A1, GPIO A0.		
				1000	Increment internal counter on rising edge of the GPIO_A0 pin.		
				1001	Increment internal counter on rising edge of the GPIO_A1 pin.		
				1010	Increment internal counter on rising edge of the GPIO_B0 pin.		
				1011	Increment internal counter on rising edge of the GPIO_B1 pin.		
		[3:0]	DDC0 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0315	DDC0 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC0 phase update index		Indexes the NCO channel whose phase and offset is updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0316	DDC0 Phase Increment 0	[7:0]	DDC0 phase increment[7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0317	DDC0 Phase Increment 1	[7:0]	DDC0 phase increment[15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0318	DDC0 Phase Increment 2	[7:0]	DDC0 phase increment[23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0319	DDC0 Phase Increment 3	[7:0]	DDC0 phase increment[31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x031A	DDC0 Phase Increment 4	[7:0]	DDC0 phase increment[39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x031B	DDC0 Phase Increment 5	[7:0]	DDC0 phase increment[47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x031D	DDC0 Phase Offset 0	[7:0]	DDC0 phase offset[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031E	DDC0 Phase Offset 1	[7:0]	DDC0 phase offset[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x031F	DDC0 Phase Offset 2	[7:0]	DDC0 phase offset[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0320	DDC0 Phase Offset 3	[7:0]	DDC0 phase offset[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0321	DDC0 Phase Offset 4	[7:0]	DDC0 phase offset[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0322	DDC0 Phase Offset 5	[7:0]	DDC0 phase offset[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0327	DDC0 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC0 Q output test mode enable		Q samples always use Test Mode B block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R
		0	DDC0 I output test mode enable		I samples always use Test Mode A block.. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0330	DDC1 control	7	DDC1 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC1 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC1 IF mode			0x0	R/W
				00	Variable IF mode.		
				01	0 Hz IF mode.		
				10	f_S Hz IF mode.		
				11	Test mode.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		3	DDC1 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. Complex to real enabled. Uses extra f_S mixing to convert to real.		
		[2:0]	DDC1 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0331, Bits[7:4].		
0x0331	DDC1 input select	[7:4]	DDC1 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
				111	TB1 filter selection: decimate by 3 (decimate by 1.5 not supported).		
				1000	FB2 + TB1 filter selection: decimate by 15 (decimate by 7.5 not supported).		
				1001	HB2 + FB2 + TB1 filter selection: decimate by 30 (decimate by 15 not supported).		
		3	Reserved		Reserved.	0x0	R
		2	DDC1 Q input select			0x1	R/W
				0	Channel A.		
				1	Channel B.		
		1	Reserved		Reserved.	0x0	R
		0	DDC1 I input select			0x1	R/W
				0	Channel A.		
				1	Channel B.		
0x0334	DDC1 NCO control	[7:4]	DDC1 NCO channel select mode		For edge control, the internal counter wraps when the Register 0x0334, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO B0, GPIO A0.		
				10	2'b0, GPIO B1, GPIO A1.		
				11	2'b00, GPIO A1, GPIO A0.		
				100	2'b00, GPIO B1, GPIO B0.		
				101	GPIO B1, GPIO A1, GPIO B0, GPIO A0.		
				110	GPIO B1, GPIO B0, GPIO A1, GPIO A0.		
				1000	Increment internal counter when rising edge of the GPIO_A0 pin.		
				1001	Increment internal counter when rising edge of the GPIO_A1 pin.		
				1010	Increment internal counter when rising edge of the GPIO_B0 pin.		
				1011	Increment internal counter when rising edge of the GPIO_B1 pin.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		[3:0]	DDC1 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		
0x0335	DDC1 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC1 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0336	DDC1 Phase Increment 0	[7:0]	DDC1 phase increment[7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0337	DDC1 Phase Increment 1	[7:0]	DDC1 phase increment[15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0338	DDC1 Phase Increment 2	[7:0]	DDC1 phase increment[23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0339	DDC1 Phase Increment 3	[7:0]	DDC1 phase increment[31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x033A	DDC1 Phase Increment 4	[7:0]	DDC1 phase increment[39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x033B	DDC1 Phase Increment 5	[7:0]	DDC1 phase increment[47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x033D	DDC1 Phase Offset 0	[7:0]	DDC1 phase offset[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033E	DDC1 Phase Offset 1	[7:0]	DDC1 phase offset[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x033F	DDC1 Phase Offset 2	[7:0]	DDC1 phase offset[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0340	DDC1 Phase Offset 3	[7:0]	DDC1 phase offset[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0341	DDC1 Phase Offset 4	[7:0]	DDC1 phase offset[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0342	DDC1 Phase Offset 5	[7:0]	DDC1 phase offset[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0347	DDC1 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC1 Q output test mode enable		Q samples always use Test Mode B block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R
		0	DDC1 I output test mode enable		I samples always use Test Mode A block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0350	DDC2 control	7	DDC2 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC2 gain select		Gain can be used to compensates for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC2 IF mode			0x0	R/W
				00	Variable IF mode.		
				01	0 Hz IF mode.		
				10	f_S Hz IF mode.		
				11	Test mode.		
		3	DDC2 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. Complex to real enabled. Uses extra f_S mixing to convert to real.		
		[2:0]	DDC2 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0351, Bits[7:4].		
0x0351	DDC2 input select	[7:4]	DDC2 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled)		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled)		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled)		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled)		
		3	Reserved		Reserved.	0x0	R
		2	DDC2 Q input select			0x0	R/W
				0	Channel A.		
				1	Channel B.		
		1	Reserved		Reserved.	0x0	R
		0	DDC2 I input select			0x0	R/W
				0	Channel A.		
				1	Channel B.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0354	DDC2 NCO control	[7:4]	DDC2 NCO channel select mode		For edge control, the internal counter wraps when the Register 0x0354, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO B0, GPIO A0.		
				10	2'b0, GPIO B1, GPIO A1.		
				11	2'b00, GPIO A1, GPIO A0.		
				100	2'b00, GPIO B1, GPIO B0.		
				101	GPIO B1, GPIO A1, GPIO B0, GPIO A0.		
				110	GPIO B1, GPIO B0, GPIO A1, GPIO A0.		
				1000	Increment internal counter when rising edge of the GPIO_A0 pin.		
				1001	Increment internal counter when rising edge of the GPIO_A1 pin.		
				1010	Increment internal counter when rising edge of the GPIO_B0 pin.		
				1011	Increment internal counter when rising edge of the GPIO_B1 pin.		
		[3:0]	DDC2 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		
0x0355	DDC2 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC2 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0356	DDC2 Phase Increment 0	[7:0]	DDC2 phase increment[7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0357	DDC2 Phase Increment 1	[7:0]	DDC2 phase increment[15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0358	DDC2 Phase Increment 2	[7:0]	DDC2 phase increment[23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0359	DDC2 Phase Increment 3	[7:0]	DDC2 phase increment[31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x035A	DDC2 Phase Increment 4	[7:0]	DDC2 phase increment[39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x035B	DDC2 Phase Increment 5	[7:0]	DDC2 phase increment[47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x035D	DDC2 Phase Offset 0	[7:0]	DDC2 phase offset[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W
0x035E	DDC2 Phase Offset 1	[7:0]	DDC2 phase offset[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x035F	DDC2 Phase Offset 2	[7:0]	DDC2 phase offset[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0360	DDC2 Phase Offset 3	[7:0]	DDC2 phase offset[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0361	DDC2 Phase Offset 4	[7:0]	DDC2 phase offset[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0362	DDC2 Phase Offset 5	[7:0]	DDC2 phase offset[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0367	DDC2 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC2 Q output test mode enable		Q samples always use Test Mode B block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R
		0	DDC2 I output test mode enable		I samples always use Test Mode A block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0370	DDC3 control	7	DDC3 mixer select			0x0	R/W
				0	Real mixer (I and Q inputs must be from the same real channel).		
				1	Complex mixer (I and Q must be from separate, real and imaginary quadrature ADC receive channels; analog demodulator).		
		6	DDC3 gain select		Gain can be used to compensate for the 6 dB loss associated with mixing an input signal down to baseband and filtering out its negative component.	0x0	R/W
				0	0 dB gain.		
				1	6 dB gain (multiply by 2).		
		[5:4]	DDC3 IF mode			0x0	R/W
				00	Variable If mode.		
				01	0 Hz IF mode.		
				10	f_S Hz IF mode.		
				11	Test mode.		
		3	DDC3 complex to real enable			0x0	R/W
				0	Complex (I and Q) outputs contain valid data.		
				1	Real (I) output only. complex to real enabled. Uses extra f_S mixing to convert to real.		
		[2:0]	DDC3 decimation rate select		Decimation filter selection.	0x0	R/W
				000	HB1 + HB2 filter selection: decimate by 2 (complex to real enabled), or decimate by 4 (complex to real disabled).		
				001	HB1 + HB2 + HB3 filter selection: decimate by 4 (complex to real enabled), or decimate by 8 (complex to real disabled).		
				010	HB1 + HB2 + HB3 + HB4 filter selection: decimate by 8 (complex to real enabled), or decimate by 16 (complex to real disabled).		
				011	HB1 filter selection: decimate by 1 (complex to real enabled), or decimate by 2 (complex to real disabled).		
				100	HB1 + TB2 filter selection: decimate by 3 (complex to real enabled), or decimate by 6 (complex to real disabled).		
				101	HB1 + HB2 + TB2 filter selection: decimate by 6 (complex to real enabled), or decimate by 12 (complex to real disabled).		
				110	HB1 + HB2 + HB3 + TB2 filter selection: decimate by 12 (complex to real enabled), or decimate by 24 (complex to real disabled).		
				111	Decimation determined by Register 0x0371, Bits[7:4].		
0x0371	DDC3 input select	[7:4]	DDC3 decimation rate select		Only valid when Register 0x0310, Bits[2:0] = 3'b111.	0x0	R/W
				0	TB2 + HB4 + HB3 + HB2 + HB1 filter selection: decimate by 48 (complex to real disabled), or decimate by 24 (complex to real enabled).		
				10	FB2 + HB1 filter selection: decimate by 10 (complex to real disabled), or decimate by 5 (complex to real enabled).		
				11	FB2 + HB2 + HB1 filter selection: decimate by 20 (complex to real disabled), or decimate by 10 (complex to real enabled).		
				100	FB2 + HB3 + HB2 + HB1 filter selection: decimate by 40 (complex to real disabled), or decimate by 20 (complex to real enabled).		
		3	Reserved		Reserved.	0x0	R

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		2	DDC3 Q input select			0x1	R/W
				0	Channel A.		
				1	Channel B.		
		1	Reserved		Reserved.	0x0	R
		0	DDC3 I input select			0x1	R/W
				0	Channel A.		
				1	Channel B.		
0x0374	DDC3 NCO control	[7:4]	DDC3 NCO channel select mode		For edge control, the internal counter wraps when the Register 0x0374, Bits[3:0] value is reached.	0x0	R/W
				0	Use Register 0x0314, Bits[3:0].		
				1	2'b0, GPIO B0, GPIO A0.		
				10	2'b0, GPIO B1, GPIO A1.		
				11	2'b00, GPIO A1, GPIO A0.		
				100	2'b00, GPIO B1, GPIO B0.		
				101	GPIO B1, GPIO A1, GPIO B0, GPIO A0.		
				110	GPIO B1, GPIO B0, GPIO A1, GPIO A0.		
				1000	Increment internal counter when rising edge of GPIO_A0 pin.		
				1001	Increment internal counter when rising edge of GPIO_A1 pin.		
				1010	Increment internal counter when rising edge of GPIO_B0 pin.		
				1011	Increment internal counter when rising edge of GPIO_B1 pin.		
		[3:0]	DDC3 NCO register map channel select		NCO channel select register map control.	0x0	R/W
				0	Select NCO Channel 0.		
				1	Select NCO Channel 1.		
				10	Select NCO Channel 2.		
				11	Select NCO Channel 3.		
				100	Select NCO Channel 4.		
				101	Select NCO Channel 5.		
				110	Select NCO Channel 6.		
				111	Select NCO Channel 7.		
				1000	Select NCO Channel 8.		
				1001	Select NCO Channel 9.		
				1010	Select NCO Channel 10.		
				1011	Select NCO Channel 11.		
				1100	Select NCO Channel 12.		
				1101	Select NCO Channel 13.		
				1110	Select NCO Channel 14.		
				1111	Select NCO Channel 15.		
0x0375	DDC3 phase control	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	DDC3 phase update index		Indexes the NCO channel whose phase and offset gets updated. The update method is based on the DDC phase update mode, which can be continuous or require chip transfer.	0x0	R/W
				0000	Update NCO Channel 0.		
				0001	Update NCO Channel 1.		
				0010	Update NCO Channel 2.		
				0011	Update NCO Channel 3.		
0x0376	DDC3 Phase Increment 0	[7:0]	DDC3 phase increment[7:0]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0377	DDC3 Phase Increment 1	[7:0]	DDC3 phase increment[15:8]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}	0x0	R/W
0x0378	DDC3 Phase Increment 2	[7:0]	DDC3 phase increment[23:16]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x0379	DDC3 Phase Increment 3	[7:0]	DDC3 phase increment[31:24]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x037A	DDC3 Phase Increment 4	[7:0]	DDC3 phase increment[39:32]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x037B	DDC3 Phase Increment 5	[7:0]	DDC3 phase increment[47:40]		FTW. Twos complement phase increment value for the NCO. Complex mixing frequency = (DDC phase increment × f_S)/2^{48}.	0x0	R/W
0x037D	DDC3 Phase Offset 0	[7:0]	DDC3 phase offset[7:0]		Twos complement phase offset value for the NCO.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x037E	DDC3 Phase Offset 1	[7:0]	DDC3 phase offset[15:8]		Twos complement phase offset value for the NCO.	0x0	R/W
0x037F	DDC3 Phase Offset 2	[7:0]	DDC3 phase offset[23:16]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0380	DDC3 Phase Offset 3	[7:0]	DDC3 phase offset[31:24]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0381	DDC3 Phase Offset 4	[7:0]	DDC3 phase offset[39:32]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0382	DDC3 Phase Offset 5	[7:0]	DDC3 phase offset[47:40]		Twos complement phase offset value for the NCO.	0x0	R/W
0x0387	DDC3 test enable	[7:3]	Reserved		Reserved.	0x0	R
		2	DDC3 Q output test mode enable		Q samples always use Test Mode B block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
		1	Reserved		Reserved.	0x0	R
		0	DDC3 I output test mode enable		I samples always use Test Mode A block. The test mode is selected using the channel dependent Register 0x0550, Bits[3:0].	0x0	R/W
				0	Test mode disabled.		
				1	Test mode enabled.		
0x0390	DDC0 Phase Increment Frac A0	[7:0]	DDC0 Phase Increment Frac A[7:0]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0391	DDC0 Phase Increment Frac A1	[7:0]	DDC0 Phase Increment Frac A[15:8]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0392	DDC0 Phase Increment Frac A2	[7:0]	DDC0 Phase Increment Frac A[23:16]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0393	DDC0 Phase Increment Frac A3	[7:0]	DDC0 Phase Increment Frac A[31:24]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0394	DDC0 Phase Increment Frac A4	[7:0]	DDC0 Phase Increment Frac A[39:32]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0395	DDC0 Phase Increment Frac A5	[7:0]	DDC0 Phase Increment Frac A[47:40]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x0398	DDC0 Phase Increment Frac B0	[7:0]	DDC0 Phase Increment Frac B[7:0]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x0399	DDC0 Phase Increment Frac B1	[7:0]	DDC0 Phase Increment Frac B[15:8]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x039A	DDC0 Phase Increment Frac B2	[7:0]	DDC0 Phase Increment Frac B[23:16]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x039B	DDC0 Phase Increment Frac B3	[7:0]	DDC0 Phase Increment Frac B[31:24]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x039C	DDC0 Phase Increment Frac B4	[7:0]	DDC0 Phase Increment Frac B[39:32]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x039D	DDC0 Phase Increment Frac B5	[7:0]	DDC0 Phase Increment Frac B[47:40]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03A0	DDC1 Phase Increment Frac A0	[7:0]	DDC1 Phase Increment Frac A[7:0]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03A1	DDC1 Phase Increment Frac A1	[7:0]	DDC1 Phase Increment Frac A[15:8]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x03A2	DDC1 Phase Increment Frac A2	[7:0]	DDC1 Phase Increment Frac A[23:16]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03A3	DDC1 Phase Increment Frac A3	[7:0]	DDC1 Phase Increment Frac A[31:24]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03A4	DDC1 Phase Increment Frac A4	[7:0]	DDC1 Phase Increment Frac A[39:32]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03A5	DDC1 Phase Increment Frac A5	[7:0]	DDC1 Phase Increment Frac A[47:40]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03A8	DDC1 Phase Increment Frac B0	[7:0]	DDC1 Phase Increment Frac B[7:0]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03A9	DDC1 Phase Increment Frac B1	[7:0]	DDC1 Phase Increment Frac B[15:8]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03AA	DDC1 Phase Increment Frac B2	[7:0]	DDC1 Phase Increment Frac B[23:16]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03AB	DDC1 Phase Increment Frac B3	[7:0]	DDC1 Phase Increment Frac B[31:24]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03AC	DDC1 Phase Increment Frac B4	[7:0]	DDC1 Phase Increment Frac B[39:32]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03AD	DDC1 Phase Increment Frac B5	[7:0]	DDC1 Phase Increment Frac B[47:40]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03B0	DDC2 Phase Increment Frac A0	[7:0]	DDC2 Phase Increment Frac A[7:0]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B1	DDC2 Phase Increment Frac A1	[7:0]	DDC2 Phase Increment Frac A[15:8]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B2	DDC2 Phase Increment Frac A2	[7:0]	DDC2 Phase Increment Frac A[23:16]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B3	DDC2 Phase Increment Frac A3	[7:0]	DDC2 Phase Increment Frac A[31:24]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B4	DDC2 Phase Increment Frac A4	[7:0]	DDC2 Phase Increment Frac A[39:32]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B5	DDC2 Phase Increment Frac A5	[7:0]	DDC2 Phase Increment Frac A[47:40]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03B8	DDC2 Phase Increment Frac B0	[7:0]	DDC2 Phase Increment Frac B[7:0]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03B9	DDC2 Phase Increment Frac B1	[7:0]	DDC2 Phase Increment Frac B[15:8]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03BA	DDC2 Phase Increment Frac B2	[7:0]	DDC2 Phase Increment Frac B[23:16]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03BB	DDC2 Phase Increment Frac B3	[7:0]	DDC2 Phase Increment Frac B[31:24]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03BC	DDC2 Phase Increment Frac B4	[7:0]	DDC2 Phase Increment Frac B[39:32]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03BD	DDC2 Phase Increment Frac B5	[7:0]	DDC2 Phase Increment Frac B[47:40]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x03C0	DDC3 Phase Increment Frac A0	[7:0]	DDC3 Phase Increment Frac A[7:0]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C1	DDC3 Phase Increment Frac A1	[7:0]	DDC3 Phase Increment Frac A[15:8]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C2	DDC3 Phase Increment Frac A2	[7:0]	DDC3 Phase Increment Frac A[23:16]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C3	DDC3 Phase Increment Frac A3	[7:0]	DDC3 Phase Increment Frac A[31:24]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C4	DDC3 Phase Increment Frac A4	[7:0]	DDC3 Phase Increment Frac A[39:32]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C5	DDC3 Phase Increment Frac A5	[7:0]	DDC3 Phase Increment Frac A[47:40]		Numerator correction term for Modulus Phase Accumulator A.	0x0	R/W
0x03C8	DDC3 Phase Increment Frac B0	[7:0]	DDC3 Phase Increment Frac B[7:0]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03C9	DDC3 Phase Increment Frac B1	[7:0]	DDC3 Phase Increment Frac B[15:8]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03CA	DDC3 Phase Increment Frac B2	[7:0]	DDC3 Phase Increment Frac B[23:16]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03CB	DDC3 Phase Increment Frac B3	[7:0]	DDC3 Phase Increment Frac B[31:24]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03CC	DDC3 Phase Increment Frac B4	[7:0]	DDC3 Phase Increment Frac B[39:32]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W
0x03CD	DDC3 Phase Increment Frac B5	[7:0]	DDC3 Phase Increment Frac B[47:40]		Denominator correction term for Modulus Phase Accumulator B.	0x0	R/W

Digital Outputs and Test Modes

Table 51.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0550	ADC test mode control (local)	7	User pattern selection		Test mode user pattern selection. This bit is only used when Register 0x0550, Bits[3:0] = 4'b1000 (user input mode). Otherwise, it is ignored. User Pattern 1 is found in the USR_PAT_1_MSB (0x0552) and USR_PAT_1_LSB (0x0551) registers. User Pattern 2 is found in the USR_PAT_2_MSB (0x0554) and USR_PAT_2_LSB (0x0553) registers, and so on.	0x0	R/W
				0	Continuous/repeat pattern. Place each user pattern (1, 2, 3, and 4) on the output for 1 clock cycle and then repeat. (Output User Pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, and so on.)		
				1	Single pattern. Place each user pattern (1, 2, 3, and 4) on the output for 1 clock cycle and then output all zeros. (Output User Pattern 1, 2, 3, 4, and then output all zeros.)		
		6	Reserved		Reserved.	0x0	R
		5	Reset PN long generator		Test mode long pseudorandom number test generator reset.	0x0	R/W
				0	Long PN enabled.		
				1	Long PN held in reset.		
		4	Reset PN short generator		Test mode short pseudorandom number test generator reset.	0x0	R/W
				0	Short PN enabled.		
				1	Short PN held in reset.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		[3:0]	Test mode selection		Test mode generation selection.	0x0	R/W
				0000	Off (normal operation).		
				0001	Midscale short.		
				0010	Positive full scale.		
				0011	Negative full scale.		
				0100	Alternating checker board.		
				0101	PN sequence (long).		
				0110	PN sequence (short).		
				0111	1/0 word toggle.		
				1000	User pattern test mode (used with Register 0x0550, Bit 7 and the User Pattern 1, User Pattern 2, User Pattern 3, and User Pattern 4 registers).		
				1111	Ramp output.		
0x0551	User Pattern 1 LSB	[7:0]	User Pattern 1[7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
0x0552	User Pattern 1 MSB	[7:0]	User Pattern 1[15:8]		User Test Pattern 1 least significant byte.	0x0	R/W
0x0553	User Pattern 2 LSB	[7:0]	User Pattern 2[7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
0x0554	User Pattern 2 MSB	[7:0]	User Pattern 2[15:8]		User Test Pattern 2 least significant byte.	0x0	R/W
0x0555	User Pattern 3 LSB	[7:0]	User Pattern 3[7:0]		User Test Pattern 3 least significant bits.	0x0	R/W
0x0556	User Pattern 3 MSB	[7:0]	User Pattern 3[15:8]		User Test Pattern 3 least significant bits.	0x0	R/W
0x0557	User Pattern 4 LSB	[7:0]	User Pattern 4[7:0]		User Test Pattern 4 least significant bits.	0x0	R/W
0x0558	User Pattern 4 MSB	[7:0]	User Pattern 4[15:8]		User Test Pattern 4 least significant bits.	0x0	R/W
0x0559	Output Mode Control 1	[7:4]	Converter control Bit 1 selection			0x0	R/W
				0000	Tie low (1'b0).		
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF.		
		[3:0]	Converter control Bit 0 selection			0x0	R/W
				0000	Tie low (1'b0).		
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF.		
0x055A	Output Mode Control 2	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	Converter control Bit 2 selection			0x1	R/W
				0000	Tie low (1'b0).		
				0001	Overrange bit.		
				0010	Signal monitor bit.		
				0011	Fast detect (FD) bit.		
				0101	SYSREF.		
0x0561	Out sample mode	[7:3]	Reserved		Reserved.	0x0	R/W
		2	Sample invert			0x0	R/W
				0	ADC sample data is not inverted.		
				1	ADC sample data is inverted.		
		[1:0]	Data format select			0x1	R/W
				00	Offset binary.		
				01	Twos complement (default)		
0x0562	Out overrange clear	[7:0]	Data format overrange clear		Overrange clear bits (one bit for each virtual converter). Writing a 1 to the overrange clear bit clears the corresponding overrange sticky bit.	0x0	R/W
				0	Overrange bit enabled.		
				1	Overrange bit cleared.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0563	Out overrange status	[7:0]	Data format overrange		Overrange sticky bit status (one bit for each virtual converter). Writing a 1 to the overrange clear bit clears the corresponding overrange sticky bit.	0x0	R
				0	No overrange has occurred.		
				1	Overrange has occurred.		
0x0564	Out channel select	[7:1]	Reserved		Reserved.	0x0	R
		0	Converter channel swap control			0x0	R/W
				0	Normal channel ordering.		
				1	Channel swap enabled.		
0x056E	PLL control	[7:4]	JESD204B lane rate control			0x3	R/W
				0000	Lane rate = 6.75 Gbps to 13.5 Gbps.		
				0001	Lane rate = 3.375 Gbps to 6.75 Gbps.		
				0011	Lane rate = 13.5 Gbps to 15.5 Gbps.		
				0101	Lane rate = 1.6875 Gbps to 3.375 Gbps.		
		[3:0]	Reserved		Reserved.	0x0	R
0x056F	PLL status	7	PLL lock status			0x0	R
				0	Not locked.		
				1	Locked.		
		[6:4]	Reserved		Reserved.	0x0	R
		3	PLL loss of lock		Loss of lock sticky bit.		
				1	Indicate a loss of lock has occurred at some time. Cleared by setting Register 0x0571, Bit 0.		
		[2:0]	Reserved		Reserved.		
0x0570	$f_S \times 4$ configuration	[7:0]			See the fS × 4 Mode section.	0xFF	R/W
				0xFE	$f_S \times 4$ mode enabled. L = 8; M = 2; F = 2; S = 4; N' = 16; N = 16; CS = 0; CF = 0; HD = 0.		
				0xFF	$f_S \times 4$ mode disabled. L, M, and F set by Register 0x058B, Bits[4:0]; Register 0x58E, Bits[7:0]; and Register 0x058C, Bits[7:0], respectively.		
0x0571	JESD204B Link Control 1	7	Standby mode			0x0	R/W
				0	Standby mode forces zeros for all converter samples.		
				1	Standby mode forces code group synchronization (K28.5 characters).		
		6	Tail bit(t) PN			0x0	R/W
				0	Disable.		
				1	Enable.		
		5	Long transport layer test			0x0	R/W
				0	JESD204B test samples disabled.		
				1	JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.		
		4	Lane synchronization			0x1	R/W
				0	Disable FACI uses /K28.7/.		
				1	Enable FACI uses /K28.3/ and /K28.7/.		
		[3:2]	ILAS sequence mode			0x1	R/W
				00	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5).		
				01	Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5).		
				11	Initial lane alignment sequence always on test mode. JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.		
		1	FACI			0x0	R/W
				0	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4).		
				1	Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		0	Link control			0x0	R/W
				0	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNC~ pin.		
				1	JESD204B serial transmit link powered down (held in reset and clock gated).		
0x0572	JESD204B Link Control 2	[7:6]	SYNCINB± pin control			0x0	R/W
				00	Normal mode.		
				10	Ignore SYNCINB± (force CGS).		
				11	Ignore SYNCINB± (force ILAS/user data).		
		5	SYNCINB± pin invert			0x0	R/W
				0	SYNCINB± pin not inverted.		
				1	SYNCINB± pin inverted.		
		4	SYNCINB± pin type			0x0	R/W
				0	LVDS differential pair SYNC~ input.		
				1	CMOS single-ended SYNC~ input. SYNCINB+ used.		
		3	Reserved		Reserved.	0x0	R
		2	8-bit/10-bit bypass			0x0	R/W
				0	8-bit/10-bit enabled.		
				1	8-bit/10-bit bypassed (most significant 2 bits are 0).		
		1	8-bit/10-bit bit invert			0x0	R/W
				0	Normal.		
				1	Invert a b c d e f g h i j symbols.		
		0	Reserved		Reserved.	0x0	R/W
0x0573	JESD204B Link Control 3	[7:6]	Checksum mode			0x0	R/W
				00	Checksum is the sum of all 8-bit registers in the link configuration table.		
				01	Checksum is the sum of all individual link configuration fields (LSB aligned).		
				10	Checksum is disabled (set to zero). For test purposes only.		
				11	Unused.		
		[5:4]	Test injection point			0x0	R/W
				0	N' sample input.		
				1	10-bit data at 8-bit/10-bit output (for PHY testing).		
				10	8-bit data at scrambler input.		
		[3:0]	JESD204B test mode patterns			0x0	R/W
				0	Normal operation (test mode disabled).		
				1	Alternating checkerboard.		
				10	1/0 word toggle.		
				11	31-bit PN sequence: $x^{31} + x^{28} + 1$.		
				100	23-bit PN sequence: $x^{23} + x^{18} + 1$.		
				101	15-bit PN sequence: $x^{15} + x^{14} + 1$.		
				110	9-bit PN sequence: $x^{9} + x^{5} + 1$.		
				111	7-bit PN sequence: $x^{7} + x^{6} + 1$.		
				1000	Ramp output.		
				1110	Continuous/repeat user test.		
				1111	Single user test.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0574	JESD204B Link Control 4	[7:4]	ILAS delay			0x0	R/W
				0	Transmit ILAS on first LMFC after SYNCINB± deasserted.		
				1	Transmit ILAS on second LMFC after SYNCINB± deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB± deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB± deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB± deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB± deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB± deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB± deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB± deasserted.		
				1001	Transmit ILAS on tenth LMFC after SYNCINB± deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB± deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB± deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted.		
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted.		
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	Link layer test mode			0x0	R/W
				000	Normal operation (link layer test mode disabled).		
				001	Continuous sequence of /D21.5/ characters.		
				010	Reserved.		
				011	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
0x0578	JESD204B LMFC offset	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value (in frame clocks). Refer to the Deterministic Latency section.	0x0	R/W
0x0580	JESD204B DID configuration	[7:0]	JESD204B Tx DID value		JESD204B serial device identification (DID) number.	0x0	R/W
0x0581	JESD204B BID configuration	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	JESD204B Tx BID value		JESD204B serial bank identification (BID) number (extension to DID).	0x0	R/W
0x0583	JESD204B LID0 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 0 LID value		JESD204B serial lane identification (LID) number for Lane 0.	0x0	R/W
0x0584	JESD204B LID1 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 1 LID value		JESD204B serial LID number for Lane 1.	0x1	R/W
0x0585	JESD204B LID2 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 2 LID value		JESD204B serial LID number for Lane 2.	0x2	R/W
0x0586	JESD204B LID3 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 3 LID value		JESD204B serial LID number for Lane 3.	0x3	R/W
0x0587	JESD204B LID4 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 4 LID value		JESD204B serial LID number for Lane 4.	0x4	R/W
0x0588	JESD204B LID5 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 5 LID value		JESD204B serial LID number for Lane 5.	0x5	R/W
0x0589	JESD204B LID6 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 6 LID value		JESD204B serial LID number for Lane 6.	0x6	R/W
0x058A	JESD204B LID7 configuration	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	Lane 7 LID value		JESD204B serial LID number for Lane 7.	0x7	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x058B	JESD204B scrambling and number lanes (L) configuration	7	JESD204B scrambling (SCR)			0x1	R/W
				0	JESD204B scrambler disabled (SCR = 0).		
				1	JESD204B scrambler enabled (SCR = 1).		
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B lanes (L)			0x7	R/W
				0x0	One lane per link (L = 1).		
				0x1	Two lanes per link (L = 2).		
				0x3	Four lanes per link (L = 4).		
				0x7	Eight lanes per Link (L = 8).		
0x058C	JESD204B link number of octets per frames (F)	[7:0]	JESD204B F configuration		JESD204B number of octets per frame (F = JESD204B F configuration + 1).	0x0	R/W
				0	F = 1.		
				1	F = 2.		
				10	F = 3.		
				11	F = 4.		
				101	F = 6.		
				111	F = 8.		
				1111	F = 16.		
0x058D	JESD204B link number of frames per multiframe (K)	[7:5]	Reserved		Reserved.	0x0	R
		[4:0]	JESD204B K configuration		JESD204B number of frames per multiframe (K = JESD204B K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x1F	R/W
0x058E	JESD204B link number of converters (M)	[7:0]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B M configuration).	0x1	R/W
				0	Link connected to one virtual converter (M = 1).		
				1	Link connected to two virtual converters (M = 2).		
				11	Link connected to four virtual converters (M = 4).		
				111	Link connected to eight virtual converters (M = 8).		
0x058F	JESD204B number of control bits (CS) and ADC resolution (N)	[7:6]	Number of control bits (CS) per sample			0x0	R/W
				0	No control bits (CS = 0).		
				1	1 control bit (CS = 1), Control Bit 2 only.		
				10	2 control bits (CS = 2), Control Bit 2 and Control Bit 1only.		
				11	3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).		
		5	Reserved		Reserved.	0x0	R
		[4:0]	ADC converter resolution (N)			0xF	R/W
				00110	N = 7-bit resolution.		
				00111	N = 8-bit resolution.		
				01000	N = 9-bit resolution.		
				01001	N = 10-bit resolution.		
				01010	N = 11-bit resolution.		
				01011	N = 12-bit resolution.		
				01100	N = 13-bit resolution.		
				01101	N = 14-bit resolution.		
				01110	N = 15-bit resolution.		
				01111	N = 16-bit resolution.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0590	JESD204B SCV NP configuration	[7:5]	Subclass support	000 001	Subclass 0. Subclass 1.	0x1	R/W
		[4:0]	ADC number of bits per sample(N')	0 0111 0 1011 0 1111	N' = 8. N' = 12 N' = 16.	0xF	R/W
0x0591	JESD204B JV S configuration	[7:5]	Reserved		Reserved.	0x1	R
		[4:0]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[4:0] + 1).	0x0	R
0x0592	JESD204B HD CF configuration	7	HD value	0 1	High density format disabled. High density format enabled.	0x0	R
		[6:5]	Reserved		Reserved.	0x0	R
		[4:0]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link (CF = Register 0x0592, Bits[4:0]).	0x0	R
0x05A0	JESD204B Checksum 0 configuration	[7:0]	Checksum 0 checksum value for SERDOUT0±		Serial checksum value for Lane 0. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 0) mod 256.	0xC3	R
0x05A1	JESD204B Checksum 1 configuration	[7:0]	Checksum 1 checksum value for SERDOUT1±		Serial checksum value for Lane 1. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 1) mod 256.	0xC4	R
0x05A2	JESD204B Checksum 2 configuration	[7:0]	Checksum 2 checksum value for SERDOUT2±		Serial checksum value for Lane 2. Automatically calculated for each lane. Sum(all link configuration parameters for each lane) mod 256.	0xC5	R
0x05A3	JESD204B Checksum 3 configuration	[7:0]	Checksum 3 checksum value for SERDOUT3±		Serial checksum value for Lane 3. Automatically calculated for each lane. Sum(all link configuration parameters for Lane 3) mod 256.	0xC6	R
0x05B0	JESD204B lane power-down	7	JESD204B Lane 7 power-down	0 1	Physical Lane 7 force power-down. SERDOUT7± normal operation. SERDOUT7± power-down.	0x0	R/W
		6	JESD204B Lane 6 power-down	0 1	Physical Lane 6 force power-down. SERDOUT6± normal operation. SERDOUT6± power-down.	0x0	R/W
		5	JESD204B Lane 5 power-down	0 1	Physical Lane 5 force power-down. SERDOUT5± normal operation. SERDOUT5± power-down.	0x0	R/W
		4	JESD204B Lane 4 power-down	0 1	Physical Lane 4 force power-down. SERDOUT4± normal operation. SERDOUT4± power-down.	0x0	R/W
		3	JESD204B Lane 3 power-down	0 1	Physical Lane 3 force power-down. SERDOUT3± normal operation. SERDOUT3± power-down.	0x0	R/W
		2	JESD204B Lane 2 power-down	0 1	Physical Lane 2 force power-down. SERDOUT2± normal operation. SERDOUT2± power-down.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		1	JESD204B Lane 1 power-down		Physical Lane 1 force power-down.	0x0	R/W
				0	SERDOUT1± normal operation.		
				1	SERDOUT1± power-down.		
		0	JESD204B Lane 0 power-down		Physical Lane 0 force power-down.	0x0	R/W
				0	SERDOUT0± normal operation.		
				1	SERDOUT0± power-down.		
0x05B2	JESD204B Lane Assign 1	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT1± lane assignment		Physical Lane 1 assignment.	0x1	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1 (default).		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT0± lane assignment		Physical Lane 0 assignment.	0x0	R/W
				0	Logical Lane 0 (default).		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7.		
0x05B3	JESD204B Lane Assign 2	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT3± lane assignment		Physical Lane 3 assignment.	0x3	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3 (default).		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT2± lane assignment		Physical Lane 2 assignment.	0x2	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2 (default).		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x05B5	JESD204B Lane Assign 3	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT5± lane assignment		Physical Lane 5 assignment.	0x5	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5 (default).		
				110	Logical Lane 6.		
				111	Logical Lane 7.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT4± lane assignment		Physical Lane 4 assignment.	0x4	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4 (default).		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7.		
0x05B6	JESD204B Lane Assign 4	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT7± lane assignment		Physical Lane 7 assignment.	0x7	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6.		
				111	Logical Lane 7 (default).		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT6± lane assignment		Physical Lane 6 assignment.	0x6	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				110	Logical Lane 6 (default).		
				111	Logical Lane 7.		
0x05BF	SERDOUTx± data invert	7	Invert SERDOUT7± data		Invert SERDOUT7± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		6	Invert SERDOUT6± data		Invert SERDOUT6± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		5	Invert SERDOUT5± data		Invert SERDOUT5± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		4	Invert SERDOUT4± data		Invert SERDOUT4± data.	0x0	R/W
				0	Normal.		
				1	Invert.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		3	Invert SERDOUT3± data		Invert SERDOUT3± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		2	Invert SERDOUT2± data		Invert SERDOUT2± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		1	Invert SERDOUT1± data		Invert SERDOUT1± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		0	Invert SERDOUT0± data		Invert SERDOUT0± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
0x05C0	JESD204B Swing Adjust 1	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT1± voltage swing adjust		Output swing level for SERDOUT1±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT0± voltage swing adjust		Output swing level for SERDOUT0±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
0x05C1	JESD204B Swing Adjust 2	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT3± voltage swing adjust		Output swing level for SERDOUT3±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT2± voltage swing adjust		Output swing level for SERDOUT2±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
0x05C2	JESD204B Swing Adjust 3	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT5± voltage swing adjust		Output swing level for SERDOUT5±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	SERDOUT4± voltage swing adjust		Output swing level for SERDOUT4±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
0x05C3	JESD204B Swing Adjust 4	7	Reserved		Reserved.	0x0	R
		[6:4]	SERDOUT7± voltage swing adjust		Output swing level for SERDOUT7±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
		3	Reserved		Reserved.	0x0	R

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
		[2:0]	SERDOUT6± voltage swing adjust		Output swing level for SERDOUT6±.	0x1	R/W
				000	1.0 × DRVDD1.		
				001	0.850 × DRVDD1.		
				010	0.750 × DRVDD1.		
0x05C4	SERDOUT0 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT0±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C5	SERDOUT1 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT1±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C6	SERDOUT2 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT2±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C7	SERDOUT3 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT3±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x05C8	SERDOUT4 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT4±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05C9	SERDOUT5 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT5±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05CA	SERDOUT6 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT6±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x05CB	SERDOUT7 pre-emphasis select	7	Post tap enable		Post tap enable.	0x0	R/W
				0	Disable.		
				1	Enable.		
		[6:4]	Set post tap level for SERDOUT7±		Set post tap level.	0x0	R/W
				000	0 dB.		
				001	3 dB.		
				010	6 dB.		
				011	9 dB.		
				100	12 dB.		
		[3:0]	Reserved		Reserved.	0x0	R/W
0x1222	JESD204B PLL calibration	[7:0]			See Table 32.	0x00	R/W
				0x00	JESD204B PLL normal operation.		
				0x04	Reset JESD204B PLL calibration.		
0x1228	JESD204B PLL startup control	[7:0]			See Table 32.	0x0F	R/W
				0x0F	JESD204B startup circuit in normal operation.		
				0x4F	Reset JESD204B startup circuit.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x1262	JESD204B PLL LOL bit control	[7:0]			See Table 32.	0x00	R/W
				0x00	Loss of lock bit normal operation.		
				0x80	Clear loss of lock bit.		

Programmable Filter Control and Coefficients Registers

Table 52.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0DF8	PFILT control	[7:3]	Reserved		Reserved.	0x0	R
		[2:0]	PFILT mode		Programmable filter (PFILT) mode.	0x0	R/W
				000	Disabled (filters bypassed).		
				001	Single filter (X only). dout_i[n] = din_i[n] * x_i[n] dout_q[n] = din_q[n] * x_q[n]		
				010	Single filter (X and Y together) dout_i[n] = din_i[n] * xy_i[n] dout_q[n] = din_q[n] * xy_q[n]		
				100	Cascaded filters (X to Y). dout_i[n] = din_i[n] * x_i[n] * y_i[n] dout_q[n] = din_q[n] * x_q[n] * y_q[n] dout_q[n] = din_q[n] * x_q[n] * y_q[n]		
				101	Complex filters. dout_i[n] = din_i[n] * x_i[n] + din_q[n] * y_q[n] dout_q[n] = din_q[n] * x_q[n] + din_i[n] * y_i[n]		
				110	Half complex filter. dout_i[n] = din_i[n] dout_q[n] = din_q[n] * xy_q[n] + din_i[n] * xy_i[n]		
				111	Real 96-tap filter. dout_i[n] = din_i[n] * xy_i[n]. dout_q[n] = din_q[n] * xy_q[n]		
0x0DF9	PFILT gain	7	Reserved		Reserved.	0x0	R
		[6:4]	PFILT Y gain		PFILT Y gain.	0x0	R/W
				110	−12 dB loss.		
				111	−6 dB loss.		
				000	0 dB gain.		
				001	+6 dB gain.		
				010	+12 dB gain.		
		3	Reserved		Reserved.	0x0	R
		[2:0]	PFILT X gain		PFILT X gain.	0x0	R/W
				110	−12 dB loss.		
				111	−6 dB loss.		
				000	0 dB gain.		
				001	+6 dB gain.		
				010	+12 dB gain.		
0x0E00	PFILT X Coefficient 0	[7:0]	PFILT X Coefficient 0		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E01	PFILT X Coefficient 1	[7:0]	PFILT X Coefficient 1		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E02	PFILT X Coefficient 2	[7:0]	PFILT X Coefficient 2		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E03	PFILT X Coefficient 3	[7:0]	PFILT X Coefficient 3		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E04	PFILT X Coefficient 4	[7:0]	PFILT X Coefficient 4		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E05	PFILT X Coefficient 5	[7:0]	PFILT X Coefficient 5		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E06	PFILT X Coefficient 6	[7:0]	PFILT X Coefficient 6		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0E07	PFILT X Coefficient 7	[7:0]	PFILT X Coefficient 7		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E08	PFILT X Coefficient 8	[7:0]	PFILT X Coefficient 8		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E09	PFILT X Coefficient 9	[7:0]	PFILT X Coefficient 9		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0A	PFILT X Coefficient 10	[7:0]	PFILT X Coefficient 10		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0B	PFILT X Coefficient 11	[7:0]	PFILT X Coefficient 11		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0C	PFILT X Coefficient 12	[7:0]	PFILT X Coefficient 12		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0D	PFILT X Coefficient 13	[7:0]	PFILT X Coefficient 13		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0E	PFILT X Coefficient 14	[7:0]	PFILT X Coefficient 14		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E0F	PFILT X Coefficient 15	[7:0]	PFILT X Coefficient 15		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E10	PFILT X Coefficient 16	[7:0]	PFILT X Coefficient 16		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E11	PFILT X Coefficient 17	[7:0]	PFILT X Coefficient 17		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E12	PFILT X Coefficient 18	[7:0]	PFILT X Coefficient 18		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E13	PFILT X Coefficient 19	[7:0]	PFILT X Coefficient 19		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E14	PFILT X Coefficient 20	[7:0]	PFILT X Coefficient 20		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E15	PFILT X Coefficient 21	[7:0]	PFILT X Coefficient 21		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E16	PFILT X Coefficient 22	[7:0]	PFILT X Coefficient 22		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E17	PFILT X Coefficient 23	[7:0]	PFILT X Coefficient 23		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E18	PFILT X Coefficient 24	[7:0]	PFILT X Coefficient 24		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E19	PFILT X Coefficient 25	[7:0]	PFILT X Coefficient 25		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1A	PFILT X Coefficient 26	[7:0]	PFILT X Coefficient 26		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1B	PFILT X Coefficient 27	[7:0]	PFILT X Coefficient 27		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1C	PFILT X Coefficient 28	[7:0]	PFILT X Coefficient 28		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1D	PFILT X Coefficient 29	[7:0]	PFILT X Coefficient 29		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1E	PFILT X Coefficient 30	[7:0]	PFILT X Coefficient 30		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E1F	PFILT X Coefficient 31	[7:0]	PFILT X Coefficient 31		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E20	PFILT X Coefficient 32	[7:0]	PFILT X Coefficient 32		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E21	PFILT X Coefficient 33	[7:0]	PFILT X Coefficient 33		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E22	PFILT X Coefficient 34	[7:0]	PFILT X Coefficient 34		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E23	PFILT X Coefficient 35	[7:0]	PFILT X Coefficient 35		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E24	PFILT X Coefficient 36	[7:0]	PFILT X Coefficient 36		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E25	PFILT X Coefficient 37	[7:0]	PFILT X Coefficient 37		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E26	PFILT X Coefficient 38	[7:0]	PFILT X Coefficient 38		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0E27	PFILT X Coefficient 39	[7:0]	PFILT X Coefficient 39		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E28	PFILT X Coefficient 40	[7:0]	PFILT X Coefficient 40		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E29	PFILT X Coefficient 41	[7:0]	PFILT X Coefficient 41		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2A	PFILT X Coefficient 42	[7:0]	PFILT X Coefficient 42		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2B	PFILT X Coefficient 43	[7:0]	PFILT X Coefficient 43		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2C	PFILT X Coefficient 44	[7:0]	PFILT X Coefficient 44		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2D	PFILT X Coefficient 45	[7:0]	PFILT X Coefficient 45		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2E	PFILT X Coefficient 46	[7:0]	PFILT X Coefficient 46		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E2F	PFILT X Coefficient 47	[7:0]	PFILT X Coefficient 47		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E30	PFILT X Coefficient 48	[7:0]	PFILT X Coefficient 48		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E31	PFILT X Coefficient 49	[7:0]	PFILT X Coefficient 49		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E32	PFILT X Coefficient 50	[7:0]	PFILT X Coefficient 50		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E33	PFILT X Coefficient 51	[7:0]	PFILT X Coefficient 51		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E34	PFILT X Coefficient 52	[7:0]	PFILT X Coefficient 52		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E35	PFILT X Coefficient 53	[7:0]	PFILT X Coefficient 53		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E36	PFILT X Coefficient 54	[7:0]	PFILT X Coefficient 54		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E37	PFILT X Coefficient 55	[7:0]	PFILT X Coefficient 55		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E38	PFILT X Coefficient 56	[7:0]	PFILT X Coefficient 56		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E39	PFILT X Coefficient 57	[7:0]	PFILT X Coefficient 57		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3A	PFILT X Coefficient 58	[7:0]	PFILT X Coefficient 58		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3B	PFILT X Coefficient 59	[7:0]	PFILT X Coefficient 59		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3C	PFILT X Coefficient 60	[7:0]	PFILT X Coefficient 60		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3D	PFILT X Coefficient 61	[7:0]	PFILT X Coefficient 61		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3E	PFILT X Coefficient 62	[7:0]	PFILT X Coefficient 62		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E3F	PFILT X Coefficient 63	[7:0]	PFILT X Coefficient 63		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E40	PFILT X Coefficient 64	[7:0]	PFILT X Coefficient 64		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E41	PFILT X Coefficient 65	[7:0]	PFILT X Coefficient 65		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E42	PFILT X Coefficient 66	[7:0]	PFILT X Coefficient 66		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E43	PFILT X Coefficient 67	[7:0]	PFILT X Coefficient 67		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E44	PFILT X Coefficient 68	[7:0]	PFILT X Coefficient 68		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E45	PFILT X Coefficient 69	[7:0]	PFILT X Coefficient 69		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E46	PFILT X Coefficient 70	[7:0]	PFILT X Coefficient 70		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0E47	PFILT X Coefficient 71	[7:0]	PFILT X Coefficient 71		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E48	PFILT X Coefficient 72	[7:0]	PFILT X Coefficient 72		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E49	PFILT X Coefficient 73	[7:0]	PFILT X Coefficient 73		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4A	PFILT X Coefficient 74	[7:0]	PFILT X Coefficient 74		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4B	PFILT X Coefficient 75	[7:0]	PFILT X Coefficient 75		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4C	PFILT X Coefficient 76	[7:0]	PFILT X Coefficient 76		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4D	PFILT X Coefficient 77	[7:0]	PFILT X Coefficient 77		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4E	PFILT X Coefficient 78	[7:0]	PFILT X Coefficient 78		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E4F	PFILT X Coefficient 79	[7:0]	PFILT X Coefficient 79		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E50	PFILT X Coefficient 80	[7:0]	PFILT X Coefficient 80		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E51	PFILT X Coefficient 81	[7:0]	PFILT X Coefficient 81		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E52	PFILT X Coefficient 82	[7:0]	PFILT X Coefficient 82		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E53	PFILT X Coefficient 83	[7:0]	PFILT X Coefficient 83		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E54	PFILT X Coefficient 84	[7:0]	PFILT X Coefficient 84		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E55	PFILT X Coefficient 85	[7:0]	PFILT X Coefficient 85		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E56	PFILT X Coefficient 86	[7:0]	PFILT X Coefficient 86		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E57	PFILT X Coefficient 87	[7:0]	PFILT X Coefficient 87		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E58	PFILT X Coefficient 88	[7:0]	PFILT X Coefficient 88		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E59	PFILT X Coefficient 89	[7:0]	PFILT X Coefficient 89		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5A	PFILT X Coefficient 90	[7:0]	PFILT X Coefficient 90		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5B	PFILT X Coefficient 91	[7:0]	PFILT X Coefficient 91		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5C	PFILT X Coefficient 92	[7:0]	PFILT X Coefficient 92		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5D	PFILT X Coefficient 93	[7:0]	PFILT X Coefficient 93		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5E	PFILT X Coefficient 94	[7:0]	PFILT X Coefficient 94		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E5F	PFILT X Coefficient 95	[7:0]	PFILT X Coefficient 95		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E60	PFILT X Coefficient 96	[7:0]	PFILT X Coefficient 96		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E61	PFILT X Coefficient 97	[7:0]	PFILT X Coefficient 97		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E62	PFILT X Coefficient 98	[7:0]	PFILT X Coefficient 98		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E63	PFILT X Coefficient 99	[7:0]	PFILT X Coefficient 99		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E64	PFILT X Coefficient 100	[7:0]	PFILT X Coefficient 100		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E65	PFILT X Coefficient 101	[7:0]	PFILT X Coefficient 101		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E66	PFILT X Coefficient 102	[7:0]	PFILT X Coefficient 102		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0E67	PFILT X Coefficient 103	[7:0]	PFILT X Coefficient 103		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E68	PFILT X Coefficient 104	[7:0]	PFILT X Coefficient 104		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E69	PFILT X Coefficient 105	[7:0]	PFILT X Coefficient 105		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6A	PFILT X Coefficient 106	[7:0]	PFILT X Coefficient 106		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6B	PFILT X Coefficient 107	[7:0]	PFILT X Coefficient 107		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6C	PFILT X Coefficient 108	[7:0]	PFILT X Coefficient 108		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6D	PFILT X Coefficient 109	[7:0]	PFILT X Coefficient 109		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6E	PFILT X Coefficient 110	[7:0]	PFILT X Coefficient 110		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E6F	PFILT X Coefficient 111	[7:0]	PFILT X Coefficient 111		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E70	PFILT X Coefficient 112	[7:0]	PFILT X Coefficient 112		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E71	PFILT X Coefficient 113	[7:0]	PFILT X Coefficient 113		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E72	PFILT X Coefficient 114	[7:0]	PFILT X Coefficient 114		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E73	PFILT X Coefficient 115	[7:0]	PFILT X Coefficient 115		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E74	PFILT X Coefficient 116	[7:0]	PFILT X Coefficient 116		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E75	PFILT X Coefficient 117	[7:0]	PFILT X Coefficient 117		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E76	PFILT X Coefficient 118	[7:0]	PFILT X Coefficient 118		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E77	PFILT X Coefficient 119	[7:0]	PFILT X Coefficient 119		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E78	PFILT X Coefficient 120	[7:0]	PFILT X Coefficient 120		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E79	PFILT X Coefficient 121	[7:0]	PFILT X Coefficient 121		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7A	PFILT X Coefficient 122	[7:0]	PFILT X Coefficient 122		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7B	PFILT X Coefficient 123	[7:0]	PFILT X Coefficient 123		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7C	PFILT X Coefficient 124	[7:0]	PFILT X Coefficient 124		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7D	PFILT X Coefficient 125	[7:0]	PFILT X Coefficient 125		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7E	PFILT X Coefficient 126	[7:0]	PFILT X Coefficient 126		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0E7F	PFILT X Coefficient 127	[7:0]	PFILT X Coefficient 127		Programmable Filter X coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F00	PFILT Y Coefficient 0	[7:0]	PFILT Y Coefficient 0		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F01	PFILT Y Coefficient 1	[7:0]	PFILT Y Coefficient 1		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F02	PFILT Y Coefficient 2	[7:0]	PFILT Y Coefficient 2		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F03	PFILT Y Coefficient 3	[7:0]	PFILT Y Coefficient 3		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F04	PFILT Y Coefficient 4	[7:0]	PFILT Y Coefficient 4		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F05	PFILT Y Coefficient 5	[7:0]	PFILT Y Coefficient 5		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F06	PFILT Y Coefficient 6	[7:0]	PFILT Y Coefficient 6		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0F07	PFILT Y Coefficient 7	[7:0]	PFILT Y Coefficient 7		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F08	PFILT Y Coefficient 8	[7:0]	PFILT Y Coefficient 8		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F09	PFILT Y Coefficient 9	[7:0]	PFILT Y Coefficient 9		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0A	PFILT Y Coefficient 10	[7:0]	PFILT Y Coefficient 10		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0B	PFILT Y Coefficient 11	[7:0]	PFILT Y Coefficient 11		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0C	PFILT Y Coefficient 12	[7:0]	PFILT Y Coefficient 12		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0D	PFILT Y Coefficient 13	[7:0]	PFILT Y Coefficient 13		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0E	PFILT Y Coefficient 14	[7:0]	PFILT Y Coefficient 14		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F0F	PFILT Y Coefficient 15	[7:0]	PFILT Y Coefficient 15		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F10	PFILT Y Coefficient 16	[7:0]	PFILT Y Coefficient 16		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F11	PFILT Y Coefficient 17	[7:0]	PFILT Y Coefficient 17		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F12	PFILT Y Coefficient 18	[7:0]	PFILT Y Coefficient 18		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F13	PFILT Y Coefficient 19	[7:0]	PFILT Y Coefficient 19		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F14	PFILT Y Coefficient 20	[7:0]	PFILT Y Coefficient 20		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F15	PFILT Y Coefficient 21	[7:0]	PFILT Y Coefficient 21		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F16	PFILT Y Coefficient 22	[7:0]	PFILT Y Coefficient 22		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F17	PFILT Y Coefficient 23	[7:0]	PFILT Y Coefficient 23		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F18	PFILT Y Coefficient 24	[7:0]	PFILT Y Coefficient 24		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F19	PFILT Y Coefficient 25	[7:0]	PFILT Y Coefficient 25		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1A	PFILT Y Coefficient 26	[7:0]	PFILT Y Coefficient 26		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1B	PFILT Y Coefficient 27	[7:0]	PFILT Y Coefficient 27		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1C	PFILT Y Coefficient 28	[7:0]	PFILT Y Coefficient 28		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1D	PFILT Y Coefficient 29	[7:0]	PFILT Y Coefficient 29		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1E	PFILT Y Coefficient 30	[7:0]	PFILT Y Coefficient 30		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F1F	PFILT Y Coefficient 31	[7:0]	PFILT Y Coefficient 31		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F20	PFILT Y Coefficient 32	[7:0]	PFILT Y Coefficient 32		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F21	PFILT Y Coefficient 33	[7:0]	PFILT Y Coefficient 33		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F22	PFILT Y Coefficient 34	[7:0]	PFILT Y Coefficient 34		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F23	PFILT Y Coefficient 35	[7:0]	PFILT Y Coefficient 35		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F24	PFILT Y Coefficient 36	[7:0]	PFILT Y Coefficient 36		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F25	PFILT Y Coefficient 37	[7:0]	PFILT Y Coefficient 37		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F26	PFILT Y Coefficient 38	[7:0]	PFILT Y Coefficient 38		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0F27	PFILT Y Coefficient 39	[7:0]	PFILT Y Coefficient 39		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F28	PFILT Y Coefficient 40	[7:0]	PFILT Y Coefficient 40		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F29	PFILT Y Coefficient 41	[7:0]	PFILT Y Coefficient 41		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2A	PFILT Y Coefficient 42	[7:0]	PFILT Y Coefficient 42		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2B	PFILT Y Coefficient 43	[7:0]	PFILT Y Coefficient 43		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2C	PFILT Y Coefficient 44	[7:0]	PFILT Y Coefficient 44		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2D	PFILT Y Coefficient 45	[7:0]	PFILT Y Coefficient 45		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2E	PFILT Y Coefficient 46	[7:0]	PFILT Y Coefficient 46		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F2F	PFILT Y Coefficient 47	[7:0]	PFILT Y Coefficient 47		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F30	PFILT Y Coefficient 48	[7:0]	PFILT Y Coefficient 48		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F31	PFILT Y Coefficient 49	[7:0]	PFILT Y Coefficient 49		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F32	PFILT Y Coefficient 50	[7:0]	PFILT Y Coefficient 50		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F33	PFILT Y Coefficient 51	[7:0]	PFILT Y Coefficient 51		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F34	PFILT Y Coefficient 52	[7:0]	PFILT Y Coefficient 52		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F35	PFILT Y Coefficient 53	[7:0]	PFILT Y Coefficient 53		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F36	PFILT Y Coefficient 54	[7:0]	PFILT Y Coefficient 54		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F37	PFILT Y Coefficient 55	[7:0]	PFILT Y Coefficient 55		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F38	PFILT Y Coefficient 56	[7:0]	PFILT Y Coefficient 56		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F39	PFILT Y Coefficient 57	[7:0]	PFILT Y Coefficient 57		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3A	PFILT Y Coefficient 58	[7:0]	PFILT Y Coefficient 58		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3B	PFILT Y Coefficient 59	[7:0]	PFILT Y Coefficient 59		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3C	PFILT Y Coefficient 60	[7:0]	PFILT Y Coefficient 60		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3D	PFILT Y Coefficient 61	[7:0]	PFILT Y Coefficient 61		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3E	PFILT Y Coefficient 62	[7:0]	PFILT Y Coefficient 62		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F3F	PFILT Y Coefficient 63	[7:0]	PFILT Y Coefficient 63		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F40	PFILT Y Coefficient 64	[7:0]	PFILT Y Coefficient 64		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F41	PFILT Y Coefficient 65	[7:0]	PFILT Y Coefficient 65		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F42	PFILT Y Coefficient 66	[7:0]	PFILT Y Coefficient 66		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F43	PFILT Y Coefficient 67	[7:0]	PFILT Y Coefficient 67		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F44	PFILT Y Coefficient 68	[7:0]	PFILT Y Coefficient 68		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F45	PFILT Y Coefficient 69	[7:0]	PFILT Y Coefficient 69		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F46	PFILT Y Coefficient 70	[7:0]	PFILT Y Coefficient 70		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0F47	PFILT Y Coefficient 71	[7:0]	PFILT Y Coefficient 71		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F48	PFILT Y Coefficient 72	[7:0]	PFILT Y Coefficient 72		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F49	PFILT Y Coefficient 73	[7:0]	PFILT Y Coefficient 73		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4A	PFILT Y Coefficient 74	[7:0]	PFILT Y Coefficient 74		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4B	PFILT Y Coefficient 75	[7:0]	PFILT Y Coefficient 75		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4C	PFILT Y Coefficient 76	[7:0]	PFILT Y Coefficient 76		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4D	PFILT Y Coefficient 77	[7:0]	PFILT Y Coefficient 77		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4E	PFILT Y Coefficient 78	[7:0]	PFILT Y Coefficient 78		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F4F	PFILT Y Coefficient 79	[7:0]	PFILT Y Coefficient 79		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F50	PFILT Y Coefficient 80	[7:0]	PFILT Y Coefficient 80		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F51	PFILT Y Coefficient 81	[7:0]	PFILT Y Coefficient 81		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F52	PFILT Y Coefficient 82	[7:0]	PFILT Y Coefficient 82		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F53	PFILT Y Coefficient 83	[7:0]	PFILT Y Coefficient 83		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F54	PFILT Y Coefficient 84	[7:0]	PFILT Y Coefficient 84		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F55	PFILT Y Coefficient 85	[7:0]	PFILT Y Coefficient 85		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F56	PFILT Y Coefficient 86	[7:0]	PFILT Y Coefficient 86		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F57	PFILT Y Coefficient 87	[7:0]	PFILT Y Coefficient 87		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F58	PFILT Y Coefficient 88	[7:0]	PFILT Y Coefficient 88		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F59	PFILT Y Coefficient 89	[7:0]	PFILT Y Coefficient 89		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5A	PFILT Y Coefficient 90	[7:0]	PFILT Y Coefficient 90		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5B	PFILT Y Coefficient 91	[7:0]	PFILT Y Coefficient 91		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5C	PFILT Y Coefficient 92	[7:0]	PFILT Y Coefficient 92		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5D	PFILT Y Coefficient 93	[7:0]	PFILT Y Coefficient 93		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5E	PFILT Y Coefficient 94	[7:0]	PFILT Y Coefficient 94		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F5F	PFILT Y Coefficient 95	[7:0]	PFILT Y Coefficient 95		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F60	PFILT Y Coefficient 96	[7:0]	PFILT Y Coefficient 96		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F61	PFILT Y Coefficient 97	[7:0]	PFILT Y Coefficient 97		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F62	PFILT Y Coefficient 98	[7:0]	PFILT Y Coefficient 98		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F63	PFILT Y Coefficient 99	[7:0]	PFILT Y Coefficient 99		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F64	PFILT Y Coefficient 100	[7:0]	PFILT Y Coefficient 100		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F65	PFILT Y Coefficient 101	[7:0]	PFILT Y Coefficient 101		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F66	PFILT Y Coefficient 102	[7:0]	PFILT Y Coefficient 102		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0F67	PFILT Y Coefficient 103	[7:0]	PFILT Y Coefficient 103		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F68	PFILT Y Coefficient 104	[7:0]	PFILT Y Coefficient 104		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F69	PFILT Y Coefficient 105	[7:0]	PFILT Y Coefficient 105		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6A	PFILT Y Coefficient 106	[7:0]	PFILT Y Coefficient 106		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6B	PFILT Y Coefficient 107	[7:0]	PFILT Y Coefficient 107		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6C	PFILT Y Coefficient 108	[7:0]	PFILT Y Coefficient 108		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6D	PFILT Y Coefficient 109	[7:0]	PFILT Y Coefficient 109		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6E	PFILT Y Coefficient 110	[7:0]	PFILT Y Coefficient 110		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F6F	PFILT Y Coefficient 111	[7:0]	PFILT Y Coefficient 111		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F70	PFILT Y Coefficient 112	[7:0]	PFILT Y Coefficient 112		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F71	PFILT Y Coefficient 113	[7:0]	PFILT Y Coefficient 113		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F72	PFILT Y Coefficient 114	[7:0]	PFILT Y Coefficient 114		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F73	PFILT Y Coefficient 115	[7:0]	PFILT Y Coefficient 115		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F74	PFILT Y Coefficient 116	[7:0]	PFILT Y Coefficient 116		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F75	PFILT Y Coefficient 117	[7:0]	PFILT Y Coefficient 117		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F76	PFILT Y Coefficient 118	[7:0]	PFILT Y Coefficient 118		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F77	PFILT Y Coefficient 119	[7:0]	PFILT Y Coefficient 119		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F78	PFILT Y Coefficient 120	[7:0]	PFILT Y Coefficient 120		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F79	PFILT Y Coefficient 121	[7:0]	PFILT Y Coefficient 121		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7A	PFILT Y Coefficient 122	[7:0]	PFILT Y Coefficient 122		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7B	PFILT Y Coefficient 123	[7:0]	PFILT Y Coefficient 123		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7C	PFILT Y Coefficient 124	[7:0]	PFILT Y Coefficient 124		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7D	PFILT Y Coefficient 125	[7:0]	PFILT Y Coefficient 125		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7E	PFILT Y Coefficient 126	[7:0]	PFILT Y Coefficient 126		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W
0x0F7F	PFILT Y Coefficient 127	[7:0]	PFILT Y Coefficient 127		Programmable Filter Y coefficients. Coefficients are only applied after the chip transfer bit has been written.	0x0	R/W

VREF/Analog Input Control Registers

Table 53.

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x0701	DC offset calibration control (local)	[7:0]	DC offset calibration control			0x06	R/W
				0x06	Disable.		
				0x86	Enable.		
0x18A6	VREF control	[7:1]	Reserved		Reserved.	0x0	R
		0	VREF control			0x0	R/W
				0	Internal reference.		
				1	External reference.		
0x18E3	External VCM buffer control	7	Reserved		Reserved.	0x0	R
		6	External VCM buffer			0x0	R/W
				0	Disable.		
				1	Enable.		
		[5:0]	External VCM buffer[5:0]		See the Input Common Mode section.	0x0	R/W
0x18E6	Temperature diode export	[7:0]	Temperature diode location select			0x0	R/W
				0x00	Central diode. VREF pin = high-Z.		
				0x01	Central diode. VREF pin = 1× diode voltage output.		
				0x02	Central diode. VREF pin = 20× diode voltage output.		
				0x03	Central diode. VREF pin = GND.		
				0x40	Channel A diode. VREF pin = high-Z.		
				0x41	Channel A diode. VREF pin = 1× diode voltage output.		
				0x42	Channel A diode. VREF pin = 20× diode voltage output.		
				0x43	Channel A diode. VREF pin = GND.		
				0x50	Channel B diode. VREF pin = high-Z.		
				0x51	Channel B diode. VREF pin = 1× diode voltage output.		
				0x52	Channel B diode. VREF pin = 20× diode voltage output.		
				0x53	Channel B diode. VREF pin = GND.		
0x1908	Analog input control (local)	[7:3]	Reserved		Reserved.	0x0	R
		2	Enable dc coupling			0x0	R/W
				0	Analog input is optimized for ac coupling.		
				1	Analog input is optimized for dc coupling.		
		[1:0]	Reserved		Reserved.	0x0	R
0x1910	Input full-scale control (local)	[7:4]	Reserved		Reserved.	0x0	R
		[3:0]	TRM VREF 1P8		Full-scale voltage setting.	0xD	R/W
				1000	1.13 V p-p differential.		
				1001	1.25 V p-p differential.		
				1101	1.7 V p-p differential.		
				1110	1.81 V p-p differential.		
				1111	1.93 V p-p differential.		
				0000	2.04 V p-p differential.		

Addr.	Name	Bit(s)	Bit Name	Setting	Description	Reset	Access
0x1A4C	Buffer Control 1 (local)	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 1		Input Buffer Main Current 1. See the Analog Input Buffer Controls and SFDR Optimization section.	0x19	R/W
				00 0100	Buffer current set to 400 µA.		
				00 1001	Buffer current set to 500 µA.		
				01 1110	Buffer current set to 600 µA.		
				10 0011	Buffer current set to 700 µA.		
				10 1000	Buffer current set to 800 µA.		
				11 0010	Buffer current set to 1000 µA.		
0x1A4D	Buffer Control 2 (local)	[7:6]	Reserved		Reserved.	0x0	R
		[5:0]	Buffer Control 2		Input Buffer Main Current 2. See the Analog Input Buffer Controls and SFDR Optimization section.	0x19	R/W
				00 0100	Buffer current set to 400 µA.		
				00 1001	Buffer current set to 500 µA.		
				01 1110	Buffer current set to 600 µA.		
				10 0011	Buffer current set to 700 µA.		
				10 1000	Buffer current set to 800 µA.		
				11 0010	Buffer current set to 1000 µA.		

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The power supplies needed to power the AD6688 are shown in Table 54. A power on sequence is not required to operate the AD6688. The power supply domains can come up in any order.

Table 54. Typical Power Supplies for AD6688

Domain	Voltage (V)	Tolerance (%)
AVDD1	0.975	±2.5
AVDD1_SR	0.975	±2.5
DVDD	0.975	±2.5
DRVDD1	0.975	±2.5
AVDD2	1.9	±2.5
DRVDD2	1.9	±2.5
SPIVDD	1.9	±2.5
AVDD3	2.5	±2.5

For applications requiring an optimal high power efficiency and low noise performance, it is recommended that the ADP5054 quad switching regulator be used to convert a 6.0 V or 15 V input voltage to intermediate rails (1.3 V, 2.4 V, and 3.0 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1763, ADP7159, and ADP151). Figure 117 shows the recommended power supply scheme for the AD6688.

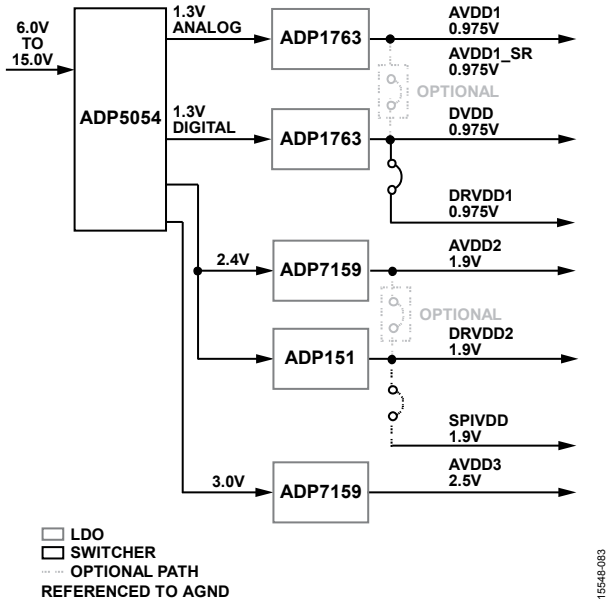


Figure 117. High Efficiency, Low Noise Power Solution for the AD6688

It is not necessary to split all of these power domains in all cases. The recommended solution shown in Figure 117 provides the lowest noise, highest efficiency power delivery system for the AD6688. If only one 0.975 V supply is available, route to AVDD1 first and then tap it off and isolate it with a ferrite bead or a filter choke, preceded by decoupling capacitors for AVDD1_SR, DVDD, and DRVDD1, in that order. Figure 118 shows the simplified schematic. The dc resistance (DCR) of the ferrite bead must be taken into consideration when choosing the appropriate ferrite bead. Otherwise, excessive loss across the ferrite bead can lead to a malfunctioning ADC. Adjustable LDOs can be employed to output a higher voltage to account for the drop across the ferrite bead.

Alternatively, the LDOs can be bypassed altogether and the AD6688 can be driven directly from the dc-to-dc converter. Note that this approach has risks in that there may be more power supply noise injected into the power supply domains of the ADC. To minimize noise, follow the layout guidelines of the dc-to-dc converter.

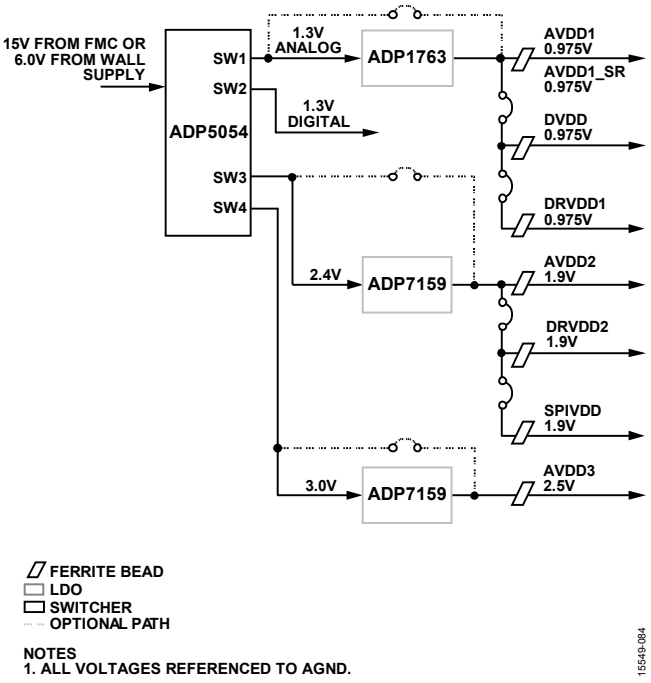


Figure 118. Simplified Power Solution for the AD6688

The user can employ several different decoupling capacitors to cover both high and low frequencies. These capacitors must be located close to the point of entry at the PCB level and close to the devices, with minimal trace lengths.

LAYOUT GUIDELINES

The ADC evaluation board can be used as a guide to follow good layout practices. The evaluation board layout is done in such a way as to

- Minimize coupling between the analog inputs (Channel A to Channel B and Channel B to Channel A).
- Minimize clock coupling to the analog inputs.
- Provide enough power and ground planes for the various supply domains while reducing cross coupling.
- Provide adequate thermal relief to the ADC.

Figure 119 shows the overall layout scheme used for the AD6688 evaluation board.

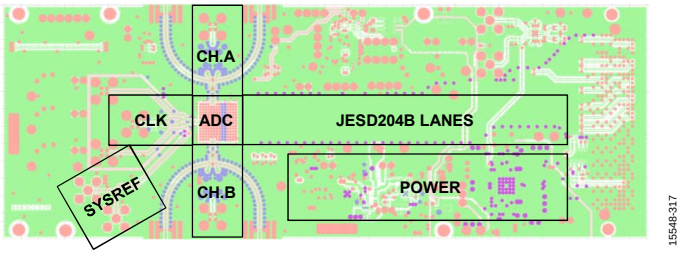
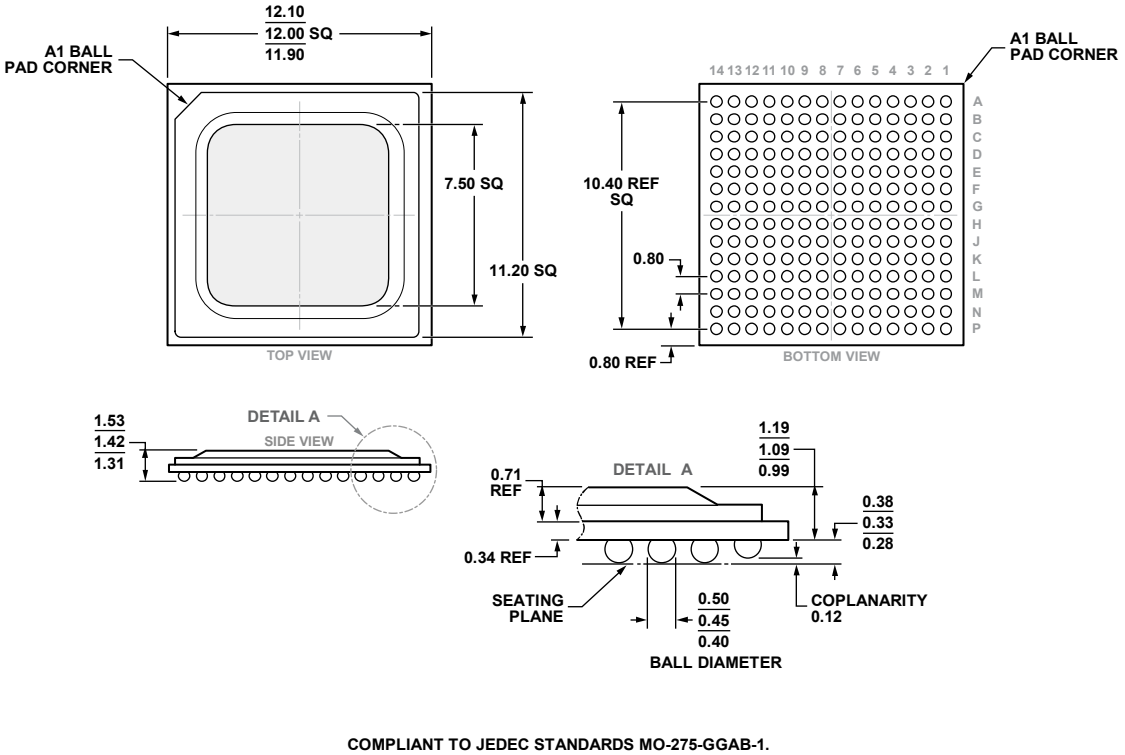


Figure 119. Recommended PCB Layout for the AD6688

AVDD1_SR (PIN E7) AND AGND (PIN E6 AND PIN E8)

AVDD1_SR (Pin E7) and AGND (Pin E6 and Pin E8) can be used to provide a separate power supply node to the SYSREF± circuits of the AD6688. If running in Subclass 1, the AD6688 can support periodic one-shot or gapped signals. To minimize the coupling of this supply into the AVDD1 supply node, adequate supply bypassing is needed.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 120. 196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
12 mm × 12 mm
(BP-196-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD6688BBPZ-3000	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-4
AD6688BBPZRL-3000	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-4
AD6688-3000EBZ		Evaluation Board for AD6688	

[1] Z = RoHS Compliant Part.

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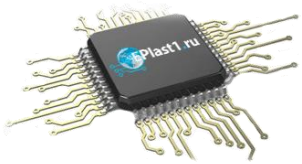
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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