

Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 123 Powerful Instructions – Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
- Non-volatile Program and Data Memories
 - 2/4/8K Byte of In-System Programmable Program Memory Flash
 - Endurance: 10,000 Write/Erase Cycles
 - 128/256/512 Bytes In-System Programmable EEPROM
 - Endurance: 100,000 Write/Erase Cycles
 - 128/256/512 Bytes Internal SRAM
 - Data retention: 20 years at 85°C / 100 years at 25°C
 - Programming Lock for Self-Programming Flash Program & EEPROM Data Security
- Peripheral Features
 - 8/16-bit Timer/Counter with Prescaler
 - 8/10-bit High Speed Timer/Counter with Separate Prescaler
 - 3 High Frequency PWM Outputs with Separate Output Compare Registers
 - Programmable Dead Time Generator
 - 10-bit ADC
 - 11 Single-Ended Channels
 - 16 Differential ADC Channel Pairs
 - 15 Differential ADC Channel Pairs with Programmable Gain (1x, 8x, 20x, 32x)
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with Separate On-chip Oscillator
 - Universal Serial Interface with Start Condition Detector
- Special Microcontroller Features
 - debugWIRE On-chip Debug System
 - In-System Programmable via SPI Port
 - External and Internal Interrupt Sources
 - Low Power Idle, ADC Noise Reduction, Standby and Power-Down Modes
 - Enhanced Power-on Reset Circuit
 - Programmable Brown-out Detection Circuit
 - Internal Calibrated Oscillator
 - On-chip Temperature Sensor
- I/O and Packages
 - 16 Programmable I/O Lines
 - Available in 20-pin PDIP, 20-pin SOIC and 32-pad MLF
- Operating Voltage:
 - 1.8 – 5.5V for ATtiny261V/461V/861V
 - 2.7 – 5.5V for ATtiny261/461/861
- Speed Grade:
 - ATtiny261V/461V/861V: 0 – 4 MHz @ 1.8 – 5.5V, 0 – 10 MHz @ 2.7 – 5.5V
 - ATtiny261/461/861: 0 – 10 MHz @ 2.7 – 5.5V, 0 – 20 MHz @ 4.5 – 5.5V
- Industrial Temperature Range
- Low Power Consumption
 - Active Mode (1 MHz System Clock): 300 µA @ 1.8V
 - Power-Down Mode: 0.1 µA at 1.8V



8-bit AVR[®] Microcontroller with 2/4/8K Bytes In-System Programmable Flash

ATtiny261/V*
ATtiny461/V
ATtiny861/V

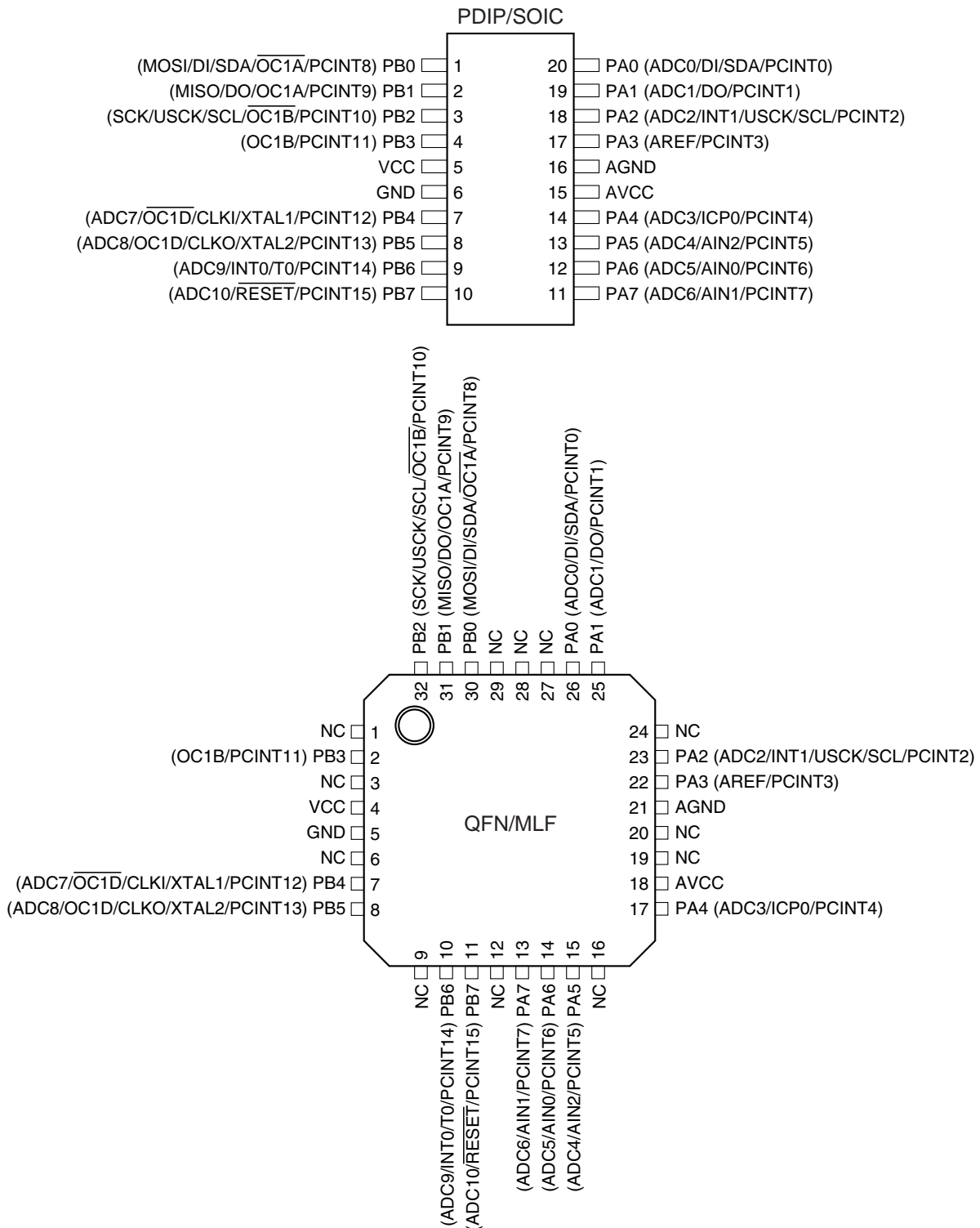
Summary

*Mature

2588FS-AVR-06/2013

1. Pin Configurations

Figure 1-1. Pinout ATtiny261/461/861 and ATtiny261V/461V/861V



Note: To ensure mechanical stability the center pad underneath the QFN/MLF package should be soldered to ground on the board.

1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 AVCC

Analog supply voltage. This is the supply voltage pin for the Analog-to-digital Converter (ADC), the analog comparator, the Brown-Out Detector (BOD), the internal voltage reference and Port A. It should be externally connected to VCC, even if some peripherals such as the ADC are not used. If the ADC is used AVCC should be connected to VCC through a low-pass filter.

1.1.4 AGND

Analog ground.

1.1.5 Port A (PA7:PA0)

An 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. Output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port pins that are externally pulled low will source current if pull-up resistors have been activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the device, as listed on [page 63](#).

1.1.6 Port B (PB7:PB0)

An 8-bit, bi-directional I/O port with internal pull-up resistors, individually selectable for each bit. Output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, port pins that are externally pulled low will source current if pull-up resistors have been activated. Port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the device, as listed on [page 66](#).

1.1.7 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. The minimum pulse length is given in [Table 19-4 on page 190](#). Shorter pulses are not guaranteed to generate a reset.

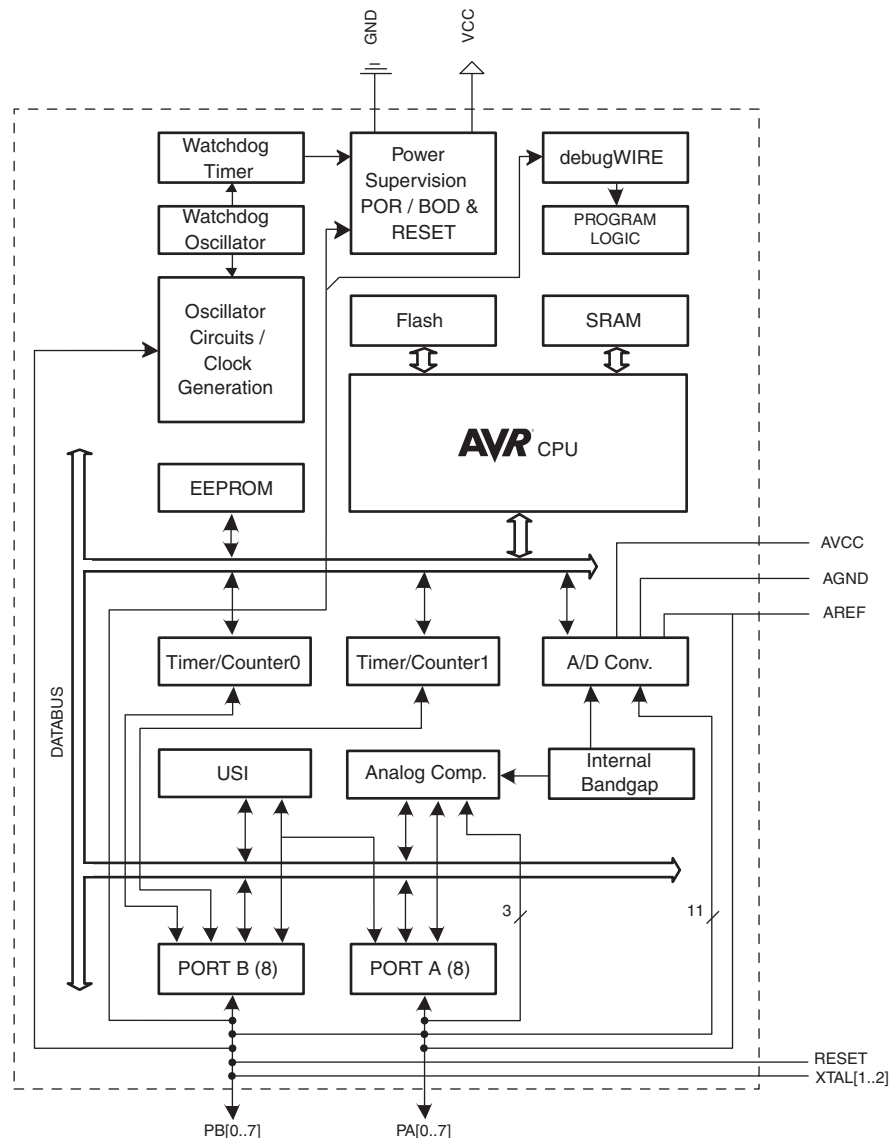
The reset pin can also be used as a (weak) I/O pin.

2. Overview

ATtiny261/461/861 are low-power CMOS 8-bit microcontrollers based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny261/461/861 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny261/461/861 provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/512 bytes SRAM, 16 general purpose I/O lines, 32 general purpose working registers, an 8-bit Timer/Counter with compare modes, an 8-bit high speed Timer/Counter, a Universal Serial Interface, Internal and External Interrupts, an 11-channel, 10-bit ADC, a programmable Watchdog Timer with internal oscillator, and four software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. Power-down mode saves the register contents, disabling all chip functions until the next Interrupt or Hardware Reset. ADC Noise Reduction mode stops the CPU and all I/O modules except ADC, to minimize switching noise during ADC conversions. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the Program memory to be re-programmed In-System through an SPI serial interface, by a conventional non-volatile memory programmer or by an On-chip boot code running on the AVR core.

The ATtiny261/461/861 AVR is supported by a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at <http://www.atmel.com/avr>.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology.

4. Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page | |
|-------------|----------|---|---------|---------|---------|---------|---------|---------|---------|---------------------------|---------|
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | page 8 | |
| 0x3E (0x5E) | SPH | – | – | – | – | – | SP10 | SP9 | SP8 | page 11 | |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | page 11 | |
| 0x3C (0x5C) | Reserved | | | | | | | | | | |
| 0x3B (0x5B) | GIMSK | INT1 | INT0 | PCIE1 | PCIE0 | – | – | – | – | page 52 | |
| 0x3A (0x5A) | GIFR | INTF1 | INTF0 | PCIF | – | – | – | – | – | page 53 | |
| 0x39 (0x59) | TIMSK | OCIE1D | OCIE1A | OCIE1B | OCIE0A | OCIE0B | TOIE1 | TOIE0 | TICIE0 | page 86, page 123 | |
| 0x38 (0x58) | TIFR | OCF1D | OCF1A | OCF1B | OCF0A | OCF0B | TOV1 | TOV0 | ICF0 | page 87, page 123 | |
| 0x37 (0x57) | SPMCSR | – | – | – | CTPB | RFLB | PGWRT | PGERS | SPMEN | page 169 | |
| 0x36 (0x56) | PRR | – | – | – | – | PRTIM1 | PRTIM0 | PRUSI | PRADC | page 37 | |
| 0x35 (0x55) | MCUCR | – | PUD | SE | SM1 | SM0 | – | ISC01 | ISC00 | page 39, page 69, page 52 | |
| 0x34 (0x54) | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | page 47, | |
| 0x33 (0x53) | TCCR0B | – | – | – | TSM | PSR0 | CS02 | CS01 | CS00 | page 85 | |
| 0x32 (0x52) | TCNT0L | Timer/Counter0 Counter Register Low Byte | | | | | | | | page 85 | |
| 0x31 (0x51) | OSCCAL | Oscillator Calibration Register | | | | | | | | page 32 | |
| 0x30 (0x50) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1B0 | FOC1A | FOC1B | PWM1A | PWM1B | page 112 | |
| 0x2F (0x4F) | TCCR1B | PWM1X | PSR1 | DTPS11 | DTPS10 | CS13 | CS12 | CS11 | CS10 | page 169 | |
| 0x2E (0x4E) | TCNT1 | Timer/Counter1 Counter Register | | | | | | | | page 121 | |
| 0x2D (0x4D) | OCR1A | Timer/Counter1 Output Compare Register A | | | | | | | | page 121 | |
| 0x2C (0x4C) | OCR1B | Timer/Counter1 Output Compare Register B | | | | | | | | page 122 | |
| 0x2B (0x4B) | OCR1C | Timer/Counter1 Output Compare Register C | | | | | | | | page 122 | |
| 0x2A (0x4A) | OCR1D | Timer/Counter1 Output Compare Register D | | | | | | | | page 122 | |
| 0x29 (0x49) | PLLCSR | LSM | – | – | – | – | PCKE | PLLE | PLOCK | page 120 | |
| 0x28 (0x48) | CLKPR | CLKPCE | – | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | page 32 |
| 0x27 (0x47) | TCCR1C | COM1A1S | COM1A0S | COM1B1S | COM1B0S | COM1D1 | COM1D0 | FOC1D | PWM1D | page 117 | |
| 0x26 (0x46) | TCCR1D | FP1E1 | FPEN1 | FPNC1 | FPES1 | FPAC1 | FPF1 | WGM11 | WGM10 | page 118 | |
| 0x25 (0x45) | TC1H | – | – | – | – | – | – | TC19 | TC18 | page 121 | |
| 0x24 (0x44) | DT1 | DT1H3 | DT1H2 | DT1H1 | DT1H0 | DT1L3 | DT1L2 | DT1L1 | DT1L0 | page 124 | |
| 0x23 (0x43) | PCMSK0 | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | page 54 | |
| 0x22 (0x42) | PCMSK1 | PCINT15 | PCINT14 | PCINT13 | PCINT12 | PCINT11 | PCINT10 | PCINT9 | PCINT8 | page 54 | |
| 0x21 (0x41) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | page 47 | |
| 0x20 (0x40) | DWDR | DWDR[7:0] | | | | | | | | page 37 | |
| 0x1F (0x3F) | EEARH | – | – | – | – | – | – | – | EEAR8 | page 20 | |
| 0x1E (0x3E) | EEARL | EEAR7 | EEAR6 | EEAR5 | EEAR4 | EEAR3 | EEAR2 | EEAR1 | EEAR0 | page 21 | |
| 0x1D (0x3D) | EEDR | EEPROM Data Register | | | | | | | | page 21 | |
| 0x1C (0x3C) | EEDR | – | – | EEDR1 | EEDR0 | EEDR7 | EEDR6 | EEDR5 | EEDR4 | page 21 | |
| 0x1B (0x3B) | PORTA | PORTA7 | PORTA6 | PORTA5 | PORTA4 | PORTA3 | PORTA2 | PORTA1 | PORTA0 | page 69 | |
| 0x1A (0x3A) | DDRA | DDA7 | DDA6 | DDA5 | DDA4 | DDA3 | DDA2 | DDA1 | DDA0 | page 69 | |
| 0x19 (0x39) | PINA | PINA7 | PINA6 | PINA5 | PINA4 | PINA3 | PINA2 | PINA1 | PINA0 | page 70 | |
| 0x18 (0x38) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | page 70 | |
| 0x17 (0x37) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | page 70 | |
| 0x16 (0x36) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | page 70 | |
| 0x15 (0x35) | TCCR0A | TCW0 | ICEN0 | ICNC0 | ICES0 | ACIC0 | – | – | CTC0 | page 84 | |
| 0x14 (0x34) | TCNT0H | Timer/Counter0 Counter Register High Byte | | | | | | | | page 86 | |
| 0x13 (0x33) | OCR0A | Timer/Counter0 Output Compare Register A | | | | | | | | page 86 | |
| 0x12 (0x32) | OCR0B | Timer/Counter0 Output Compare Register B | | | | | | | | page 86 | |
| 0x11 (0x31) | USIPP | – | – | – | – | – | – | – | USIPOS | page 136 | |
| 0x10 (0x30) | USIBR | USI Buffer Register | | | | | | | | page 133 | |
| 0x0F (0x2F) | USIDR | USI Data Register | | | | | | | | page 132 | |
| 0x0E (0x2E) | USISR | USISIF | USIOIF | USIPF | USIDC | USICNT3 | USICNT2 | USICNT1 | USICNT0 | page 133 | |
| 0x0D (0x2D) | USICR | USISIE | USIOIE | USIWM1 | USIWM0 | USICS1 | USICS0 | USICLK | USITC | page 134 | |
| 0x0C (0x2C) | GPOR2 | General Purpose I/O Register 2 | | | | | | | | page 22 | |
| 0x0B (0x2B) | GPOR1 | General Purpose I/O Register 1 | | | | | | | | page 23 | |
| 0x0A (0x2A) | GPOR0 | General Purpose I/O Register 0 | | | | | | | | page 23 | |
| 0x09 (0x29) | ACSRB | HSEL | HLEV | – | – | – | ACM2 | ACM1 | ACM0 | page 140 | |
| 0x08 (0x28) | ACSRA | ACD | ACBG | ACO | ACI | ACIE | ACME | ACIS1 | ACIS0 | page 139 | |
| 0x07 (0x27) | ADMUX | REFS1 | REFS0 | ADLAR | MUX4 | MUX3 | MUX2 | MUX1 | MUX0 | page 155 | |
| 0x06 (0x26) | ADCSRA | ADEN | ADSC | ADATE | ADIF | ADIE | ADPS2 | ADPS1 | ADPS0 | page 159 | |
| 0x05 (0x25) | ADCH | ADC Data Register High Byte | | | | | | | | page 160 | |
| 0x04 (0x24) | ADCL | ADC Data Register Low Byte | | | | | | | | page 160 | |
| 0x03 (0x23) | ADCSRB | BIN | GSEL | – | REFS2 | MUX5 | ADTS2 | ADTS1 | ADTS0 | page 161 | |
| 0x02 (0x22) | DIDR1 | ADC10D | ADC9D | ADC8D | ADC7D | – | – | – | – | page 162 | |
| 0x01 (0x21) | DIDR0 | ADC6D | ADC5D | ADC4D | ADC3D | AREFD | ADC2D | ADC1D | ADC0D | page 162 | |
| 0x00 (0x20) | TCCR1E | – | – | OC1OE5 | OC1OE4 | OC1OE3 | OC1OE2 | OC1OE1 | OC1OE0 | page 119 | |

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
 3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|--|----------|--|--|---------------|---------|
| ARITHMETIC AND LOGIC INSTRUCTIONS | | | | | |
| ADD | Rd, Rr | Add two Registers | $Rd \leftarrow Rd + Rr$ | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | $Rd \leftarrow Rd + Rr + C$ | Z,C,N,V,H | 1 |
| ADIW | Rd,K | Add Immediate to Word | $Rdh:Rdl \leftarrow Rdh:Rdl + K$ | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | $Rd \leftarrow Rd - Rr$ | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | $Rd \leftarrow Rd - K$ | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | $Rd \leftarrow Rd - Rr - C$ | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | $Rd \leftarrow Rd - K - C$ | Z,C,N,V,H | 1 |
| SBIW | Rd,K | Subtract Immediate from Word | $Rdh:Rdl \leftarrow Rdh:Rdl - K$ | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | $Rd \leftarrow Rd \bullet Rr$ | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | $Rd \leftarrow Rd \bullet K$ | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | $Rd \leftarrow Rd \vee Rr$ | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | $Rd \leftarrow Rd \oplus Rr$ | Z,N,V | 1 |
| COM | Rd | One's Complement | $Rd \leftarrow 0xFF - Rd$ | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | $Rd \leftarrow 0x00 - Rd$ | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | $Rd \leftarrow Rd \vee K$ | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | $Rd \leftarrow Rd \bullet (0xFF - K)$ | Z,N,V | 1 |
| INC | Rd | Increment | $Rd \leftarrow Rd + 1$ | Z,N,V | 1 |
| DEC | Rd | Decrement | $Rd \leftarrow Rd - 1$ | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | $Rd \leftarrow Rd \bullet Rd$ | Z,N,V | 1 |
| CLR | Rd | Clear Register | $Rd \leftarrow Rd \oplus Rd$ | Z,N,V | 1 |
| SER | Rd | Set Register | $Rd \leftarrow 0xFF$ | None | 1 |
| BRANCH INSTRUCTIONS | | | | | |
| RJMP | k | Relative Jump | $PC \leftarrow PC + k + 1$ | None | 2 |
| IJMP | | Indirect Jump to (Z) | $PC \leftarrow Z$ | None | 2 |
| RCALL | k | Relative Subroutine Call | $PC \leftarrow PC + k + 1$ | None | 3 |
| ICALL | | Indirect Call to (Z) | $PC \leftarrow Z$ | None | 3 |
| RET | | Subroutine Return | $PC \leftarrow STACK$ | None | 4 |
| RETI | | Interrupt Return | $PC \leftarrow STACK$ | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | $Rd - Rr$ | Z, N, V, C, H | 1 |
| CPC | Rd,Rr | Compare with Carry | $Rd - Rr - C$ | Z, N, V, C, H | 1 |
| CPI | Rd,K | Compare Register with Immediate | $Rd - K$ | Z, N, V, C, H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) $PC \leftarrow PC + 2$ or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N \oplus V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N \oplus V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if (I = 1) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if (I = 0) then $PC \leftarrow PC + k + 1$ | None | 1/2 |
| BIT AND BIT-TEST INSTRUCTIONS | | | | | |
| SBI | P,b | Set Bit in I/O Register | $I/O(P,b) \leftarrow 1$ | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | $I/O(P,b) \leftarrow 0$ | None | 2 |
| LSL | Rd | Logical Shift Left | $Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$ | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | $Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$ | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | $Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$ | Z,C,N,V | 1 |
| ROR | Rd | Rotate Right Through Carry | $Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$ | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|-----------------------------------|----------|----------------------------------|--|---------|---------|
| ASR | Rd | Arithmetic Shift Right | $Rd(n) \leftarrow Rd(n+1), n=0..6$ | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | $Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$ | None | 1 |
| BSET | s | Flag Set | $SREG(s) \leftarrow 1$ | SREG(s) | 1 |
| BCLR | s | Flag Clear | $SREG(s) \leftarrow 0$ | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | $T \leftarrow Rr(b)$ | T | 1 |
| BLD | Rd, b | Bit load from T to Register | $Rd(b) \leftarrow T$ | None | 1 |
| SEC | | Set Carry | $C \leftarrow 1$ | C | 1 |
| CLC | | Clear Carry | $C \leftarrow 0$ | C | 1 |
| SEN | | Set Negative Flag | $N \leftarrow 1$ | N | 1 |
| CLN | | Clear Negative Flag | $N \leftarrow 0$ | N | 1 |
| SEZ | | Set Zero Flag | $Z \leftarrow 1$ | Z | 1 |
| CLZ | | Clear Zero Flag | $Z \leftarrow 0$ | Z | 1 |
| SEI | | Global Interrupt Enable | $I \leftarrow 1$ | I | 1 |
| CLI | | Global Interrupt Disable | $I \leftarrow 0$ | I | 1 |
| SES | | Set Signed Test Flag | $S \leftarrow 1$ | S | 1 |
| CLS | | Clear Signed Test Flag | $S \leftarrow 0$ | S | 1 |
| SEV | | Set Twos Complement Overflow. | $V \leftarrow 1$ | V | 1 |
| CLV | | Clear Twos Complement Overflow | $V \leftarrow 0$ | V | 1 |
| SET | | Set T in SREG | $T \leftarrow 1$ | T | 1 |
| CLT | | Clear T in SREG | $T \leftarrow 0$ | T | 1 |
| SEH | | Set Half Carry Flag in SREG | $H \leftarrow 1$ | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | $H \leftarrow 0$ | H | 1 |
| DATA TRANSFER INSTRUCTIONS | | | | | |
| MOV | Rd, Rr | Move Between Registers | $Rd \leftarrow Rr$ | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | $Rd+1:Rd \leftarrow Rr+1:Rr$ | None | 1 |
| LDI | Rd, K | Load Immediate | $Rd \leftarrow K$ | None | 1 |
| LD | Rd, X | Load Indirect | $Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | $Rd \leftarrow (X), X \leftarrow X + 1$ | None | 2 |
| LD | Rd, -X | Load Indirect and Pre-Dec. | $X \leftarrow X - 1, Rd \leftarrow (X)$ | None | 2 |
| LD | Rd, Y | Load Indirect | $Rd \leftarrow (Y)$ | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Y), Y \leftarrow Y + 1$ | None | 2 |
| LD | Rd, -Y | Load Indirect and Pre-Dec. | $Y \leftarrow Y - 1, Rd \leftarrow (Y)$ | None | 2 |
| LDD | Rd, Y+q | Load Indirect with Displacement | $Rd \leftarrow (Y + q)$ | None | 2 |
| LD | Rd, Z | Load Indirect | $Rd \leftarrow (Z)$ | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | $Z \leftarrow Z - 1, Rd \leftarrow (Z)$ | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | $Rd \leftarrow (Z + q)$ | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | $Rd \leftarrow (k)$ | None | 2 |
| ST | X, Rr | Store Indirect | $(X) \leftarrow Rr$ | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | $(X) \leftarrow Rr, X \leftarrow X + 1$ | None | 2 |
| ST | -X, Rr | Store Indirect and Pre-Dec. | $X \leftarrow X - 1, (X) \leftarrow Rr$ | None | 2 |
| ST | Y, Rr | Store Indirect | $(Y) \leftarrow Rr$ | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | $(Y) \leftarrow Rr, Y \leftarrow Y + 1$ | None | 2 |
| ST | -Y, Rr | Store Indirect and Pre-Dec. | $Y \leftarrow Y - 1, (Y) \leftarrow Rr$ | None | 2 |
| STD | Y+q, Rr | Store Indirect with Displacement | $(Y + q) \leftarrow Rr$ | None | 2 |
| ST | Z, Rr | Store Indirect | $(Z) \leftarrow Rr$ | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ | None | 2 |
| STD | Z+q, Rr | Store Indirect with Displacement | $(Z + q) \leftarrow Rr$ | None | 2 |
| STS | k, Rr | Store Direct to SRAM | $(k) \leftarrow Rr$ | None | 2 |
| LPM | | Load Program Memory | $R0 \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z | Load Program Memory | $Rd \leftarrow (Z)$ | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | $Rd \leftarrow (Z), Z \leftarrow Z + 1$ | None | 3 |
| SPM | | Store Program Memory | $(z) \leftarrow R1:R0$ | None | |
| IN | Rd, P | In Port | $Rd \leftarrow P$ | None | 1 |
| OUT | P, Rr | Out Port | $P \leftarrow Rr$ | None | 1 |
| PUSH | Rr | Push Register on Stack | $STACK \leftarrow Rr$ | None | 2 |
| POP | Rd | Pop Register from Stack | $Rd \leftarrow STACK$ | None | 2 |
| MCU CONTROL INSTRUCTIONS | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/Timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

6. Ordering Information

6.1 ATtiny261 - Mature

| Speed (MHz) ⁽³⁾ | Power Supply (V) | Ordering Code ⁽⁴⁾⁽⁵⁾ | Package ⁽²⁾ | Operational Range |
|----------------------------|------------------|---|--|---|
| 10 | 1.8 - 5.5 | ATtiny261V-10MU ATtiny261V-10MUR ATtiny261V-10PU ATtiny261V-10SU ATtiny261V-10SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |
| 20 | 2.7 - 5.5 | ATtiny261-20MU ATtiny261-20MUR ATtiny261-20PU ATtiny261-20SU ATtiny261-20SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |

- Notes:
1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 3. For Speed vs. V_{CC} , see [Figure 19.3 on page 188](#).
 4. Code indicators:
 - U: matte tin
 - R: tape & reel
 5. Mature devices, replaced by ATtiny261A.

| Package Type | |
|---------------------|---|
| 32M1-A | 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |
| 20P3 | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20S2 | 20-lead, 0.300" Wide, Plastic Gull Wing Smal Outline Package (SOIC) |

6.2 ATtiny461

| Speed (MHz) ⁽³⁾ | Power Supply (V) | Ordering Code ⁽⁴⁾ | Package ⁽²⁾ | Operational Range |
|----------------------------|------------------|---|--|---|
| 10 | 1.8 - 5.5 | ATtiny461V-10MU ATtiny461V-10MUR ATtiny461V-10PU ATtiny461V-10SU ATtiny461V-10SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |
| 20 | 2.7 - 5.5 | ATtiny461-20MU ATtiny461-20MUR ATtiny461-20PU ATtiny461-20SU ATtiny461-20SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |

Notes: 1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).

3. For Speed vs. V_{CC} , see [Figure 19.3 on page 188](#).

4. Code indicators:

- U: matte tin
- R: tape & reel

| Package Type | |
|---------------|---|
| 32M1-A | 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |
| 20P3 | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20S2 | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC) |

6.3 ATtiny861

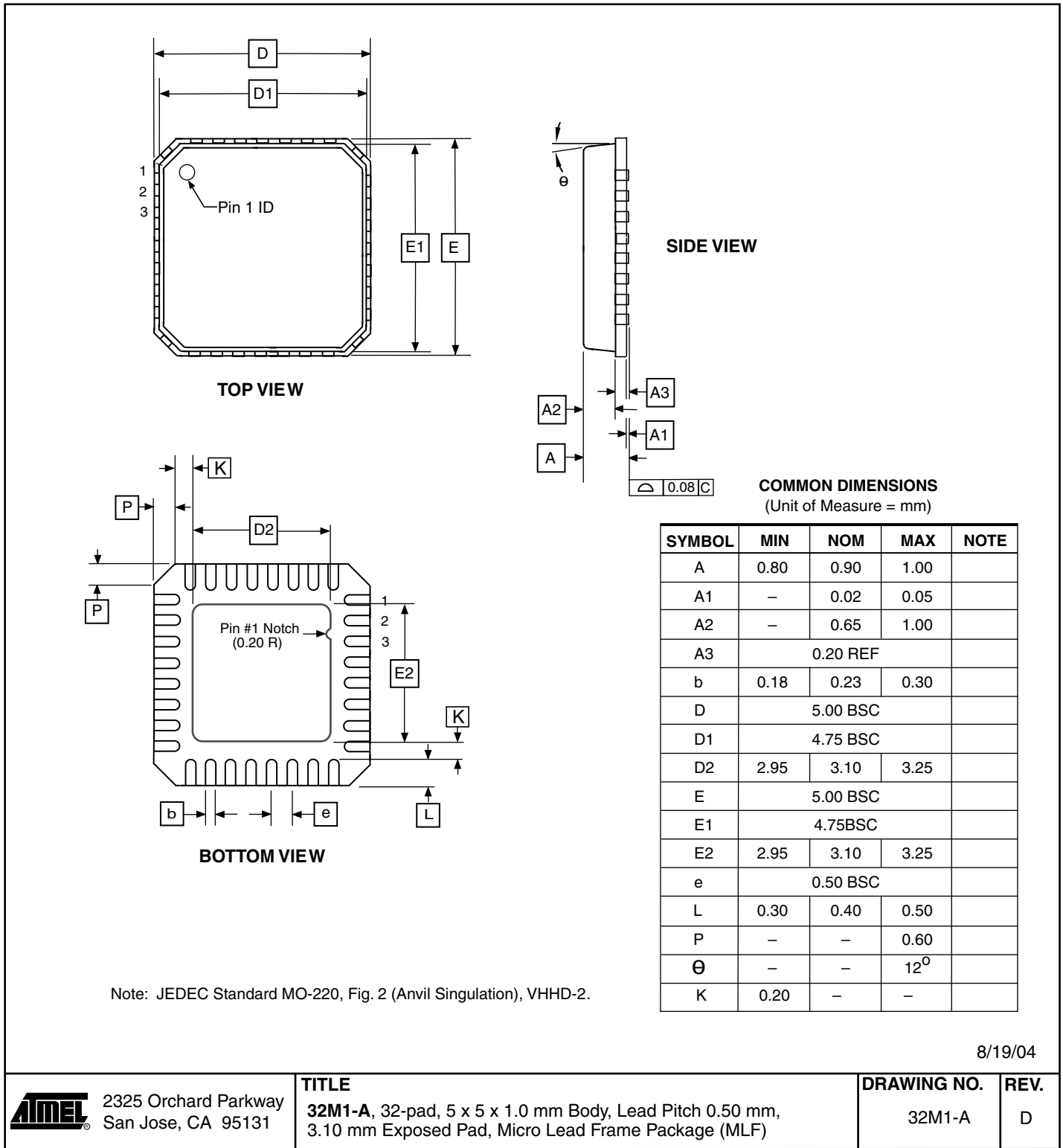
| Speed (MHz) ⁽³⁾ | Power Supply (V) | Ordering Code ⁽⁴⁾ | Package ⁽²⁾ | Operational Range |
|----------------------------|------------------|---|--|---|
| 10 | 1.8 - 5.5 | ATtiny861V-10MU ATtiny861V-10MUR ATtiny861V-10PU ATtiny861V-10SU ATtiny861V-10SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |
| 20 | 2.7 - 5.5 | ATtiny861-20MU ATtiny861-20MUR ATtiny861-20PU ATtiny861-20SU ATtiny861-20SUR | 32M1-A 32M1-A 20P3 20S2 20S2 | Industrial (-40°C to +85°C) ⁽¹⁾ |

- Notes:
1. These devices can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
 2. All packages are Pb-free, halide-free and fully green and they comply with the European directive for Restriction of Hazardous Substances (RoHS).
 3. For Speed vs. V_{CC} , see [Figure 19.3 on page 188](#).
 4. Code indicators:
 - U: matte tin
 - R: tape & reel

| Package Type | |
|---------------|---|
| 32M1-A | 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm, Micro Lead Frame Package (MLF) |
| 20P3 | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 20S2 | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC) |

7. Packaging Information

7.1 32M1-A



8/19/04



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32M1-A, 32-pad, 5 x 5 x 1.0 mm Body, Lead Pitch 0.50 mm,
3.10 mm Exposed Pad, Micro Lead Frame Package (MLF)

DRAWING NO.

32M1-A

REV.

D

7.2 20P3

7.3 20S2



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|-------|------|
| A | 2.35 | | 2.65 | |
| A1 | 0.10 | | 0.30 | |
| b | 0.33 | | 0.51 | 4 |
| C | 0.23 | | 0.32 | |
| D | 12.60 | | 13.00 | 1 |
| E | 7.40 | | 7.60 | 2 |
| H | 10.00 | | 10.65 | |
| L | 0.40 | | 1.27 | 3 |
| e | 1.27 BSC | | | |

- Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
 2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006") per side.
 3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010") per side.
 4. 'L' is the length of the terminal for soldering to a substrate.
 5. The lead width 'b', as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.



2325 Orchard Parkway
San Jose, CA 95131

TITLE

20S2, 20-lead, 0.300" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)

DRAWING NO.

20S2

REV.

B

8. Errata

8.1 Errata ATtiny261

The revision letter in this section refers to the revision of the ATtiny261 device.

8.1.1 Rev A

No known errata.

8.2 Errata ATtiny461

The revision letter in this section refers to the revision of the ATtiny461 device.

8.2.1 Rev B

Yield improvement. No known errata.

8.2.2 Rev A

No known errata.

8.3 Errata ATtiny861

The revision letter in this section refers to the revision of the ATtiny861 device.

8.3.1 Rev B

No known errata.

8.3.2 Rev A

Not sampled.

9. Datasheet Revision History

Please note that the referring page numbers in this section refer to the complete document.

9.1 Rev. 2588F – 06/13

1. ATtiny261 changed status to "Mature".

9.2 Rev. 2588E – 08/10

1. Added tape and reel in "Ordering Information" on page 11.
2. Clarified [Section 6.4 "Clock Output Buffer"](#) on page 32.
3. Removed text "Not recommended for new designs" from cover page.

9.3 Rev. 2588D – 06/10

1. Removed "Preliminary" from cover page.
2. Added clarification before [Table 6-10, "Capacitance for Low-Frequency Crystal Oscillator,"](#) on page 29.
3. Updated [Figure 15-1 "Analog to Digital Converter Block Schematic"](#) on page 143, changed INTERNAL 1.18V REFERENCE to 1.1V.
4. Updated [Table 18-8, "No. of Words in a Page and No. of Pages in the EEPROM,"](#) on page 173, No. of Pages from 64 to 32 for ATtiny261.
5. Adjusted notes in [Table 19-1, "DC Characteristics. T_A = -40°C to +85°C, V_{CC} = 1.8V to 5.5V \(unless otherwise noted\).,"](#) on page 187.

9.4 Rev. 2588C – 10/09

1. Updated document template. Re-arranged some sections.
2. Changed device status to "Not Recommended for New Designs".
3. Added Sections:
 - "Data Retention" on page 6
 - "Clock Sources" on page 25
 - "Low Level Interrupt" on page 51
 - "Prescaling and Conversion Timing" on page 145
 - "Clock speed considerations" on page 131
4. Updated Sections:
 - "Code Examples" on page 6
 - "High-Frequency PLL Clock" on page 26
 - "Normal Mode" on page 99
 - "Features" on page 142
 - "Temperature Measurement" on page 154
 - "Limitations of debugWIRE" on page 164
 - Step 1. on page 174
 - "Programming the Flash" on page 180
 - "System and Reset Characteristics" on page 190
5. Added Figures:
 - "Flash Programming Waveforms" on page 182

- “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)” on page 209
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)” on page 209
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)” on page 209
 - “Reset Pin Output Voltage vs. Sink Current ($V_{CC} = 3V$)” on page 209
 - “Bandgap Voltage vs. Supply Voltage (V_{CC}).” on page 216
6. Updated Figures:
 - “Block Diagram” on page 4
 - “Clock Distribution” on page 24
 7. Added Table:
 - “Capacitance for Low-Frequency Crystal Oscillator” on page 29
 8. Updated Tables:
 - “Start-up Times for the Internal Calibrated RC Oscillator Clock Selection” on page 28
 - “Start-up Times for the 128 kHz Internal Oscillator” on page 29
 - “Active Clock Domains and Wake-up Sources in Different Sleep Modes” on page 36
 - “Serial Programming Characteristics, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = 1.8 - 5.5V$ (Unless Otherwise Noted)” on page 193
 9. Updated Register Descriptions:
 - “TCCR1A – Timer/Counter1 Control Register A” on page 112
 - “TCCR1C – Timer/Counter1 Control Register C” on page 117
 - “ADMUX – ADC Multiplexer Selection Register” on page 155
 10. Updated assembly program example in section “Write” on page 17.
 11. Updated “DC Characteristics. $T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = 1.8V$ to $5.5V$ (unless otherwise noted).” on page 187.

9.5 Rev. 2588B – 11/06

1. Updated “Ordering Information” on page 11.
2. Updated “Packaging Information” on page 15.

9.6 Rev. 2588A – 10/06

1. Initial Revision.



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Atmel Corporation

1600 Technology Drive
San Jose, CA 95110
USA

Tel: (+1) (408) 441-0311

Fax: (+1) (408) 487-2600

www.atmel.com

Atmel Asia Limited

Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5

418 Kwun Tong Roa

Kwun Tong, Kowloon

HONG KONG

Tel: (+852) 2245-6100

Fax: (+852) 2722-1369

Atmel Munich GmbH

Business Campus

Parking 4

D-85748 Garching b. Munich

GERMANY

Tel: (+49) 89-31970-0

Fax: (+49) 89-3194621

Atmel Japan G.K.

16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku

Tokyo 141-0032

JAPAN

Tel: (+81) (3) 6417-0300

Fax: (+81) (3) 6417-0370

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.