

# TPW4R008NH

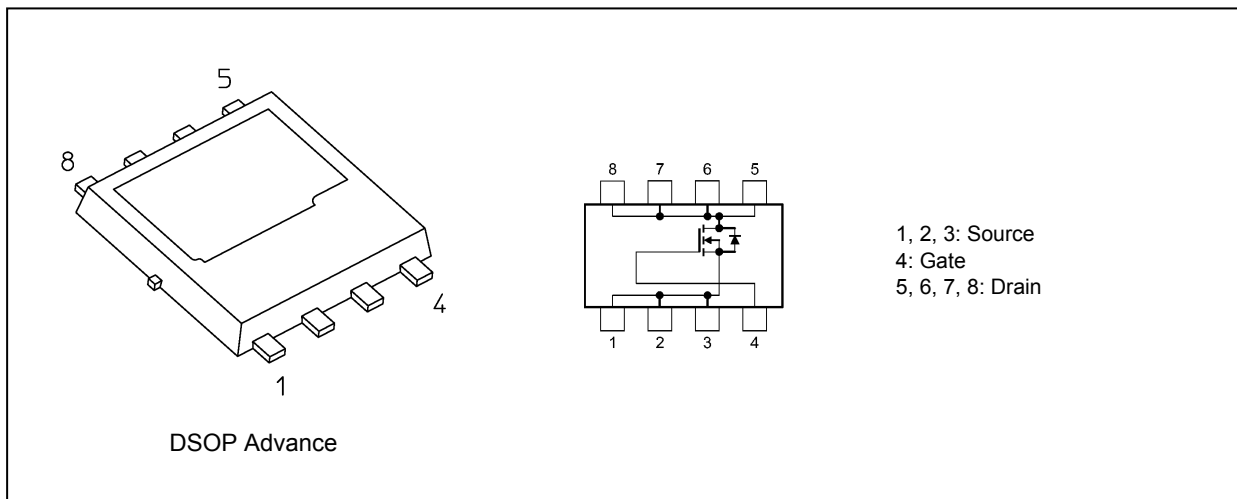
## 1. Applications

- DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

## 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 18 \text{ nC (typ.)}$
- (3) Low drain-source on-resistance:  $R_{DS(ON)} = 3.3 \text{ m}\Omega \text{ (typ.)}$  ( $V_{GS} = 10 \text{ V}$ )
- (4) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A (max)}$  ( $V_{DS} = 80 \text{ V}$ )
- (5) Enhancement mode:  $V_{th} = 2.0 \text{ to } 4.0 \text{ V}$  ( $V_{DS} = 10 \text{ V}$ ,  $I_D = 1.0 \text{ mA}$ )

## 3. Packaging and Internal Circuit



Start of commercial production

2014-09

**4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	80	V
Gate-source voltage	$V_{GSS}$	$\pm 20$	
Drain current (DC) ( $T_c = 25\text{ }^\circ\text{C}$ ) (Bottom drain)	$I_D$	116	A
Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ )	$I_{DP}$	440	A
Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ ) (Bottom drain)	$P_D$	142	W
Power dissipation	$P_D$	2.5	W
Power dissipation	$P_D$	0.8	W
Single-pulse avalanche energy	$E_{AS}$	125	mJ
Single-pulse avalanche current	$I_{AS}$	116	A
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance Bottom drain ( $T_c = 25\text{ }^\circ\text{C}$ )	$R_{th(ch-c)}$	0.88	$^\circ\text{C/W}$
Channel-to-case thermal resistance Top source ( $T_c = 25\text{ }^\circ\text{C}$ )	$R_{th(ch-c)}$	0.93	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ )	$R_{th(ch-a)}$	50	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ )	$R_{th(ch-a)}$	156	$^\circ\text{C/W}$

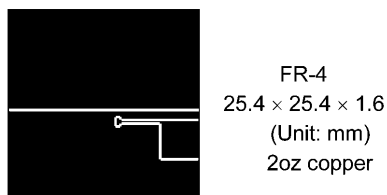
Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Limited by silicon chip capability.

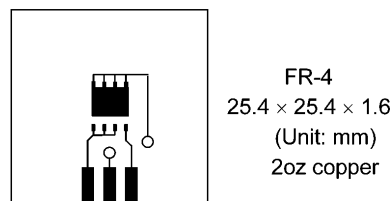
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5:  $V_{DD} = 60\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 7.9\text{ }\mu\text{H}$ ,  $I_{AS} = 116\text{ A}$



**Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)**



**Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)**

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

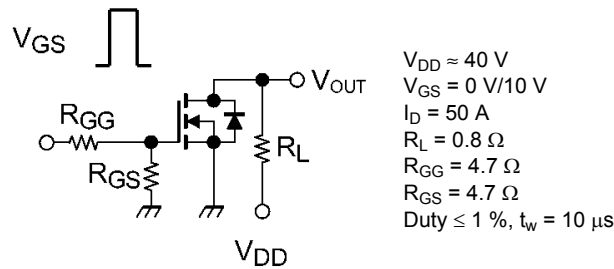
**6. Electrical Characteristics**

**6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	80	—	—	V
	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	60	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 1.0\text{ mA}$	2.0	—	4.0	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	—	3.3	4.0	$\text{m}\Omega$

**6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	4100	5300	$\mu\text{F}$
Reverse transfer capacitance	$C_{rss}$		—	32	64	
Output capacitance	$C_{oss}$		—	890	—	
Gate resistance	$r_g$	—	—	1.2	1.8	$\Omega$
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	8.6	—	ns
Switching time (turn-on time)	$t_{on}$		—	25	—	
Switching time (fall time)	$t_f$		—	12	—	
Switching time (turn-off time)	$t_{off}$		—	52	—	



**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 50\text{ A}$	—	59	—	nC
Gate-source charge 1	$Q_{gs1}$		—	18	—	
Gate-drain charge	$Q_{gd}$		—	12	—	
Gate switch charge	$Q_{sw}$		—	18	—	

**6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 6)	$I_{DRP}$ ( $t = 100\text{ }\mu\text{s}$ )	—	—	—	440	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 116\text{ A}, V_{GS} = 0\text{ V}$	—	—	-1.2	V
Reverse recovery time	$t_{rr}$	$V_R = 40\text{ V}, I_{DR} = 29\text{ A},$ $V_{GS} = 0\text{ V}, -dI_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	54	—	ns
Reverse recovery charge	$Q_{rr}$		—	72	—	nC

Note 6: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

7. Marking

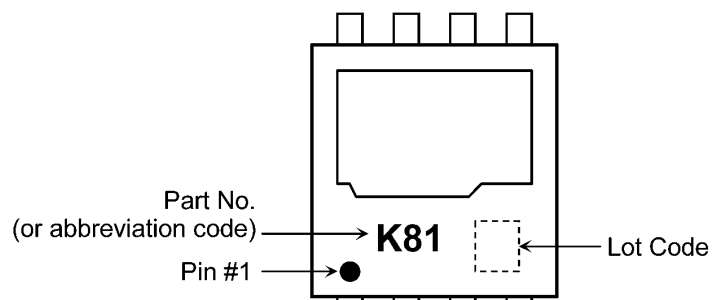
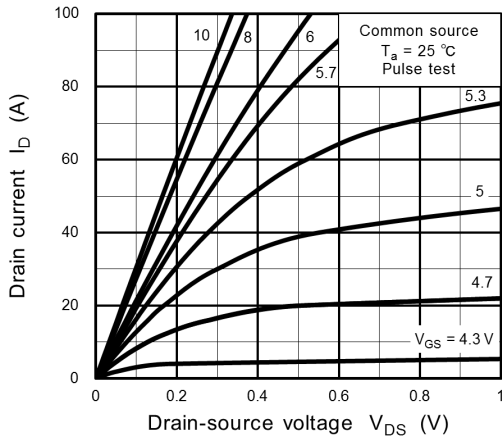
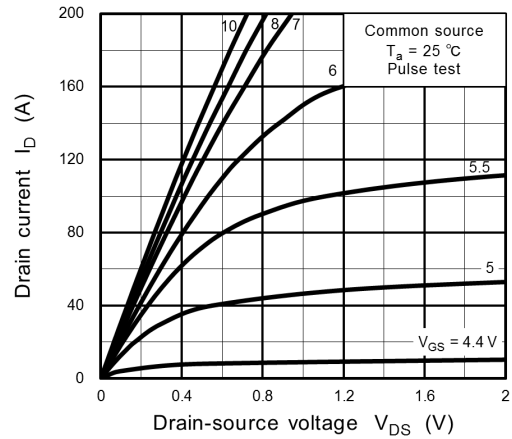


Fig. 7.1 Marking

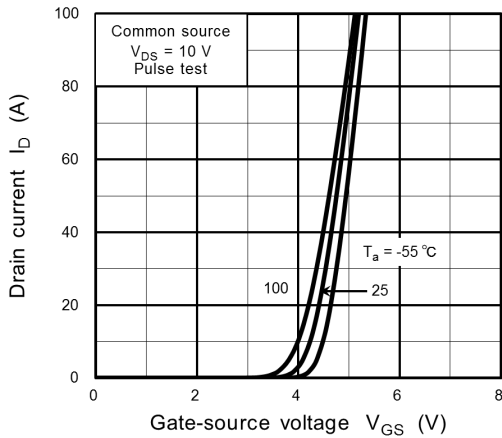
**8. Characteristics Curves (Note)**



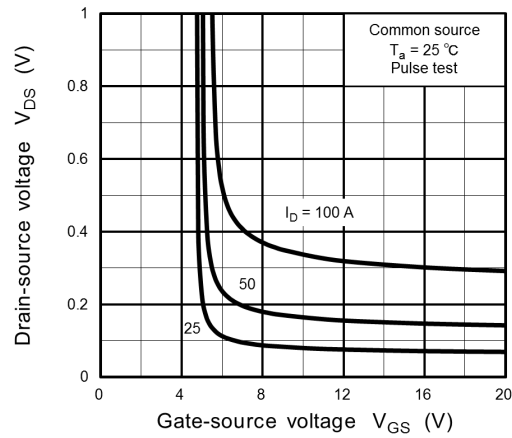
**Fig. 8.1  $I_D - V_{DS}$**



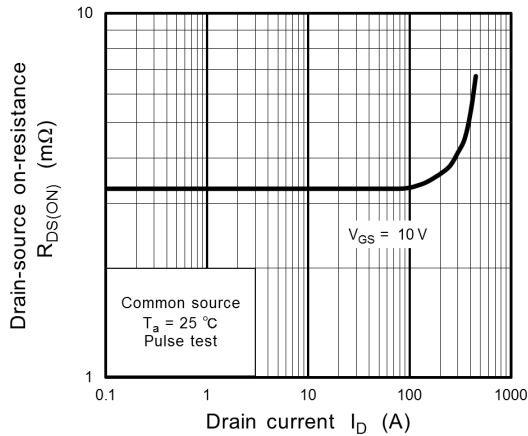
**Fig. 8.2  $I_D - V_{DS}$**



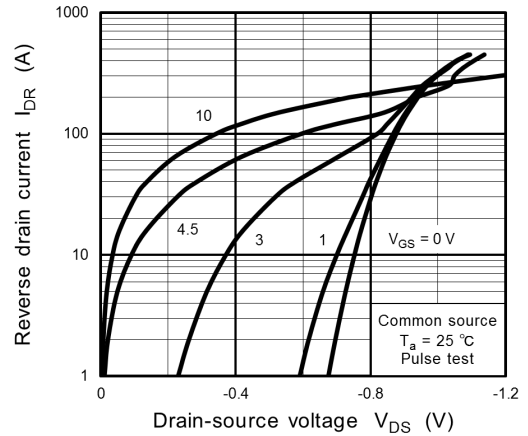
**Fig. 8.3  $I_D - V_{GS}$**



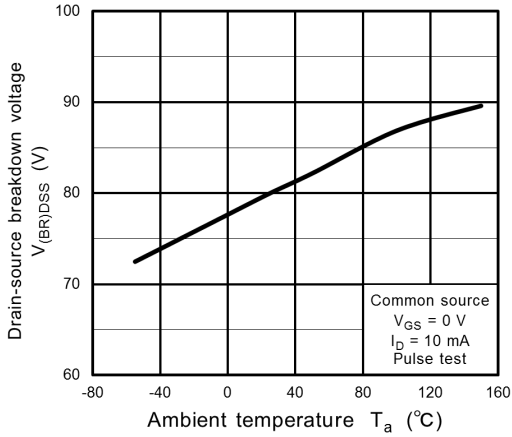
**Fig. 8.4  $V_{DS} - V_{GS}$**



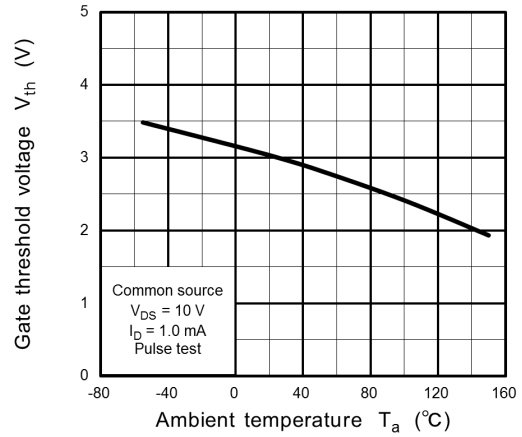
**Fig. 8.5  $R_{DS(ON)} - I_D$**



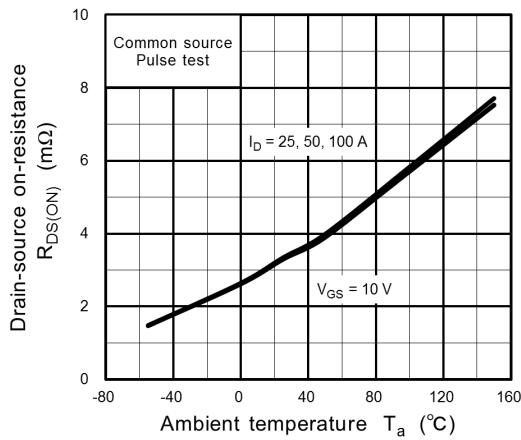
**Fig. 8.6  $I_{DR} - V_{DS}$**



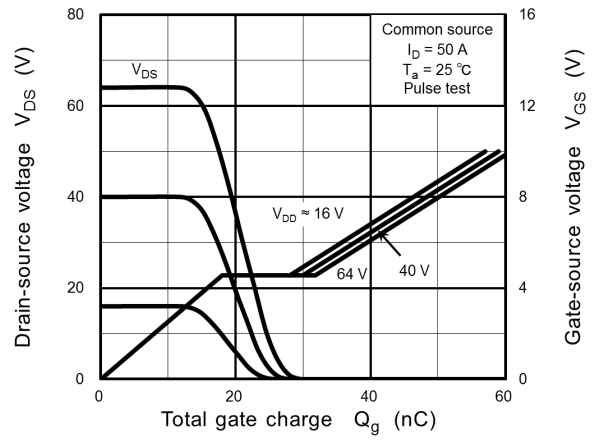
**Fig. 8.7  $V_{(BR)DSS} - T_a$**



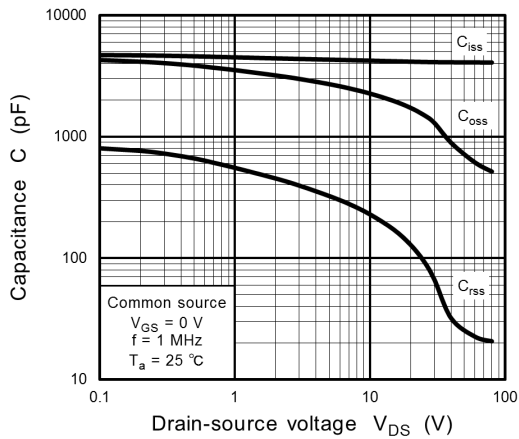
**Fig. 8.8  $V_{th} - T_a$**



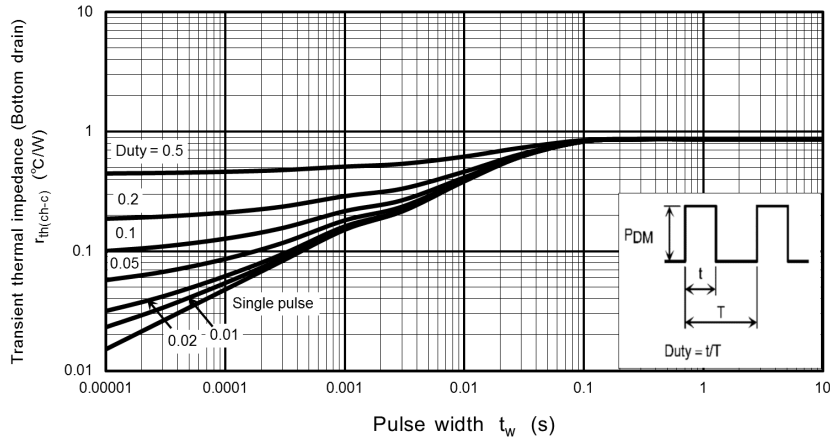
**Fig. 8.9  $R_{DS(ON)} - T_a$**



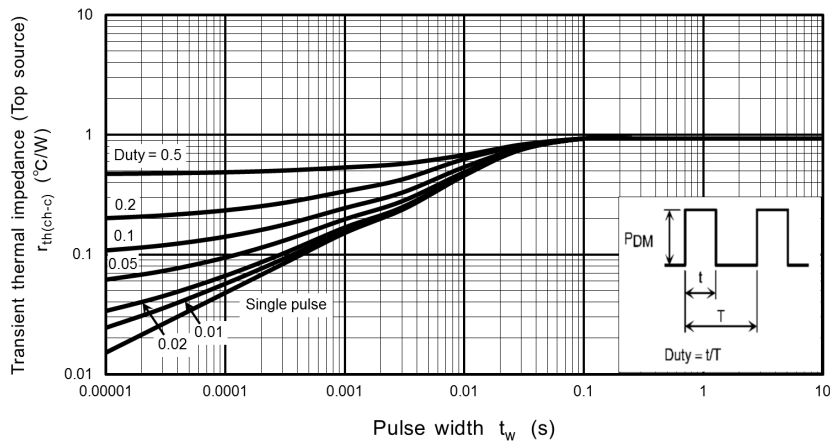
**Fig. 8.10 Dynamic Input/Output Characteristics**



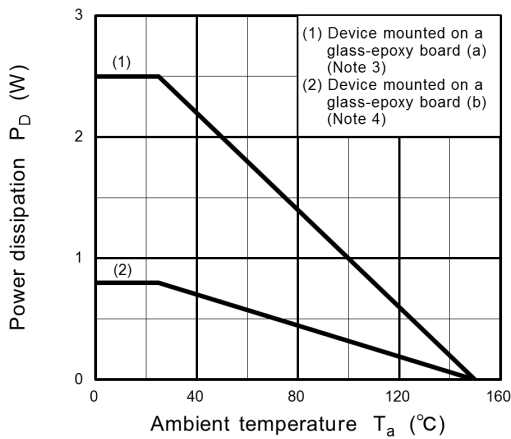
**Fig. 8.11 Capacitance -  $V_{DS}$**



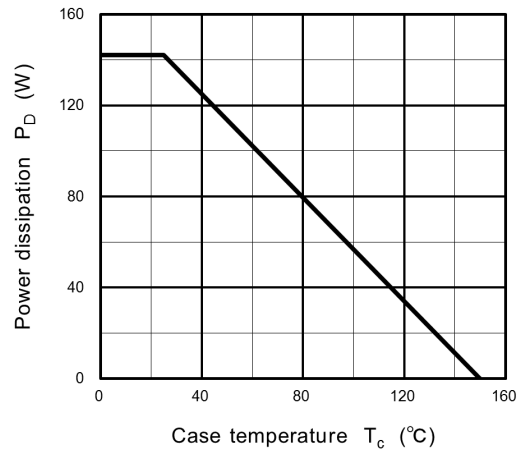
**Fig. 8.12  $r_{th} - t_w$  (Bottom drain)**  
(Guaranteed Maximum)



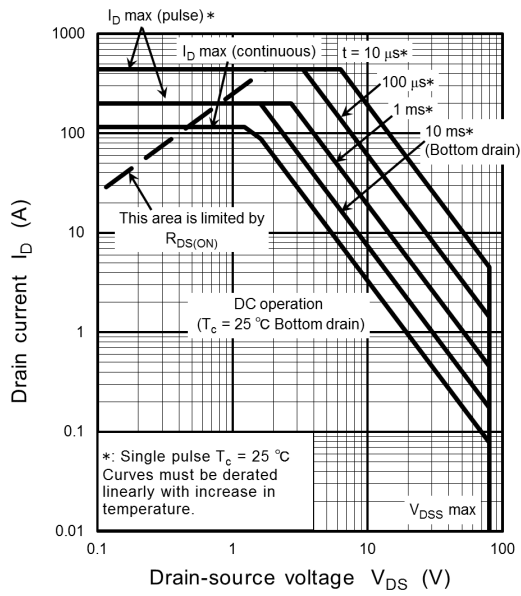
**Fig. 8.13  $r_{th} - t_w$  (Top source)**  
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_a$**   
(Guaranteed Maximum)



**Fig. 8.15  $P_D - T_c$  (Bottom drain)**  
(Guaranteed Maximum)



**Fig. 8.16 Safe Operating Area (Guaranteed Maximum)**

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.