

NSBC115TDP6

Dual NPN Bias Resistor Transistors

R1 = 100 kΩ, R2 = ∞ kΩ

NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C, common for Q1 and Q2, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CB0}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current - Continuous	I _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	6	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

Device	Package	Shipping†
NSBC115TDP6T5G	SOT-963	8,000 / Tape & Reel

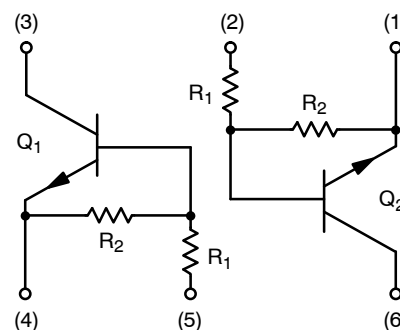
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



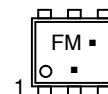
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PIN CONNECTIONS



MARKING DIAGRAMS



SOT-963
CASE 527AD

- F = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

NSBC115TDP6

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
NSBC115TDP6 (SOT-963) One Junction Heated			
Total Device Dissipation $T_A = 25^\circ\text{C}$	P_D	231	mW
	(Note 1)	269	
Derate above 25°C	(Note 1)	1.9	mW/ $^\circ\text{C}$
	(Note 2)	2.2	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	540	$^\circ\text{C}/\text{W}$
	(Note 2)	464	
NSBC115TDP6 (SOT-963) Both Junction Heated (Note 3)			
Total Device Dissipation $T_A = 25^\circ\text{C}$	P_D	339	mW
	(Note 1)	408	
Derate above 25°C	(Note 1)	2.7	mW/ $^\circ\text{C}$
	(Note 2)	3.3	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	369	$^\circ\text{C}/\text{W}$
	(Note 2)	306	
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

- FR-4 @ 100 mm², 1 oz. copper traces, still air.
- FR-4 @ 500 mm², 1 oz. copper traces, still air.
- Both junction heated values assume total power is sum of two equally powered channels.

NSBC115TDP6

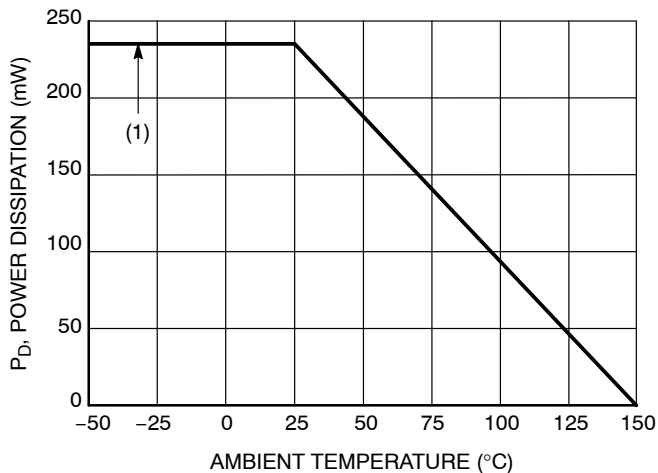
ELECTRICAL CHARACTERISTICS (T_A = 25°C, common for Q₁ and Q₂, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0)	I _{EBO}	-	-	0.1	mAdc
Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 4) (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc

ON CHARACTERISTICS

DC Current Gain (Note 4) (I _C = 5.0 mA, V _{CE} = 10 V)	h _{FE}	160	350	-	
Collector-Emitter Saturation Voltage (Note 4) (I _C = 10 mA, I _B = 5.0 mA)	V _{CE(sat)}	-	-	0.25	Vdc
Input Voltage (off) (V _{CE} = 5.0 V, I _C = 100 μA)	V _{i(off)}	-	0.6	-	Vdc
Input Voltage (on) (V _{CE} = 0.2 V, I _C = 1.0 mA)	V _{i(on)}	-	1.0	-	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.25 V, R _L = 1.0 kΩ)	V _{OH}	4.9	-	-	Vdc
Input Resistor	R ₁	70	100	130	kΩ
Resistor Ratio	R ₁ /R ₂	-	-	-	

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.



(1) SOT-963; 100 mm², 1 oz. copper trace

Figure 1. Derating Curve

NSBC115TDP6

TYPICAL CHARACTERISTICS NSBC115TDP6

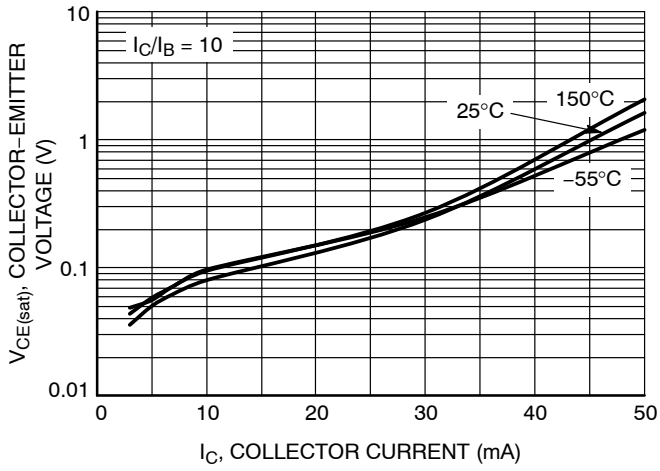


Figure 2. $V_{CE(sat)}$ vs. I_C

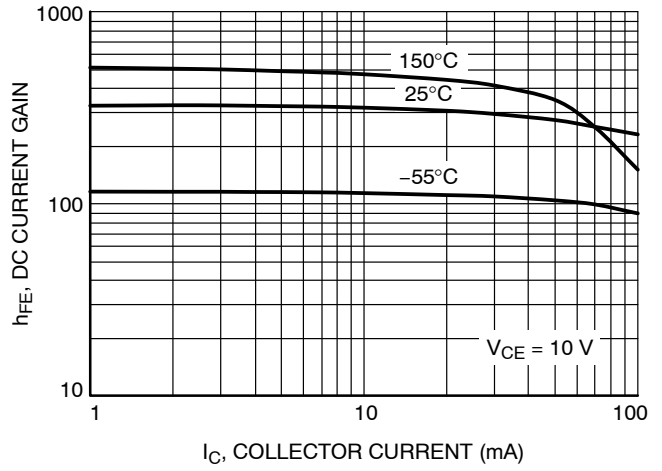


Figure 3. DC Current Gain

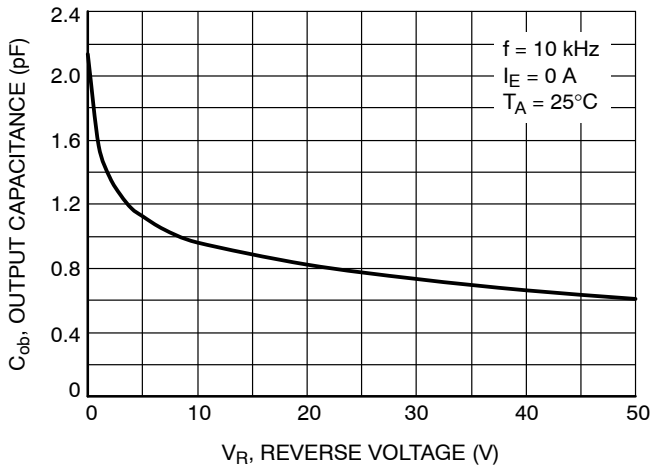


Figure 4. Output Capacitance

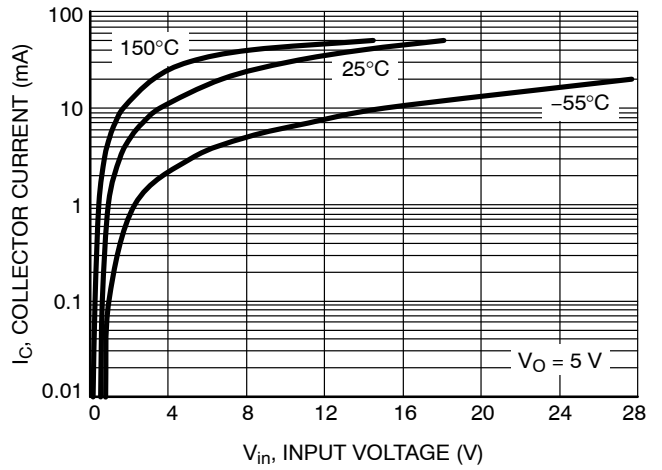


Figure 5. Output Current vs. Input Voltage

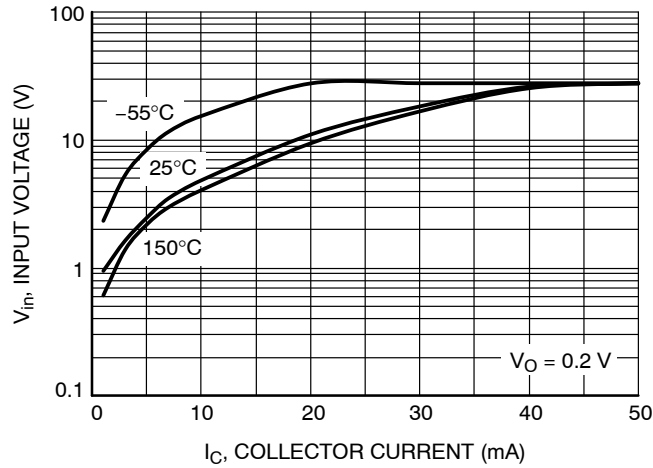
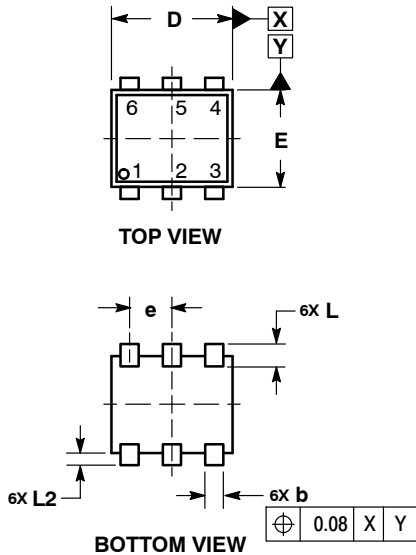


Figure 6. Input Voltage vs. Output Current

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PACKAGE DIMENSIONS

SOT-963 CASE 527AD ISSUE E

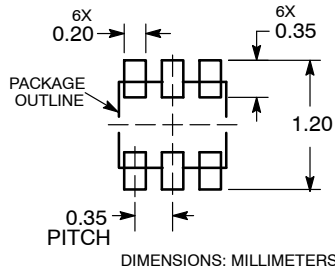



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H_E	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

RECOMMENDED MOUNTING FOOTPRINT



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