



SCCS014 - May 1994 - Revised February 2000

CY54/74FCT157T

Quad 2-Input Multiplexer

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 4.3 ns max. (Com'l), FCT-A speed at 5.0 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- ESD > 2000V
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Sink current 64 mA (Com'l), 32 mA (Mil)
- Source current 32 mA (Com'l), 12 mA (Mil)

Functional Description

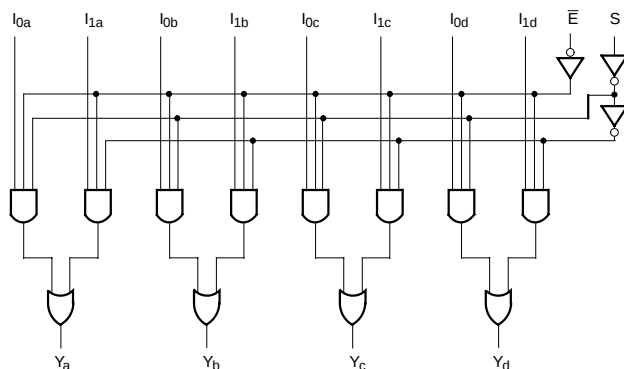
The FCT157T is a quad two-input multiplexer that selects four bits of data from two sources under the control of a common data Select input (S). The Enable input (E) is Active LOW. When ($\bar{E}$) is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the FCT157T. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the sixteen different functions of two variables with one variable common.

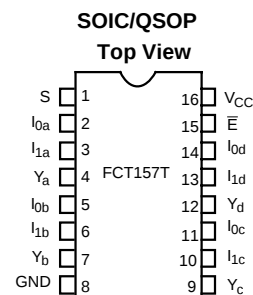
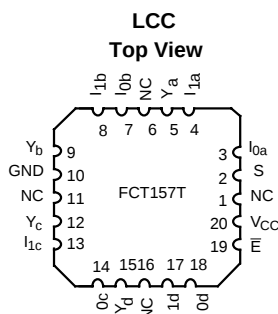
The FCT157T is a logic implementation of a four-pole, two-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

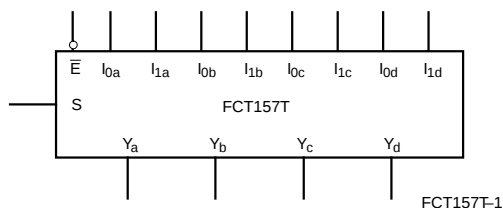
Logic Block Diagram, FCT157T



Pin Configurations



Logic Symbol



Pin Description

Name	Description
S	Common Select Input
$\bar{E}$	Enable Inputs (Active LOW)
I ₀	Data Inputs from Source 0
I ₁	Data Inputs from Source 1
Y	Non-Inverted Output

Function Table^[1]

Inputs				Outputs
E	S	I ₀	I ₁	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

Maximum Ratings^[2,3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -65°C to +135°C

Supply Voltage to Ground Potential..... -0.5V to +7.0V

DC Input Voltage -0.5V to +7.0V

DC Output Voltage -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) 120 mA

Power Dissipation 0.5W

Static Discharge Voltage..... >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	All	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	2.0			V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.3		V
		V _{CC} =Min., I _{OH} =-12 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.3	0.55	V
		V _{CC} =Min., I _{OL} =32 mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[6]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA
I _{OZH}	Off State HIGH-Level Output Current	V _{CC} = Max., V _{OUT} = 2.7V			10	μA
I _{OZL}	Off State LOW-Level Output Current	V _{CC} = Max., V _{OUT} = 0.5V			-10	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C_{IN}	Input Capacitance	5	10	pF
C_{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$	0.1	0.2	mA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC} = \text{Max.}, V_{IN} = 3.4V,^{[8]}$ $f_1 = 0, \text{Outputs Open}$	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ^[9]	$V_{CC} = \text{Max.}, \text{One Input Toggling,}$ $50\% \text{ Duty Cycle, Outputs Open,}$ $\overline{OE} = \text{GND}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.06	0.12	mA/MHz
I_C	Total Power Supply Current ^[10]	$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle,}$ Outputs Open, $\text{One Input Toggling at } f_1 = 10 \text{ MHz,}$ $\overline{OE} = \text{GND}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle,}$ Outputs Open, $\text{One Input Toggling at } f_1 = 10 \text{ MHz,}$ $\overline{OE} = \text{GND}, V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.0	2.4	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle,}$ Outputs Open, $\text{Four Bits Toggling at } f_1 = 2.5 \text{ MHz,}$ $\overline{OE} = \text{GND}, V_{IN} \leq 0.2V \text{ or } V_{IN} \geq V_{CC} - 0.2V$	0.7	1.4 ^[11]	mA
		$V_{CC} = \text{Max.}, 50\% \text{ Duty Cycle,}$ Outputs Open, $\text{Four Bits Toggling at } f_1 = 2.5 \text{ MHz,}$ $\overline{OE} = \text{GND}, V_{IN} = 3.4V \text{ or } V_{IN} = \text{GND}$	1.7	5.4 ^[11]	mA

Notes:

8. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0/2 + f_1 N_1)$
 I_{CC} = Quiescent Current with CMOS input levels
 ΔI_{CC} = Power Supply Current for a TTL HIGH input ($V_{IN} = 3.4V$)
 D_H = Duty Cycle for TTL inputs HIGH
 N_T = Number of TTL inputs at D_H
 I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
 f_0 = Clock frequency for registered devices, otherwise zero
 f_1 = Input signal frequency
 N_1 = Number of inputs changing at f_1
 All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT157T		FCT157AT				FCT157CT		Unit	Fig. No. ^[13]
		Commercial		Military		Commercial		Commercial			
		Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.	Min. ^[12]	Max.		
t _{PLH} t _{PHL}	Propagation Delay I to Y	1.5	6.0	1.5	5.8	1.5	5.0	1.5	4.3	ns	1, 3
t _{PLH} t _{PHL}	Propagation Delay E to Y	1.5	10.5	1.5	7.4	1.5	6.0	1.5	4.8	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay S to Y	1.5	10.5	1.5	8.1	1.5	7.0	1.5	5.2	ns	1, 3

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.3	CY74FCT157CTQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT157CTSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
5.0	CY74FCT157ATQCT	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT157ATSOC/SOCT	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY54FCT157ATLMB	L61	20-Pin Square Leadless Chip Carrier	Military

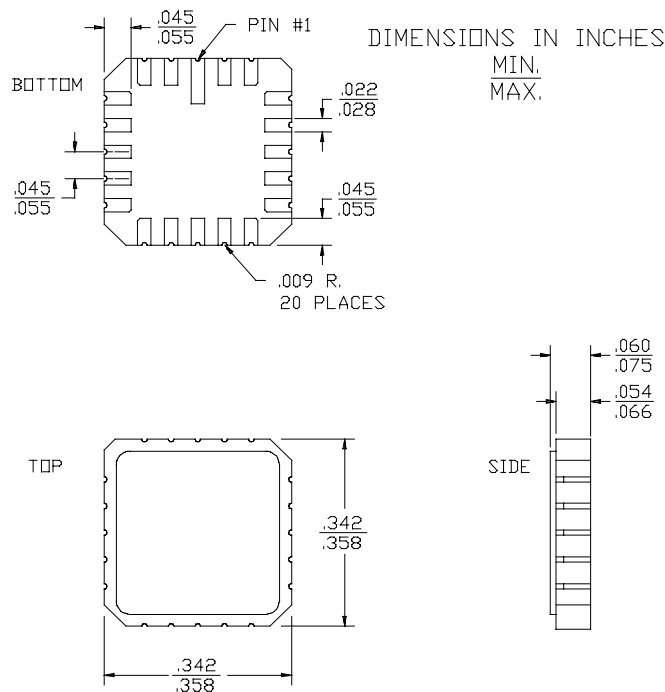
Note:

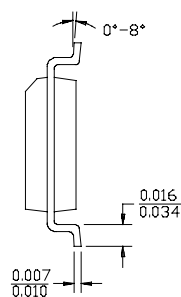
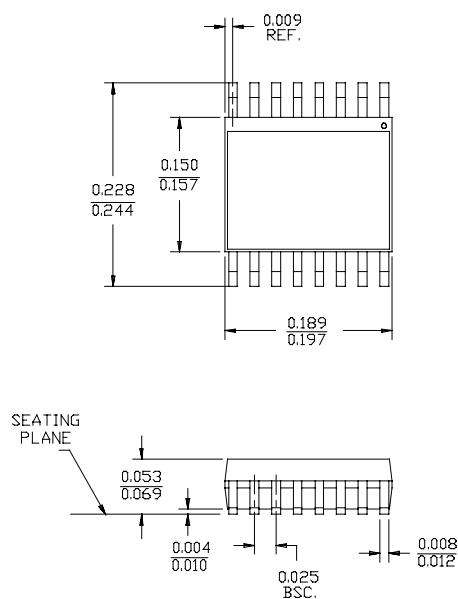
12. Minimum limits are specified but not tested on Propagation Delays.
 13. See "Parameter Measurement Information" in the General Information Section

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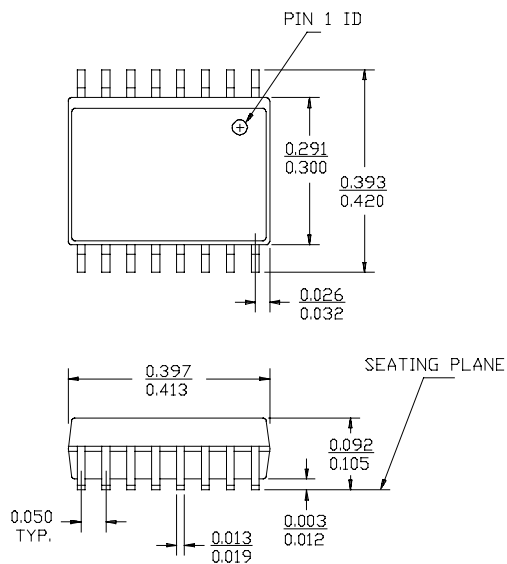
Package Diagrams
20-Pin Square Leadless Chip Carrier L61

MIL-STD-1835 C-2A

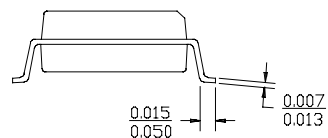


Package Diagrams (continued)
16-Lead Quarter Size Outline Q1


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.

16-Lead Molded SOIC S1


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.



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