



# BTW67 and BTW69 Series

STANDARD

50A SCRs

**Table 1: Main Features**

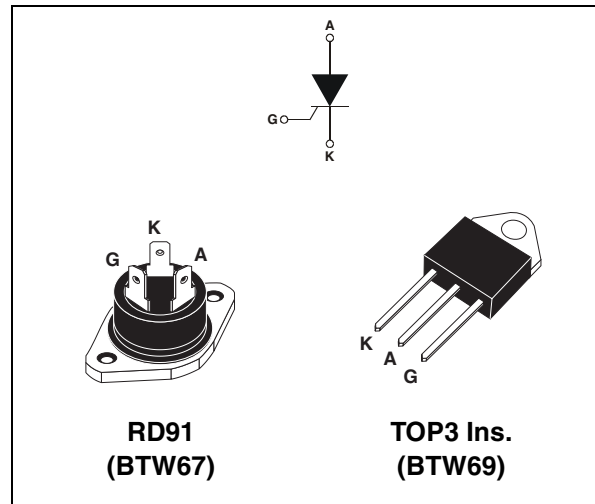
Symbol	Value	Unit
$I_{T(RMS)}$	50	A
$V_{DRM}/V_{RRM}$	600 to 1200	V
$I_{GT}$	80	mA

## DESCRIPTION

Available in high power packages, the **BTW67 / BTW69** Series is suitable in applications where power handling and power dissipation are critical, such as solid state relays, welding equipment, high power motor control.

Based on a clip assembly technology, they offer a superior performance in surge current handling capabilities.

Thanks to their internal ceramic pad, they provide high voltage insulation (2500V<sub>RMS</sub>), complying with UL standards (file ref: E81734).



**Table 2: Order Codes**

Part Numbers	Marking
BTW67-xxx	BTW67xxx
BTW69-xxxRG	BTW69xxx

**Table 3: Absolute Ratings** (limiting values)

Symbol	Parameter	Value	Unit	
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)	RD91 $T_c = 70^\circ\text{C}$	50	A
		TOP3 Ins. $T_c = 75^\circ\text{C}$		
$I_{T(AV)}$	Average on-state current (180° conduction angle)	RD91 $T_c = 70^\circ\text{C}$	32	A
		TOP3 Ins. $T_c = 75^\circ\text{C}$		
$I_{TSM}$	Non repetitive surge peak on-state current	$t_p = 8.3 \text{ ms}$ $T_j = 25^\circ\text{C}$	610	A
		$t_p = 10 \text{ ms}$ $T_j = 25^\circ\text{C}$	580	
$I^2t$	$I^2t$ Value for fusing	$T_j = 25^\circ\text{C}$	1680	A <sup>2</sup> s
$di/dt$	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r \leq 100 \text{ ns}$	F = 60 Hz $T_j = 125^\circ\text{C}$	50	A/ $\mu\text{s}$
$I_{GM}$	Peak gate current	$t_p = 20 \mu\text{s}$ $T_j = 125^\circ\text{C}$	8	A
$P_{G(AV)}$	Average gate power dissipation	$T_j = 125^\circ\text{C}$	1	W
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range		- 40 to + 150 - 40 to + 125	$^\circ\text{C}$
$V_{RGM}$	Maximum peak reverse gate voltage		5	V

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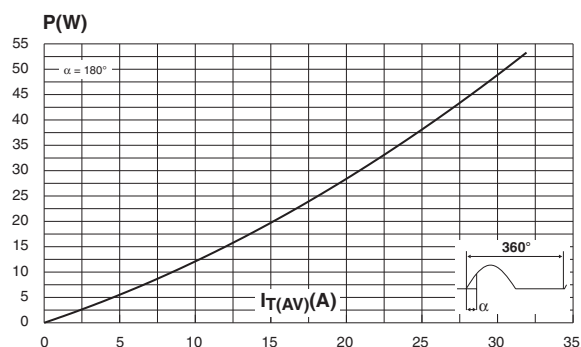
**Tables 4: Electrical Characteristics** ( $T_j = 25^\circ\text{C}$ , unless otherwise specified)

Symbol	Test Conditions		Value	Unit		
$I_{GT}$	$V_D = 12\text{ V}$	$R_L = 33\ \Omega$	MIN.	8	mA	
			MAX.	80		
$V_{GT}$			MAX.	1.3	V	
$V_{GD}$	$V_D = V_{DRM}$	$R_L = 3.3\ \text{k}\Omega$	$T_j = 125^\circ\text{C}$	MIN.	0.2	V
$I_H$	$I_T = 500\ \text{mA}$ Gate open			MAX.	150	mA
$I_L$	$I_G = 1.2 \times I_{GT}$			MAX.	200	mA
dV/dt	$V_D = 67\% V_{DRM}$ Gate open		$T_j = 125^\circ\text{C}$	MIN.	1000	V/ $\mu\text{s}$
$V_{TM}$	$I_{TM} = 100\ \text{A}$ $t_p = 380\ \mu\text{s}$		$T_j = 25^\circ\text{C}$	MAX.	1.9	V
$V_{T0}$	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	1.0	V
$R_d$	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	8.5	m $\Omega$
$I_{DRM}$ $I_{RRM}$	$V_{DRM} = V_{RRM}$		$T_j = 25^\circ\text{C}$	MAX.	10	$\mu\text{A}$
			$T_j = 125^\circ\text{C}$		5	mA

**Table 5: Thermal resistance**

Symbol	Parameter	Value	Unit	
$R_{th(j-c)}$	Junction to case (D.C.)	RD91 (Insulated)	1.0	$^\circ\text{C/W}$
		TOP3 Insulated	0.9	
$R_{th(j-a)}$	Junction to ambient (D.C.)	TOP3 Insulated	50	$^\circ\text{C/W}$

**Figure 1: Maximum average power dissipation versus average on-state current**



**Figure 2: Average and D.C. on-state current versus case temperature**

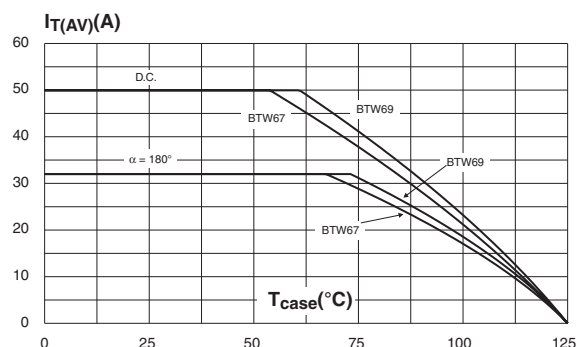


Figure 3: Relative variation of thermal impedance versus pulse duration

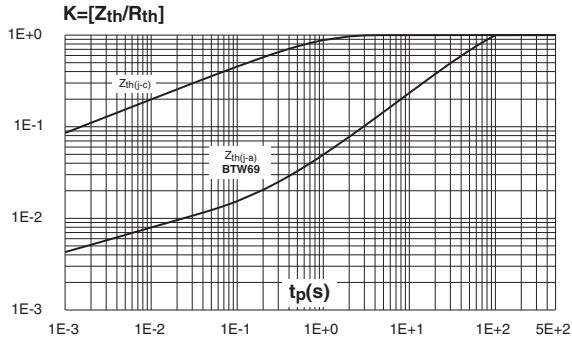


Figure 4: Relative variation of gate trigger current, holding current and latching current versus junction temperature

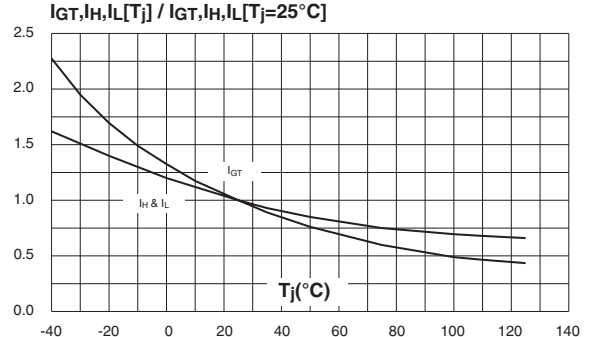


Figure 5: Surge peak on-state current versus number of cycles

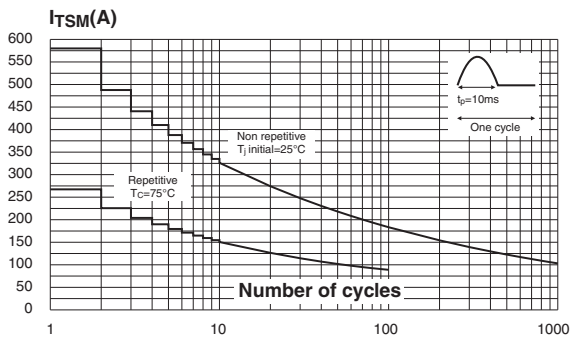


Figure 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10$  ms, and corresponding values of  $I^2t$

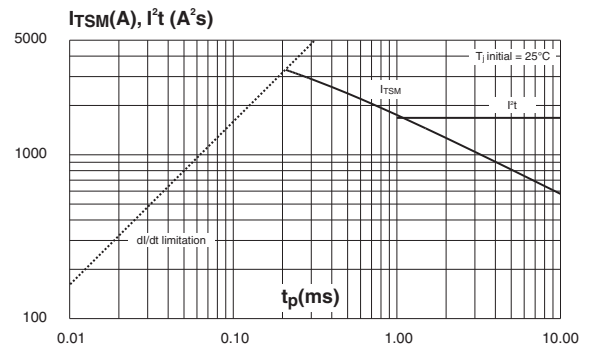
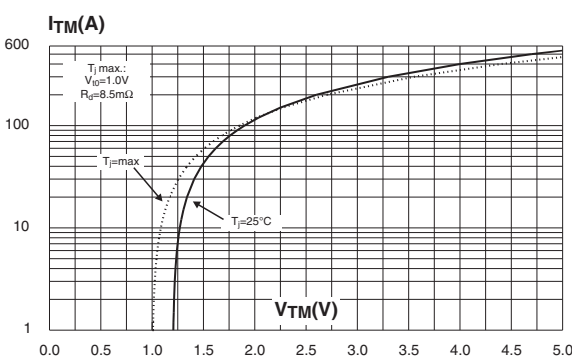


Figure 7: On-state characteristics (maximum values)



## BTW67 and BTW69 Series

Figure 8: Ordering Information Scheme

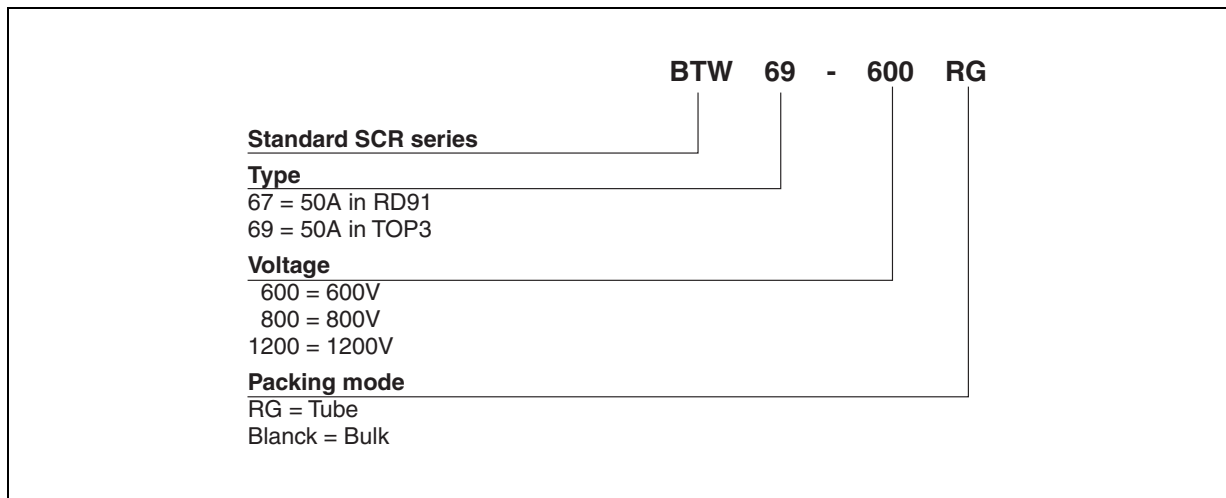


Table 6: Product Selector

Part Numbers	Voltage (xxx)			Sensitivity	Package
	600 V	800 V	1200 V		
BTW67-xxx	X	X	X	80 mA	RD91
BTW69-xxx	X	X	X	80 mA	TOP3 Ins.

Figure 9: RD91 Package Mechanical Data

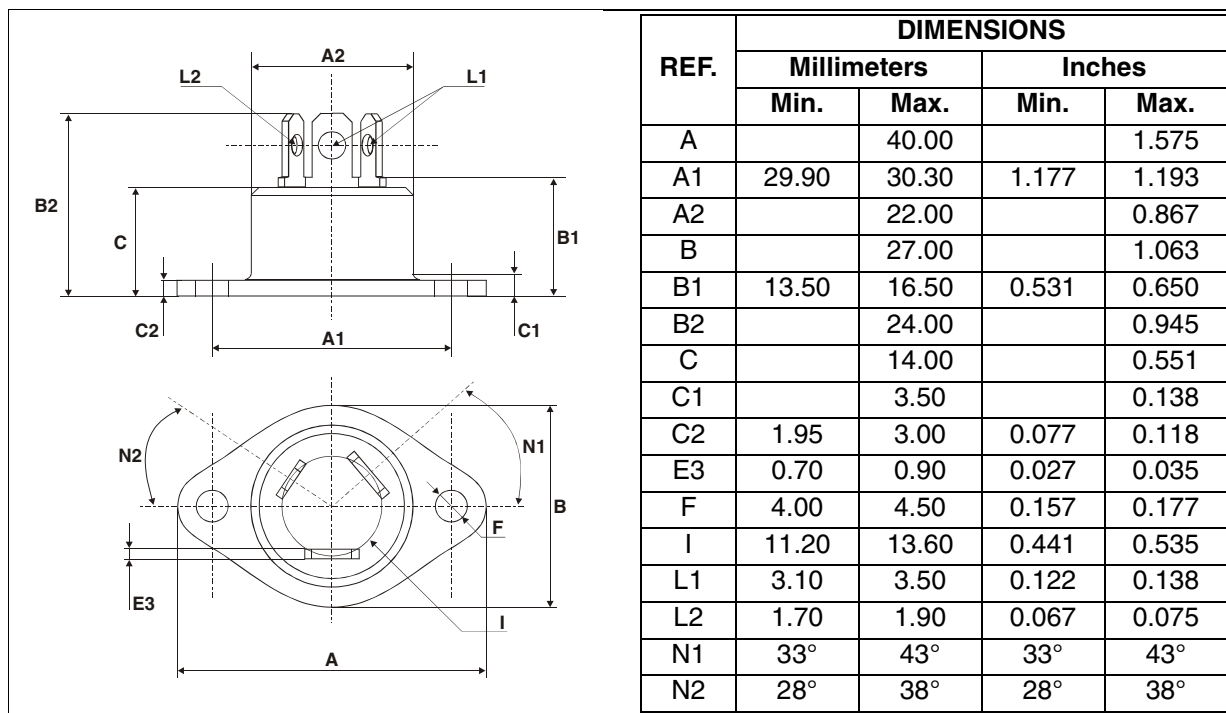
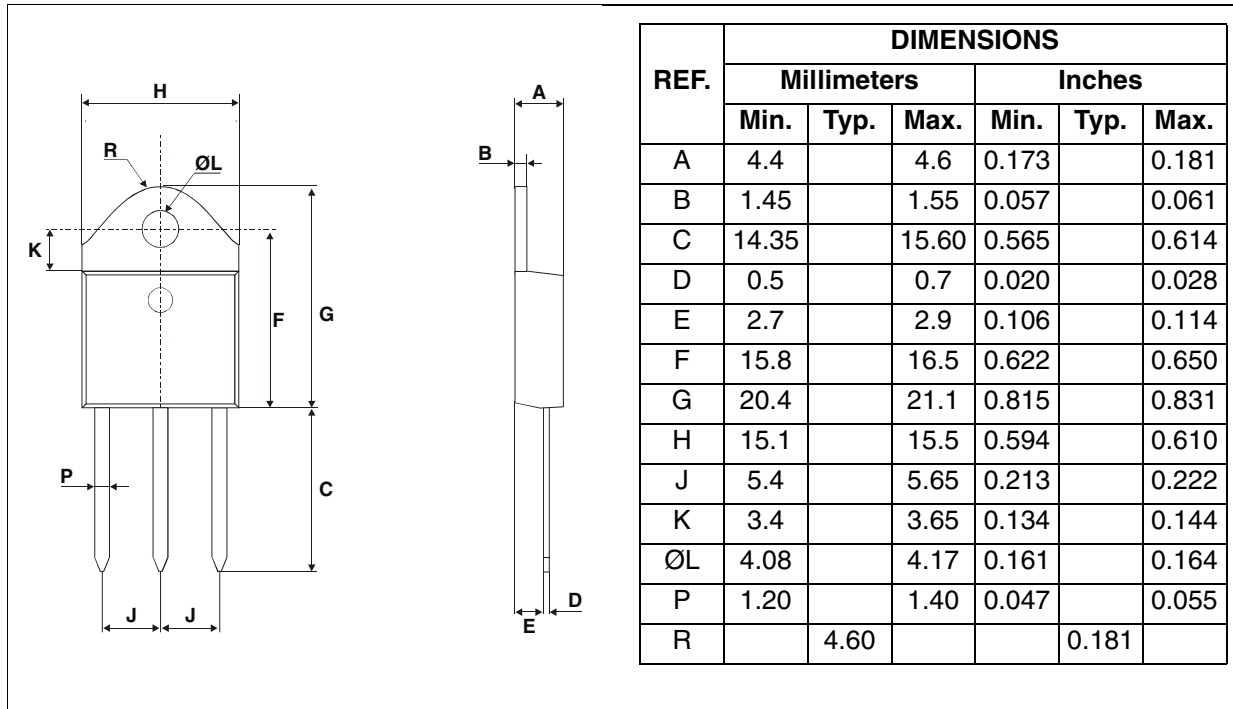


Figure 10: TOP3 Insulated Package Mechanical Data



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Table 7: Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
BTW67-xxx	BTW67xxx	RD91	20 g	25	Bulk
BTW69-xxxRG	BTW69xxx	TOP3 Ins.	4.5 g	30	Tube

Note: xxx = voltage

Table 8: Revision History

Date	Revision	Description of Changes
Apr-2001	4A	Last update.
13-Feb-2006	5	TOP3 Insulated delivery mode changed from bulk to tube. ECOPACK statement added.

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