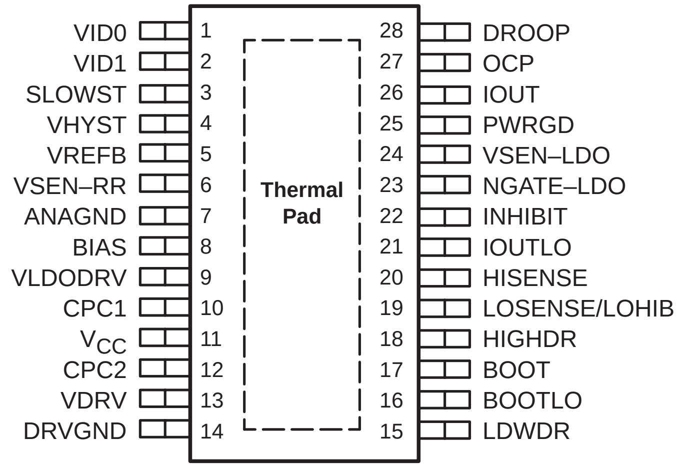
- **2.8 V – 5.5 V Input Voltage Range**
- **Programmable Dual Output Controller Supports Popular DSP and Microcontroller Core and I/O Voltages**
  - **Switching Regulator Controls Core Voltage**
  - **Low Dropout Controller Regulates I/O Voltage**
- **Programmable Slow-Start Ensures Simultaneous Powerup of Both Outputs**
- **Power Good Output Monitors Both Outputs**
- **Fast Ripple Regulator Reduces Bulk Capacitance for Lower System Costs**
- **±1.5% Reference Voltage Tolerance**
- **Efficiencies Greater than 90%**
- **Overvoltage, Undervoltage, and Adjustable Overcurrent Protection**
- **Drives Low-Cost Logic Level N-Channel MOSFETs Through Entire Input Voltage Range**
- **Evaluation Module TPS56300EVM–139 Available**

PWP PACKAGE
(TOP VIEW)

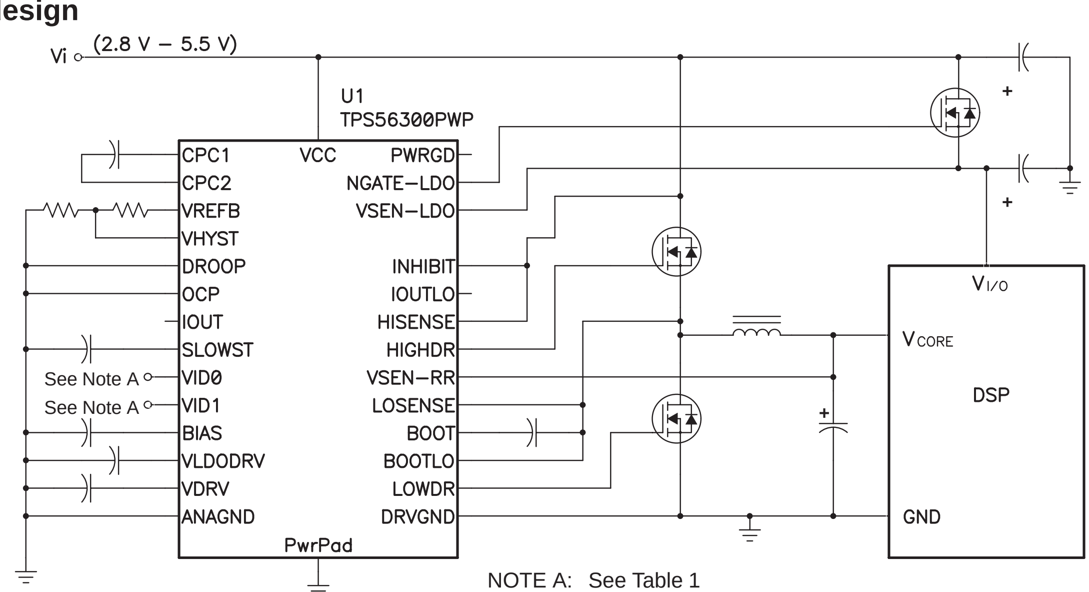


PowerPAD™ Package

description

The high performance TPS56300 synchronous-buck regulator provides two supply voltages to power the core and I/O of digital signal processors, such as the ‘C6000 family. The ripple regulator, using hysteretic control with droop compensation, is configured for the core voltage and features fast transient response time reducing output bulk capacitance (continued).

typical design



NOTE A: See Table 1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

description (continued)

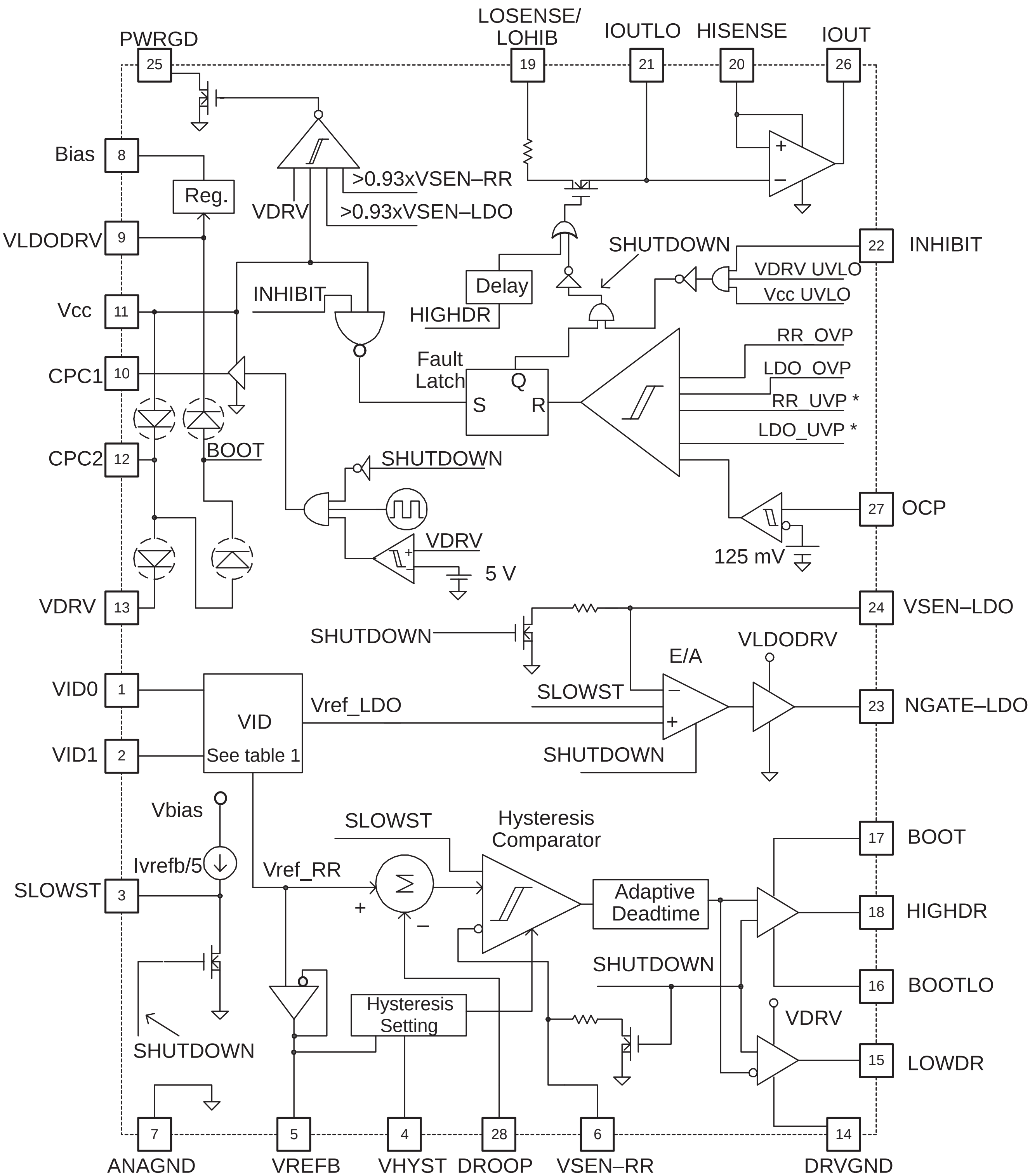
The LDO controller drives an external N-channel power MOSFET and functions as an LDO regulator, suitable for powering the I/O or as a power distribution switch. To promote better system reliability during power up, voltage sequencing and protection are controlled such that the core and I/O power up together with the same slow-start voltage. At power down, the LDO and ripple regulator are discharged towards ground for added protection. The TPS56300 also includes inhibit, slowstart, and under-voltage lockout features to aide in controlling power sequencing. A tri-level voltage identification network (VID) sets both regulated voltages to any of 9 preset voltage pairs from 1.3 V to 3.3 V. Other voltages are possible by implementing an external voltage divider. Strong MOSFET drivers, with a typical peak current rating of 2-A sink and source are included on chip, enabling high system currents beyond 30 A. The high-side driver features a floating bootstrap driver with the internal bootstrap synchronous rectifier. Many protection features are incorporated within the device to ensure better system integrity. An open-drain output POWER GOOD status circuit monitors both output voltages, and is pulled low if either output fall below the threshold. An over current shutdown circuit protects the high-side power MOSFET against short-to-ground faults at load or the phase node, while over voltage protection turns off the output drivers and LDO controller if either output exceeds its threshold. Under voltage protection turns off the high-side and low-side MOSFET drivers and the LDO controller if either output is 25% below V_{REF}. Lossless current-sensing is done by detecting the drain-source voltage drop across the high-side power MOSFET while it is conducting. The TPS56300 is fully compliant with TI DSP power requirements such as the ‘C6000 family.

AVAILABLE OPTIONS

T_J	PACKAGES	EVALUATION MODULE
	TSSOP† (PWP)	
–40°C to 125°C	TPS56300PWP	TPS56300EVM–139 (SLVP139)

† The PWP package is also available taped and reel. To order, add an R to the end of the part number (e.g., TPS56300PWPR).

functional block diagram



RR–Ripple Regulator

Synchronous FET

* UVP is disabled during slowstart

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
VID0	1	Voltage Identification input 0. VID pins are tri-level programming pins that set the output voltages for both converters. The code pattern for setting the output voltage is located in table 1. The VID pins are internally pulled to Vbias/2, allowing floating voltage set to logic 1 (see table 1).
VID1	2	Voltage Identification input 1 (see VID0 above and table 1).
SLOWST	3	Slow start (soft start). A capacitor from pin 3 to GND sets the slowstart time for VOUT-RR and VOUT-LDO. Both supplies will ramp-up together while tracking the slow-start voltage.
VHYST	4	Hysteresis set pin. The hysteresis is set by 2 × (VREFB – Vhyst).
VREFB	5	Buffered ripple regulator reference voltage from VID network.
VSEN-RR	6	Ripple regulator VOLTAGE SENSE input. This pin is connected to the ripple regulator output. It is used to sense the ripple regulator voltage for regulation, OVP, UVP, and Powergood functions.. It is recommended that an RC low pass filter be connected at this pin to filter high frequency noise.
ANAGND	7	Analog ground
BIAS	8	Analog BIAS pin. Recommended that a 1-µF capacitor be connected to ANAGND.
VLDODRV	9	Output of charge pump generated through bootstrap diode. Approximately equal to VDRV + V_{IN} – 300mV. Used as supply for LDO driver and Bias regulator. Recommended that a 1-µF capacitor be connected to DRVGND.
CPC1	10	Connect one end of Charge pump capacitor. Recommended that a 1-µF capacitor be connected from CPC1 to CPC2.
V_{CC}	11	3.3 V or 5 V supply (2.8 V – 5.5 V). Recommended that a low ESR capacitor be connected directly from V_{CC} to DRVGND. (Bulk capacitors supplied at power stage input).
CPC2	12	Other end of charge pump capacitor from CPC1.
VDRV	13	Regulated output of internal charge pump. Supplies DRIVE charge for the low-side MOSFET driver (5V). Recommended that a 10-µF capacitor be connected to DRVGND.
DRVGND	14	Drive ground. Ground for FET drivers. Connect to source of low-side FET.
LOWDR	15	Low drive. Output drive to synchronous rectifier low-side FET.
BOOTLO	16	Bootstrap low. This pin connects to the junction of the high-side and low-side FETs.
BOOT	17	Bootstrap pin. Connect a 1-µF low ESR capacitor to BOOTLO to generate floating drive for the high-side FET driver.
HIGHDR	18	High drive. Output drive to high-side power switching FETs
LOSENSE/ LOHIB	19	Low sense/low-side inhibit. This pin is connected to the junction of the high and low-side FETs and is used in current sensing and the anti-cross-conduction to eliminate shoot-through current.
HISENSE	20	High current sense. For current sensing across high-side FETs, connect to the drain of the high-side FETs.
IOUTLO	21	Current sense low output. Voltage on this pin is the voltage on the LOSENSE pin when the high-side FETs are on.
INHIBIT	22	Inhibits the drive signals to the MOSFET drivers. IC is in low Iq state if INHIBIT is grounded. It is recommended that an external pullup resistor be connected to 5 V.
NGATE-LDO	23	Drives external N-channel power MOSFET to regulate LDO voltage to VREF-LDO.
VSEN–LDO	24	LDO voltage sense. This pin is connected to the LDO output. It is used to sense the LDO voltage for regulation, OVP, UVP, and power good functions.
PWRGD	25	Power good. Power good signal goes high when output voltage is about 93% of V_{REF} for both ripple regulator and LDO. This is an open-drain output.

Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IOUT	26		Current signal output. Output voltage on this pin is proportional to the load current as measured across the high-side FETs on-resistance. The voltage on this pin equals $2 \times R_{ON} \times$ IOUT, where Ron is the equivalent on-resistance of the high-side FETs
OCP	27		Over current protection. Current limit trip point for ripple regulator is set with a resistor divider between IOUT pin and ANAGND.
DROOP	28		Droop voltage. Voltage input used to set the amount of output voltage droop as a function of load current. The amount of droop compensation is set with a resistor divider between the IOUT pin and ANAGND.

Table 1. Voltage Identification Code§¶

VID Terminals†		VREF–RR‡ (Vdc)	VREF–LDO‡ (Vdc)
VID1	VID0		
0	0	1.30	1.5
0	1	1.50	1.80
0	2	1.30	1.80
1	0	1.80	3.30
1	1	1.30	1.30
1	2	2.50	3.30
2	0	1.30	2.50
2	1	1.50	3.30
2	2	1.80	2.50

† 0 = ground (GND), 1 = floating(Vbias/2), 2 = (Vbias)
‡ RR = Ripple Regulator, LDO = Low Drop-Out Regulator
§ Vbias/2 is internal, leave VID pin floating. Adding an external 0.1-µF capacitor to ANAGND may be used to avoid erroneous level.
¶ External resistors may be used as a voltage divider (from V_{OUT} to VSEN–xx to Gnd) to program output voltages to other values.

absolute maximum ratings over operating virtual junction temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note1)		–0.3 V to 6 V
Input voltage range:	VDRV	–0.3 V to 7 V
	BOOT to DRVGND (High-side Driver ON)	–0.3 V to 15 V
	BOOT to BOOTLO	–0.3 V to 7 V
	BOOT to HIGHDRV	–0.3 V to 7 V
	BOOTLO to DRVGND	–0.5 V to 15 V
	DRV to DRVGND	–0.3 V to 7 V
	BIAS to ANAGND	–0.3 V to 7 V
	INHIBIT	–0.3 V to 7 V
	DROOP	–0.3 V to V_{CC} + 0.3 V
	OCP	–0.3 V to 7 V
	VID0, VID1 (tri-level terminals)	–0.3 V to VBIAS + 0.3 V
	PWRGD	–0.3 V to 6 V
	LOSENSE, LOHIB	–0.5 V to 14 V
	IOUTLO	–0.3 V to 14 V
	HISENSE	–0.3 V to 7 V
	VSEN–LDO	–0.3 V to 6 V
	VSEN–RR	–0.3 V to 6 V
Voltage difference between ANAGND and DRVGND		±300 mV
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		–40°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to ANAGND.

DISSIPATION RATING TABLE

PWP	T_A < 25°C	Derating Factor‡	T_A = 70°C	T_A = 85°C
PowerPAD mounted	3.58 W	0.0358 W/°C	1.96 W	1.43 W
PowerPAD unmounted	1.78 W	0.0178 W/°C	0.98 W	0.71 W

JUNCTION-CASE THERMAL RESISTANCE TABLE

Junction-case thermal resistance	0.72 °C/W

‡ Test Board Conditions:

1. Thickness: 0.062”
2. 3”x 3” (for packages < 27 mm long)
3. 4” x 4” (for packages > 27 mm long)
4. 2 oz. Copper traces located on the top of the board (0.071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1oz. Copper (0.036 mm thick)
7. Thermal vias, 0.33 mm diameter, 1.5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief SLMA002.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

input

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Supply voltage range		2.8	3.3	5.5	V
I_{CC} Quiescent current	INHIBIT = 0 V, V_{CC} = 5 V		15		mA

NOTE 2. Ensured by design, not production tested.

reference/voltage identification

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
D0–D1 High level input voltage (2)		Vbias – 0.3 V			V
D0–D1 Mid level floating voltage (1)		$\frac{V_{bias}}{2} - 1$		$\frac{V_{bias}}{2} + 1$	V
D0–D1 Low level input voltage (0)				0.3	V
Input pull-to-mid resistance		36.5	73	95	KΩ

cumulative reference

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Cumulative accuracy ripple regulator	V_{REF} = 1.3 V, T_J = 25°C, Hysteresis window = 30 mV,	–1.3	0.25	1.3	%
	V_{REF} = 1.3 V, T_J = –40°C, Hysteresis window = 30 mV, See Note 2		–0.2		
	V_{REF} = full range, Droop = 0, Hysteresis window = 30 mV, See Note 2	–1.5		1.5	
Cumulative accuracy LDO	V_{REF} = 1.3 V, Closed Loop, T_J = 25°C, I_O=0.1 A, Pass device = IRFZ24N, See Note 2	–2		2	%
	V_{REF} = full range, Closed Loop, See Note 2, I_O=0.1 A, Pass device = IRFZ24N,	–2.5		2.5	

NOTE 2. Ensured by design, not production tested.

hysteretic comparator(ripreg)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current	See Note 2			500	nA
Hysteresis accuracy	$V_{VREFB} - V_{VHYST}$ = 15 mV, Hysteresis window = 30mV	–3.5		3.5	mV
Maximum hysteresis setting	$V_{VREFB} - V_{VHYST}$ = 30 mV, See Note 2	60			mV
Propagation delay time from VSENSE to HIGHDR or LOWDR (excluding deadtime)	10 mV overdrive, 1.3 V <= V_{REF} <= 3.3 V, See Note 2		150	250	ns
Prefilter pole frequency	See Note 2		5		MHz

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

overvoltage protection

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVP ripple regulator trip point (RR)	Upper threshold	112	115	120	$\%V_{REF}$
Hysteresis (RR)	Upper threshold – lower threshold, See Note 2		10		mV
Comparator propagation delay time (RR)	$V_{overdrive}$ = 30mV, See Note 2		1		µs
Deglitch time (includes comparator propagation delay time) (RR)	$V_{overdrive}$ = 30mV, See Note 2	2.25		11	µs
OVP LDO trip point (LDO)	Upper threshold	112	115	120	$\%V_{REF}$
Hysteresis (LDO)	Upper threshold – lower threshold, See Note 2		10		mV
Comparator propagation delay time (LDO)	$V_{overdrive}$ = 50mV, See Note 2		1		µs
Deglitch time (includes comparator propagation delay time) (LDO)	$V_{overdrive}$ = 50mV, See Note 2	2.25		11	µs

NOTE 2. Ensured by design, not production tested.

undervoltage protection

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UVP ripple regulator trip point (RR)	Lower threshold	70	75	80	$\%V_{REF}$
Hysteresis (RR)	Upper threshold – lower threshold, See Note 2		10		mV
Comparator propagation delay time (RR)	$V_{overdrive}$ = 50mV, See Note 2		1		µs
Deglitch time (includes comparator propagation delay time) (RR)	$V_{overdrive}$ = 50mV, See Note 2	0.1		1	ms
UVP LDO trip point (LDO)	Lower threshold	70	75	80	$\%V_{REF}$
Hysteresis (LDO)	Upper threshold – lower threshold, See Note 2		10		mV
Comparator propagation delay time (LDO)	$V_{overdrive}$ = 50mV, See Note 2		1		µs
Deglitch time (includes comparator propagation delay time) (LDO)	$V_{overdrive}$ = 50mV, See Note 2	0.1		1	ms

NOTE 2. Ensured by design, not production tested.

inhibit comparator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold			2.1	2.35	V
	T_J = –40°C, See Note 2		2.1		
Stop threshold		1.79			V

NOTE 2. Ensured by design, not production tested.

VDRV UVLO

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold	See Note 2			4.9	V
Hysteresis	See Note 2	0.3	0.35		V
Stop threshold	See Note 2	4.4			V

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

slowstart

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Charge current	$V_{(S/S)}$ = 0.5V, Resistance from VREFB pin to ANAGND = 20 kΩ VREFB = 1.3 V, Ichg = (I_{VREFB}/5)	10.4	13	15.6	µA
Discharge current	$V_{(S/S)}$ = 1.3 V	3			mA
Comparator input offset voltage				10	mV
Comparator input bias current	See Note 2		10	100	nA
Hysteresis accuracy		–7.5		7.5	mV
Comparator propagation delay	Overdrive = 10 mV, See Note 2		560	1000	ns

NOTE 2. Ensured by design, not production tested.

V_{CC} UVLO

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Start threshold	See Note 2		2.72	2.80	V
	T_J = –40°C, See Note 2		2.71		
Stop threshold	See Note 2	2.48			V

NOTE 2. Ensured by design, not production tested.

power good

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage trip point ripple regulator (VSENSE–RR)	V_{IN} and VDRV above UVLO thresholds	90	93	95	%V_{REF}
	T_J = –40°C, See Note 2		93		
Undervoltage trip point LDO (VSENSE–LDO)	V_{IN} and VDRV above UVLO thresholds	90	93	95	%V_{REF}
	T_J = –40°C, See Note 2		93		
Output saturation voltage	I_O=5 mA		0.5	0.75	V
Leakage current	V_{PGD} = 4.5V		1		µA
Hysteresis	V_{REF} = 1.3V, 1.5V, or 1.8V		50	75	mV
	V_{REF} = 2.5V, or 3.3V		100	125	mV
Comparator high–low transition time (propagation delay only)	See Note 2		1		µs
Comparator low–high transition time (propagation delay + deglitch)	See Note 2	0.2	1	2	ms

NOTE 2. Ensured by design, not production tested.

droop compensation

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Initial accuracy	V_{DROOP} = 50 mV	46		54	mV

overcurrent protection (RR)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OCP trip point		118	130	142	mV
Input bias current				300	nA
Comparator propagation delay time	$V_{overdrive}$ = 30mV, See Note 2		1		µs
Deglitch time (includes comparator propagation delay time)	$V_{overdrive}$ = 30mV, See Note 2	2.25		11	µs

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

high-side VDS sensing

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain			2		V/V
Initial accuracy	$V_{HISENSE}$ = 3.3 V, V_{IOUTLO} = 3.2 V, Differential input to Vds sensing amp = 100 mV	194		208	mV
Common-mode rejection ratio	$V_{HISENSE}$=2.8 V to 5.5 V, $V_{HISENSE}$– V_{IOUTLO}=100 mV	69	75		dB
Sink current (IOUTLO)	2.8 V < V_{IOUTLO} < 5.5 V			250	nA
Source current (IOUT)	V_{IOUT} = 0.5 V, $V_{HISENSE}$=3.3 V, V_{IOUTLO}=2.8 V	500			µA
Sink current (IOUT)	V_{IOUT} = 0.05 V, $V_{HISENSE}$=3.35 V, V_{IOUTLO}=3.3 V	50			µA
Output voltage swing	$V_{HISENSE}$=5.5 V, R_{IOUT} = 10 kΩ	0		1.75	V
	$V_{HISENSE}$=4.5 V, R_{IOUT} = 10 kΩ	0		1.5	
	$V_{HISENSE}$=3 V, R_{IOUT} = 10 kΩ	0		0.75	
LOSENSE high level input voltage	$V_{HISENSE}$=2.8 V, See Note 2	1.77			V
LOSENSE low level input voltage	$V_{HISENSE}$=2.8 V, See Note 2			1.49	V
LOSENSE high level input voltage	$V_{HISENSE}$=4.5 V, See Note 2	2.85			V
LOSENSE low level input voltage	$V_{HISENSE}$=4.5 V, See Note 2			2.4	V
LOSENSE high level input voltage	$V_{HISENSE}$=5.5 V, See Note 2	3.80			V
LOSENSE low level input voltage	$V_{HISENSE}$=5.5 V, See Note 2			3.2	V
Sample/hold resistance	$V_{HISENSE}$ = 6 V, See Note 2	70		90	Ω
	$V_{HISENSE}$ = 4.5 V, See Note 2	80		100	
	$V_{HISENSE}$ = 3.6 V, See Note 2	90		120	
	$V_{HISENSE}$ = 2.8 V, See Note 2	120		180	
Response time (measured from 90% of V_{IOUTLO} to 90% of V_{IOUT})	$V_{HISENSE}$ = 2.55 V, V_{IOUTLO} pulsed from 2.55 V to 2.45 V, 100 ns rise and fall times, See Note 2			4	µs
	$V_{HISENSE}$ = 2.8 V, V_{IOUTLO} pulsed from 2.8 V to 2.7 V, 100 ns rise and fall times, See Note 2			3.5	
	$V_{HISENSE}$ = 4.5 V, V_{IOUTLO} pulsed from 4.5V to 4.4V, 100 ns rise and fall times, See Note 2			3	
	$V_{HISENSE}$ = 5.5 V, V_{IOUTLO} pulsed from 5.5 V to 5.9 V, 100 ns rise and fall times, See Note 2			3	
Short circuit protection rising edge delay	LOSENSE grounded, See Note 2	300		500	ns
Sample/hold switch turnon/turnoff delay	2.8V < $V_{HISENSE}$ < 5.5V, $V_{LOSENSE}$ = $V_{HISENSE}$, See Note 2	30		100	ns

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

buffered reference

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VREFB output voltage	I_{REFB}=50 µA,	Accuracy from V_{REF} nominal	V_{REF} –1.5%	V_{REF}	V_{REF} +1.5%	V
	I_{REFB}=50 µA, T_J = –40°C,	Accuracy from V_{REF} nominal See Note 2		V_{REF}–0.6%		
VREFB load regulation	10 µA < I_{REFB} < 500 µA			2		mV

NOTE 2. Ensured by design, not production tested.

thermal shutdown

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Over temperature trip point	See Note 2		145		°C
Hysteresis	See Note 2		10		°C

NOTE 2. Ensured by design, not production tested.

synch charge pump regulator

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Internal oscillator frequency	2.8 V < V_{IN} < 5.5 V, I_{DRV} = 50 mA,	VDRV=5 V	200	300	400	kHz
Internal oscillator turnon threshold	V_{CC} above UVLO threshold,	See Note 2	5.05	5.2		V
Internal oscillator turnon hysteresis	V_{CC} above UVLO threshold,	See Note 2			20	mV

NOTE 2. Ensured by design, not production tested.

hysteretic comparator (charge pump)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Threshold	V_{IN} above UVLO threshold,	See Note 2	5.05	5.2		V
Hysteresis	V_{IN} above UVLO threshold,	See Note 2			20	mV

NOTE 2. Ensured by design, not production tested.

bias regulator

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output voltage	2.8V < V_{IN} < 5.5 V, Rip reg operating	See Note 3		6.1		V

NOTE 3. The BIAS regulator is designed to provide a quiet bias supply for TPS56300 controller. External loads should not be driven by the BIAS Regulator.

deadtime circuit

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LOSENSE/LOHIB high level input voltage	$V_{HISENSE}$=2.55 V – 5.5 V,	See Note 2	2.4			V
LOSENSE/LOHIB low level input voltage	$V_{HISENSE}$=2.55 V – 5.5 V,	See Note 2			1.33	V
LOWDR high level input voltage	$V_{HISENSE}$=2.55 V–5.5 V,	See Note 2	3			V
LOWDR low level input voltage	$V_{HISENSE}$=2.55 V–5.5 V,	See Note 2			1.7	V
Driver nonoverlap time	C_{lowdr} = 9 nF, 10% threshold on LOWDR, VDRV=5 V		40		170	ns

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

output drivers (see Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Peak output current	Duty cycle < 2%, tpw < 100 us, $V_{BOOT} - V_{BOOTLO}$ = 4.5V, V_{HIGHDR} = 4V (sink), See Note 2 and Figure 15	0.7	2		A
	Duty cycle < 2%, tpw < 100 us, $V_{BOOT} - V_{BOOTLO}$ = 4.5V, V_{HIGHDR} = 0.5V (src), See Note 2 and Figure 15	1.2	2		
	Duty cycle < 2%, tpw < 100 µs, V_{DRV} = 4.5 V, V_{LOWDR} = 4 V (sink) See Note 2 and Figure 15	1.3	2		
	Duty cycle < 2%, tpw < 100 us, V_{DRV} = 4.5 V, V_{LOWDR} = 0.5 V (src), See Note 2 and Figure 15	1.4	2		
Output resistance	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5 V See Note 2			5	Ω
	$V_{BOOT} - V_{BOOTLO}$ = 4.5V, V_{HIGHDR} = 4 V, See Note 2			45	
	V_{DRV} = 4.5V, V_{LOWDR} = 0.5V, See Note 2			9	
	V_{DRV} = 4.5V, V_{LOWDR} = 4V, See Note 2			45	
HIGHDR rise/fall time (see Note 7)	C_I = 3.3 nF, V_{BOOT}= 4.5V, V_{BOOTLO}=grounded			60	ns
LOWDR rise/fall time (see Note 7)	C_I = 3.3 nF, V_{DRV}= 4.5V			40	ns
High-side driver quiescent current	INHIBIT grounded, V_{IN} < UVLO; VBOOT=6V, BOOTLO grounded			10	µA
	INHIBIT connected to +5 V, V_{IN} > UVLO Fswx = 200KHz, VBOOT = 5.5 V, BOOTLO = 0 C_{HIGHDR} = 50 pF See Note 2		2		mA

NOTES: 2. Ensured by design, not production tested.
5. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{ds(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

LDO N-channel output driver

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Peak output current	V_{LDODRV} = 7.5V, V_{N-DRV}=3 V(src), $V_{IOSENSE} = 0.9 \times V_{LDOREF}$, See Note 2	190	200		µA
	V_{LDODRV} = 7.5V, V_{N-DRV}=0 V(snk), $V_{IOSENSE} = 1.1 \times V_{LDOREF}$, See Note 2	1.5			mA
Open loop voltage gain ($V_{NGATE-LDO} / V_{SENSE-LDO}$)	V_{IN} = 5.5 V, 7.5 V ≥ $V_{NGATE-LDO}$ ≥ 0.5 V, See Note 2	3000 (70)			V/V (dB)
Power supply ripple rejection	f=1 kHz, C_O=10 µF, T_J=125 °C, 5.5 V ≥ V_{IN} ≥ 2.55 V, See Note 2	60			dB

NOTE 2. Ensured by design, not production tested.

electrical characteristics T_J = 0° to 125°C, V_{CC} = 2.8 V to 5.5 V (unless otherwise noted)

$V_{SENSE-RR}$ and $V_{SENSE-LDO}$ discharge

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{SENSE-RR}$ discharge FET current saturation	$V_{SENSE-RR}$ = 1.5 V,	See Note 2		5		mA
$V_{SENSE-RR}$ discharge series resistance (limits current)	INHIBIT = 0 V,	V_{IN} = 5.5 V		1		kΩ
$V_{SENSE-RR}$ discharge FET propagation delay time	See Note 2				100	ns
$V_{SENSE-LDO}$ discharge FET current saturation	$V_{SENSE-LDO}$ = 3.3 V,	See Note 2		5		mA
$V_{SENSE-LDO}$ discharge series resistance (limits current)	INHIBIT = 0 V,	V_{IN} = 5.5 V,		1		kΩ
$V_{SENSE-LDO}$ discharge FET propagation delay time	See Note 2				100	ns

NOTE 2. Ensured by design, not production tested.

detailed description

reference/voltage identification

The reference/voltage identification (VID) section consists of a temperature compensated bandgap reference and a 2-pin voltage selection network. Both ripple regulator and LDO reference voltages are programmed with each VID setting. The 2 VID pins are inputs to the VID selection network and are tri-level inputs that may be set to GND, floating (internally 2.5V), or VDRV. The VID codes allow the controller to power both current and future DSP products. The output voltages may also be programmed by external resistor voltage dividers for any values not included in the VID code settings. Refer to Table 1 for the VID code settings. The output voltages of the VID network, VREF–RR & VREF–LDO, are within 1.5% of the nominal setting for all the VID range of 1.3V to 3.3V. The reference tolerance conditions include a junction temperature range of –40°C to +125°C and a V_{CC} supply voltage range of 2.8 V to 5.5 V. The VREF–RR output of the reference/VID network is indirectly brought out through a buffer to the VREFB pin. The voltage on this pin will be within 1.5% of VREF–RR. It is not recommended to drive loads with VREFB, other than setting the hysteresis of the hysteretic comparator, because the current drawn from VREFB sets the charging current for the slowstart capacitor. Refer to the *Slowstart* section for additional information.

hysteretic comparator

The hysteretic comparator regulates the output voltage of the synchronous-buck converter. The hysteresis is set by 2 external resistors and is centered around V_{REF}. The 2 external resistors form a resistor divider from VREFB to ANAGND, and the divided down voltage connects to the VHYST pin. The hysteresis of the comparator will be equal to twice the voltage difference that is across the VREFB and VHYST pins. The propagation delay from the comparator inputs to the driver outputs is 250 ns maximum. The maximum hysteresis setting is 60 mv.

low-side driver

The low-side driver is designed to drive low Rds(on) logic-level N-channel MOSFETs. The current rating of the driver is 2 amps typical, source and sink. The bias to the low-side driver is internally connected to the regulated synchronous charge pump output.

detailed description (continued)

high-side driver

The high-side driver is designed to drive low Rds(on) logic-level N-channel MOSFETs. The current rating of the driver is 2 amps typical, source and sink. The high-side driver can be configured either as a floating bootstrap driver or as a ground-reference driver. When configured as a floating driver, the bias voltage to the driver is developed from the charge pump VDRV voltage. The internal synchronous bootstrap rectifier, connected between the VDRV and BOOT pins, is a synchronously-rectified MOSFET for improved drive efficiency. The maximum voltage that can be applied between the BOOT pin and ground is 14 V. The driver can be referenced to ground by connecting BOOTLO to DRVGND, and connecting a voltage ≥ (4.5 V + V_{CC}) to the BOOT pin.

deadtime control

Deadtime control prevents shoot-through current from flowing through the main power FETs during switching transitions by actively controlling the turn-on time of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is below 1 V, and the low-side driver is not allowed to turn on until the voltage at the junction of the 2 FETs (Vphase) is below 2 V.

current sensing

Current sensing is achieved by sampling and holding the voltage across the high-side power FET while the high-side FET is on. The sampling network consists of an internal 60-Ω switch and an external hold capacitor. Internal logic controls the turnon and turnoff of the sample/hold switch such that the switch does not turn on until the Vphase voltage transitions high, and the switch turns off when the input to the high-side driver goes low. Thus sampling will occur only when the high-side FET is conducting current. The voltage on the IOUT pin equals 2 times the sensed high-side voltage.

droop compensation

The droop compensation network reduces the load transient overshoot / undershoot on V_{OUT}, relative to V_{REF} (see *application information* for more details). V_{OUT} is programmed to a voltage greater than V_{REF} by an external resistor divider from V_{OUT} to the VSENSE pin to reduce the undershoot on V_{OUT} during a low to high load transient. The overshoot during a high to low load transient is reduced by subtracting the voltage that is on the DROOP pin from V_{REF}. The voltage on the IOUT pin is divided down with an external resistor divider, and connected to the DROOP pin.

inhibit

INHIBIT is a TTL compatible comparator pin that is used to enable the controller. When INHIBIT is lower than the threshold, the output drivers are low and the slowstart capacitor is discharged. When INHIBIT goes high (above 2.1 V), the short across the slowstart capacitor is released and normal converter operation begins. When another system logic supply is connected to the INHIBIT pin, this pin controls power sequencing by locking out controller operation until the system logic supply exceeds the input threshold voltage of the inhibit circuit; thus the +3.3-V supply and another system logic supply (either +5 V or +12 V) must be above UVLO thresholds before the controller is allowed to start up. Toggling the INHIBIT pin down clears the fault latch.

V_{CC} & VDRV undervoltage lockout

The V_{CC} undervoltage lockout circuit disables the controller while the V_{CC} supply is below the 2.8-V start threshold. The VDRV undervoltage lockout circuit disables the controller while the VDRV supply is below the 4.9 V start threshold during powerup. While the controller is disabled, the output drivers will be low, the LDO drive is off, and the slowstart capacitor will be shorted. When V_{CC} and VDRV exceed the start threshold, the short across the slowstart capacitor is released and normal converter operation begins.

detailed description (continued)

slowstart

The slowstart circuit controls the rate at which VOUT–RR and VOUT–LDO power up (at same time). A capacitor is connected between the SLOWST and ANAGND pins and is charged by an internal current source. The value of the current source is proportional to the reference voltage, so that the charging rate of C_{slowst} is proportional to the ripple regulator reference voltage. The slowstart charging current is determined by the following equation:

$$I_{SLOWSTART} = \frac{I_{VREFB}}{5}$$

Where I_{VREFB} is the current flowing out of the VREFB pin. It is recommended that no additional loads be connected to VREFB, other than the resistor divider for setting the hysteresis voltage. Thus these resistor values will determine the slowstart charging current. The maximum current that can be sourced by the VREFB circuit is 500 µA. The equation for the slowstart time is:

$$T_{SLOWSTART} = 5 \times C_{SLOWSTART} \times R_{VREFB}$$

Where R_{VREFB} is the total external resistance from VREFB to ANAGND.

power good

The power good circuit monitors for an undervoltage condition on VOUT–RR and VOUT–LDO. The powergood (PWRGD) pin is pulled low if either VOUT–RR is 7% below VREF–RR, or VOUT–LDO is 7% below VREF–LDO. PWRGD is an open drain output. The powergood pin is also pulled down, if either V_{CC} or VDRV are below their UVLO thresholds.

overvoltage protection

The overvoltage protection circuit monitors VOUT–RR and VOUT–LDO for an overvoltage condition. If VOUT–RR or VOUT–LDO are 15% above their reference voltage, then a fault latch is set and both output drivers and LDO are turned off. The latch will remain set until the V_{CC} or inhibit voltages go below their undervoltage lockout values. A 1-µs to 5 µs deglitch timer is included for noise immunity.

overcurrent protection

The overcurrent protection circuit monitors the current through the high-side FET. The overcurrent threshold is adjustable with an external resistor divider between IOUT and ANAGND pins, with the divider voltage connected to the OCP pin. If the voltage on the OCP pin exceeds 125 mV, then a fault latch is set and the output drivers are turned off. The latch will remain set until the V_{CC} or inhibit voltages go below their undervoltage lockout values. A 1-µs to 5-µs deglitch timer is included for noise immunity. The OCP circuit is also designed to protect the high-side power FET against a short-to-ground fault on the terminal common to both power FETs.

undervoltage protection

The undervoltage protection circuit monitors VOUT–RR and VOUT–LDO for an undervoltage condition. If VOUT–RR or VOUT–LDO is 15% below their reference voltage, then a fault latch is set and both output drivers and LDO are turned off. The latch will remain set until the V_{CC} or inhibit voltages go below their undervoltage lockout values. A 100-µs to 1-ms deglitch timer is included for noise immunity.

detailed description (continued)

synchronous charge pump

The regulated synchronous charge pump provides drive voltage to the low-side driver at VDRV (5V), and to the high-side driver when the high-side driver is configured as a floating driver. The minimum drive voltage is 4.5V, (typical 5V). The minimum short circuit current is 80 mA. The bootstrap capacitor is used to provide Vdrive for the high-side FET, the power for VLDODRV, and the bias regulator. Instead of diodes, synchronous rectified MOSFETs are used to reduce voltage drop losses and allow a lower input voltage threshold. The charge pump oscillator operates at 300 kHz until the UVLO VDRV is set; after which it is synchronized to the converter switching frequency and is turned on and off to regulate VDRV at 5 V.

The charge pump is designed to operate at a switching frequency of 200 kHz to 400 kHz. Operation at low frequency may require larger capacitors on CPC and VDRV pin. High frequency (> 400 kHz) may not be possible.

power sequence

The VOUT–LDO voltage is powered up with respect to the same slowstart reference voltage as the VOUT–RR. Also, at power down, the VOUT–RR and VOUT–LDO are discharged to ground through P-channel MOSFETs in series with 1-kΩ resistors.

TYPICAL CHARACTERISTICS

QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE

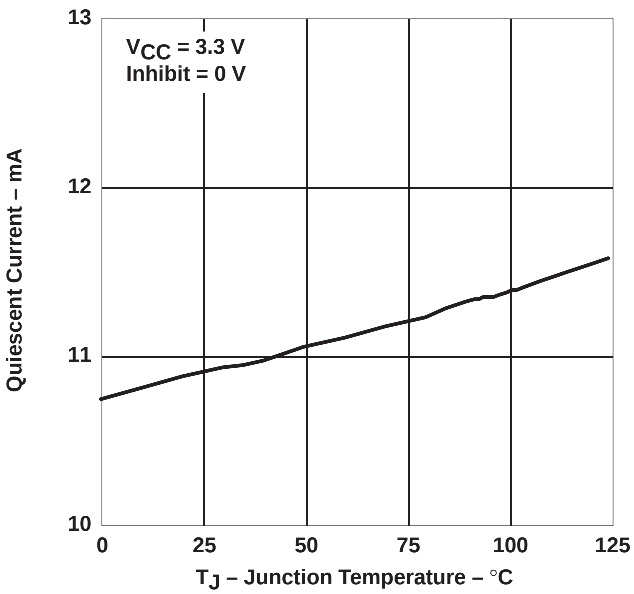


Figure 1

V_{CC} UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

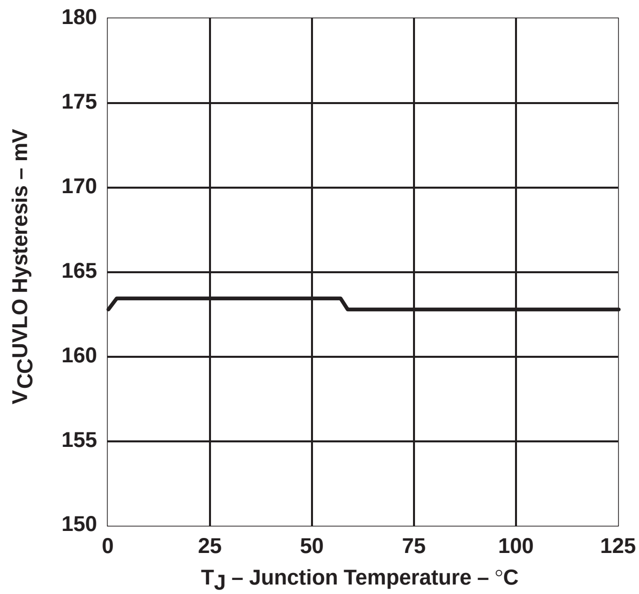


Figure 2

TYPICAL CHARACTERISTICS

V_{CC} UVLO START THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

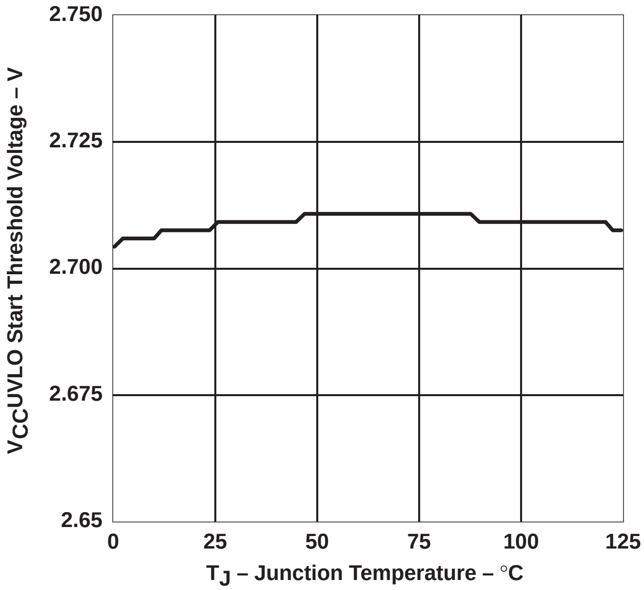


Figure 3

SLOWSTART CHARGE CURRENT vs JUNCTION TEMPERATURE

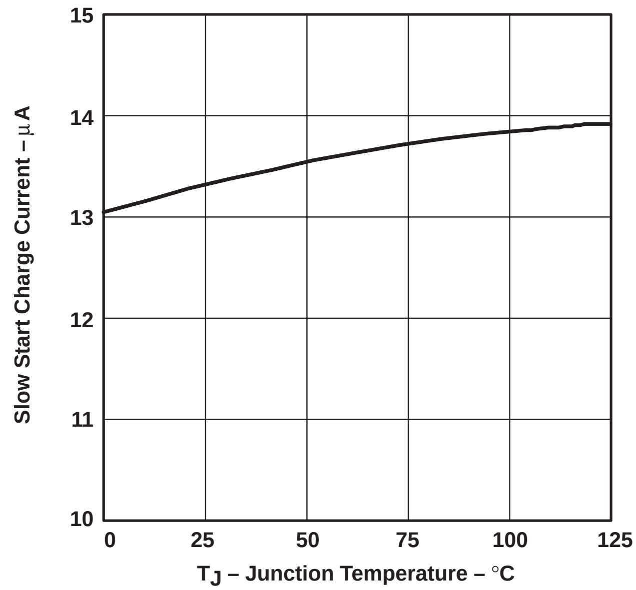


Figure 4

SLOWSTART TIME vs SUPPLY CURRENT (VREFB)

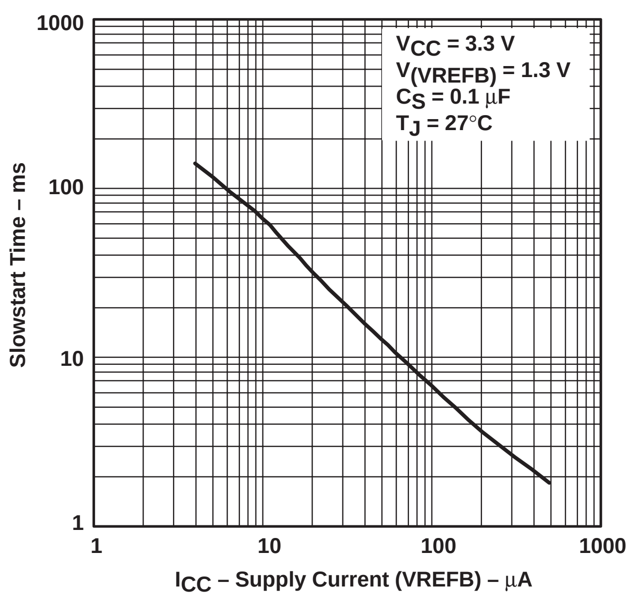


Figure 5

SLOWSTART TIME† vs SLOWSTART CAPACITANCE

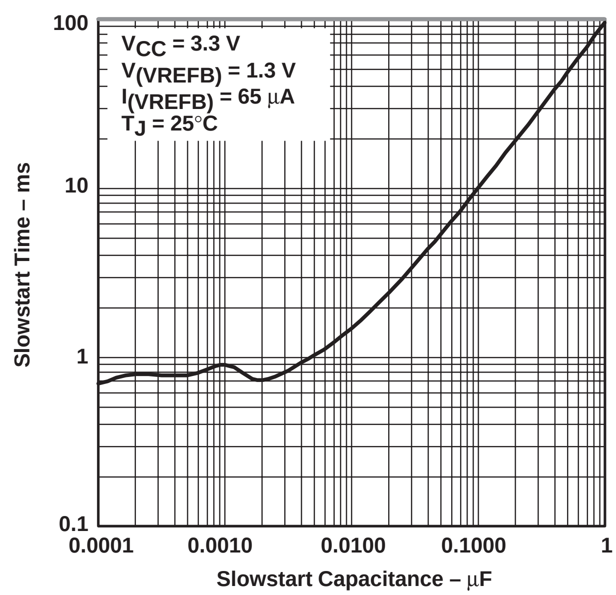


Figure 6

TYPICAL CHARACTERISTICS

DRIVER
RISE TIME
vs
LOAD CAPACITANCE

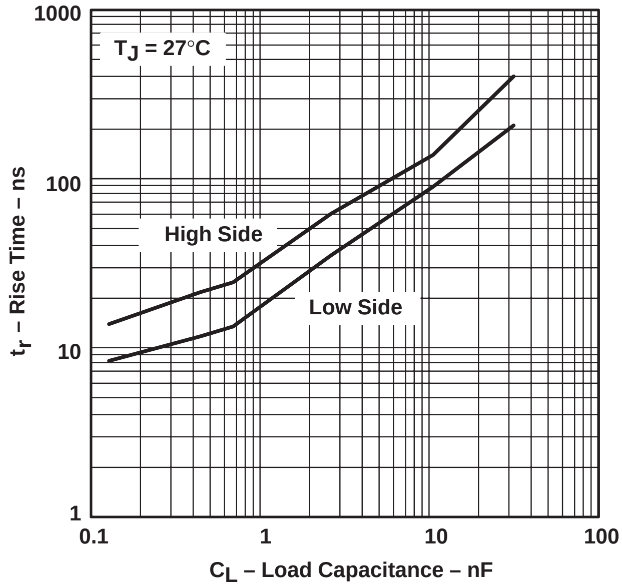


Figure 7

DRIVER
FALL TIME
vs
LOAD CAPACITANCE

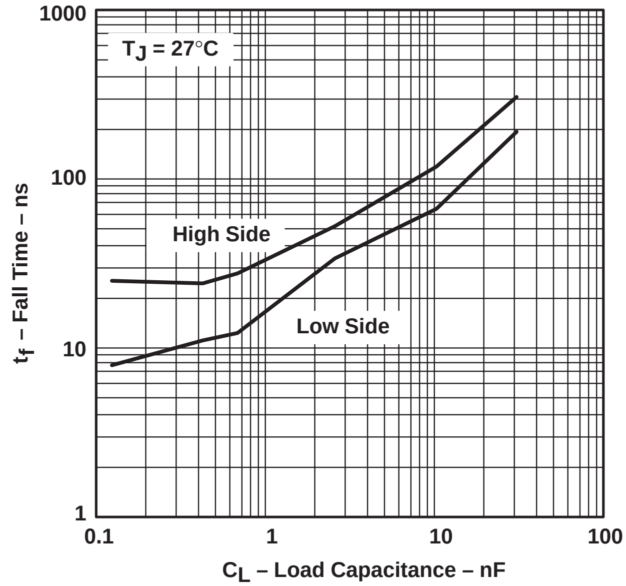


Figure 8

DRIVER
HIGH-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

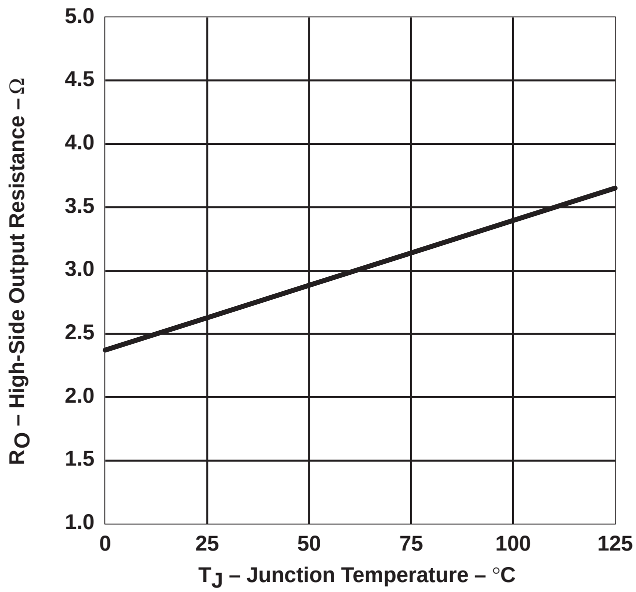


Figure 9

DRIVER
LOW-SIDE OUTPUT RESISTANCE
vs
JUNCTION TEMPERATURE

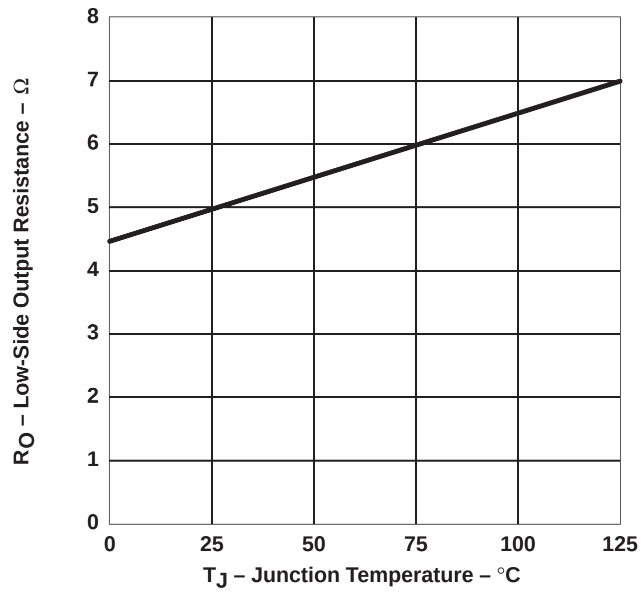


Figure 10

TYPICAL CHARACTERISTICS

DRIVER
INPUT CURRENT
vs
OUTPUT VOLTAGE

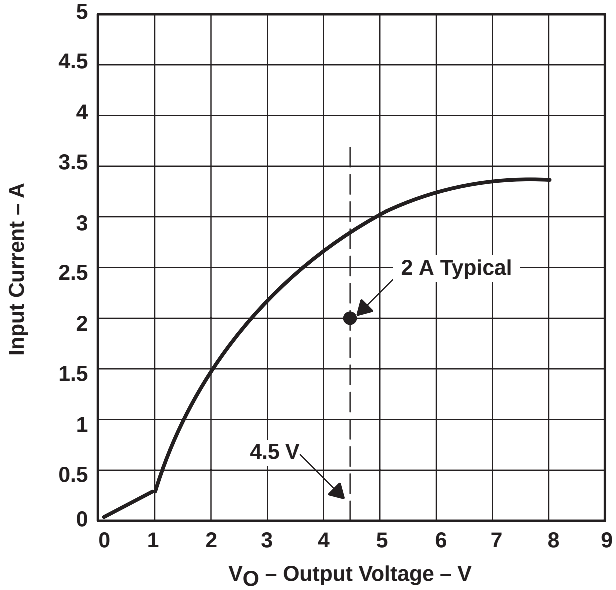


Figure 11

VDRV UVLO START THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

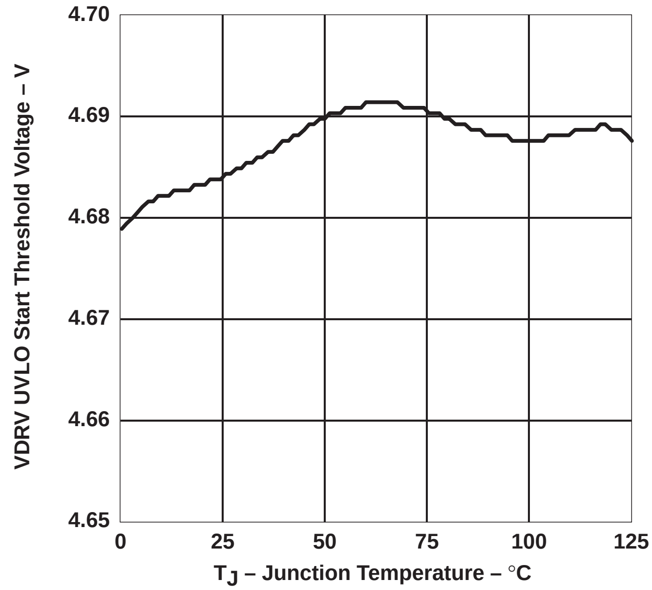


Figure 12

VDRV UVLO HYSTERESIS
vs
JUNCTION TEMPERATURE

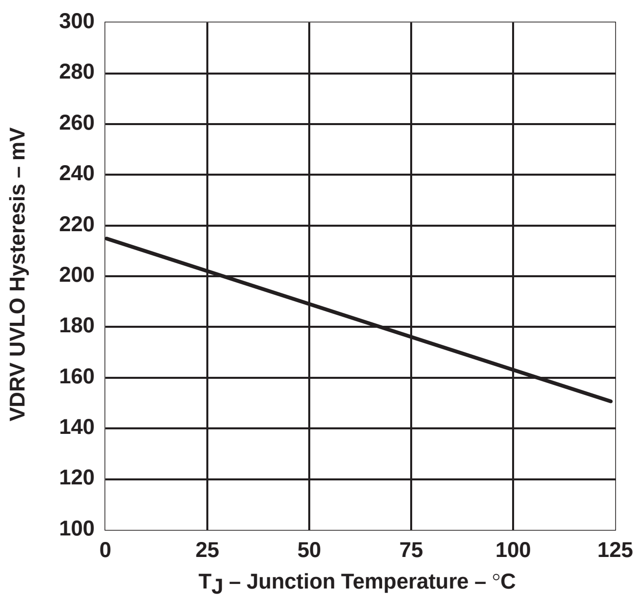


Figure 13

RIPPLE REGULATOR
POWERGOOD THRESHOLD
vs
JUNCTION TEMPERATURE

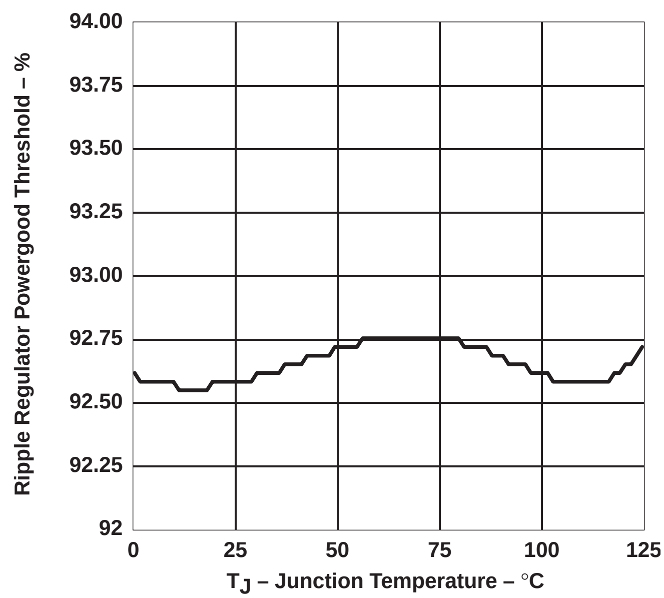


Figure 14

TYPICAL CHARACTERISTICS

INHIBIT START THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

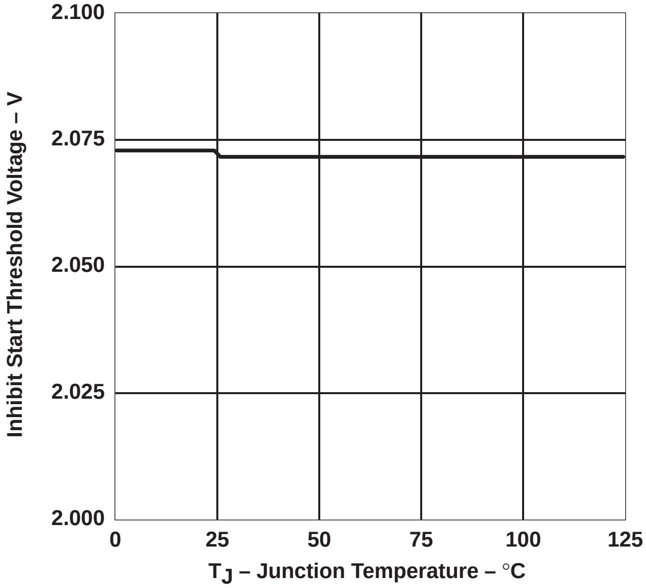


Figure 15

INHIBIT HYSTERESIS VOLTAGE vs JUNCTION TEMPERATURE

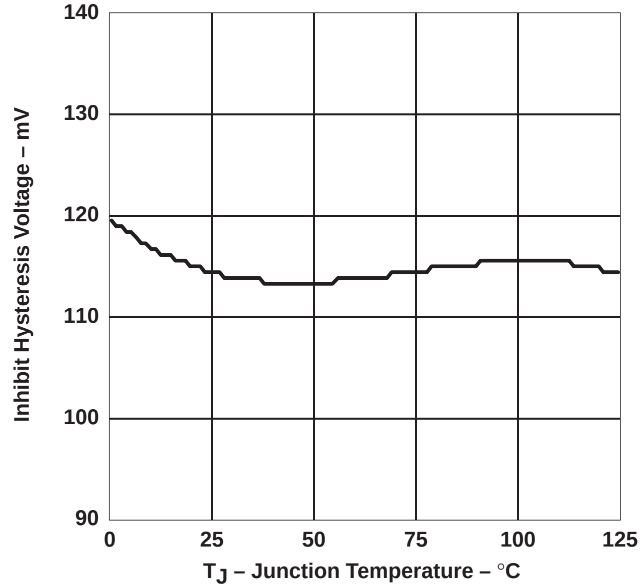


Figure 16

RIPPLE REGULATOR OVP THRESHOLD vs JUNCTION TEMPERATURE

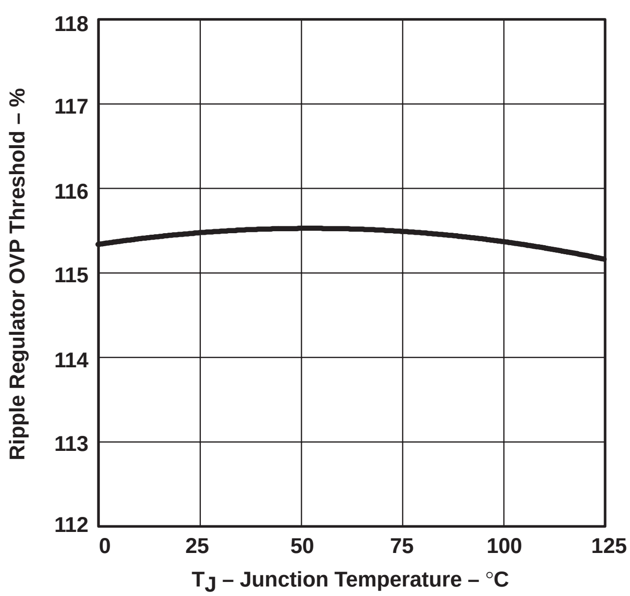


Figure 17

RIPPLE REGULATOR UVP THRESHOLD vs JUNCTION TEMPERATURE

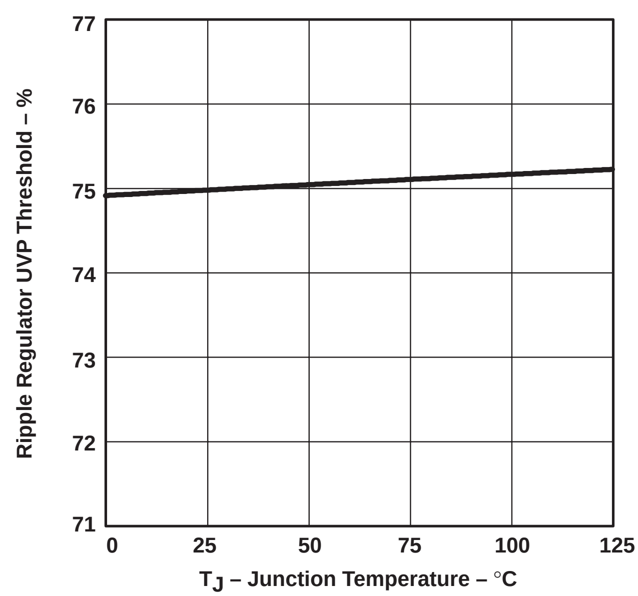


Figure 18

TYPICAL CHARACTERISTICS

OCP THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

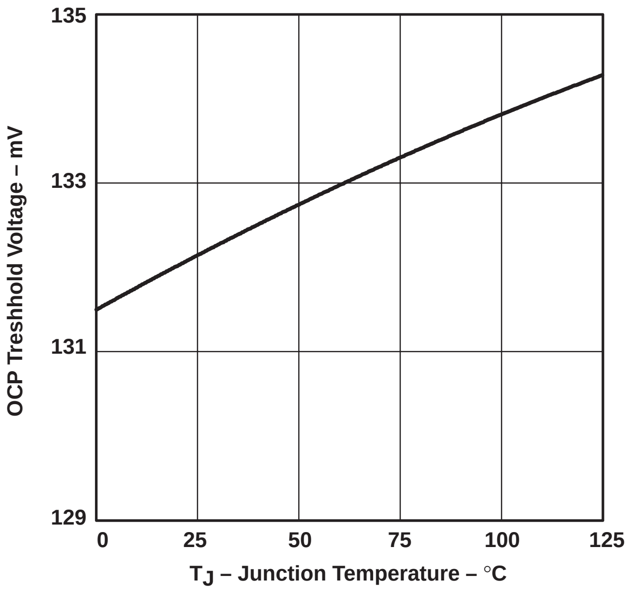


Figure 19

LDO OVP THRESHOLD
vs
JUNCTION TEMPERATURE

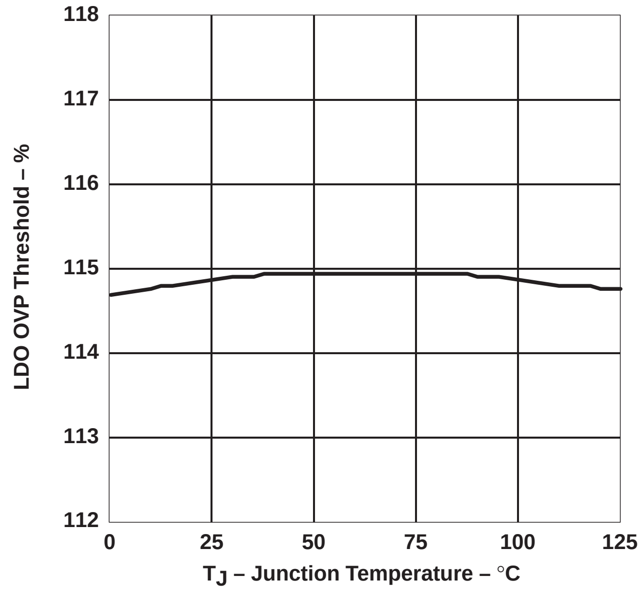


Figure 20

LDO UVP THRESHOLD
vs
JUNCTION TEMPERATURE

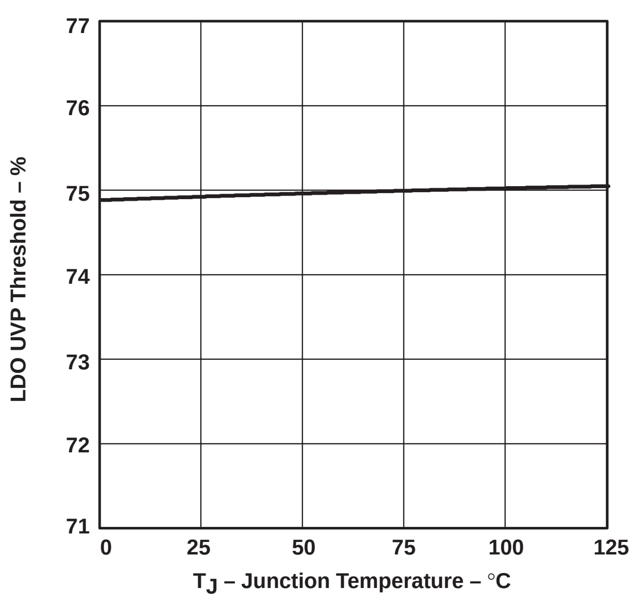


Figure 21

APPLICATION INFORMATION

The design shown in this datasheet is a reference design for a DSP application. An evaluation module (EVM), TPS56300EVM–139 (SLVP139), is available for customer testing and evaluation. The following figure is an application schematic for reference. The circuit can be divided into the power-stage section and the control-circuit section. The power stage must be tailored to the input/output requirements of the application. The control circuit is basically the same for all applications with some minor tweaking of specific values. Table 2 shows the values of the power stage components for various output-current options.

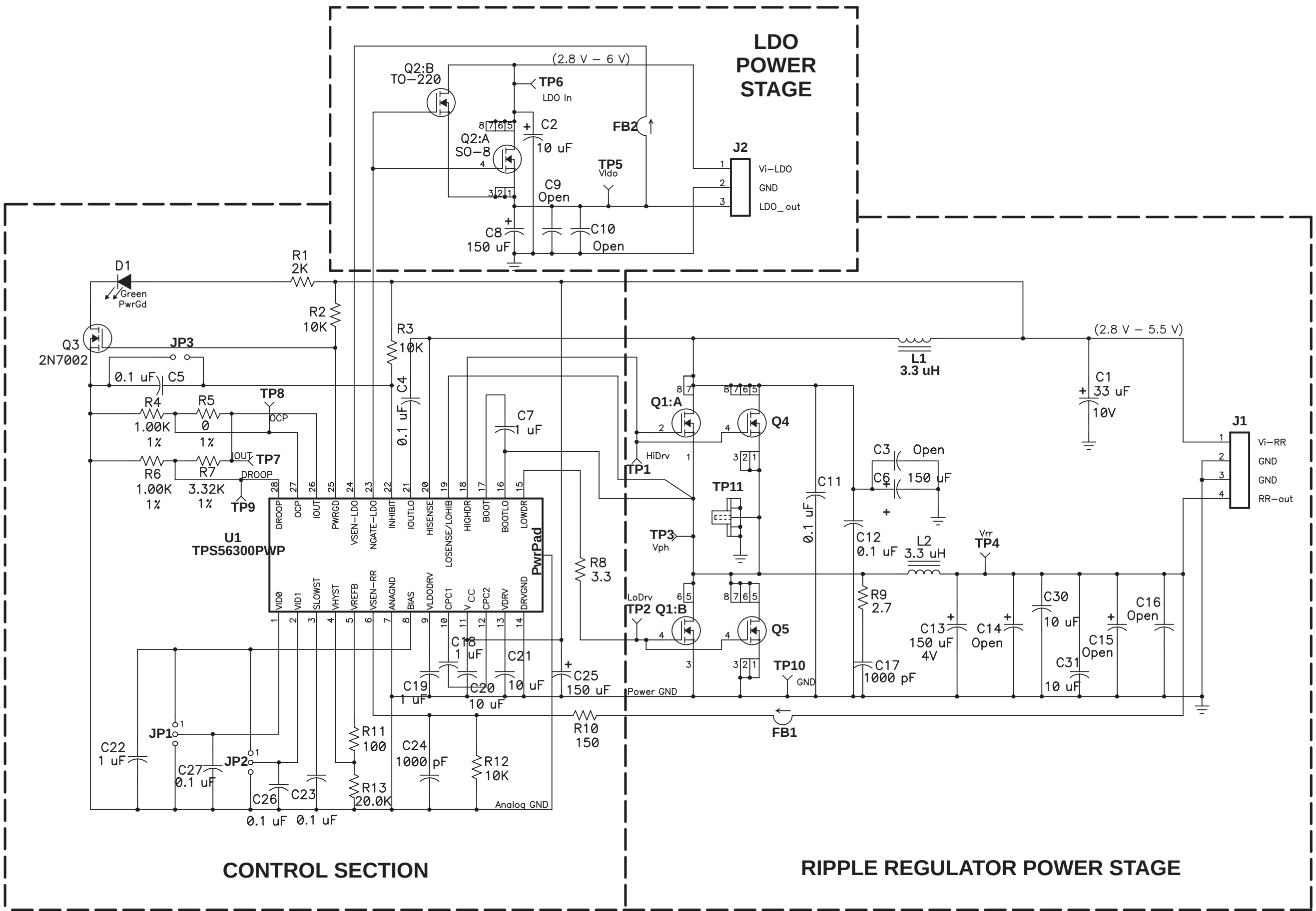


Figure 22. EVM Schematic

Table 2. EVM Input and Outputs

V_{IN}	I_{IN}	V_{RR}	I_{RR}	V_{LDO}	I_{LDO}
5 V	4 A	1.8 V	4 A	3.3 V	0.5 A

APPLICATION INFORMATION

Table 3. Ripple Regulator Power Stage Components

Ripple Regulator Section					
Ref Des	**Function**	**4A (EVM Design)**	**8A**	**12A**	**20A**
C3, C6	Input Bulk Capacitor	C3: open C6: 150 µF (Sanyo, 6TPB150M)	C3: 150 µF C6: 150 µF (Sanyo, 6TPB150M)	C3: 150 µF C6: 150 µF (Sanyo, 6TPB150M)	C3: 150 µF C6: 2x150 µF (Sanyo, 6TPB150M)
C11, C2	Input high–freq Capacitor	C2: 0.1 µF C11: 0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)	C2: 0.1 µF C11: 0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)	C2: 0.1 µF C11: 0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)	C2: 0.33 µF C11: 0.33 µF (muRata GRM39X7R334K016A, 0.33 µF, 16–V, X7R)
C13, C14	Output Bulk Capacitor	C13: 150 µF (Sanyo, 6TPB150M) C14: open	C13: 150 µF (Sanyo, 6TPB150M) C14: open	C13: 150 µF C14: 150 µF (Sanyo, 6TPB150M)	C13: 150 µF C14: 150 µF (Sanyo, 6TPB150M)
C15,C30, C31	Output Mid–freq Capacitor	C15: open C30: 10 µF C31: 10 µF (muRata GRM39X7R106K016A, 10 µF, 16–V, X7R)	C15: open C30: 10 µF C31: 10 µF (muRata GRM39X7R106K016A, 10 µF, 16–V, X7R)	C15: 10 µF C30: 10 µF C31: 10 µF (muRata GRM39X7R106K016A, 10 µF, 16–V, X7R)	C15: 10 µF C30: 10 µF C31: 10 µF (muRata GRM39X7R106K016A, 10 µF, 16–V, X7R)
C16	Output High–freq Capacitor	open	0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)	0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)	0.1 µF (muRata GRM39X7R104K016A, 0.1 µF, 16–V, X7R)
L1	Input filter	3.3 µH Coilcraft DO3316P–332, 5.4 A	3.3 µH Coilcraft DO3316P–332,5.4 A	1.5 µH Coilcraft DO3316P–152,6.4 A	1 µH Coiltronics UP3B–1R0, 12.5–A
L2	Output filter	3.3 µH Coilcraft DO3316P–332, 5.4 A	3.3 µH Coilcraft DO5022P–332HC, 10 A	1.5 µH Coilcraft DO5022P–152HC, 15 A	3.3 µH Micrometals, T68–8/90 Core w/7T, #16, 25 A
R8	Low Side Gate Resistor	10 Ω	10 Ω	5.1 Ω	5.1 Ω
Q1A,Q4	Power Switch	Q1A: Dual FET IRF7311	Q4: IRF7811	Q4: 2xIRF7811	Q4: 2xIRF7811
Q1B,Q5	Synchronous Switch	Q1B: Dual FET IRF7311	Q5: IRF7811	Q5: 2xIRF7811	Q5: 2xIRF7811

The values listed in Table 3 are recommendations based on actual test circuits. Many variations of the above are possible based upon the desires and/or requirements of the user. Performance of the circuit is equally, if not more, dependent upon the layout than on the specific components, as long as the device parameters are not exceeded. Fast-response, low-noise circuits require circuits require critical attention to the layout details.

APPLICATION INFORMATION

Table 4. LDO Power Stage Components

LDO Section				
Ref. Des	Part	V_{IN}	V_{OUT}	Description
Q2:A	IRF7811(EVM) or Si4410, IRF7413 FDS6680	V_{IN}	$V_{IN}– V_{DROPOUT}$†	Used as a power distribution switch for LDO output control
Q2:A	IRF9410, Si9410			Low cost solution for low LDO output current $(V_{IN}–V_{OUT})*I_{OUT} < 1$ W
Q2:A	IRF7811			Higher current and still surface mount $1 \text{ W} < (V_{IN}–V_{OUT})*I_{OUT}) < 2$ W
Q2: B	IRLZ24N			High output current requiring heat sink. Low cost but through–hole package. $(V_{IN}–V_{OUT})*I_{OUT} > 2$ W

† $V_{DROPOUT} = I_{OUT} \times$ Rdson. It should be as small as possible.

frequency calculation

With hysteretic control, the switching frequency is a function of the input voltage, the output voltage, the hysteresis window, the delay of the hysteresis comparator and the driver, the output inductance, the resistance in the output inductor, the output capacitance, the ESR and ESL in the output capacitor, the output current, and the turnon resistance of high-side and low-side MOSFET. It is a very complex equation if everything is included. To make it more useful to designers, a simplified equation is developed that considers only the most influential factors. The tolerance of the result for this equation is about 30%:

$$f_S = \frac{V_{OUT} \times \left(V_{IN} - V_{OUT}\right) \times \left[\dfrac{ESR - \left(250 \times 10^{-9} + T_d\right)}{C_{out}}\right]}{V_{IN} \times \left(V_{IN} \times ESR \times \left(250 \times 10^{-9} + T_d\right) + V_{hys} \times L_{OUT} - ESL \times V_{IN}\right)}$$

Where fs is the switching frequency (Hz); V_{OUT} is the output voltage (V); V_{IN} is the input voltage (V); C_{OUT} is the output capacitance; ESR is the equivalent series resistance in the output capacitor (Ω); ESL is the equivalent series inductance in the output capacitor (H); L_{OUT} is the output inductance (H); Td is output feedback RC filter time constant (S); Vhys is the hysteresis window (V).

hysteresis window

The changeable hysteresis window in TPS56300 is used for switching frequency and output voltage ripple adjustment. The hysteresis window setup is decided by a two-resistor voltage divider on VREFB and VHYST pin. Two times of the voltage drop on the top resistor is the hysteresis window. The formula is shown in the following:

$$\text{Vhyswindow} = 2 \times \text{VREFB} \times \left(1 - \frac{R13}{R11 + R13}\right)$$

Where Vhyswindow is the hysteresis window (V); VREFB is the regulated voltage from VREVB (pin 5); R11 is the top resistor in the voltage divider; R13 is the bottom resistor in the voltage divider. The maximum hysteresis window is 60 mV.

APPLICATION INFORMATION

slowstart

Slowstart reduces the start-up stresses on the power-stage components and reduces the input current surge. The minimum slowstart time is limited to 1 ms due to the power good function deglitch time. Slowstart timing is dependent of the timing capacitor value on the slowstart pin. The following formula can be used for setting the slowstart timing:

$$T_{SLOWSTART} = 5 \times C_{SLOWSTART} \times R_{VREFB}$$

$T_{SLOWSTART}$ is the slowstart time; $C_{SLOWSTART}$ is the capacitor value on SLOWST (pin 3). R_{VREFB} is the total resistance on VREFB (pin 5).

current limit

Current limit can be implemented using the on-resistance of the upper FETs as the sensing elements. The IOUT signal is used for the current limit and the droop function. The voltage at IOUT at the output current trip point will be:

$$V_{IOUT} = R_{ON} \times I_O \times 2$$

R_{ON} is the high-side on-time resistance; I_O is the output current. The current limit is calculated by using the formula:

$$R5 = \frac{R4 \times \left(I_{O(MAX)} \times 2 \times R_{ON} - 0.125\right)}{0.125}$$

Where R4 is the bottom resistor in the voltage divider on OCP pin, and R5 is the top resistor; $I_{O(MAX)}$ is the maximum current allowed; R_{ON} is the high-side FET on-time resistance.

Since the FET on-time resistance varies according to temperature, the current limit is basically for catastrophic failure.

droop compensation

Droop compensation with the offset resistor divider from V_{OUT} to the VSENSE is used to keep the output voltage in range during load transients by increasing the output voltage setpoint toward the upper tolerance limit during light loads and decreasing the voltage setpoint toward the lower tolerance limit during heavy loads. This allows the output voltage to swing a greater amount and still remain within the tolerance window. The maximum droop voltage is set with R6 and R7:

$$V_{DROOP(max)} = V_{IOUT(max)} \times \frac{R6}{R6 + R7}$$

Where $V_{DROOP(max)}$ is the maximum droop voltage; $V_{IOUT(max)}$ is the maximum VIOUT that reflects the maximum output current (full load); R6 is the bottom resistor of the divider connected to the DROOP pin, R7 is the top resistor.

The offset voltage is set to be half of the maximum droop voltage higher than the nominal output voltage, so the whole droop voltage range is symmetrical to the nominal output voltage. The formula for setting the offset voltage is:

APPLICATION INFORMATION

$$V_{OFFSET} = \frac{1}{2} \times V_{DROOP(max)} = V_O \times \left(\frac{R12}{R10 + R12}\right)$$

Where V_{OFFSET} is the desired offset voltage; $V_{DROOP(max)}$ is the droop voltage at full load; Vo is the nominal output voltage; R10 is the top resistor of the offset resistor divider, and R12 is the bottom one.

Therefore, with the setup above, at light load, the output voltage is:

$$V_{O(NO\ LOAD)} = V_{O(nom)} + V_{OFFSET} = V_{O(nom)} + \frac{1}{2} \times V_{DROOP}$$

And, at full load, the output voltage is:

$$V_{O(FULL\ LOAD)} = V_{O(nom)} - V_{OFFSET} = V_{O(nom)} - \frac{1}{2} \times V_{DROOP}$$

output inductor ripple current

The output inductor current ripple can affect not only the efficiency, but also the output voltage ripple. The equation for calculating the inductor current ripple is exhibited in the following:

$$I_{ripple} = \frac{V_{IN} - V_{OUT} - I_{out} \times \left(Rdson + R_L\right)}{L_{OUT}} \times D \times Ts$$

Where I_{ripple} is the peak-to-peak ripple current (A) through the inductor; V_{IN} is the input voltage (V); V_{OUT} is the output voltage (V); I_{OUT} is the output current; Rdson is the on-time resistance of MOSFET (Ω); R_L is the output inductor equivalent series resistance; D is the duty cycle; and Ts is the switch cycle (S). From the equation, it can be seen that the current ripple can be adjusted by changing the output inductor value.

Example:

V_{IN} = 5 V; V_{OUT} = 1.8 V; I_{OUT} = 5 A; Rdson = 10 mΩ; R_L = 5 mΩ; D = 0.36; Ts = 5 µs; L_{OUT} = 6 µH

Then, the ripple I_{ripple} = 1 A.

output capacitor RMS current

Assuming the inductor ripple current totally goes through the output capacitor to the ground, the RMS current in the output capacitor can be calculated as:

$$I_{O(rms)} = \frac{\Delta I}{\sqrt{12}}$$

Where $I_{O(rms)}$ is the maximum RMS current in the output capacitor (A); ΔI is the peak-to-peak inductor ripple current (A).

Example:

ΔI = 1 A, so $I_{O(rms)}$ = 0.29 A

input capacitor RMS current

The input capacitor RMS current is important for input capacitor design. Assuming the input ripple current totally goes into the input capacitor to the power ground, the RMS current in the input capacitor can be calculated as:

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$$I_{I(rms)} = \sqrt{I_O{}^2 \times D \times (1 - D) + \frac{1}{12} \times D \times I_{ripple}{}^2}$$

Where $I_{I(rms)}$ is the input RMS current in the input capacitor (A); I_O is the output current (A); Iripple is the peak-to-peak output inductor ripple current; D is the duty cycle. From the equation, it can be seen that the highest input RMS current usually occurs at the lowest input voltage, so it is the worst case design for input capacitor ripple current.

Example:

I_O = 5 A; D = 0.36; I_{ripple} = 1 A,
Then, $I_{I(rms)}$ = 2.46 A

layout and component value consideration

Good power supply results will only occur when care is given to proper design and layout. Layout and component value will affect noise pickup and generation and can cause a good design to perform with less than expected results. With a range of current from milliamps to tens or even hundreds of amps, good power supply layout and component selection, especially for a fast ripple controller, is much more difficult than most general PCB design. The general design should proceed from the switching node to the output, then back to the driver section, and, finally, to placing the low-level components. In the following list are several specific points to consider before layout and component selection for TPS56300:

1. All sensitive analog components should be referenced to ANAGND. These include components connected to SLOWST, DROOP, IOUT, OCP, VSENSE, VREFB, VHYST, BIAS, and LOSENSE/LOHIB.
2. The input voltage range for TPS56300 is low from 2.8-V to 5.5-V, so it has a voltage tripler (charge pump) inside to deliver proper voltage for internal circuitry. To avoid any possible noise coupling, a low ESR capacitor on V_{CC} is recommended.
3. For the same reason in Item 2, the ANAGND and DRVGND should be connected as close as possible to the IC.
4. The bypass capacitor should be placed close to the TPS56300.
5. When configuring the high-side driver as a boot-strap driver, the connection from BOOTLO to the power FETs should be as short and as wide as possible. LOSENSE/LOHIB should have a separate connection to the FETs since BOOTLO will have large peak current flowing through it.
6. The bulk storage capacitors across V_{IN} should be placed close to the power FETs. High-frequency bypass capacitors should be placed in parallel with the bulk capacitors and connected close to the drain of the high-side FET and to the source of the low-side FET.
7. HISENSE and LOSENSE should be connected very close to the drain and source, respectively, of the high-side FET. HISENSE and LOSENSE should be routed very close to each other to minimize differential-mode noise coupling to these traces. Ceramic decoupling capacitors should be placed close to where HISENSE connects to V_{IN}, to reduce high-frequency noise coupling on HISENSE.

The EVM board (SLVP-139) is used in the test. The test results are shown in the following.

APPLICATION INFORMATION

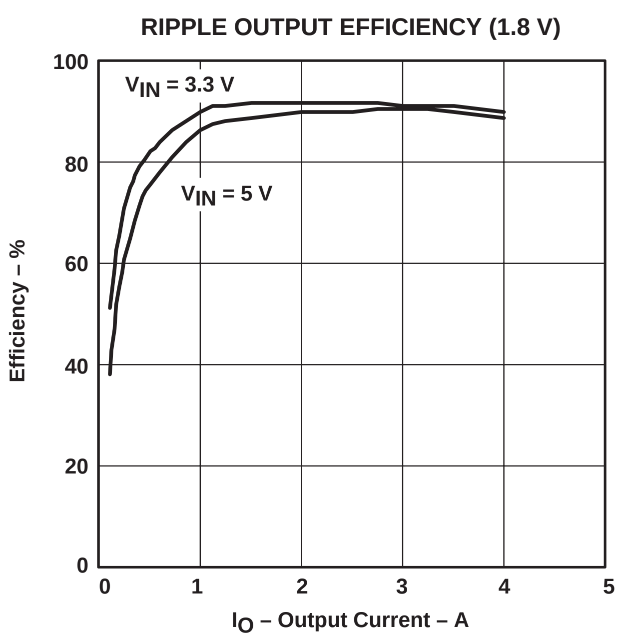


Figure 23

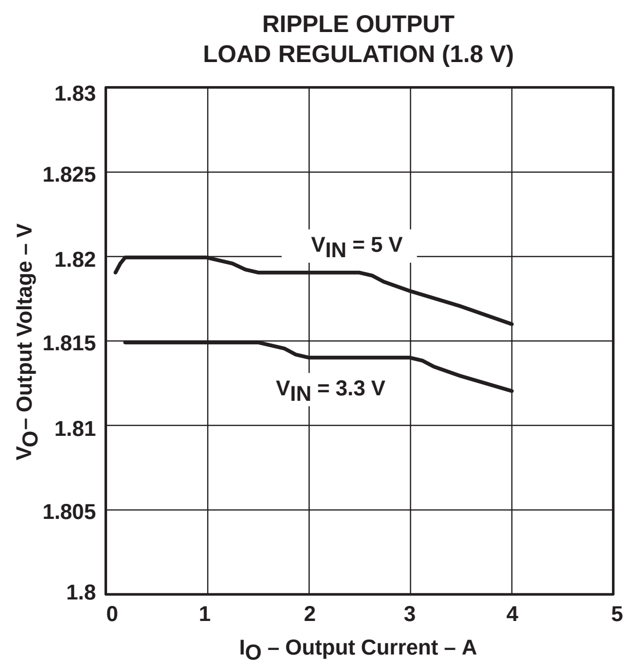


Figure 24

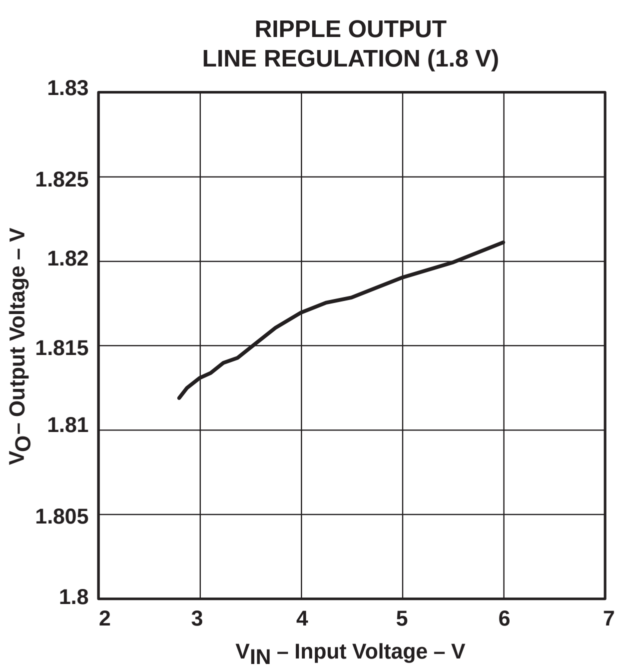


Figure 25

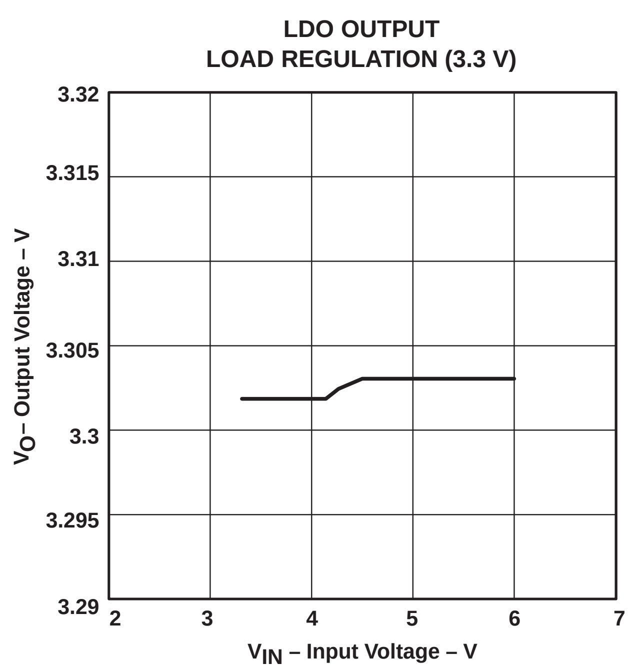


Figure 26

APPLICATION INFORMATION

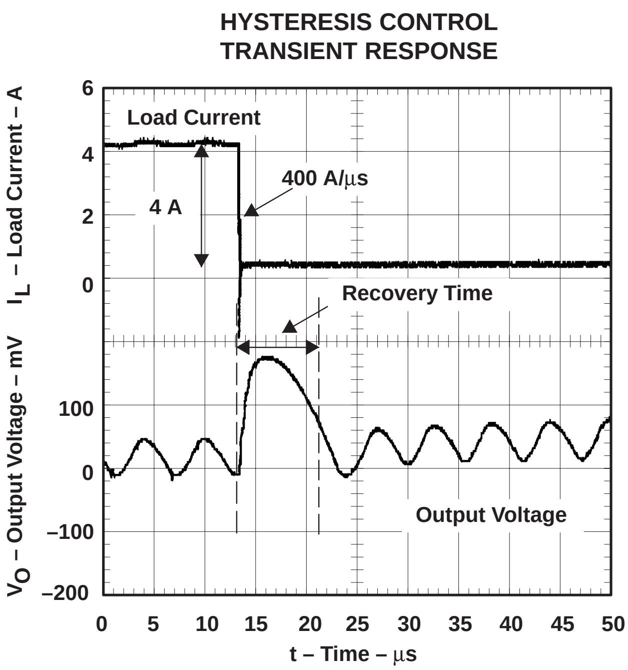


Figure 27

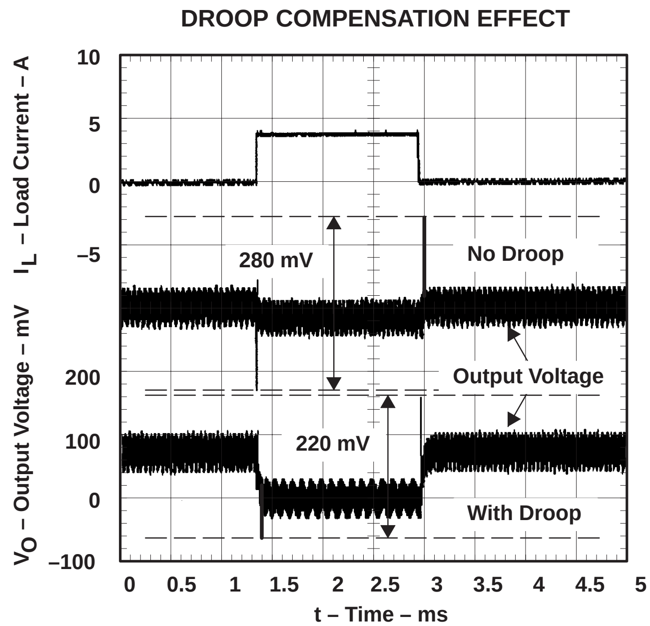


Figure 28

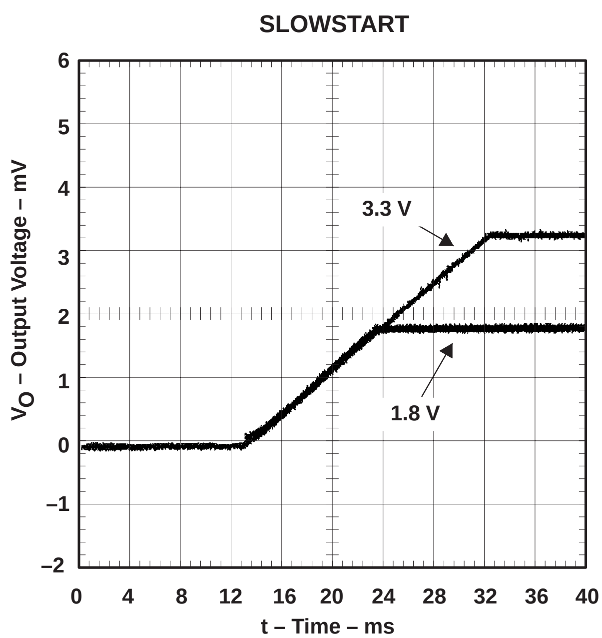


Figure 29

APPLICATION INFORMATION

layouts

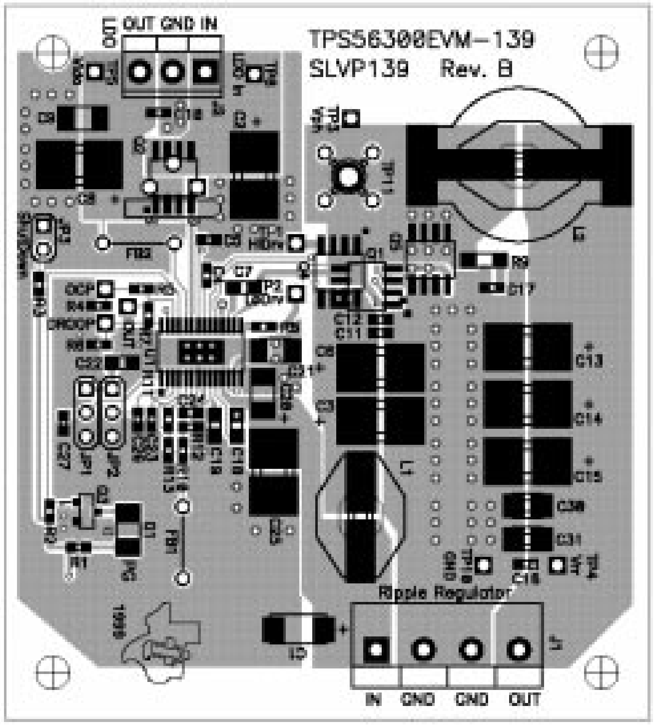


Figure 30. Top Layer

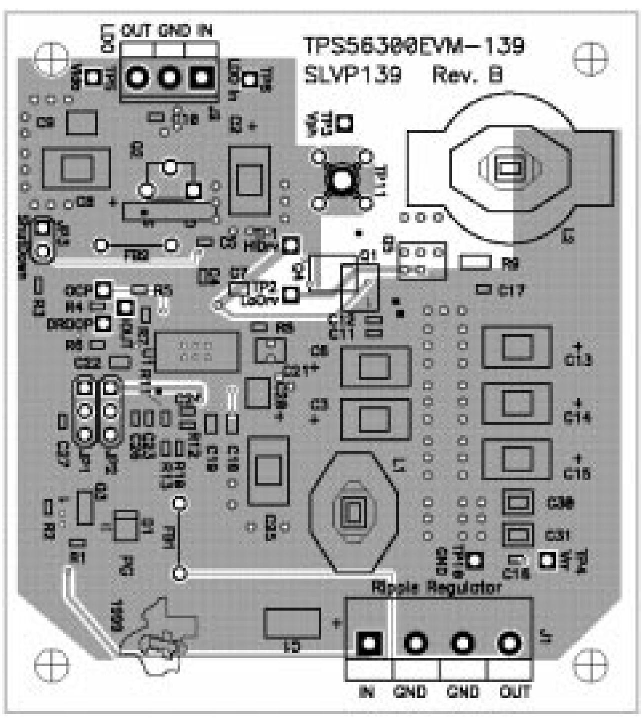


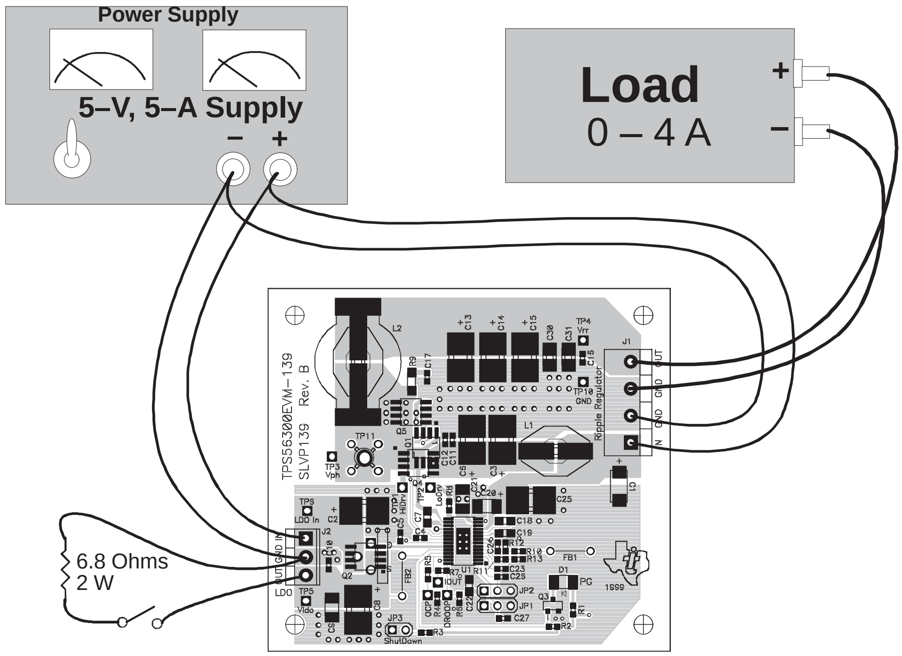
Figure 31. Bottom Layer (Top View)

APPLICATION INFORMATION

bill of materials

REF	PN	Description	MFG	Size
C1	10TPA33M	Capacitor, POSCAP, 33 µF, 10 V	Sanyo	C
C2, C20, C21, C30, C31	Std	Capacitor, Ceramic, 10 µF, 16 V	Sanyo	1210
C3. C6, C8, C13, C25	6TPB150M	Capacitor, POSCAP, 150 µF, 6 V	Sanyo	D
C4, C5, C11, C12, C23, C26, C27,	Std	Capacitor, Ceramic, 0.1 µF, 16 V	Sanyo	603
C7, C22	Std	Capacitor, Ceramic, 1 µF, 16 V	Sanyo	805
C9	Std	Open		1210
C10, C16	Std	Open		603
C14, C15	Std	Open		D
C17, C24	Std	Capacitor, Ceramic, 1000 pF, 16 V	Sanyo	603
C18, C19	Std	Capacitor, Ceramic, 1 µF, 16 V	Sanyo	805
D1	SML-LX2832G	Diode, LED, Green, 2.1 V SM	Lumwx	1210
L1, L2	DO3316P-332	Inductor, 3.3 µH, 5.4 A	Coilcraft	0.5 × 0.37 in
J1	ED2227	Terminal Block, 4-pin, 15 A, 5.08 mm	OST	5.08 mm
J2	ED1515	Terminal Block, 3-pin, 6 A, 3.5 mm	OST	n, 6 A,
JP1, JP2	S1132-3-ND	Header, Right straight, 3-pin, 0.1 ctrs, 0.3” pins	Sullins	#S1132-3-ND
JP1shunt	929950-00-ND	Shunt jumper, 0.1” (for JP1)	3M	0.1”
J3	S1132-2-ND	Header, Right straight, 2-pin, 0.1 ctrs, 0.3” pins	Sullins	#S1132-2-ND
Q1		Open		SO-8
Q2:A, Q4, Q5	IRF7811	MOSFET, N-ch, 30 V, 10 mΩ		SO-8
Q2:B		Open		?
Q3	2N7002DICT-N	MOSFET, N-ch, 115 mA, 1.2 Ω	Diodes, Inc.	TO-236
R3	std	Resistor, 10 kohms, 5 %		603
R4	std	Resistor, 1 kohms, 1%		603
R5	std	Resistor, 0 ohms, 1%		603
R6	std	Resistor, 1 kohms, 1%		603
R7	std	Resistor, 3.32 kohms, 1%		603
R8	std	Resistor, 10 ohms, 5 %		603
R9	std	Resistor, 2.7 ohms, 5 %		1206
R10	std	Resistor, 150 ohms, 5 %		603
R11	std	Resistor, 100 ohms, 1 %		603
R12	std	Resistor, 10 kohms, 5 %		603
R13	std	Resistor, 20.0 kohms, 1 %		603
TP1–TP10	240–345	Test Point, Red	Farnell	
TP11	131–4244–00	Adaptor, 3.5-mm probe clip (or 131–5031–00)	Tektronix	
U1	TPS56300PWP	Dual controller		TSSOP–28pin

APPLICATION INFORMATION



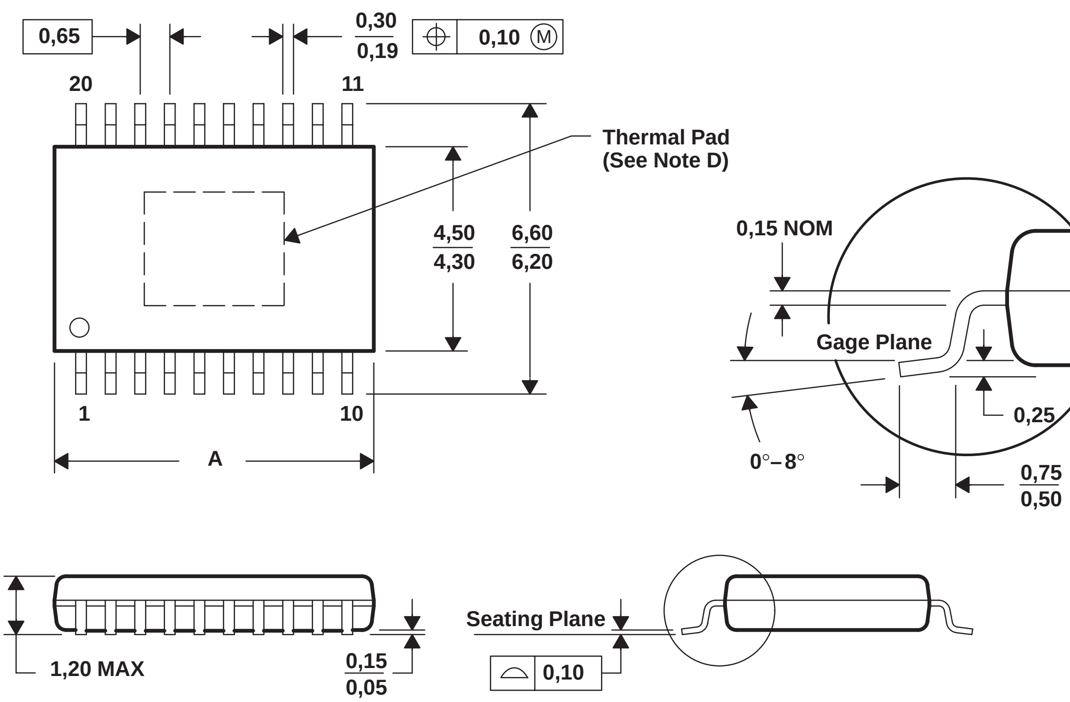
Note: All wire pairs should be twisted.

Figure 32. Test Setup

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES: B. All linear dimensions are in millimeters.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusions.
E. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
F. Falls within JEDEC MO-153

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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