A5970AD

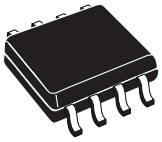
Up to 1 A switch step down switching regulator for automotive applications

Features

- Qualified following the AEC-Q100 requirements (temperature grade 3), see PPAP for more details.
- 1 A DC output current
- Operating input voltage from 4 V to 36 V
- 3.3 V / (±2 %) reference voltage
- Output voltage adjustable from 1.235 V to 35 V
- Low dropout operation: 100 % duty cycle
- 500 kHz internally fixed frequency
- Voltage feedforward
- Zero load current operation
- Internal current limiting
- Inhibit for zero current consumption
- Synchronization
- Protection against feedback disconnection
- Thermal shutdown

Applications

- Dedicated to automotive applications



SO-8

Description

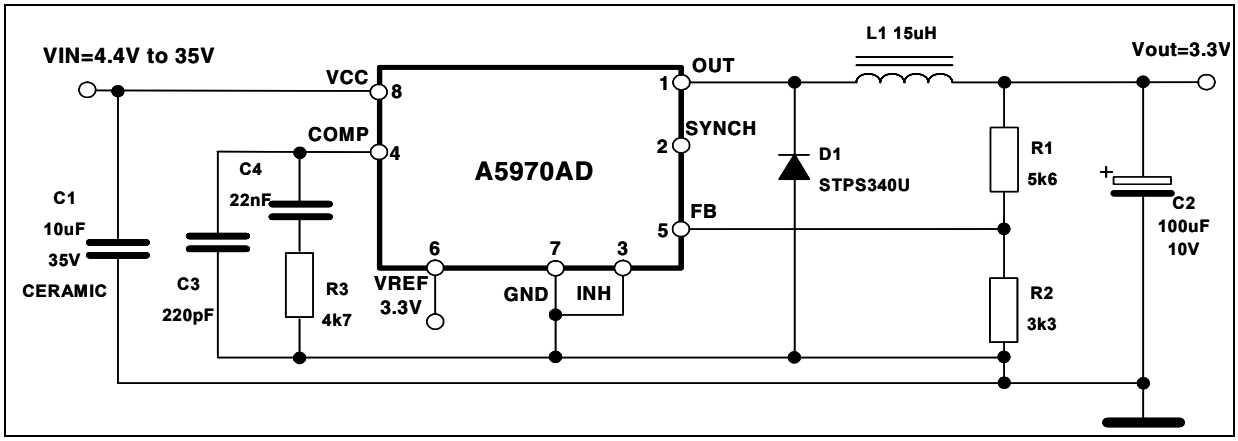
The A5970AD is a step down monolithic power switching regulator with a switch current limit of 1.35 A so it is able to deliver more than 1 A DC current to the load depending on the application conditions.

The output voltage can be set from 1.235 V to 35 V. The device uses an internal P-channel D-MOS transistor (with a typical $R_{DS(on)}$ of 250 mΩ) as switching element to avoid the use of bootstrap capacitor and guarantee high efficiency.

An internal oscillator fixes the switching frequency at 500 kHz to minimize the size of external components. Having a minimum input voltage of 4 V only, it is particularly suitable for 5 V bus, available in all computer related applications.

Pulse by pulse current limit with the internal frequency modulation offers an effective constant current short circuit protection.

Figure 1. Application schematic

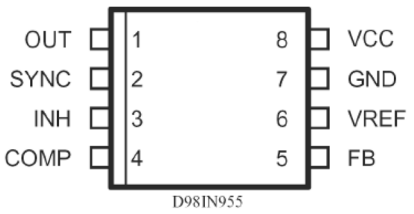


Contents

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Pin	Description
1	OUT	Regulator output.
2	SYNCH	Master/slave synchronization. When it is open, a signal synchronous with the turn-off of the internal power is present at the pin. When connected to an external signal at a frequency higher than the internal one, then the device is synchronized by the external signal. Connecting together the SYNC pin of two devices, the one with the higher frequency works as master and the other one, works as slave.
3	INH	A logical signal (active high) disables the device. With IHN higher than 2.2 V the device is OFF and with INH lower than 0.8 V, the device is ON. If INH is not used the pin must be grounded. When it is open, an internal pull-up disables the device.
4	COMP	E/A output for frequency compensation.
5	FB	Feedback input. Connecting directly to this pin results in an output voltage of 1.235 V. An external resistive divider is required for higher output voltages (the typical value for the resistor connected between this pin and ground is 4.7 k).
6	VREF	3.3 V V_{REF}. No cap is requested for stability.
7	GND	Ground.
8	V_{CC}	Unregulated DC input voltage.

2 Electrical data

2.1 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_8	Input voltage	40	V
V_1	OUT pin DC voltage OUT pin peak voltage at $\Delta t = 0.1\mu s$	-1 to 40 -5 to 40	V V
I_1	Maximum output current	int. limit.	
V_4, V_5	Analog pins	4	V
V_3	INH	-0.3 to V_{CC}	V
V_2	SYNCH	-0.3 to 4	V
P_{TOT}	Power dissipation at $T_A \leq 70$ °C	0.75	W
T_J	Operating junction temperature range	-40 to 150	°C
T_{STG}	Storage temperature range	-55 to 150	°C

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	SO8	Unit
R_{thJA}	Maximum thermal resistance junction-ambient	120 (1)	°C/W

1. Package mounted on board

3 Electrical characteristics

Table 4. Electrical characteristics
(T_J = -40 °C to 125 °C, V_{CC} = 12 V, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{CC}	Operating input voltage range		4		36	V
$R_{DS(on)}$	MOSFET on resistance			0.250	0.5	Ω
I_L	Maximum limiting current (1)	V_{CC} = 5 V	1.35	1.8		A
		V_{CC} = 5 V, T_J = 25 °C	1.5	1.8		
f_{SW}	Switching frequency		430	500	570	kHz
	Duty cycle		0		100	%
Dynamic characteristics (see test circuit).						
V_5	Voltage feedback	4.4 V < V_{CC} < 36 V	1.220	1.235	1.25	V
η	Efficiency	V_0 = 5 V, V_{CC} = 12 V		90		%
DC characteristics						
I_{qop}	Total operating quiescent current			5	7	mA
I_q	Quiescent current	Duty cycle = 0; V_{FB} = 1.5 V			2.7	mA
I_{qst-by}	Total stand-by quiescent current	V_{inh} > 2.2 V		50	100	µA
Inhibit						
	INH threshold voltage	Device ON			0.8	V
		Device OFF	2.2			V
Error amplifier						
V_{OH}	High level output voltage	V_{FB} = 1 V	3.5			V
V_{OL}	Low level output voltage	V_{FB} = 1.5 V			0.4	V
$I_{o\ source}$	Source output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	190	300		µA
$I_{o\ sink}$	Sink output current	V_{COMP} = 1.9 V; V_{FB} = 1 V	1	1.5		mA
I_b	Source bias current			2.5	4	µA
	DC open loop gain	R_L=∞	50	57		dB
gm	Transconductance	I_{COMP} = -0.1 mA to 0.1 mA; V_{COMP} = 1.9 V		2.3		mS

Table 4. Electrical characteristics (continued)
(T_J = -40 °C to 125 °C, V_{CC} = 12 V, unless otherwise specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Synch function						
	High input voltage	V_{CC} = 4.4 to 36 V;	2.5		V_{REF}	V
	Low input voltage	V_{CC} = 4.4 to 36 V;			0.74	V
	Slave synch current	V_{synch} = 0.74 V (2) V_{synch} = 2.33 V	0.11 0.21		0.25 0.45	mA
	Master output amplitude	I_{source}= 3 mA	2.75	3		V
	Output pulse width	No load, V_{synch}= 1.65 V	0.20	0.35		µs
Reference section						
	Reference voltage		3.234	3.3	3.366	V
		I_{REF} = 0 to 5 mA V_{CC} = 4.4 V to 36 V	3.2	3.3	3.399	V
	Line regulation	I_{REF} = 0 mA V_{CC} = 4.4 V to 36 V		5	10	mV
	Load regulation	I_{REF} = 0 mA		8	15	mV
	Short circuit current		5	18	30	mA

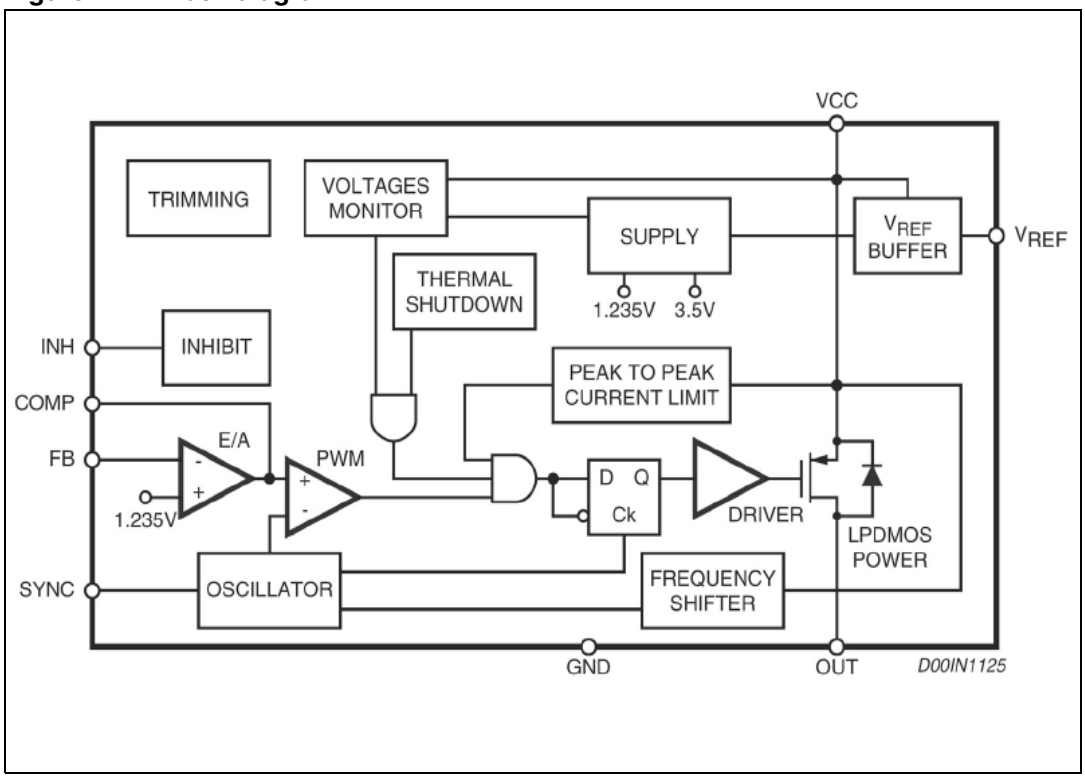
1. With T_J = 85 °C, I_{lim_min} = 1.5 A, assured by design, characterization and statistical correlation.
2. Guaranteed by design.

4 Functional description

The main internal blocks are shown in *Figure 2*, where is reported the device block diagram. They are:

- A voltage regulator that supplies the internal circuitry. From this regulator, a 3.3 V reference voltage is externally available.
- A voltage monitor circuit that checks the input and internal voltages.
- A fully integrated sawtooth oscillator whose frequency is 500 kHz
- Two embedded current limitations circuitries which control the current that flows through the power switch. The pulse by pulse current limit forces the power switch OFF cycle by cycle if the current reaches an internal threshold, while the frequency shifter reduces the switching frequency in order to strongly reduce the duty cycle.
- A transconductance error amplifier.
- A pulse width modulator (PWM) comparator and the relative logic circuitry necessary to drive the internal power.
- An high side driver for the internal P-MOS switch.
- An inhibit block for stand-by operation
- A circuit to realize the thermal protection function.

Figure 2. Block diagram



4.1 Power supply and voltage reference

The internal regulator circuit (shown in *Figure 2*) consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks.

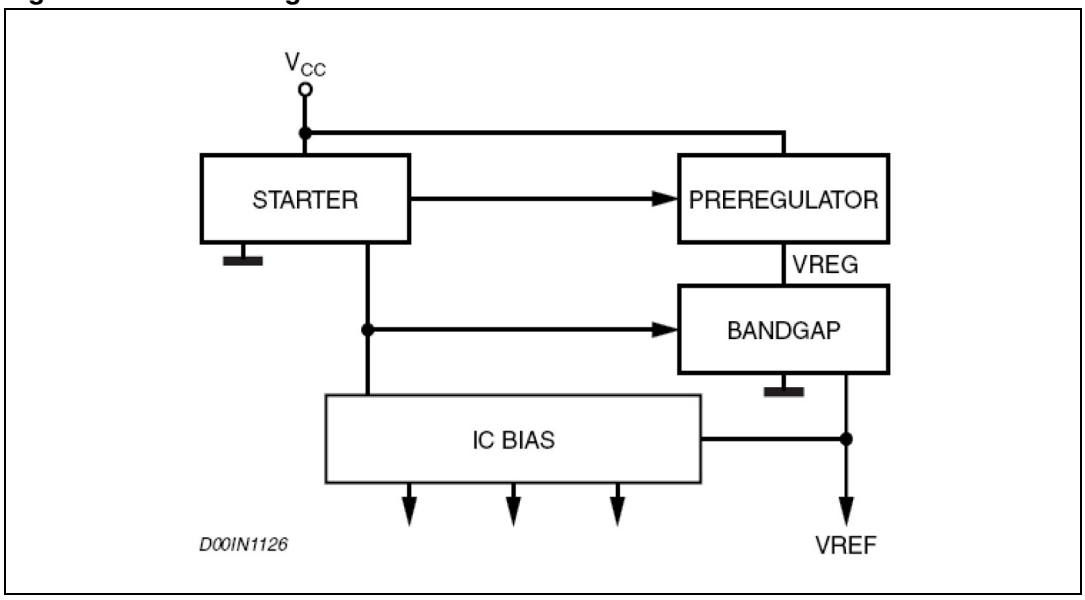
The starter gives the start-up currents to the whole device when the input voltage goes high and the device is enabled (inhibit pin connected to ground).

The preregulator block supplies the bandgap cell with a preregulated voltage V_{REG} that has a very low supply voltage noise sensitivity.

4.2 Voltages monitor

An internal block senses continuously the V_{CC}, V_{REF} and V_{BG}. If the voltages go higher than their thresholds, the regulator starts to work. There is also an hysteresis on the V_{CC} (UVLO).

Figure 3. Internal regulator circuit



4.3 Oscillator and synchronizer

Figure 4 shows the block diagram of the oscillator circuit.

The clock generator provides the switching frequency of the device that is internally fixed at 500 kHz. The frequency shifter block acts reducing the switching frequency in case of strong overcurrent or short circuit. The clock signal is then used in the internal logic circuitry and is the input of the ramp generator and Synchronizer blocks.

The ramp generator circuit provides the sawtooth signal, used to realize the PWM control and the internal voltage feed forward, while the synchronizer circuit generates the synchronization signal. In fact the device has a synchronization pin that can works both as master and slave.

As master to synchronize external devices to the internal switching frequency.

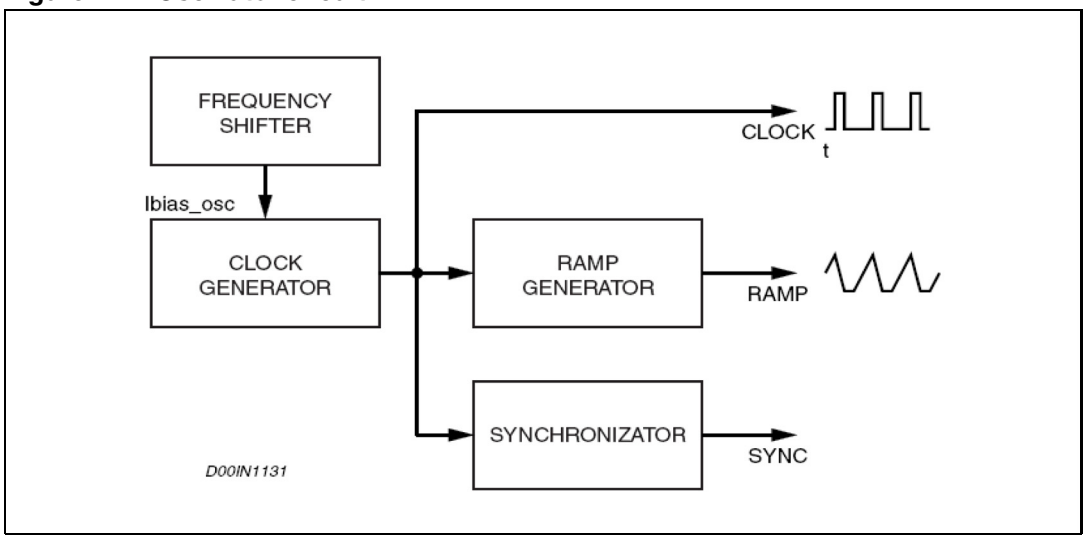
As slave to synchronize itself by external signal.

In particular, connecting together two devices, the one with the lower switching frequency works as slave and the other one works as master.

To synchronize the device, the SYNC pin has to pass from a low level to a level higher than the synchronization threshold with a duty cycle that can vary approximately from 10 % to 90 %, depending also on the signal frequency and amplitude.

The frequency of the synchronization signal must be at least higher than the internal switching frequency of the device (500 kHz).

Figure 4. Oscillator circuit



4.4 Current protection

The A5970AD has two current limit protections, pulse by pulse and frequency fold back.

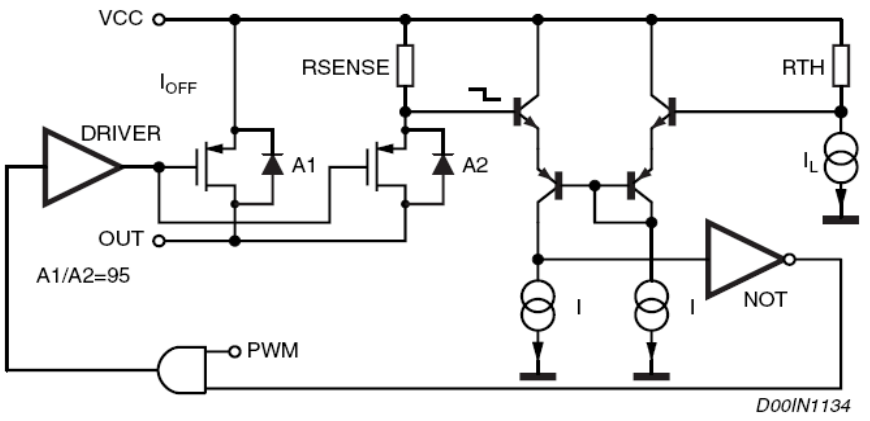
The schematic of the current limitation circuitry for the pulse by pulse protection is shown in *Figure 5*.

The output power PDMOS transistor is split in two parallel PDMOS. The smallest one has a resistor in series, R_{SENSE}. The current is sensed through Rsense and if reaches the threshold, the mirror is unbalanced and the PDMOS is switched off until the next falling edge of the internal clock pulse.

Due to this reduction of the ON time, the output voltage decreases.

Since the minimum switch ON time (necessary to avoid false overcurrent signal) is not enough to obtain a sufficiently low duty cycle at 500 kHz, the output current, in strong overcurrent or short circuit conditions, could increase again. For this reason the switching frequency is also reduced, so keeping the inductor current under its maximum threshold. The frequency shifter (see *Figure 4*) depends on the feedback voltage. As the feedback voltage decreases (due to the reduced duty cycle), the switching frequency decreases too.

Figure 5. Current limitation circuitry



4.5 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (1.235 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage. The output (COMP) is connected to the external compensation network.

The uncompensated error amplifier has the following characteristics:

Table 5. Uncompensated error amplifier

Tranconductance	2300 µS
Low frequency gain	65 dB
Minimum sink/source voltage	1500 µA/300 µA
Output voltage swing	0.4 V/3.65 V
Input bias current	2.5 µA

Note: The error amplifier output is compared with the oscillator sawtooth to perform PWM control.

4.6 PWM comparator and power stage

This block compares the oscillator sawtooth and the error amplifier output signals generating the PWM signal for the driving stage. The power stage is a very critical block cause it has to guarantee a correct turn on and turn OFF of the PDMOS. The turn ON of the power element, or better, the rise time of the current at turn on, is a very critical parameter to compromise.

At a first approach, it looks like the faster it is the rise time, the lower are the turn on losses. But there is a limit introduced by the recovery time of the recirculation diode. In fact when the current of the power element equals the inductor current, the diode turns off and the drain of the power is free to go high. But during its recovery time, the diode can be considered as an

high value capacitor and this produces a very high peak current, responsible of many problems:

- Spikes on the device supply voltage that cause oscillations (and thus noise) due to the board parasites.
- Turn ON overcurrent causing a decrease of the efficiency and system reliability.
- Big EMI problems.
- Shorter freewheeling diode life.

The fall time of the current during the turn off is also critical. In fact it produces voltage spikes (due to the parasites elements of the board) that increase the voltage drop across the PDMOS.

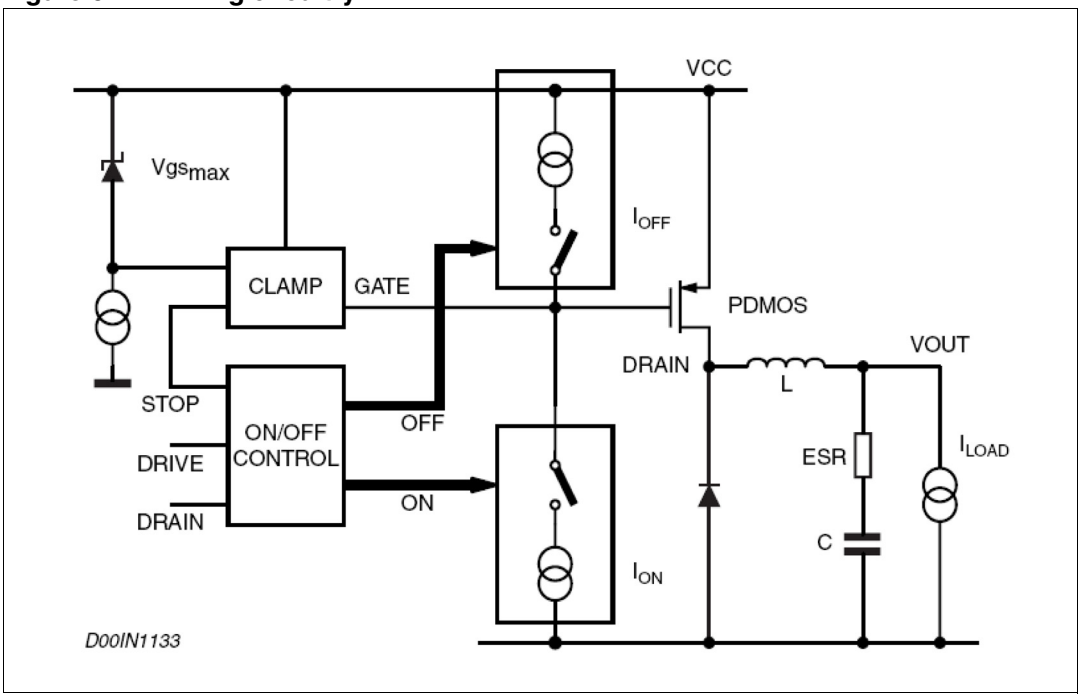
In order to minimize all these problems, a new topology of driving circuit has been used and its block diagram is shown in *Figure 6*.

The basic idea is to change the current levels used to turn on and off the power switch, according with the PDMOS status and with the gate clamp status.

This circuitry allow to turn off and on quickly the power switch and to manage the above question related to the freewheeling diode recovery time problem.

The gate clamp is necessary to avoid that Vgs of the internal switch goes higher than Vgsmax. The ON/OFF control block avoids any cross conduction between the supply line and ground.

Figure 6. Driving circuitry



4.7 Inhibit function

The inhibit feature allows to put in stand-by mode the device. With INH pin higher than 2.2 V the device is disabled and the power consumption is reduced to less than 100 μA. With INH pin lower than 0.8 V, the device is enabled. If the INH pin is left floating, an internal pull up ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{CC} compatible.

4.8 Thermal shutdown

The shutdown block generates a signal that turns off the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 °C). The sensing element of the chip is very close to the PDMOS area, so ensuring an accurate and fast temperature detection. An hysteresis of approximately 20 °C avoids that the devices turns on and off continuously

5 Additional features and protections

5.1 Feedback disconnection

In case of feedback disconnection, the duty cycle increases versus the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is turned off if the feedback pin remains floating.

5.2 Output overvoltage protection

The overvoltage protection, OVP, is realized by using an internal comparator, which input is connected to the feedback, that turns off the power stage when the OVP threshold is reached. This threshold is typically 30 % higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage (see test application circuit), the OVP intervention will be set at:

Equation 1

$$V_{OVP} = 1.3 \times \frac{R_1 + R2}{R_2} \times V_{FB}$$

Where R1 is the resistor connected between the output voltage and the feedback pin, while R2 is between the feedback pin and ground.

5.3 Zero load

Due to the fact that the internal power is a PDMOS, no boostrap capacitor is required and so, the device works properly also with no load at the output. In this condition it works in burst mode, with random repetition rate of the burst.

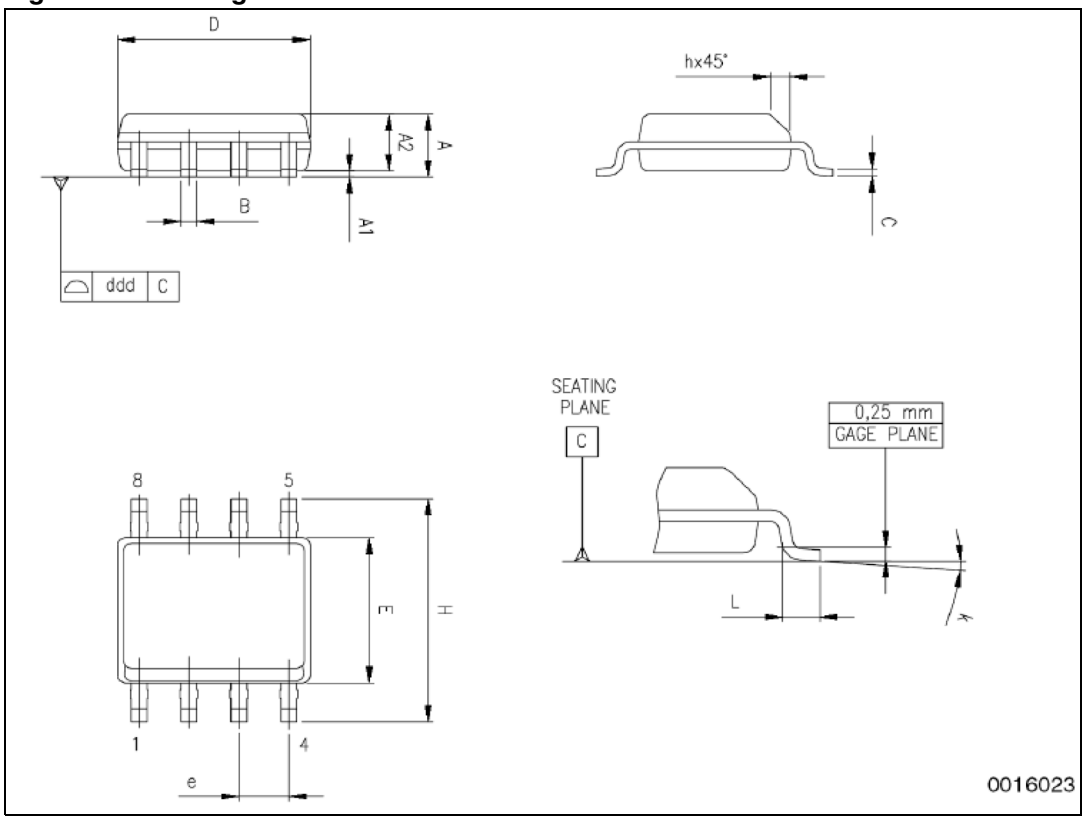
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Table 6. SO-8 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D(1)	4.80		5.00	0.1890		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min), 8° (max)					
ccc			0.10			0.0039

Figure 7. Package dimensions



7 Revision history

Table 7. Document revision history

Date	Revision	Changes
02-May-2008	1	Initial release
27-Aug-2008	2	Updated: Coverpage and *Table 4 on page 5*

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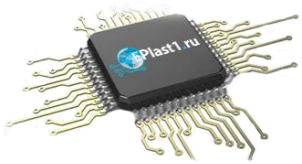

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