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# MR45V256A

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256k(32,768-Word × 8-Bit) FeRAM (Ferroelectric Random Access Memory) SPI

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## GENERAL DESCRIPTION

The MR45V256A is a nonvolatile 32,768-word x 8-bit ferroelectric random access memory (FeRAM) developed in the ferroelectric process and silicon-gate CMOS technology. The MR45V256A is accessed using Serial Peripheral Interface. Unlike SRAMs, this device, whose cells are nonvolatile, eliminates battery backup required to hold data. This device has no mechanisms of erasing and programming memory cells and blocks, such as those used for various EEPROMs. Therefore, the write cycle time can be equal to the read cycle time and the power consumption during a write can be reduced significantly.

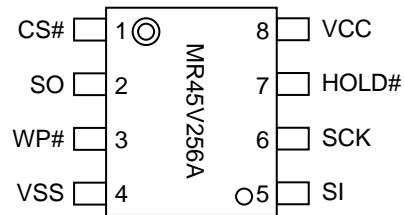
The MR45V256A can be used in various applications, because the device is guaranteed for the write/read tolerance of  $10^{12}$  cycles per bit and the rewrite count can be extended significantly.

## FEATURES

- 32,768-word × 8-bit configuration (Serial Peripheral Interface : SPI)
- A single 3.3 V ± 0.3 V power supply
- Operating frequency: 15MHz
- Read/write tolerance:  $10^{12}$  cycles/bit
- Data retention: 10 years
- Guaranteed operating temperature range: -40 to 85°C (Extended temperature version)
- Package options:
  - 8-pin plastic SOP (P-SOP8-200-1.27-T2K )

**PIN CONFIGURATION**

8-pin plastic SOP



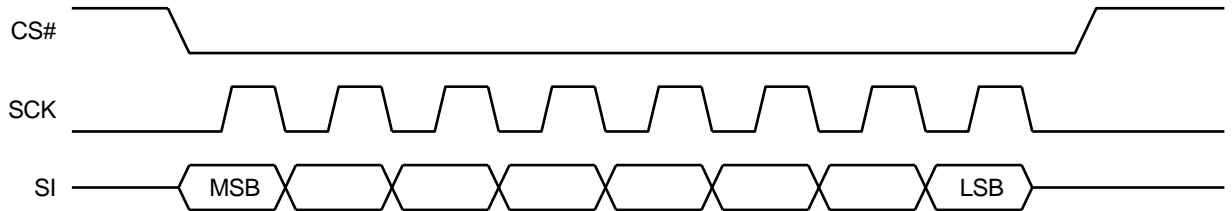
Note:

Signal names that end with # indicate that the signals are negative-true logic.

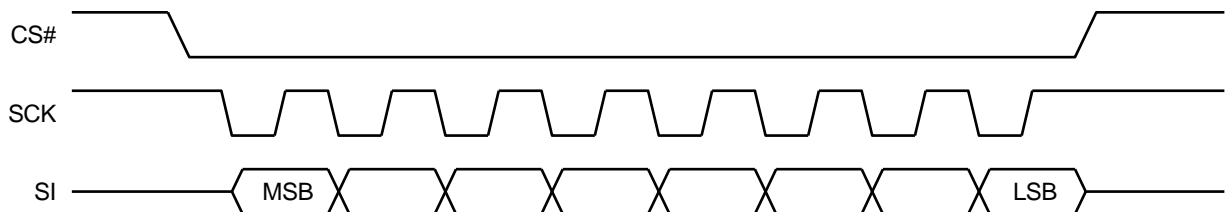
**PIN DESCRIPTIONS**

| Pin Name                          | Description   |
|-----------------------------------|---|
| CS#                               | Chip Select (input, negative logic)<br>Latches an address by low input, activates the FeRAM, and enables a read or write operation.   |
| WP#                               | Write Protect( input , negative logic )<br>Write Protect pin controls write-operation to the status-register(BP0,BP1). This pin should be fixed low or high in write-operations.  |
| HOLD#                             | HOLD( input , negative logic )<br>Hold pin is used when the serial-communication suspended without disable the chip select. When HOLD# is low ,the serial-output is in High-Z status and serial-input/serial-clock are "Don' t Care" . CS# should be low in hold operation. |
| SCK                               | Serial Clock<br>Serial Clock is the clock input pin for setting for serial data timing. Inputs are latched on the rising edge and output occur on the falling edge.   |
| SI                                | Serial input<br>SI pins are serial input pins for Operation-code , addresses ,and data-inputs .   |
| SO                                | Serial output<br>SO pins are serial output pins.  |
| V <sub>CC</sub> , V <sub>SS</sub> | Power supply<br>Apply the specified voltage to V <sub>CC</sub> . Connect V <sub>SS</sub> to ground.   |

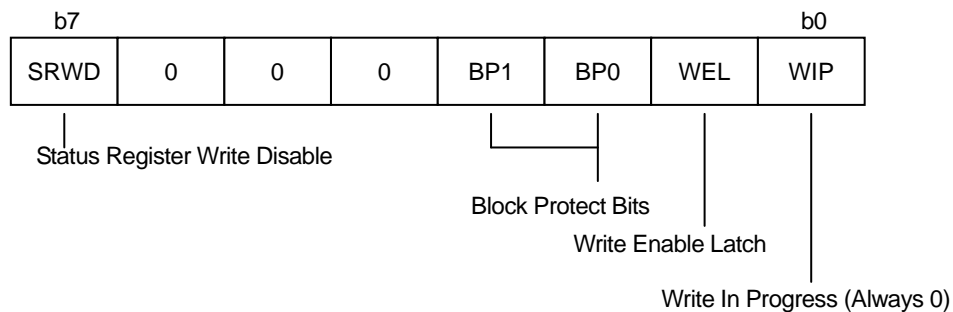
**SPI mode0 (CPOL=0, CPHA=0)**



**SPI mode3 (CPOL=1, CPHA=1)**



**Status Register**



| Name    | Function   |
|---------|--|
| WIP     | Fixed to 0.  |
| WEL     | Write Enable Latch. This indicates internal WEL condition.   |
| BP0,BP1 | Block Protect :These bits can be changed protect area .<br>This is the software protect.   |
| SRWD    | Status Register Write Disable (SRWD) : SRWD controls the effect of the hardware WP# pin. This device will be in hardware-protect by combination of SRWD and WP#. |
| 0       | Fixed to 0.  |

Status Register data are volatile.

Set Status Register data by WRSR(Write status register) command, after power on.

**Operation-Code**

Operation codes are listed in the table below.If the device receives invalid operation code,the device will be deselected.

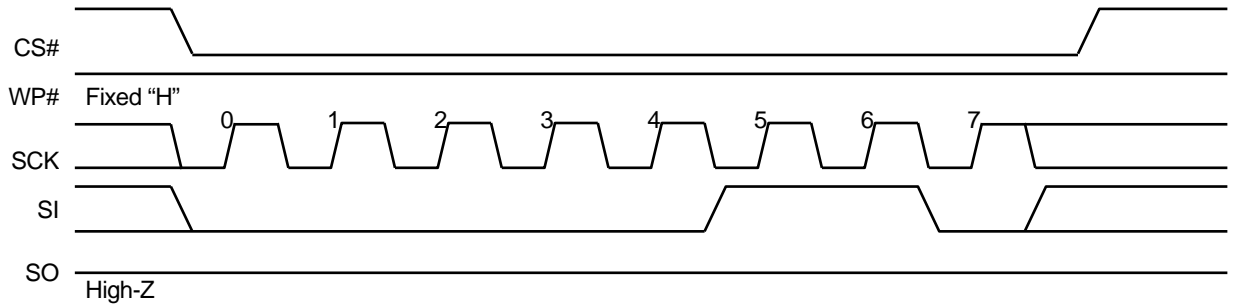
| Instruction | Description            | Instruction format |
|-------------|------------------------|--------------------|
| WREN        | Write Enable           | 0000 0110          |
| WRDI        | Write Disable          | 0000 0100          |
| RDSR        | Read Status Register   | 0000 0101          |
| WRSR        | Write Status Register  | 0000 0001          |
| READ        | Read from Memory Array | 0000 0011          |
| WRITE       | Write to Memory Array  | 0000 0010          |

**Commands**

**WREN(Write Enable)**

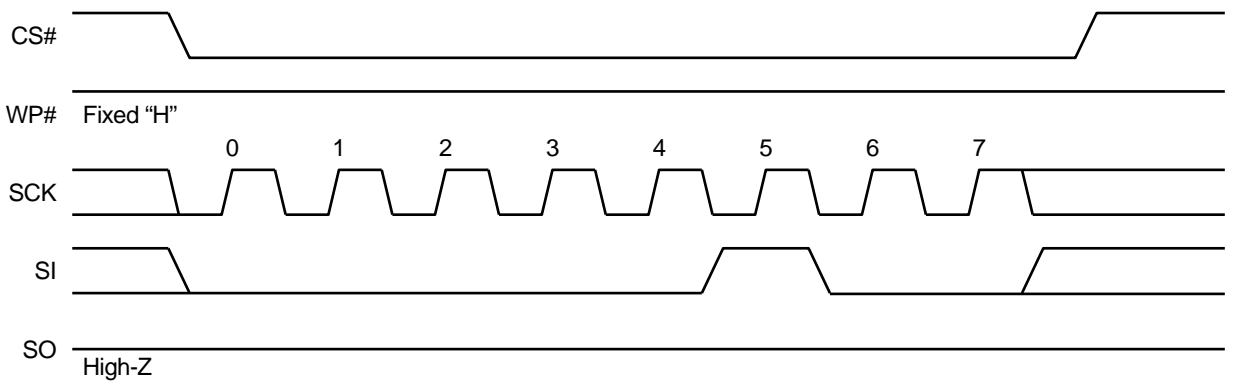
It is necessary to set Write Enable Latch (WEL) bit before write-operation (WRITE and WRSR).

WREN command sets WEL bit.



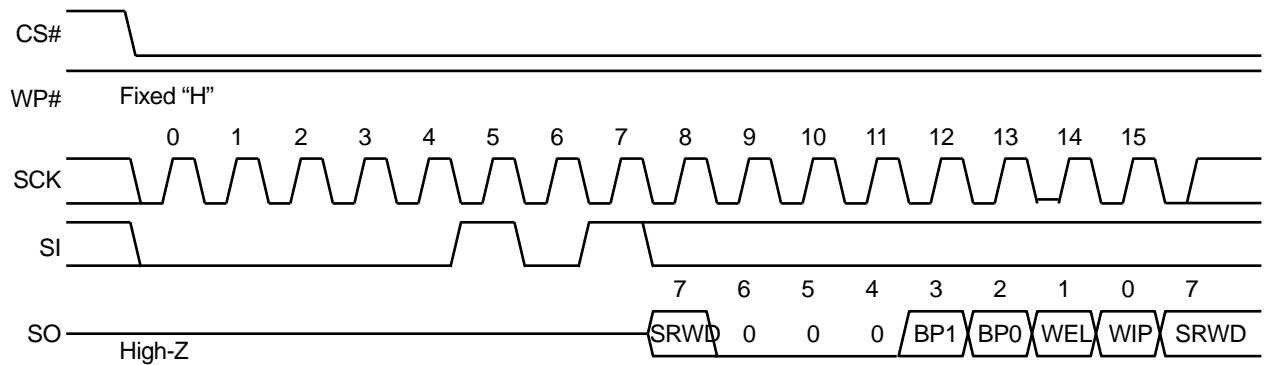
**WRDI(Write Disable)**

WRDI command resets WEL bit.



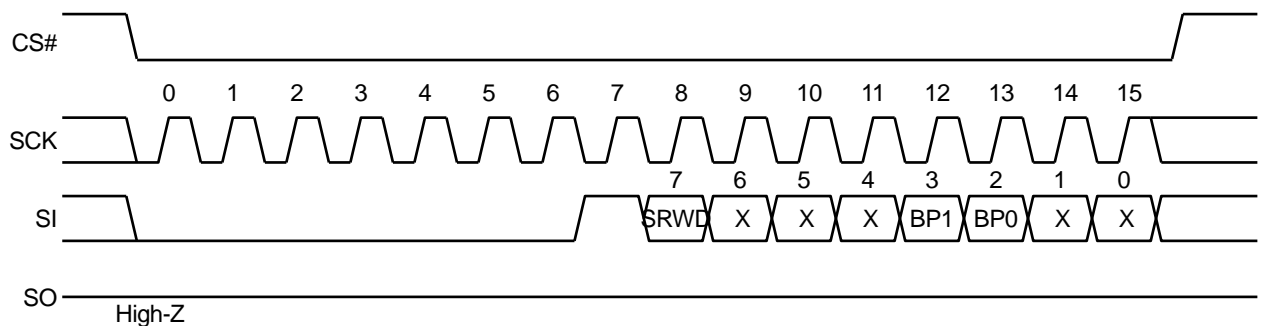
**RDSR(READ Status Register)**

The RDSR command allows to read data of status register.



**WRSR(WRITE Status Register)**

WRSR command allows to write data to status register(SRWD,BP0,BP1). It is necessary to set Write Enable Latch (WEL) bit by WREN command before executing WRSR.

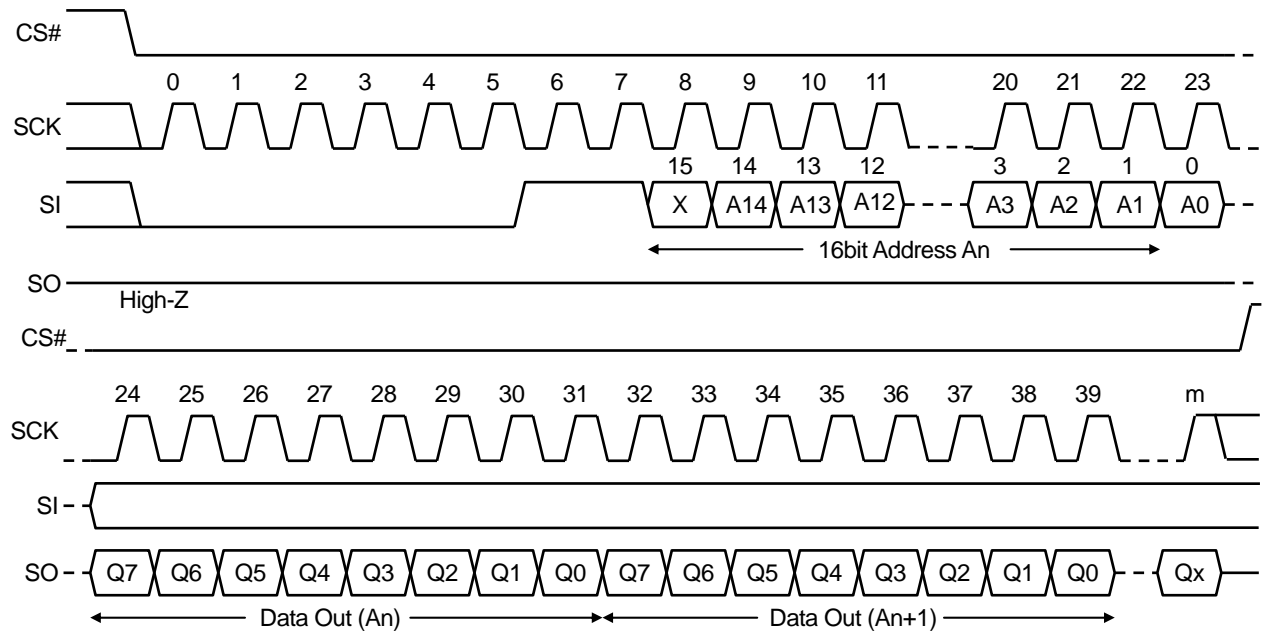


Note:

WP# = Fix "H"

**READ(Read from Memory Array)**

READ command can be valid when CS# goes "L", then the op-code and 16bit-addresses are inputted to serial input "SI". The inputted addresses are loaded to internal register, then the data from corresponded address is output at serial-output "SO". If CS# will keep "L", the internal address will be increased automatically after 8 clocks and will output the data from new-address. When it reaches the most significant address, the address counter rolls over to starting address, and reading cycle can be continued infinitely.



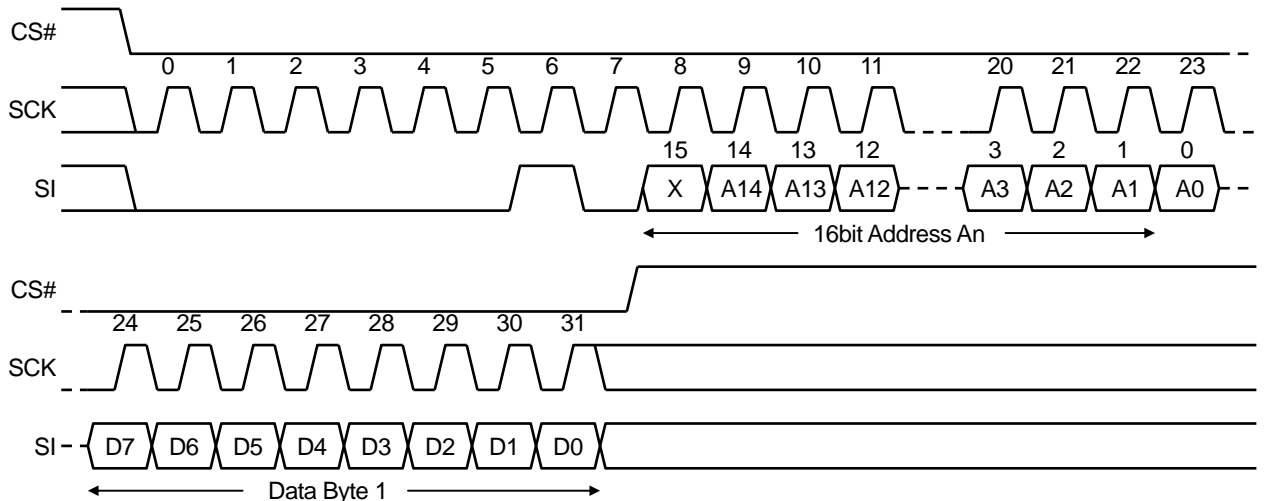
Note : WP# = fixed "H"



**WRITE(Write to Memory Array)**

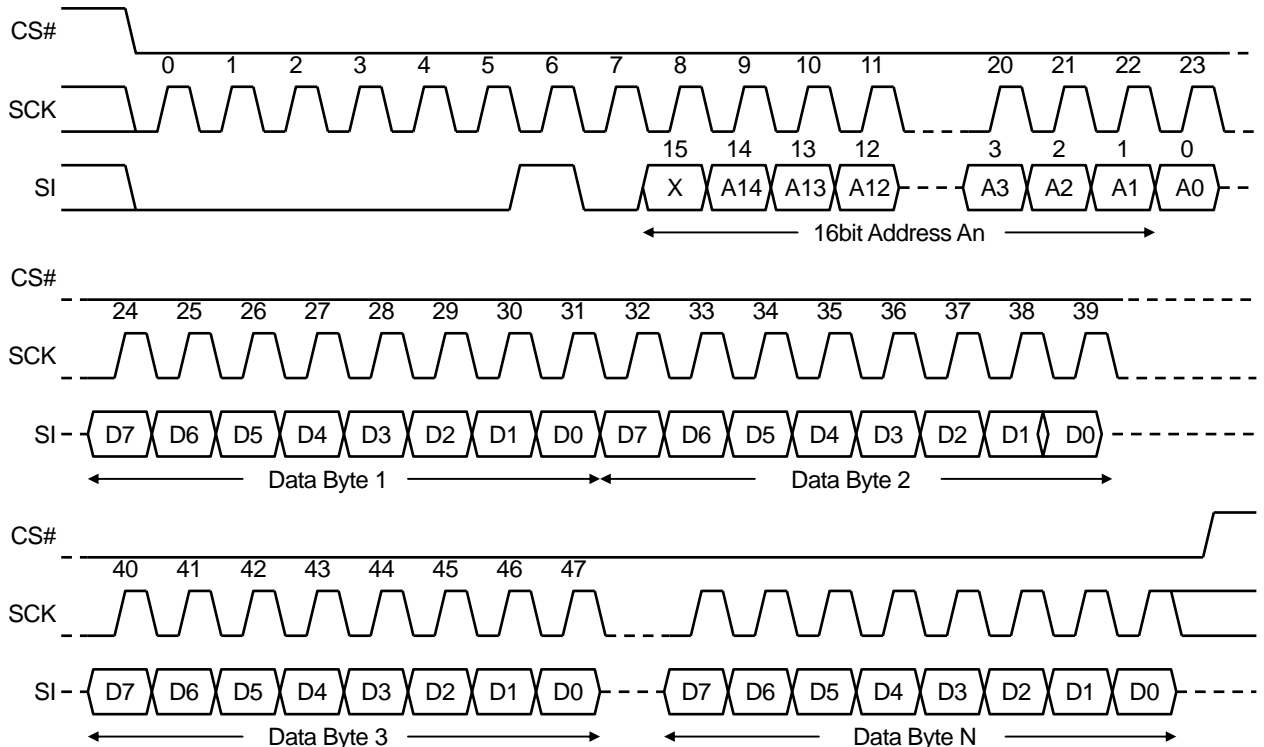
Write command can be valid when CS# goes “L”, then the op-code and 16bit-addresses are inputted to serial input “SI”. Writing is terminated when CS# goes high after data-input. If CS# will keep “L”, the internal address will be increased automatically. When it reaches the most significant address, the address counter rolls over to starting address 0000h, and writing cycle (overwriting) can be continued infinitely.

**WRITE(1Byte)**



Note : WP# = Fixed "H" , SO=High-Z

**WRITE(Page)**



Note : WP# = Fixed "H" , SO=High-Z

**Write Protection**

Writing protection block is shown as follows:

Protect Block size

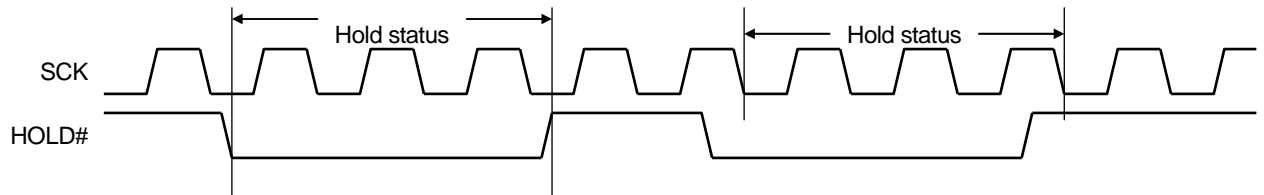
| Block Protect BIT |     | Protected Block | Protected Address Area |
|-------------------|-----|-----------------|------------------------|
| BP1               | BP0 |                 |                        |
| 0                 | 0   | None            | None                   |
| 0                 | 1   | Upper 1/4 block | 6000h – 7FFFh          |
| 1                 | 0   | Upper 1/2 block | 4000h – 7FFFh          |
| 1                 | 1   | All             | 0000h – 7FFFh          |

Writing Protect

| WP# | SRWD | mode                      | Writing protection status in status register   | Protection status in memory |                    |
|-----|------|---------------------------|--|-----------------------------|--------------------|
|     |      |                           |  | Protected blocks            | Unprotected blocks |
| 1   | 0    | Software protection (SPM) | Status register is unprotected when WEL-bit is set by WREN command. BP0 and BP1 are unprotected. | Protected                   | Unprotected        |
| 0   | 0    |                           |  |                             |                    |
| 1   | 1    |                           |  |                             |                    |
| 0   | 1    | Hardware protection (HPM) | Status register is protected. BP0 and BP1 are protected.   | Protected                   | Unprotected        |

**HOLD**

Hold status is used for suspending serial communication without disable the chip. SO becomes "High-Z" and SI is "Don't care" during the hold status. It is necessary to keep CS#=L in hold status.



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

The application of stress (voltage, current, or temperature) that exceeds the absolute maximum rating may damage the device. Therefore, do not allow actual characteristics to exceed any one parameter ratings

**Pin voltages**

| Parameter                          | Symbol              | Rating |                | Unit |
|------------------------------------|---------------------|--------|----------------|------|
|                                    |                     | Min.   | Max.           |      |
| Pin Voltage (Input Signal)         | $V_{IN}$            | -0.5   | $V_{CC} + 0.5$ | V    |
| Pin Voltage (Input/Output Voltage) | $V_{INQ}, V_{OUTQ}$ | -0.5   | $V_{CC} + 0.5$ | V    |
| Power Supply Voltage               | $V_{CC}$            | -0.5   | 4.0            | V    |

**Temperature Range**

| Parameter   | Symbol | Rating |      | Unit | Note |
|---|--------|--------|------|------|------|
|   |        | Min.   | Max. |      |      |
| Storage Temperature<br>(Extended Temperature Version)   | Tstg   | -55    | 125  | °C   |      |
| Operating Temperature<br>(Extended Temperature Version) | Topr   | -40    | 85   | °C   |      |

**Others**

| Parameter                | Symbol    | Rating   | Unit    |
|--------------------------|-----------|----------|---------|
| Power Dissipation        | $P_D$     | 1,000mW  |         |
| Allowable Input Current  | $I_{IN}$  | +/- 20mA | Ta=25°C |
| Allowable Output Current | $I_{OUT}$ | +/- 20mA | Ta=25°C |

**Recommended Operating Conditions****Power Supply Voltage**

[V]

| Parameter            | Symbol   | Min. | Typ. | Max. | Note |
|----------------------|----------|------|------|------|------|
| Power Supply Voltage | $V_{CC}$ | 3.0  | 3.3  | 3.6  |      |
| Ground Voltage       | $V_{SS}$ | 0    | 0    | 0    |      |

**DC Input Voltage**

[V]

| Parameter          | Symbol   | Min.                | Max.                | Note |
|--------------------|----------|---------------------|---------------------|------|
| Input High Voltage | $V_{IH}$ | $V_{CC} \times 0.8$ | $V_{CC} + 0.3$      |      |
| Input Low Voltage  | $V_{IL}$ | -0.3                | $V_{CC} \times 0.2$ |      |

**Overshoot/Undershoot tolerance**

| Parameter | Symbol              | Pulse Width        | Peak                   |
|-----------|---------------------|--------------------|------------------------|
| "H" input | $V_{IH}$ OVERSHOOT  | $\leq 20\text{ns}$ | $V_{CC} + 1.0\text{V}$ |
| "L" input | $V_{IL}$ UNDERSHOOT | $\leq 20\text{ns}$ | -1.0V                  |

**DC Characteristics****DC Input/Output Characteristics**

| Parameter              | Symbol   | Condition              | Min.                 | Max.                 | Unit          | Note |
|------------------------|----------|------------------------|----------------------|----------------------|---------------|------|
| Output High Voltage    | $V_{OH}$ | $I_{OH} = -2\text{mA}$ | $V_{CC} \times 0.85$ | —                    | V             |      |
| Output Low Voltage     | $V_{OL}$ | $I_{OL} = 2\text{mA}$  | —                    | $V_{CC} \times 0.15$ | V             |      |
| Input Leakage Current  | $I_{LI}$ | —                      | -10                  | 10                   | $\mu\text{A}$ |      |
| Output Leakage Current | $I_{LO}$ | —                      | -10                  | 10                   | $\mu\text{A}$ |      |

**Power Supply Current** $V_{CC} = \text{Max. to Min.}, T_a = \text{Topr}$ 

| Parameter                        | Symbol    | Condition   | Max. | Unit          | Note |
|----------------------------------|-----------|---|------|---------------|------|
| Power Supply Current (Standby)   | $I_{CCS}$ | $V_{IN} = 0.2\text{V}$ or $V_{CC} - 0.2\text{V}$  | 400  | $\mu\text{A}$ |      |
| Power Supply Current (Operating) | $I_{CCA}$ | $V_{IN} = 0.2\text{V}$ or $V_{CC} - 0.2\text{V}$ ,<br>SCK=15MHz, $I_{OUT} = 0\text{mA}$ | 10   | mA            |      |

## AC Characteristics (Read Cycle)

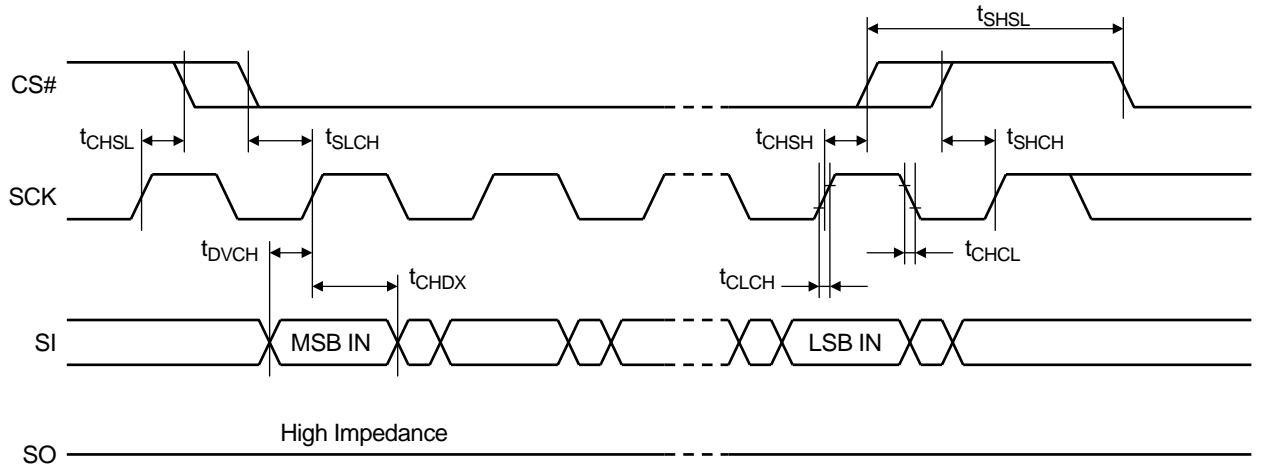
V<sub>CC</sub>=Max. to Min., Ta=Topr.

| Parameter                                 | Symbol            | MR45V256A |      | Unit | Note |
|---|-------------------|-----------|------|------|------|
|   |                   | Min.      | Max. |      |      |
| Clock frequency                           | f <sub>C</sub>    | D.C.      | 15   | MHz  |      |
| CS# Active setup time                     | t <sub>SLCH</sub> | 10        | —    | ns   |      |
| CS# In-active setup-time                  | t <sub>SHCH</sub> | 10        | —    | ns   |      |
| CS# De-select time                        | t <sub>SHSL</sub> | 10        | —    | ns   |      |
| CS# Active hold time                      | t <sub>CHSH</sub> | 10        | —    | ns   |      |
| CS# In-active hold-time                   | t <sub>CHSL</sub> | 10        | —    | ns   |      |
| SCK High time                             | t <sub>CH</sub>   | 30        | —    | ns   | 1    |
| SCK Low time                              | t <sub>CL</sub>   | 30        | —    | ns   | 1    |
| SCK Rise time                             | t <sub>CLCH</sub> | —         | 1    | ns   | 2    |
| SCK Fall time                             | t <sub>CHCL</sub> | —         | 1    | ns   | 2    |
| Data Setup time                           | t <sub>DVCH</sub> | 5         | —    | ns   |      |
| Data Hold time                            | t <sub>CHDX</sub> | 5         | —    | ns   |      |
| SCK Low Hold time after HOLD# inactive    | t <sub>HHCH</sub> | 10        | —    | ns   |      |
| SCK Low Hold time after HOLD# active      | t <sub>HLCH</sub> | 10        | —    | ns   |      |
| SCK High Setup time before HOLD# active   | t <sub>CHHL</sub> | 10        | —    | ns   |      |
| SCK High Setup time before HOLD# inactive | t <sub>CHHH</sub> | 10        | —    | ns   |      |
| Output disable time                       | t <sub>SHQZ</sub> | —         | 20   | ns   | 2    |
| SCK Low to Output Valid time              | t <sub>CLQV</sub> | —         | 35   | ns   |      |
| Output Hold time                          | t <sub>CLQX</sub> | 0         | —    | ns   |      |
| Output Rise time                          | t <sub>QLQH</sub> | —         | 50   | ns   | 2    |
| Output Fall time                          | t <sub>QHQL</sub> | —         | 50   | ns   | 2    |
| HOLD# High to Output Low impedance time   | t <sub>HHQX</sub> | —         | 20   | ns   | 2    |
| HOLD# High to Output High impedance time  | t <sub>HLQZ</sub> | —         | 20   | ns   | 2    |

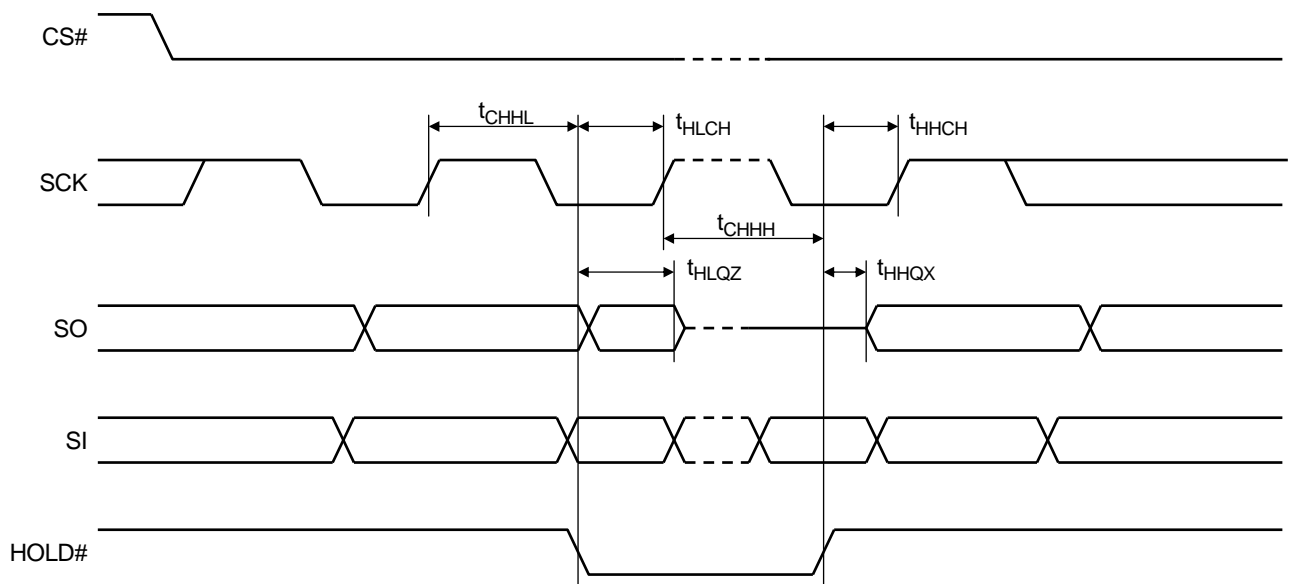
Note: 1. t<sub>CH</sub>+t<sub>CL</sub>≥1/f<sub>C</sub>  
2. sample value

**Timing Diagrams**

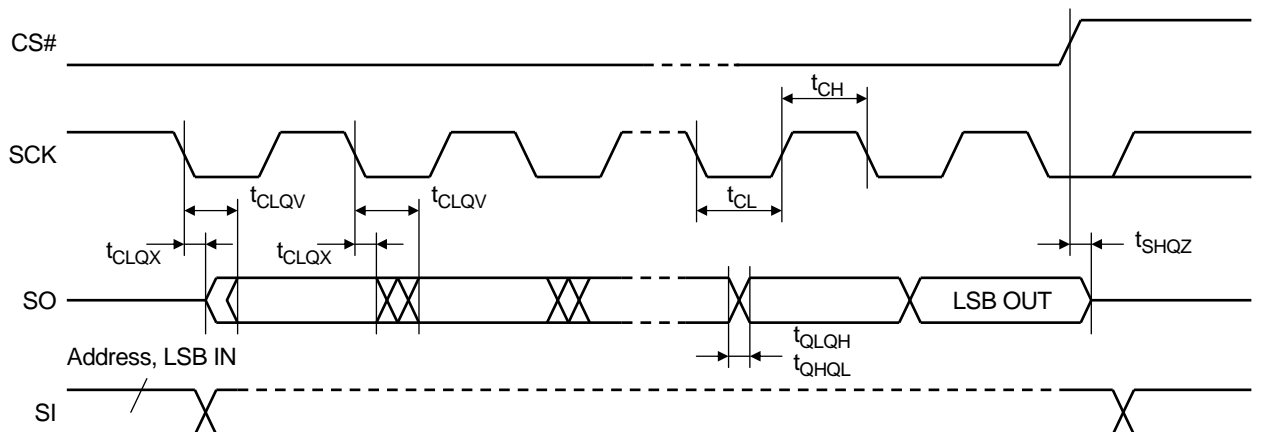
**Serial Input Timing**



**Hold Timing**



**Output Timing**





•Power-On and Power-Off Characteristics

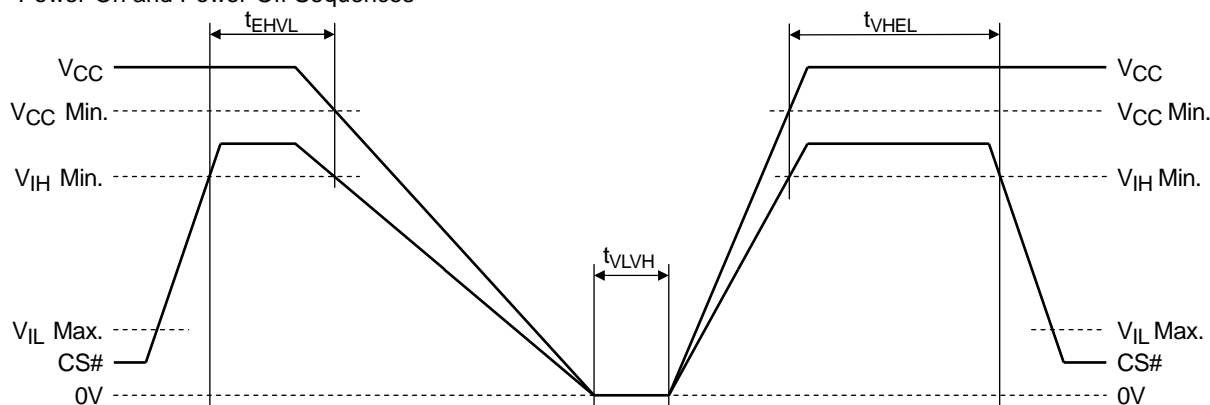
(Under recommended operating conditions)

| Parameter                    | Symbol     | Min. | Max. | Unit          | Note |
|------------------------------|------------|------|------|---------------|------|
| Power-On CS# High Hold Time  | $t_{VHEL}$ | 50   | —    | $\mu\text{s}$ | 1, 2 |
| Power-Off CS# High Hold Time | $t_{EHVL}$ | 100  | —    | ns            | 1    |
| Power-On Interval Time       | $t_{VLVH}$ | 1    | —    | $\mu\text{s}$ | 2    |

Notes:

1. To prevent an erroneous operation, be sure to maintain CS#="H", and set the FeRAM in an inactive state (standby mode) before and after power-on and power-off.
2. Powering on at the intermediate voltage level will cause an erroneous operation; thus, be sure to power up from 0 V.
3. Enter all signals at the same time as power-on or enter all signals after power-on.

•Power-On and Power-Off Sequences



**Read/Write Cycles and Data Retention**

(Under recommended operating conditions)

| Parameter        | Min.             | Max. | Unit  | Note |
|------------------|------------------|------|-------|------|
| Read/Write Cycle | 10 <sup>12</sup> | —    | Cycle |      |
| Data Retention   | 10               | —    | Year  |      |

**Capacitance**

| Signal                   | Symbol           | Min. | Max. | Unit | Note |
|--------------------------|------------------|------|------|------|------|
| Input Capacitance        | C <sub>IN</sub>  | —    | 10   | pF   | 1    |
| Input/Output Capacitance | C <sub>OUT</sub> | —    | 10   | pF   | 1    |

Note:

Sampling value. Measurement conditions are V<sub>IN</sub> = V<sub>OUT</sub> = GND, f = 1MHz, and Ta = 25°C

**REVISION HISTORY**

| Document No.   | Date          | Page             |                 | Description   |
|----------------|---------------|------------------|-----------------|---|
|                |               | Previous Edition | Current Edition |   |
| PEDR45V256A-01 | Jun. 03, 2010 | –                | –               | Preliminary edition 1 from PJDR45V256A-03               |
| PEDR45V256A-02 | Sep. 10, 2010 | 1,13             | 1,13            | Input Voltage   |
|                |               | 7,8,9            | 7,8,9           | fixed CS# waveform                                      |
|                |               | 14               | 14              | I <sub>CCS</sub> I <sub>CCA</sub>                       |
| PEDR45V256A-03 | Mar. 04, 2011 | 1,12             | 1,12            | temperature version ⇒ Extended version                  |
| PEDR45V256A-04 | Sep. 05, 2011 | 4<br>17          | 4<br>17         | Status Register<br>Input signal state in power-on       |
| PEDR45V256A-05 | Oct. 17, 2011 | 1-20             | 1-20            | Changed corporate name and logo to LAPIS Semiconductor. |

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