

# 2N7002K, 2V7002K

## Small Signal MOSFET

60 V, 380 mA, Single, N-Channel, SOT-23

### Features

- ESD Protected
- Low  $R_{DS(on)}$
- Surface Mount Package
- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Low Side Load Switch
- Level Shift Circuits
- DC-DC Converter
- Portable Applications i.e. DSC, PDA, Cell Phone, etc.

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (Note 1) Steady State 1 sq in Pad	$I_D$	380 270	mA
		$T_A = 25^\circ\text{C}$	
		$T_A = 85^\circ\text{C}$	
Drain Current (Note 2) Steady State Minimum Pad	$I_D$	320 230	mA
		$T_A = 25^\circ\text{C}$	
		$T_A = 85^\circ\text{C}$	
Power Dissipation Steady State 1 sq in Pad Steady State Minimum Pad	$P_D$	420 300	mW
Pulsed Drain Current ( $t_p = 10 \mu\text{s}$ )	$I_{DM}$	1.5	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C
Source Current (Body Diode)	$I_S$	300	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	°C
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.
2. Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

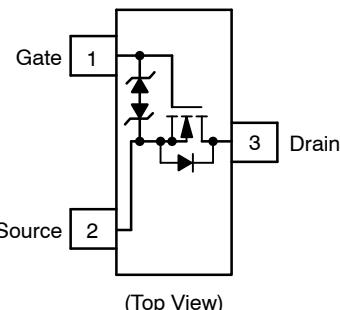


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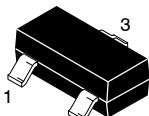
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	1.6 Ω @ 10 V	
	2.5 Ω @ 4.5 V	380 mA

### SIMPLIFIED SCHEMATIC

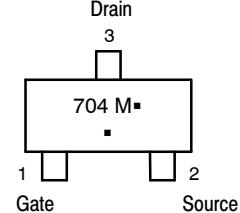


(Top View)



SOT-23  
CASE 318  
STYLE 21

### MARKING DIAGRAM & PIN ASSIGNMENT



704 = Specific Device Code\*  
M = Date Code\*  
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Specific Device Code, Date Code or overbar orientation and/or location may vary depending upon manufacturing location. This is a representation only and actual devices may not match this drawing exactly.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
2N7002KT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
2V7002KT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	300	°C/W
Junction-to-Ambient – $t \leq 5$ s (Note 3)		92	
Junction-to-Ambient – Steady State (Note 4)		417	
Junction-to-Ambient – $t \leq 5$ s (Note 4)		154	

3. Surface-mounted on FR4 board using 1 sq in pad size with 1 oz Cu.  
 4. Surface-mounted on FR4 board using 0.08 sq in pad size with 1 oz Cu.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ C$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu A$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			71		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 60$ V	$T_J = 25^\circ C$		1	$\mu A$
			$T_J = 125^\circ C$		10	
		$V_{GS} = 0$ V, $V_{DS} = 50$ V	$T_J = 25^\circ C$		100	nA
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 10$	$\mu A$
		$V_{DS} = 0$ V, $V_{GS} = \pm 10$ V			450	nA
		$V_{DS} = 0$ V, $V_{GS} = \pm 5.0$ V			150	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250$ $\mu A$	1.0		2.3	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 500$ mA		1.19	1.6	$\Omega$
		$V_{GS} = 4.5$ V, $I_D = 200$ mA		1.33	2.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 5$ V, $I_D = 200$ mA		530		mS

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 20$ V		24.5		pF
Output Capacitance	$C_{OSS}$			4.2		
Reverse Transfer Capacitance	$C_{RSS}$			2.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 10$ V; $I_D = 200$ mA		0.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	$Q_{GS}$			0.3		
Gate-to-Drain Charge	$Q_{GD}$			0.1		

### SWITCHING CHARACTERISTICS, $V_{GS} = V$ (Note 6)

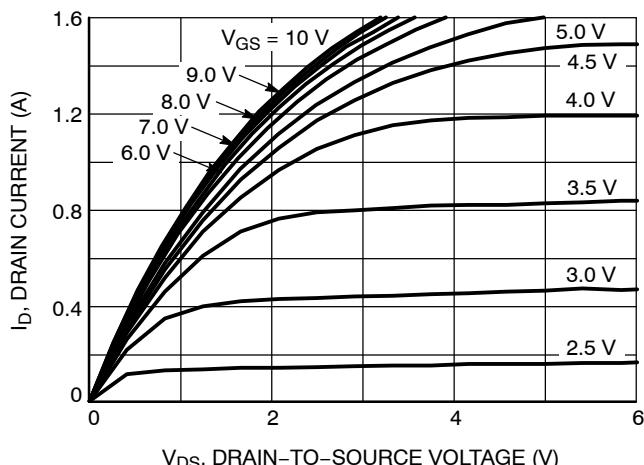
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10$ V, $V_{DD} = 25$ V, $I_D = 500$ mA, $R_G = 25$ $\Omega$		12.2		ns
Rise Time	$t_r$			9.0		
Turn-Off Delay Time	$t_{d(OFF)}$			55.8		
Fall Time	$t_f$			29		

### DRAIN-SOURCE DIODE CHARACTERISTICS

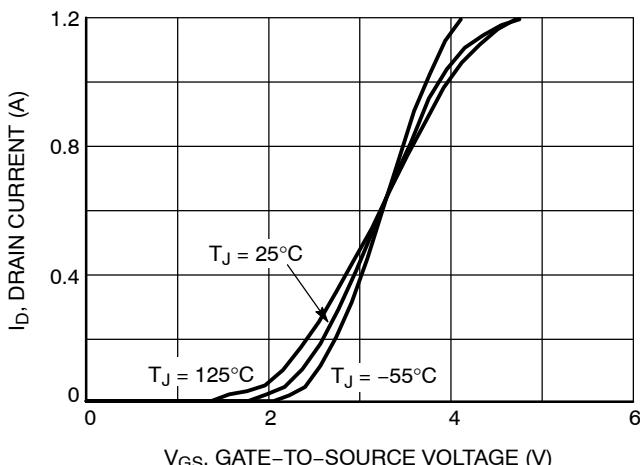
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0$ V, $I_S = 200$ mA	$T_J = 25^\circ C$		0.8	1.2	V
			$T_J = 85^\circ C$		0.7		

5. Pulse Test; pulse width  $\leq 300$   $\mu s$ , duty cycle  $\leq 2\%$   
 6. Switching characteristics are independent of operating junction temperatures

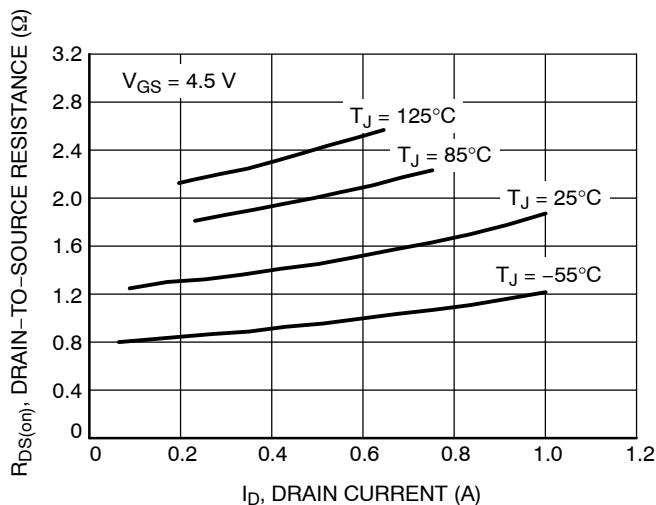
**TYPICAL CHARACTERISTICS**



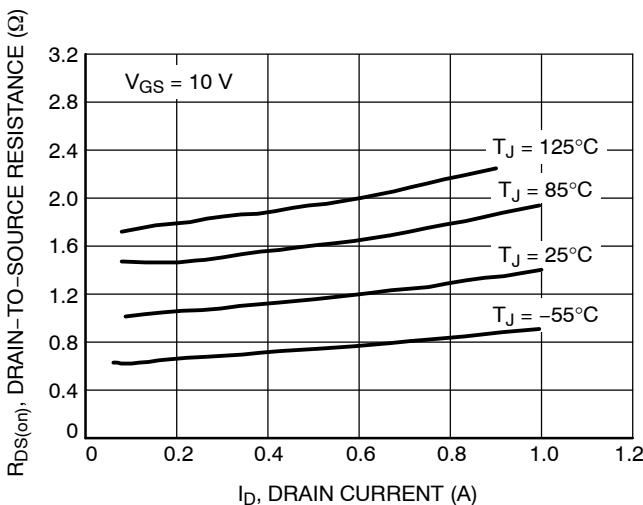
**Figure 1. On-Region Characteristics**



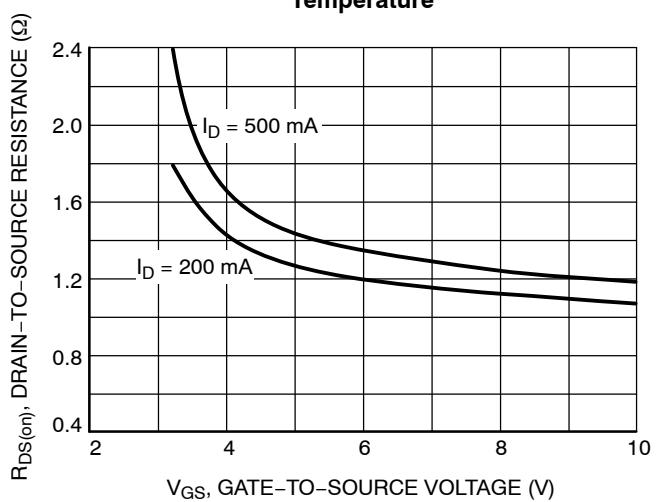
**Figure 2. Transfer Characteristics**



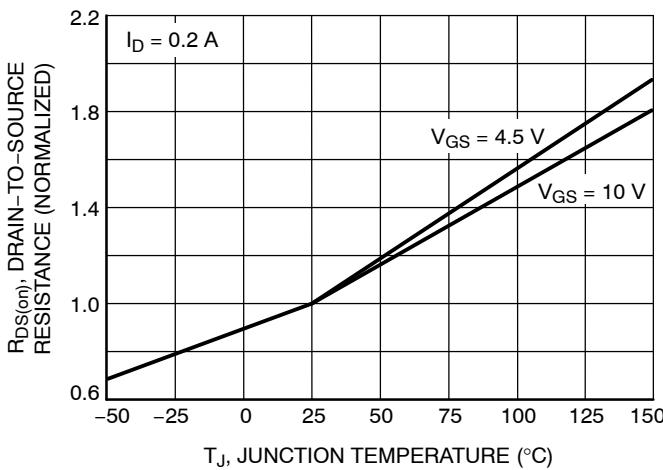
**Figure 3. On-Resistance vs. Drain Current and Temperature**



**Figure 4. On-Resistance vs. Drain Current and Temperature**

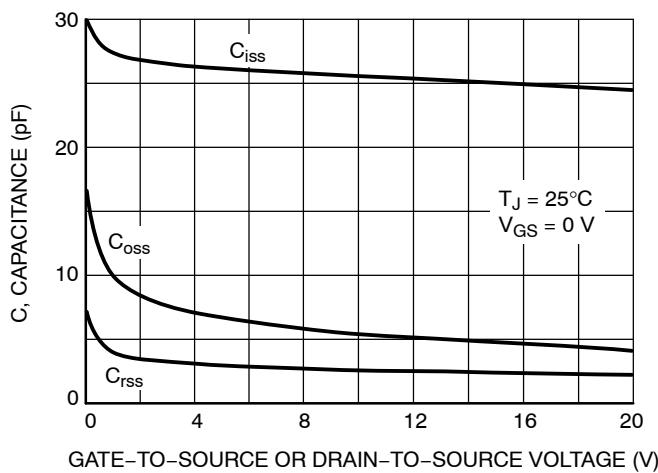


**Figure 5. On-Resistance vs. Gate-to-Source Voltage**

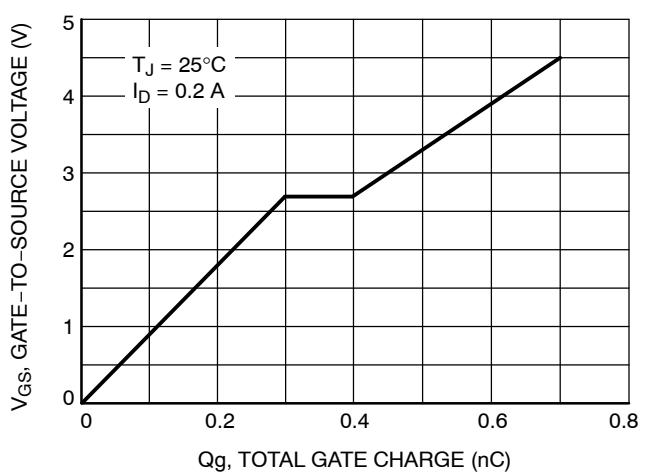


**Figure 6. On-Resistance Variation with Temperature**

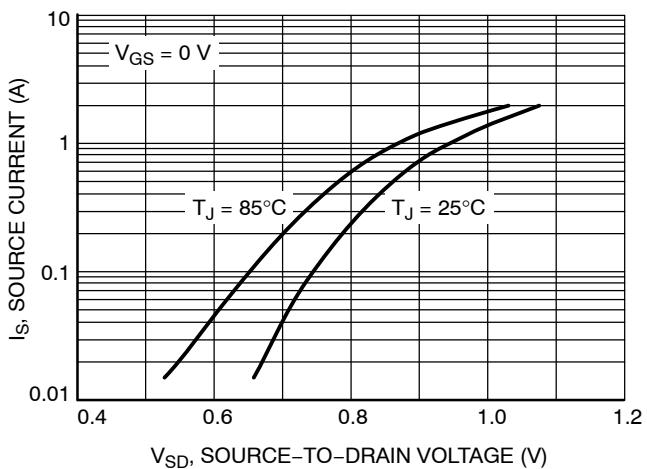
**TYPICAL CHARACTERISTICS**



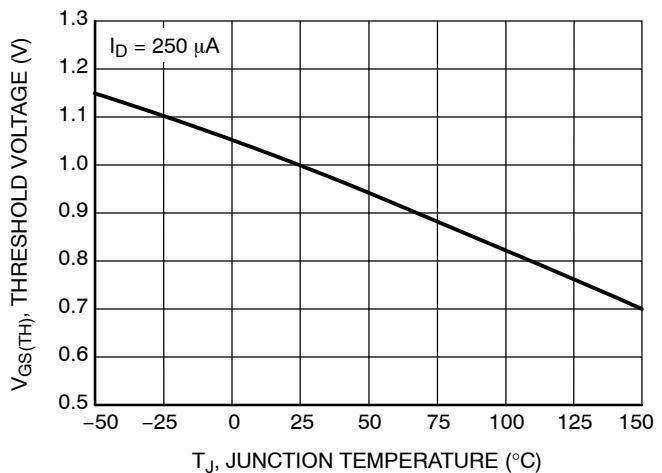
**Figure 7. Capacitance Variation**



**Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 9. Diode Forward Voltage vs. Current**



**Figure 10. Threshold Voltage with Temperature**

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## TYPICAL CHARACTERISTICS

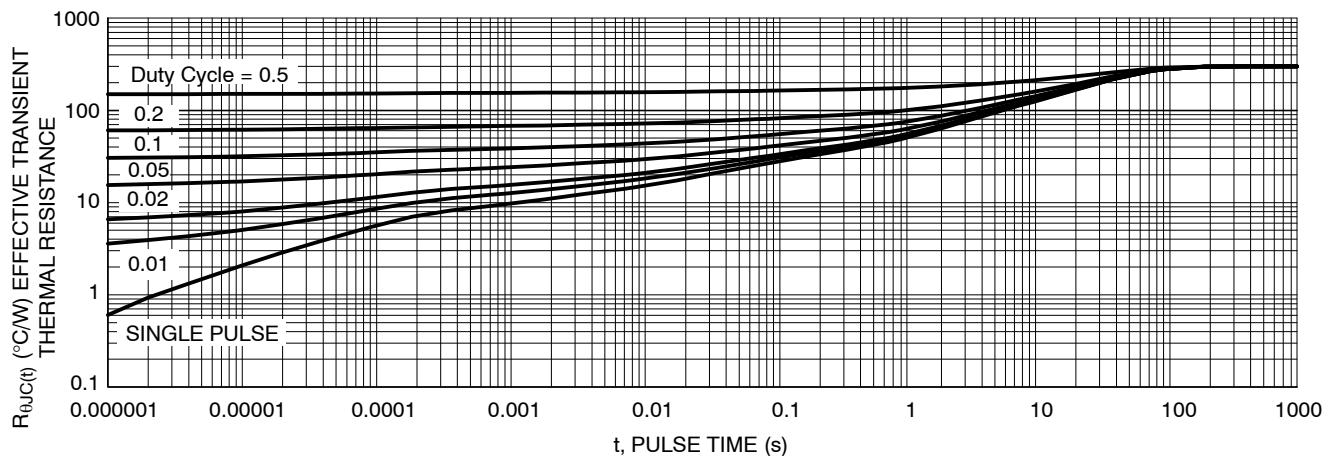


Figure 11. Thermal Response – 1 sq in pad

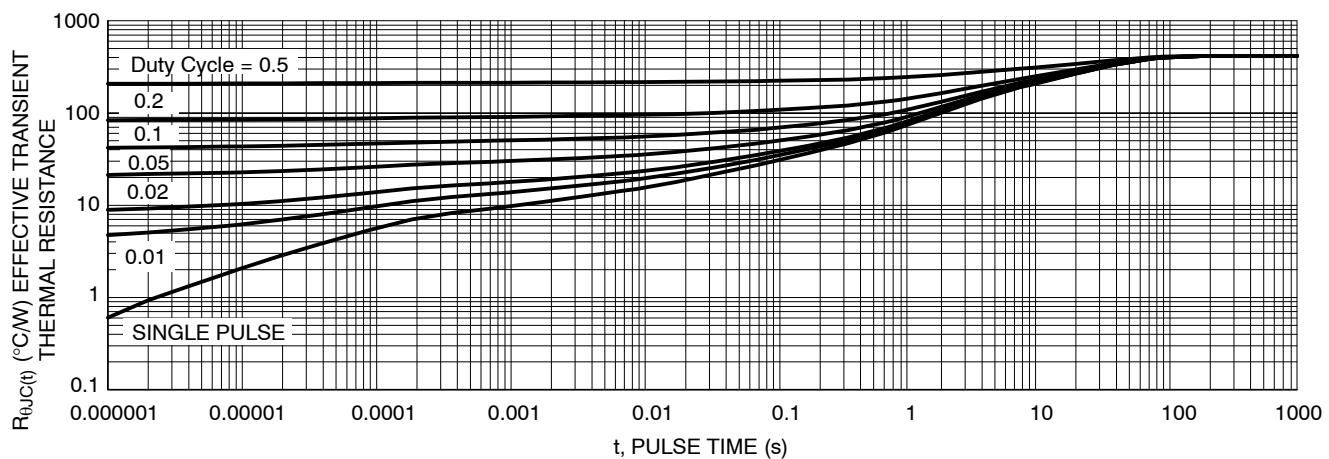
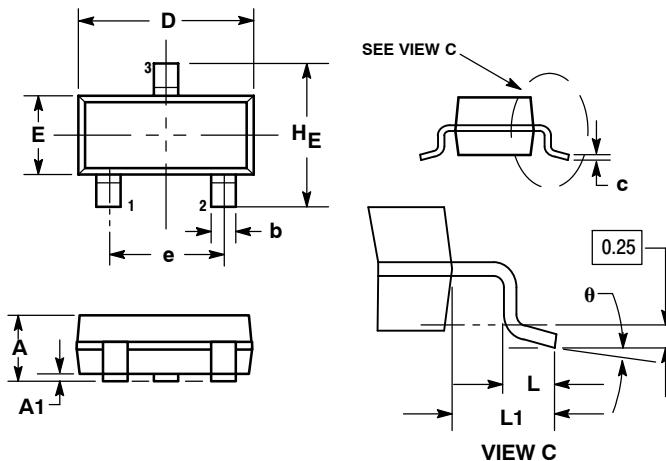


Figure 12. Thermal Response – minimum pad

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## PACKAGE DIMENSIONS

### SOT-23 (TO-236) CASE 318-08 ISSUE AP

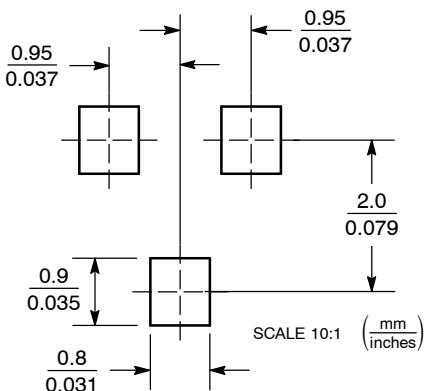


NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.  
 3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.  
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:  
 1. GATE  
 2. SOURCE  
 3. DRAIN

### SOLDERING FOOTPRINT



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