Dual, Low Noise, Wideband Variable Gain Amplifiers

AD600/AD602

FEATURES

2 channels with independent gain control
- **Linear in dB gain response**

2 gain ranges
- **AD600: 0 dB to 40 dB**
- **AD602: −10 dB to +30 dB**

Accurate absolute gain: ±0.3 dB
Low input noise: 1.4 nV/√Hz
Low distortion: −60 dBc THD at ±1 V output
High bandwidth: dc to 35 MHz (−3 dB)
Stable group delay: ±2 ns
Low power: 125 mW (maximum) per amplifier
Signal gating function for each amplifier
Drives high speed ADCs
MIL-STD-883-compliant and DESC versions available

APPLICATIONS

Ultrasound and sonar time-gain controls
High performance audio and RF AGC systems
Signal measurement

GENERAL DESCRIPTION

The AD600/AD602[1] dual channel, low noise, variable gain amplifiers are optimized for use in ultrasound imaging systems but are applicable to any application requiring precise gain, low noise and distortion, and wide bandwidth. Each independent channel provides a gain of 0 dB to +40 dB in the AD600 and −10 dB to +30 dB in the AD602. The lower gain of the AD602 results in an improved signal-to-noise ratio (SNR) at the output. However, both products have the same 1.4 nV/√Hz input noise spectral density. The decibel gain is directly proportional to the control voltage, accurately calibrated, and supply and temperature stable.

To achieve the difficult performance objectives, a proprietary circuit form, the X-AMP®, was developed. Each channel of the X-AMP comprises a variable attenuator of 0 dB to −42.14 dB followed by a high speed fixed gain amplifier. In this way, the amplifier never has to cope with large inputs and can benefit from the use of negative feedback to precisely define the gain and dynamics. The attenuator is realized as a 7-stage R-2R ladder network having an input resistance of 100 Ω, laser trimmed to ±2%. The attenuation between tap points is 6.02 dB; the gain-control circuit provides continuous interpolation between these taps. The resulting control function is linear in dB.

FUNCTIONAL BLOCK DIAGRAM

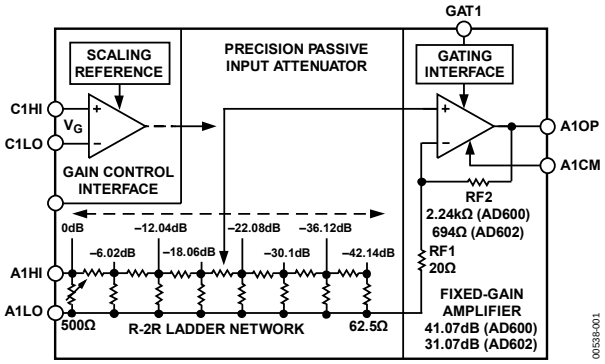

Figure 1.

The gain-control interfaces are fully differential, providing an input resistance of ~15 MΩ and a scale factor of 32 dB/V (that is, 31.25 mV/dB) defined by an internal voltage reference. The response time of this interface is less than 1 µs. Each channel also has an independent gating facility that optionally blocks signal transmission and sets the dc output level to within a few millivolts of the output ground. The gating control input is TTL- and CMOS-compatible.

The maximum gain of the AD600 is 41.07 dB, and the maximum gain of the AD602 is 31.07 dB; the −3 dB bandwidth of both models is nominally 35 MHz, essentially independent of the gain. The SNR for a 1 V rms output and a 1 MHz noise bandwidth is typically 76 dB for the AD600 and 86 dB for the AD602. The amplitude response is flat within ±0.5 dB from 100 kHz to 10 MHz; over this frequency range, the group delay varies by less than ±2 ns at all gain settings.

Each amplifier channel can drive 100 Ω load impedances with low distortion. For example, the peak specified output is ±2.5 V minimum into a 500 Ω load or ±1 V into a 100 Ω load. For a 200 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically −60 dBc.

The AD600J/AD602J are specified for operation from 0°C to 70°C and are available in 16-lead PDIP (N) and 16-lead SOIC_W packages. The AD600A/AD602A are specified for operation from −40°C to +85°C and are available in 16-lead CERDIP (Q) and 16-lead SOIC_W packages. The AD600S/ AD602S are specified for operation from −55°C to +125°C, are available in a 16-lead CERDIP (Q) package, and are MIL-STD-883-compliant. The AD600S/AD602S are also available under DESC SMD 5962-94572.

[1] Patented.

Rev. E
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8/01—Rev. A to Rev. B
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SPECIFICATIONS

Each amplifier section at T_A = 25°C, V_S = ±5 V, −625 mV ≤ V_G ≤ +625 mV, R_L = 500 Ω, and C_L = 5 pF, unless otherwise noted. Specifications for the AD600/AD602 are identical, unless otherwise noted.

Table 1.

		AD600J/AD602J[1]			AD600A/AD602A[1]			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
INPUT CHARACTERISTICS								
Input Resistance	Pin 2 to Pin 3; Pin 6 to Pin 7	**98**	100	**102**	**95**	100	**105**	Ω
Input Capacitance			2			2		pF
Input Noise Spectral Density[2]			1.4			1.4		nV/√Hz
Noise Figure	R_S = 50 Ω, maximum gain		5.3			5.3		dB
	R_S = 200 Ω, maximum gain		2			2		dB
Common-Mode Rejection Ratio	f = 100 kHz		30			30		dB
OUTPUT CHARACTERISTICS								
−3 dB Bandwidth	V_{OUT} = 100 mV rms		35			35		MHz
Slew Rate			275			275		V/µs
Peak Output[3]	R_L ≥ 500 Ω	±2.5	±3		±2.5	±3		V
Output Impedance	f ≤ 10 MHz		2			2		Ω
Output Short-Circuit Current			50			50		mA
Group Delay Change vs. Gain	f = 3 MHz; full gain range		±2			±2		ns
Group Delay Change vs. Frequency	V_G = 0 V, f = 1 MHz to 10 MHz		±2			±2		ns
Total Harmonic Distortion	R_L= 200 Ω, V_{OUT} = ±1 V peak, R_{PD} = 1 kΩ		−60			−60		dBc
ACCURACY								
AD600								
Gain Error	0 dB to 3 dB gain	**0**	+0.5	**+1**	**−0.5**	+0.5	**+1.5**	dB
	3 dB to 37 dB gain	**−0.5**	±0.2	**+0.5**	**−1.0**	±0.2	**+1.0**	dB
	37 dB to 40 dB gain	**−1**	−0.5	**0**	**−1.5**	−0.5	**+0.5**	dB
Maximum Output Offset Voltage[4]	V_G = −625 mV to +625 mV		10	**50**		10	**65**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		10	**50**		10	**65**	mV
AD602								
Gain Error	−10 dB to −7 dB gain	**0**	+0.5	**+1**	**−0.5**	+0.5	**+1.5**	dB
	−7 dB to +27 dB gain	**−0.5**	±0.2	**+0.5**	**−1.0**	±0.2	**+1.0**	dB
	27 dB to 30 dB gain	**−1**	−0.5	**0**	**−1.5**	−0.5	**+0.5**	dB
Maximum Output Offset Voltage[4]	V_G = −625 mV to +625 mV		5	**30**		10	**45**	mV
Output Offset Variation	V_G = −625 mV to +625 mV		5	**30**		10	**45**	mV
GAIN CONTROL INTERFACE								
Gain Scaling Factor	+3 dB to +37 dB (AD600); −7 dB to +27 dB (AD602)	**31.7**	32	**32.3**	**30.5**	32	**33.5**	dB/V
Common-Mode Range		−0.75		+2.5	−0.75		+2.5	V
Input Bias Current			0.35	1		0.35	1	µA
Input Offset Current			10	50		10	50	nA
Differential Input Resistance	Pin 1 to Pin 16; Pin 8 to Pin 9		15			15		MΩ
Response Rate	Full 40 dB gain change		40			40		dB/µs

Parameter	Conditions	AD600J/AD602J[1] Min	Typ	Max	AD600A/AD602A[1] Min	Typ	Max	Unit
SIGNAL GATING INTERFACE								
Logic Input LO (Output On)				0.8			0.8	V
Logic Input HI (Output Off)		2.4			2.4			V
Response Time	On to off, off to on		0.3			0.3		µs
Input Resistance	Pin 4 to Pin 3; Pin 5 to Pin 6		30			30		kΩ
Output Gated Off								
Output Offset Voltage			±10	**±100**		±10	**±400**	mV
Output Noise Spectral Density			65			65		nV/√Hz
Signal Feedthrough @ 1 MHz								
AD600			−80			−80		dB
AD602			−70			−70		dB
POWER SUPPLY								
Specified Operating Range		±4.75		±5.25	±4.75		±5.25	V
Quiescent Current			11	**12.5**		11	**14**	mA

[1] Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All minimum and maximum specifications guaranteed, although only those shown in **boldface** are tested on all production units.
[2] Typical open- or short-circuited input; noise is lower when the system is set to maximum gain and the input is short-circuited. This figure includes the effects of both voltage and current noise sources.
[3] With an additional 1 kΩ pull-down resistor, if R_L < 500 Ω.
[4] The dc gain of the main amplifier in the AD600 is × 113; therefore, an input offset of only 100 µV becomes an 11.3 mV output offset. In the AD602, the amplifier's gain is × 35.7; therefore, an input offset of 100 µV becomes a 3.57 mV output offset.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage $\pm V_S$	±7.5 V
Input Voltages	
Pin 1, Pin 8, Pin 9, Pin 16	$\pm V_S$
Pin 2, Pin 3, Pin 6, Pin 7	±2 V continuous
	$\pm V_S$ for 10 ms
Pin 4, Pin 5	$\pm V_S$
Internal Power Dissipation	600 mW
Operating Temperature Range	
J Grade	0°C to 70°C
A Grade	−40°C to +85°C
S Grade	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C
θ_{JA}	
16-Lead PDIP	85°C/W
16-Lead SOIC_W	100°C/W
16-Lead CERDIP	120°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

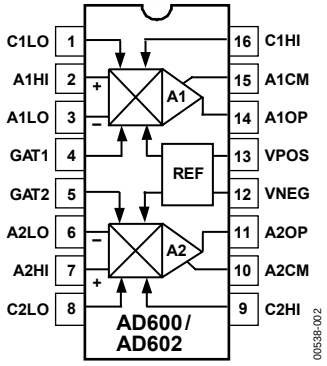


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	C1LO	CH1 Gain-Control Input LO (Positive Voltage Reduces CH1 Gain)
2	A1HI	CH1 Signal Input HI (Positive Voltage Increases CH1 Output)
3	A1LO	CH1 Signal Input LO (Usually Connected to CH1 Input Ground)
4	GAT1	CH1 Gating Input (A Logic HI Shuts Off CH1 Signal Path)
5	GAT2	CH2 Gating Input (A Logic HI Shuts Off CH2 Signal Path)
6	A2LO	CH2 Signal Input LO (Usually Connected to CH2 Input Ground)
7	A2HI	CH2 Signal Input HI (Positive Voltage Increases CH2 Output)
8	C2LO	CH2 Gain-Control Input LO (Positive Voltage Reduces CH2 Gain)
9	C2HI	CH2 Gain-Control Input HI (Positive Voltage Increases CH2 Gain)
10	A2CM	CH2 Common (Usually Connected to CH2 Output Ground)
11	A2OP	CH2 Output
12	VNEG	Negative Supply for Both Amplifiers
13	VPOS	Positive Supply for Both Amplifiers
14	A1OP	CH1 Output
15	A1CM	CH1 Common (Usually Connected to CH1 Output Ground)
16	C1HI	CH1 Gain-Control Input HI (Positive Voltage Increases CH1 Gain)

TYPICAL PERFORMANCE CHARACTERISTICS

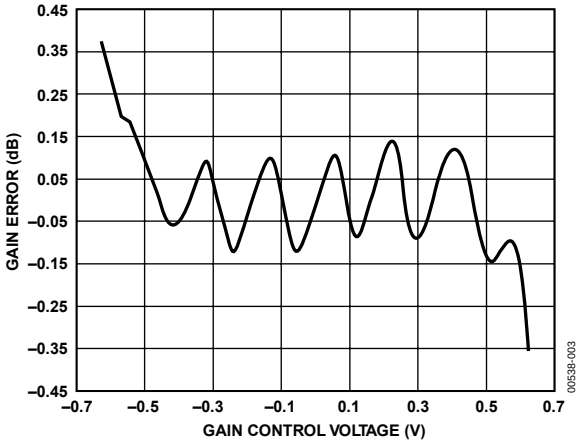


Figure 3. Gain Error vs. Gain Control Voltage

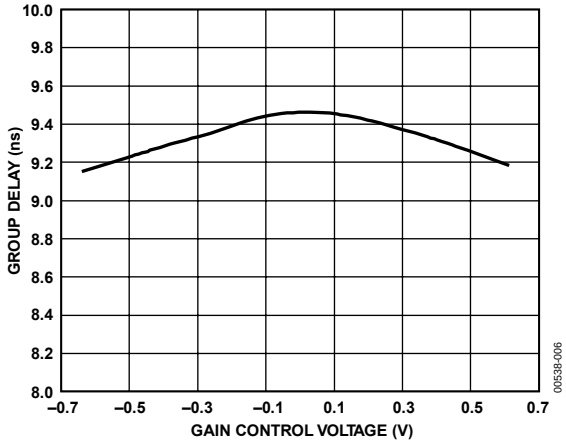


Figure 6. AD600 and AD602 Typical Group Delay vs. V_C

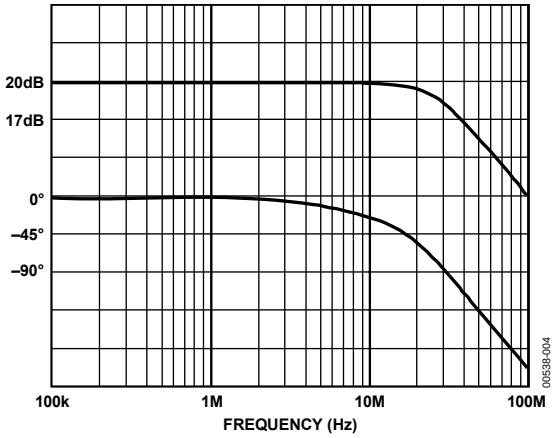


Figure 4. AD600 Frequency and Phase Response vs. Gain

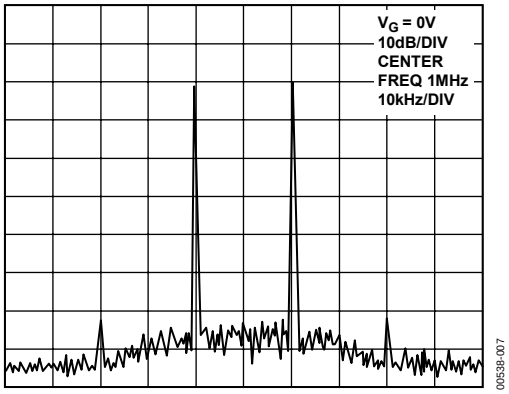


Figure 7. Third-Order Intermodulation Distortion, V_{OUT} = 2 V p-p, R_L = 500 Ω

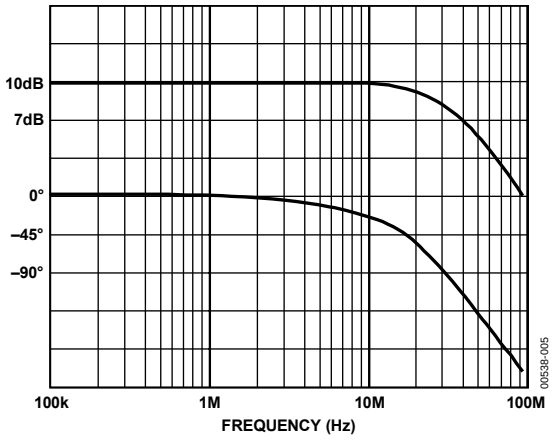


Figure 5. AD602 Frequency and Phase Response vs. Gain

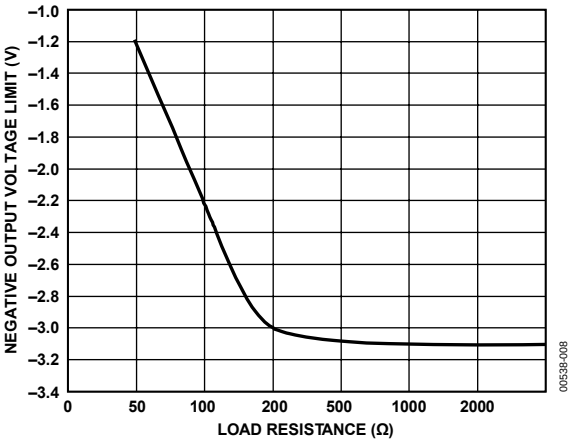


Figure 8. Typical Output Voltage vs. Load Resistance (Negative Output Swing Limits First)

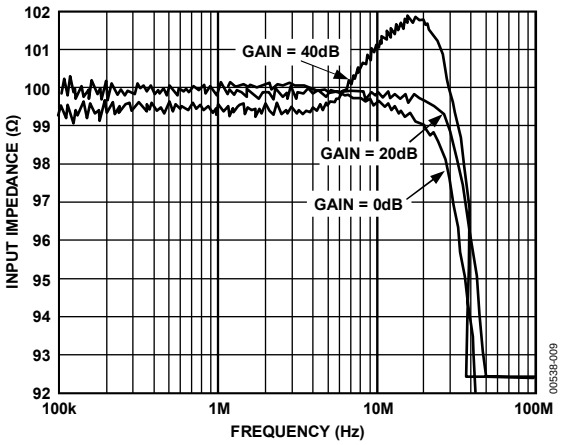


Figure 9. Input Impedance vs. Frequency

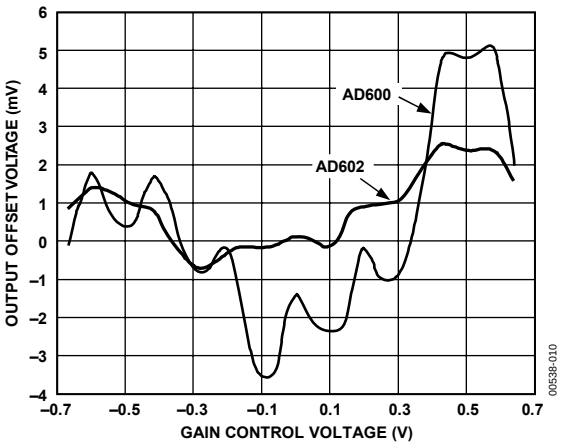


Figure 10. Output Offset Voltage vs. Gain Control Voltage (Control Channel Feedthrough)

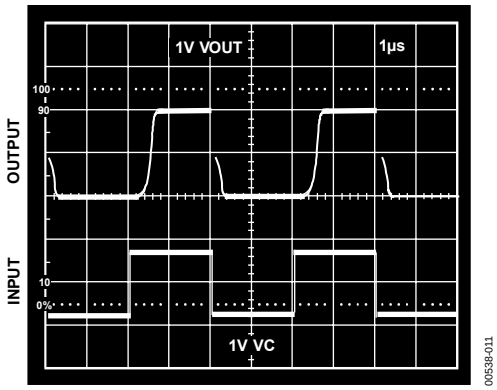


Figure 11. Gain Control Channel Response Time. Top: Output Voltage, 2 V max, Bottom: Gain Control Voltage $V_C = \pm 625$ mV

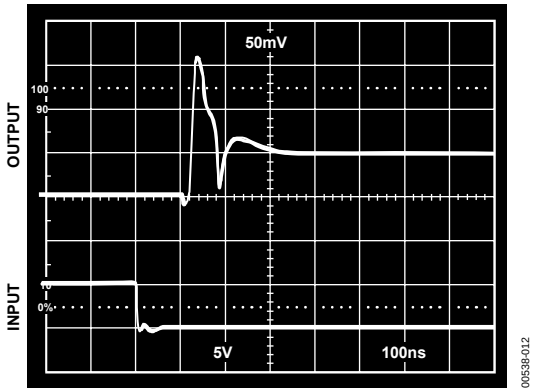


Figure 12. Gating Feedthrough to Output, Gating Off to On

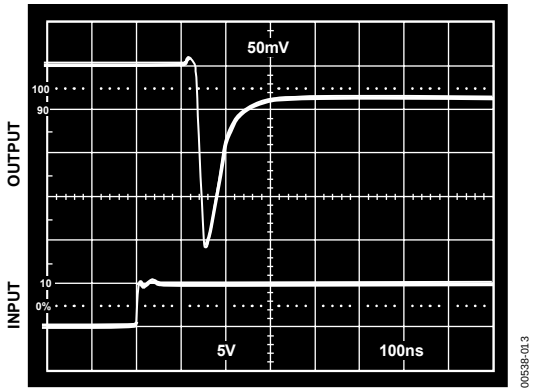


Figure 13. Gating Feedthrough to Output, Gating On to Off

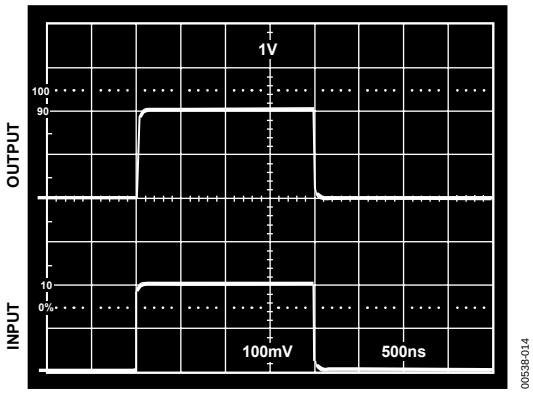


Figure 14. Transient Response, Medium and High Gain

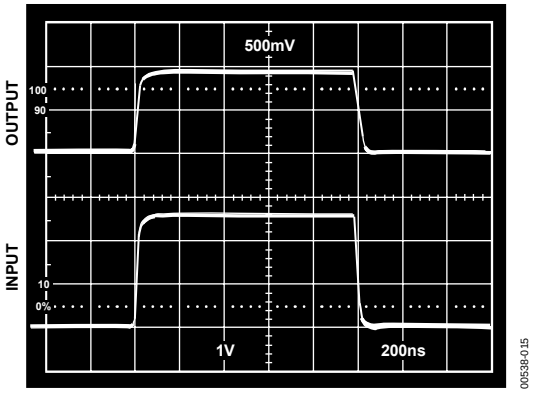


Figure 15. Input Stage Overload Recovery Time

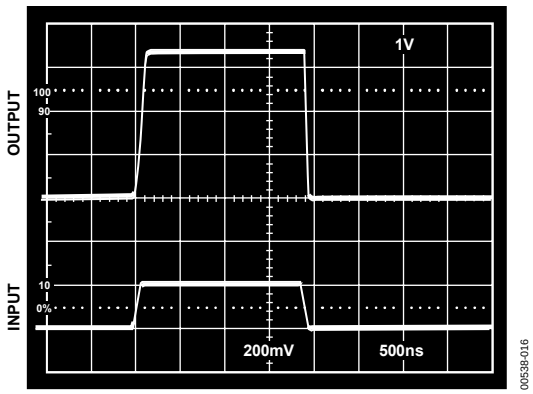


Figure 16. Output Stage Overload Recovery Time

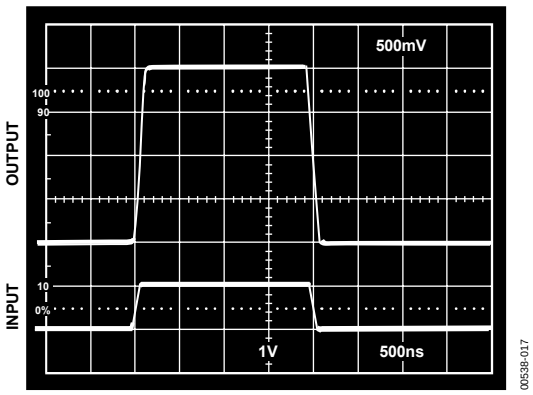


Figure 17. Transient Response Minimum Gain

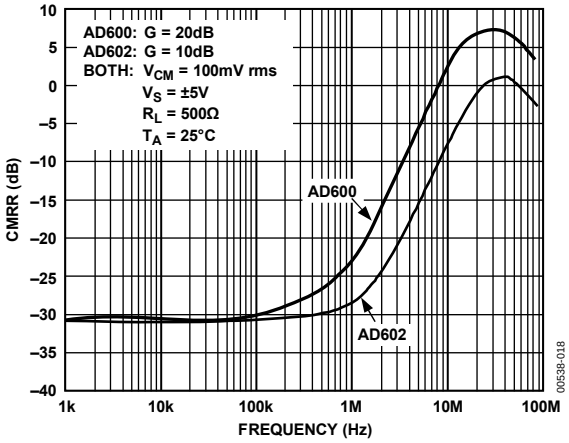


Figure 18. CMRR vs. Frequency

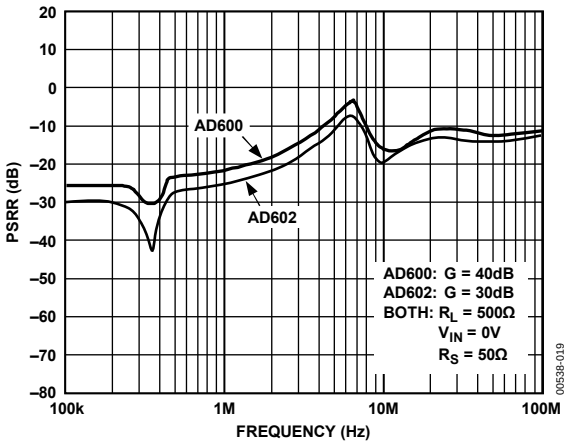


Figure 19. PSRR vs. Frequency

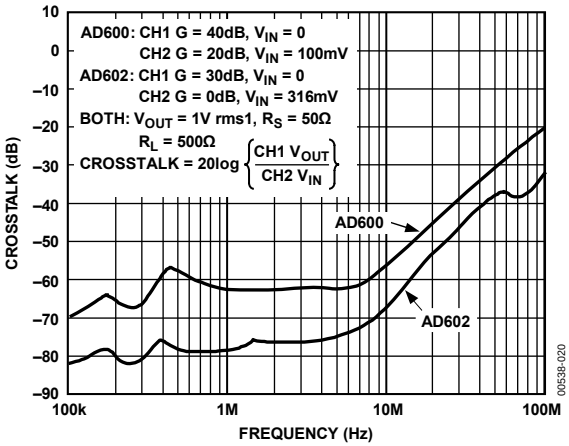


Figure 20. Crosstalk Between A1 and A2 vs. Frequency

THEORY OF OPERATION

The AD600/AD602 have the same general design and features. They comprise two fixed gain amplifiers, each preceded by a voltage-controlled attenuator of 0 dB to 42.14 dB with independent control interfaces, each having a scaling factor of 32 dB per volt. The AD600 amplifiers are laser trimmed to a gain of 41.07 dB (×113), providing a control range of −1.07 dB to +41.07 dB (0 dB to +40 dB with overlap). The AD602 amplifiers have a gain of 31.07 dB (×35.8) and provide an overall gain of −11.07 dB to +31.07 dB (−10 dB to +30 dB with overlap).

The advantage of this topology is that the amplifier can use negative feedback to increase the accuracy of its gain. In addition, because the amplifier does not have to handle large signals at its input, the distortion can be very low. Another feature of this approach is that the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 21 is a simplified schematic of one channel. The input attenuator is a 7-stage R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 2%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

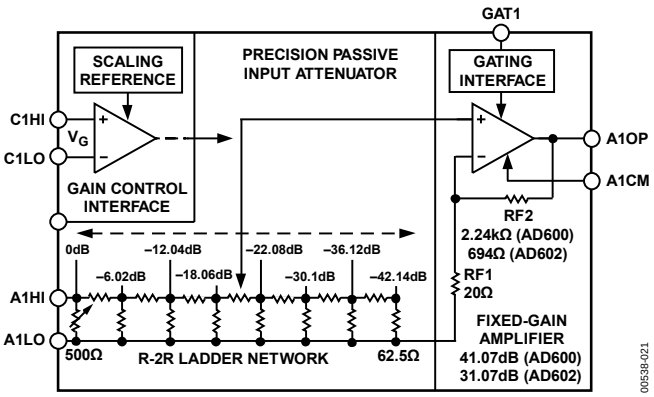


Figure 21. Simplified Block Diagram of Single Channel of the AD600/AD602

The nominal maximum signal at input A1HI is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies; although, operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. Each attenuator is provided with a separate signal LO connection for use in rejecting common mode, the voltage between input and output grounds. Circuitry is included to provide rejection of up to ±100 mV.

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB, and 42.14 dB. A unique circuit technique is employed to interpolate between these tap points, indicated by the slider in Figure 21, providing continuous attenuation from 0 dB to 42.14 dB.

To understand the AD600, it helps to think in terms of a mechanical means for moving this slider from left to right; in fact, it is voltage controlled. The details of the control interface are discussed later. Note that the gain is exactly determined at all times, and a linear decibel relationship is guaranteed automatically between the gain and the control parameter that determines the position of the slider. In practice, the gain deviates from the ideal law by about ±0.2 dB peak (see Figure 28).

Note that the signal inputs are not fully differential. A1LO, A1CM (for CH1), A2LO, and A2CM (for CH2) provide separate access to the input and output grounds. This recognizes that even when using a ground plane, small differences arise in the voltages at these nodes. It is important that A1LO and A2LO be connected directly to the input ground(s). Significant impedance in these connections reduces the gain accuracy. A1CM and A2CM should be connected to the load ground(s).

NOISE PERFORMANCE

An important reason for using this approach is the superior noise performance that can be achieved. The nominal resistance seen at the inner tap points of the attenuator is 41.7 Ω (one third of 125 Ω), which, at 27°C, exhibits a Johnson noise spectral density (NSD) of 0.84 nV/√Hz (that is, √4kTR), a large fraction of the total input noise. The first stage of the amplifier contributes another 1.12 nV/√Hz, for a total input noise of 1.4 nV/√Hz.

The noise at the 0 dB tap depends on whether the input is short-circuited or open-circuited. When shorted, the minimum NSD of 1.12 nV/√Hz is achieved. When open, the resistance of 100 Ω at the first tap generates 1.29 nV/√Hz, so the noise increases to 1.71 nV/√Hz. This last calculation would be important if the AD600 were preceded, for example, by a 900 Ω resistor to allow operation from inputs up to ±10 V rms. However, in most cases, the low impedance of the source limits the maximum noise resistance.

It is apparent from the foregoing that it is essential to use a low resistance in the design of the ladder network to achieve low noise. In some applications, this can be inconvenient, requiring the use of an external buffer or preamplifier. However, very few amplifiers combine the needed low noise with low distortion at maximum input levels, and the power consumption required to achieve this performance is quite high (due to the need to maintain very low resistance values while also coping with large inputs). On the other hand, there is little value in providing a buffer with high input impedance, because the usual reason for this—the minimization of loading of a high resistance source—is not compatible with low noise.

Apart from the small variations just mentioned, the SNR at the output is essentially independent of the attenuator setting, because the maximum undistorted output is 1 V rms and the NSD at the output of the AD600 is fixed at 113 × 114 nV/√Hz, or 158 nV/√Hz. Therefore, in a 1 MHz bandwidth, the output SNR is 76 dB. The input NSD of the AD600/AD602 are the same, but because of the 10 dB lower gain in the AD602's fixed amplifier, its output SNR is 10 dB better, or 86 dB in a 1 MHz bandwidth.

THE GAIN-CONTROL INTERFACE

The attenuation is controlled through a differential, high impedance (15 MΩ) input, with a scaling factor that is laser trimmed to 32 dB per volt, that is, 31.25 mV/dB. Each of the two amplifiers has its own control interface. An internal band gap reference ensures stability of the scaling with respect to supply and temperature variations and is the only circuitry common to both channels.

When the differential input voltage $V_G = 0$ V, the attenuator slider is centered, providing an attenuation of +21.07 dB, resulting in an overall gain of +20 dB (= −21.07 dB + +41.07 dB). When the control input is −625 mV, the gain is lowered by +20 dB (= +0.625 × +32) to 0 dB; when set to +625 mV, the gain is increased by +20 dB to +40 dB. When this interface is overdriven in either direction, the gain approaches either −1.07 dB (= −42.14 dB + +41.07 dB) or +41.07 dB (= 0 + +41.07 dB), respectively.

The gain of the AD600 can be calculated by

$$Gain\ (\text{dB}) = 32\ V_G + 20 \quad (1)$$

where V_G is in volts.

For the AD602, the expression is

$$Gain\ (\text{dB}) = 32\ V_G + 10 \quad (2)$$

Operation is specified for V_G in the range from −625 mV dc to +625 mV dc. The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple-channel applications. The differential input configuration provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, the gain-control input can be fed differentially to the inputs or single-ended by simply grounding the unused input. In another example, if the gain is controlled by a DAC providing a positive-only, ground-referenced output, the gain control LO pin (either C1LO or C2LO) should be biased to a fixed offset of 625 mV to set the gain to 0 dB when gain control HI (C1HI or C2HI) is at zero and to set the gain to 40 dB when at 1.25 V.

It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC with an FS output of 2.55 V (10 mV/bit), a 1.6 divider ratio (generating 6.25 mV/bit) results in a gain setting resolution of 0.2 dB/bit. Later in this data sheet, cascading the two sections of an AD600 or AD602 when various options exist for gain control is explained (see the Achieving 80 DB Gain Range section.)

SIGNAL-GATING INPUTS

Each amplifier section of the AD600/AD602 is equipped with a signal gating function, controlled by a TTL or CMOS logic input (GAT1 or GAT2). The ground references for these inputs are the signal input grounds A1LO and A2LO, respectively. Operation of the channel is unaffected when this input is LO or left open-circuited. Signal transmission is blocked when this input is HI. The dc output level of the channel is set to within a few millivolts of the output ground (A1CM or A2CM) and simultaneously the noise level drops significantly. The reduction in noise and spurious signal feedthrough is useful in ultrasound beam-forming applications, where many amplifier outputs are summed.

COMMON-MODE REJECTION

A special circuit technique provides rejection of voltages appearing between input grounds (A1LO and A2LO) and output grounds (A1CM and A2CM). This is necessary because of the op amp form of the amplifier, as shown in Figure 21. The feedback voltage is developed across the RF1 resistor (which, to achieve low noise, has a value of only 20 Ω). The voltage developed across this resistor is referenced to the input common, so the output voltage is also referred to that node.

For zero differential signal input between A1HI and A1LO, the output A1OP simply follows the voltage at A1CM. Note that the range of voltage differences that can exist between A1LO and A1CM (or A2LO and A2CM) is limited to about ±100 mV. Figure 18 shows the typical common-mode rejection ratio vs. frequency.

ACHIEVING 80 dB GAIN RANGE

The two amplifier sections of the X-AMP can be connected in series to achieve higher gain. In this mode, the output of A1 (A1OP and A1CM) drives the input of A2 via a high-pass network (usually just a capacitor) that rejects the dc offset. The nominal gain range is now −2 dB to +82 dB for the AD600 or −22 dB to +62 dB for the AD602.

There are several options in connecting the gain-control inputs. The choice depends on the desired SNR and gain error (output ripple). The following examples feature the AD600; the arguments generally apply to the AD602, with appropriate changes to the gain values.

SEQUENTIAL MODE (MAXIMUM SNR)

In the sequential mode of operation, the SNR is maintained at its highest level for as much of the gain control range as possible, as shown in Figure 22. Note here that the gain range is 0 dB to 80 dB. Figure 23, Figure 24, and Figure 25 show the general connections to accomplish this. Both gain-control inputs, C1HI and C2HI, are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to 2.5 V.

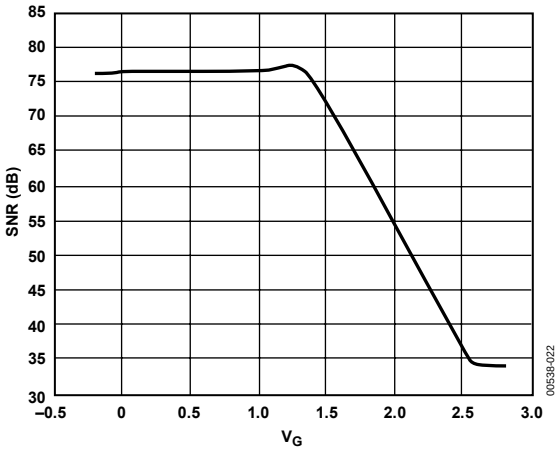


Figure 22. SNR vs. Control Voltage Sequential Control (1 MHz Bandwidth)

An auxiliary amplifier that senses the voltage difference between input and output commons is provided to reject this common voltage.

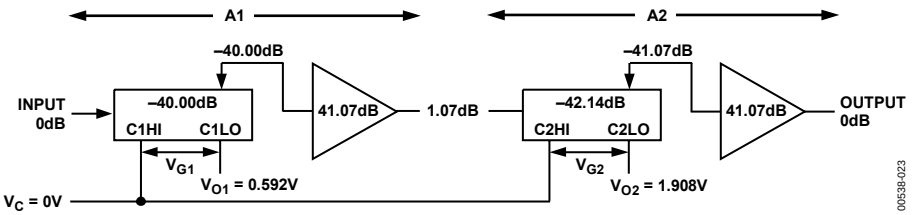


Figure 23. AD600 Gain Control Input Calculations for Sequential Control Operation (A)

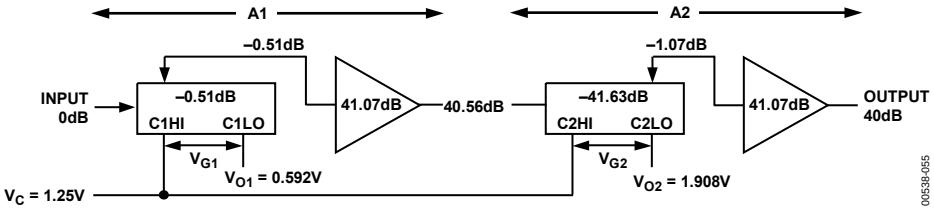


Figure 24. AD600 Gain Control Input Calculations for Sequential Control Operation (B)

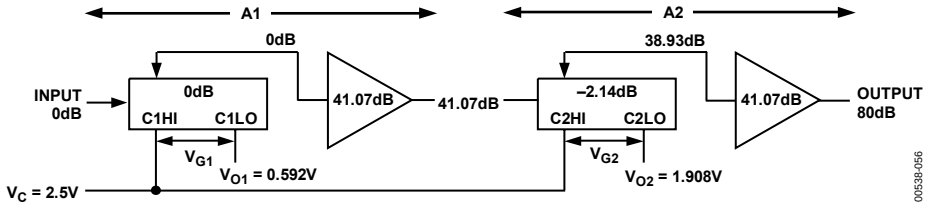


Figure 25. AD600 Gain Control Input Calculations for Sequential Control Operation (C)

The gains are offset such that A2's gain is increased only after A1's gain has reached its maximum value (see Figure 26). Note that for a differential input of −700 mV or less, the gain of a single amplifier (A1 or A2) is at its minimum value of −1.07 dB; for a differential input of +700 mV or more, the gain is at its maximum value of +41.07 dB. Control inputs beyond these limits do not affect the gain and can be tolerated without damage or foldover in the response. See the Specifications section for more details on the allowable voltage range. The gain is now

$$Gain\ (\text{dB}) = 32\ V_C \quad (3)$$

where V_C is the applied control voltage.

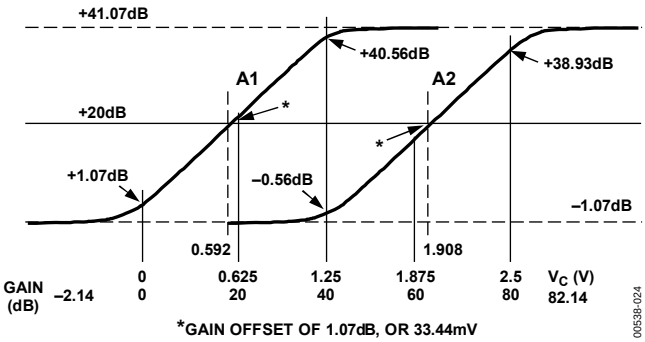


Figure 26. Explanation of Offset Calibration for Sequential Control

When V_C is set to zero, V_{G1} = −0.592 V and the gain of A1 is 1.07 dB (recall that the gain of each amplifier section is 0 dB for V_G = 625 mV); meanwhile, V_{G2} = −1.908 V, so the gain of A2 is −1.07 dB. The overall gain is thus 0 dB (see Figure 23). When V_C = 1.25 V, V_{G1} = 1.25 V − 0.592 V = 0.658 V, which sets the gain of A1 to 40.56 dB, while V_{G2} = 1.25 V − 1.908 V = −0.658 V, which sets A2's gain at −0.56 dB. The overall gain is now 40 dB (see Figure 24). When V_C = 2.5 V, the gain of A1 is 41.07 dB and the gain of A2 is 38.93 dB, resulting in an overall gain of 80 dB (see Figure 25). This mode of operation is further clarified by Figure 27, which is a plot of the separate gains of A1 and A2 and the overall gain vs. the control voltage. Figure 28 is a plot of the gain error of the cascaded amplifiers vs. the control voltage.

PARALLEL MODE (SIMPLEST GAIN-CONTROL INTERFACE)

In this mode, the gain-control voltage is applied to both inputs in parallel—C1HI and C2HI are connected to the control voltage, and C1LO and C2LO are optionally connected to an offset voltage of 0.625 V. The gain scaling is then doubled to 64dB/V, requiring only 1.25 V for an 80 dB change of gain. In this case, the amplitude of the gain ripple is also doubled, as is shown in Figure 29, and the instantaneous SNR at the output of A2 decreases linearly as the gain is increased (see Figure 30).

LOW RIPPLE MODE (MINIMUM GAIN ERROR)

As can be seen in Figure 28 and Figure 29, the output ripple is periodic. By offsetting the gains of A1 and A2 by half the period of the ripple, or 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 31 shows the much lower gain ripple when configured in this manner. Figure 32 plots the SNR as a function of gain; it is very similar to that in the parallel mode.

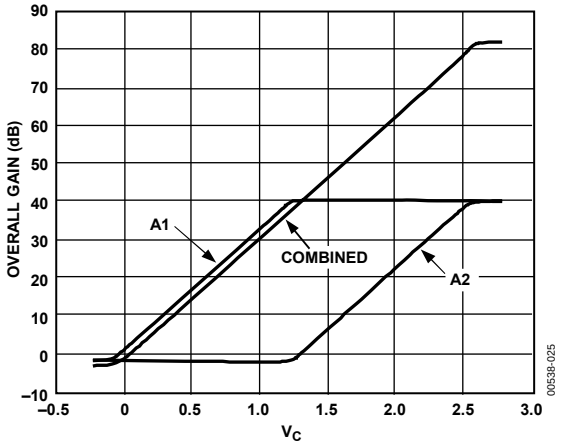


Figure 27. Plot of Separate and Overall Gains in Sequential Control

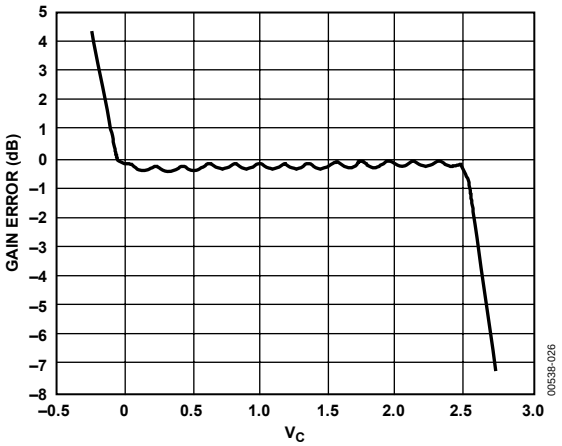


Figure 28. Gain Error for Cascaded Stages—Sequential Control

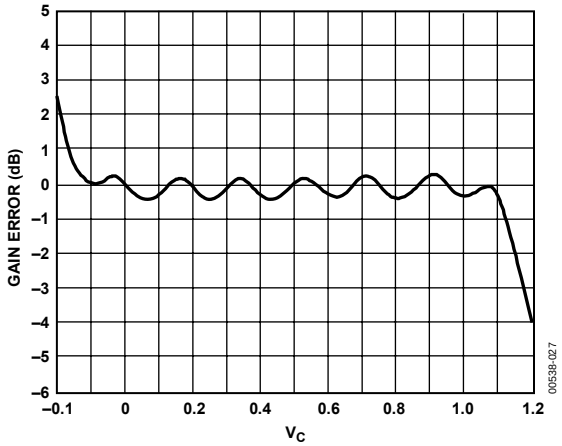


Figure 29. Gain Error for Cascaded Stages—Parallel Control

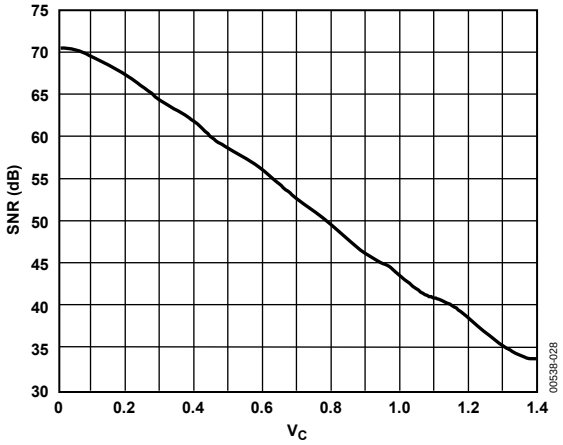


Figure 30. SNR for Cascaded Stages—Parallel Control

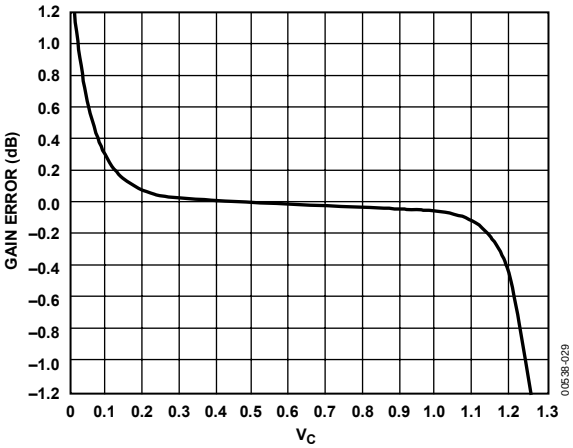


Figure 31. Gain Error for Cascaded Stages—Low Ripple Mode

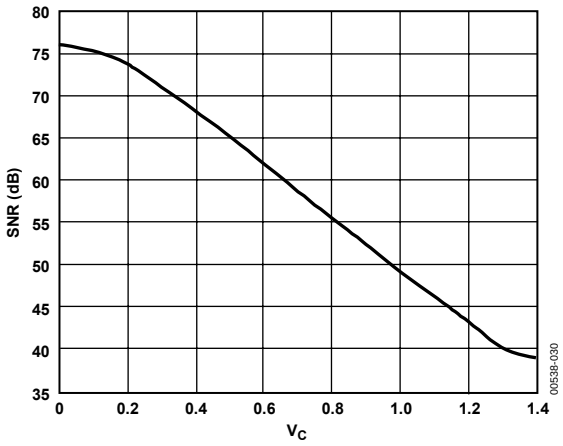


Figure 32. SNR vs. Control Voltage—Low Ripple Mode

APPLICATIONS

The full potential of any high performance amplifier can only be realized by careful attention to details in its applications. The following pages describe fully tested circuits in which many such details have already been considered. However, as is always true of high accuracy, high speed analog circuits, the schematic is only part of the story; this is no less true for the AD600/AD602. Appropriate choices in the overall board layout and the type and placement of power supply decoupling components are very important. As explained previously, the input grounds A1LO and A2LO must use the shortest possible connections.

The following circuits show examples of time-gain control for ultrasound and sonar, methods for increasing the output drive, and AGC amplifiers for audio and RF/IF signal processing using both peak and rms detectors. These circuits also illustrate methods of cascading X-AMPs for either maintaining the optimal SNR or maximizing the accuracy of the gain-control voltage for use in signal measurement. These AGC circuits can be modified for use as voltage-controlled amplifiers in sonar and ultrasound applications by removing the detector and substituting a DAC or other voltage source for supplying the control voltage.

TIME-GAIN CONTROL (TGC) AND TIME-VARIABLE GAIN (TVG)

Ultrasound and sonar systems share a similar requirement: both need to provide an exponential increase in gain in response to a linear control voltage, that is, a gain control that is linear in dB. Figure 33 shows the AD600/AD602 configured for a control voltage ramp starting at −625 mV and ending at +625 mV for a gain-control range of 40 dB. The polarity of the gain-control voltage can be reversed, and the control voltage inputs C1HI and C1LO can be reversed to achieve the same effect. The gain-control voltage can be supplied by a voltage-output DAC, such as the AD7244, which contains two complete DACs, operates from ±5 V supplies, has an internal reference of +3 V, and provides ±3 V of output swing. As such, it is well suited for use with the AD600/AD602, needing only a few resistors to scale the output voltage of the DACs to the levels needed by the AD600/AD602.

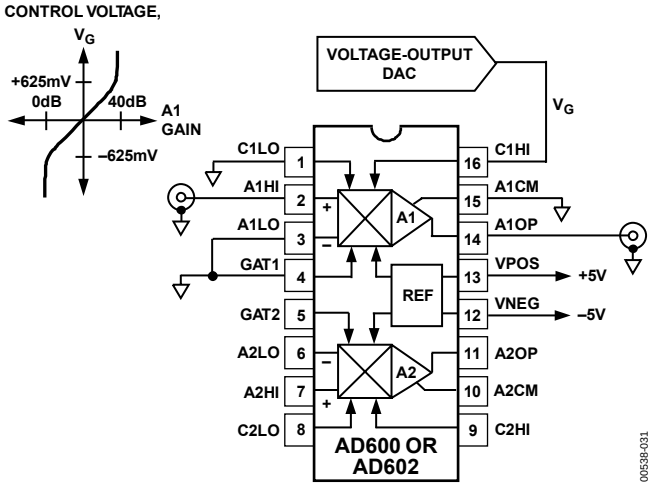


Figure 33. The Simplest Application of the X-AMP Is as a TGC or TVG Amplifier in Ultrasound or Sonar. Only the A1 connections are shown for simplicity.

INCREASING OUTPUT DRIVE

The AD600/AD602's output stage has limited capability for negative-load driving capability. For driving loads less than 500 Ω, the load drive can be increased by approximately 5 mA by connecting a 1 kΩ pull-down resistor from the output to the negative supply (see Figure 34).

DRIVING CAPACITIVE LOADS

For driving capacitive loads of greater than 5 pF, insert a 10 Ω resistor between the output and the load. This lowers the possibility of oscillation.

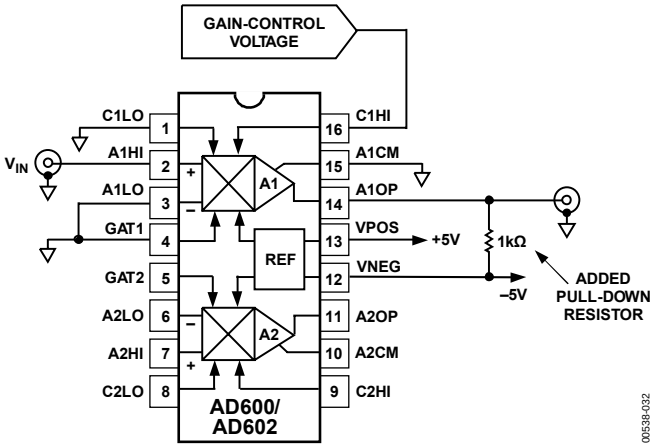


Figure 34. Adding a 1 kΩ Pull-Down Resistor Increases the X-AMP's Output Drive by About 5 mA. Only the A1 connections are shown for simplicity.

REALIZING OTHER GAIN RANGES

Larger gain ranges can be accommodated by cascading amplifiers. Combinations built by cascading two amplifiers include −20 dB to +60 dB (using one AD602), −10 dB to +70 dB (using ½ of an AD602 followed by ½ of an AD600), and 0 dB to 80 dB (using one AD600). In multiple-channel applications, extra protection against oscillation can be provided by using amplifier sections from different packages.

AN ULTRALOW NOISE VCA

The two channels of the AD600 or AD602 can operate in parallel to achieve a 3 dB improvement in noise level, providing 1 nV/√Hz without any loss of gain accuracy or bandwidth.

In the simplest case, as shown in Figure 35, the signal inputs A1HI and A2HI are tied directly together. The outputs A1OP and A2OP are summed via R1 and R2 (100 Ω each), and the control inputs C1HI/C2HI and C1LO/C2LO operate in parallel. Using these connections, both the input and output resistances are 50 Ω. Thus, when driven from a 50 Ω source and terminated in a 50 Ω load, the gain is reduced by 12 dB, so the gain range becomes −12 dB to +28 dB for the AD600 and −22 dB to +18 dB for the AD602. The peak input capability remains unaffected (1 V rms at the IC pins, or 2 V rms from an unloaded 50 Ω source). The loading on each output, with a 50 Ω load, is effectively 200 Ω, because the load current is shared between the two channels, so the overall amplifier still meets its specified maximum output and distortion levels for a 200 Ω load. This amplifier can deliver a maximum sine wave power of 10 dBm to the load.

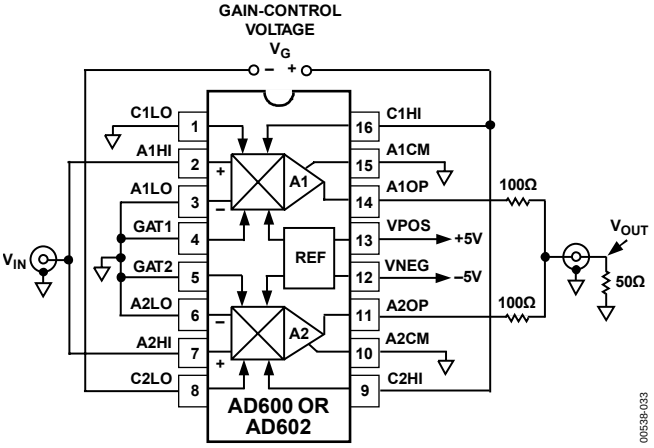


Figure 35. An Ultralow Noise VCA Using the AD600 or AD602

A LOW NOISE, 6 dB PREAMPLIFIER

In some ultrasound applications, a high input impedance preamplifier is needed to avoid the signal attenuation that results from loading the transducer by the 100 Ω input resistance of the X-AMP. High gain cannot be tolerated because the peak transducer signal is typically ±0.5 V, while the peak input capability of the AD600 or AD602 is only slightly more than ±1 V. A gain of 2 is a suitable choice. It can be shown that if the preamplifier's overall referred-to-input (RTI) noise is the same as that due to the X-AMP alone (1.4 nV/√Hz), the input noise of nX2 preamplifier must be √(3/4) times as large, that is, 1.2 nV/√Hz.

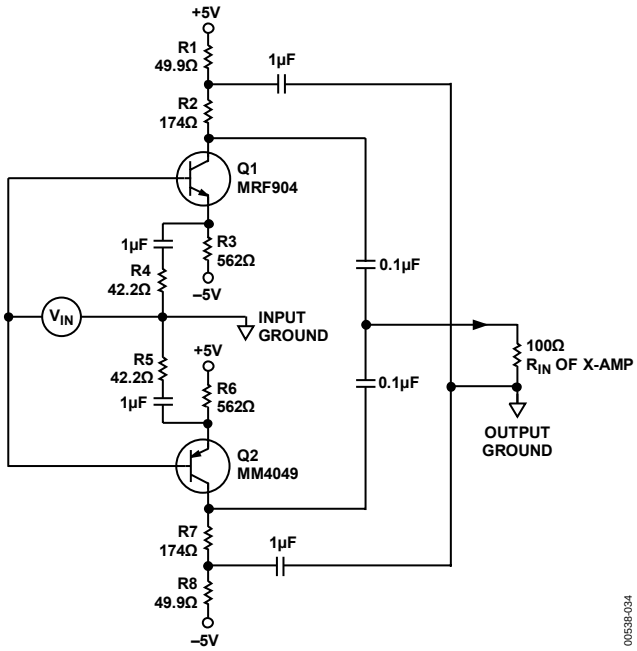


Figure 36. A Low Noise Preamplifier for the AD600/AD602

An inexpensive circuit using complementary transistor types chosen for their low r_{bb} is shown in Figure 36. The gain is determined by the ratio of the net collector load resistance to the net emitter resistance. It is an open-loop amplifier. The gain is ×2 (6 dB) only into a 100 Ω load, assumed to be provided by the input resistance of the X-AMP; R2 and R7 are in shunt with this load, and their value is important in defining the gain. For small-signal inputs, both transistors contribute an equal transconductance that is rendered less sensitive to signal level by the emitter resistors, R4 and R5. They also play a dominant role in setting the gain.

This is a Class AB amplifier. As V_{IN} increases in a positive direction, Q1 conducts more heavily and its r_e becomes lower while Q2 increases. Conversely, increasingly negative values of V_{IN} result in the r_e of Q2 decreasing, while the r_e of Q1 increases. The design is chosen such that the net emitter resistance is essentially independent of the instantaneous value of V_{IN}, resulting in moderately low distortion. Low values of resistance and moderately high bias currents are important in achieving the low noise, wide bandwidth, and low distortion of this preamplifier. Heavy decoupling prevents noise on the power supply lines from being conveyed to the input of the X-AMP.

Table 4. Measured Preamplifier Performance

Measurement		Value	Unit
Gain (f = 30 MHz)		6	dB
Bandwidth (−3 dB)		250	MHz
Input Signal for 1 dB Compression		1	V p-p
Distortion			
V_{IN} = 200 mV p-p	HD2	0.27	%
	HD3	0.14	%
V_{IN} = 500 mV p-p	HD2	0.44	%
	HD3	0.58	%
System Input Noise Spectral Density (NSD) (Preamp plus X-AMP)		1.03	nV/√Hz
Input Resistance		1.4	kΩ
Input Capacitance		15	pF
Input Bias Current		±150	µA
Power Supply Voltage		±5	V
Quiescent Current		15	mA

A LOW NOISE AGC AMPLIFIER WITH 80 dB GAIN RANGE

Figure 37 provides an example of the ease with which the AD600 can be connected as an AGC amplifier. A1 and A2 are cascaded, with 6 dB of attenuation introduced by the 100 Ω resistor R1, while a time constant of 5 ns is formed by C1 and the 50 Ω of net resistance at the input of A2. This has the dual effect of lowering the overall gain range from 0 dB to 80 dB to −6 dB to 74 dB and introducing a single-pole, low-pass filter with a −3 dB frequency of about 32 MHz. This ensures stability at the maximum gain for a slight reduction in the overall bandwidth. The Capacitor C4 blocks the small dc offset voltage at the output of A1 (which may otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 8 kHz, useful in eliminating low frequency noise and spurious signals that can be present at the input.

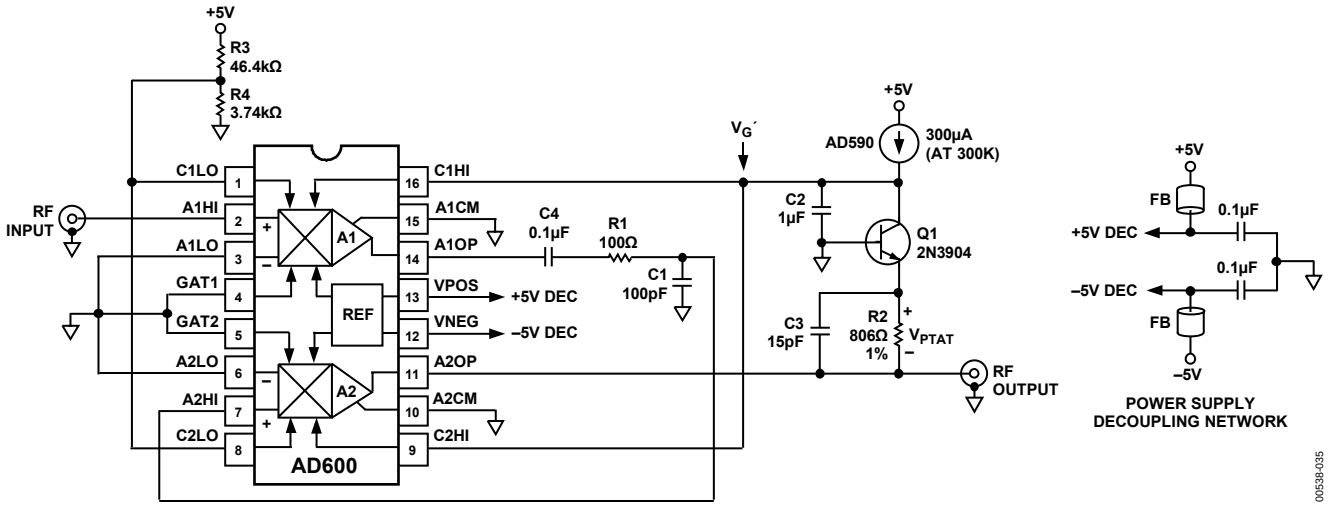


Figure 37. This Accurate HF AGC Amplifier Uses Three Active Components

A simple half-wave detector is used based on Q1 and R2. The average current into Capacitor C2 is the difference between the current provided by the AD590 (300 µA at 300 K, 27°C) and the collector current of Q1. In turn, the control voltage V_G is the time integral of this error current. When V_G (thus the gain) is stable, the rectified current in Q1 must, on average, balance exactly the current in the AD590. If the output of A2 is too small to do this, V_G ramps up, causing the gain to increase until Q1 conducts sufficiently. The operation of this control system follows.

First, consider the particular case where R2 is zero and the output voltage V_{OUT} is a square wave at, for example, 100 kHz, well above the corner frequency of the control loop. During the time V_{OUT} is negative, Q1 conducts. When V_{OUT} is positive, it is cut off. Since the average collector current is forced to be 300 µA and the square wave has a 50% duty-cycle, the current when conducting must be 600 µA. With R2 omitted, the peak value of V_{OUT} would be just the V_{BE} of Q1 at 600 µA (typically about 700 mV) or 2 V_{BE} p-p. This voltage, thus the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. While this may not be troublesome in some applications, the correct value of R2 renders the output stable with temperature.

To understand this, first note that the current in the AD590 is closely proportional to absolute temperature (PTAT). In fact, this IC is intended for use as a thermometer. For the moment, assume that the signal is a square wave. When Q1 is conducting, V_{OUT} is the sum of V_{BE}. V_{OUT} is also a voltage that is PTAT and that can be chosen to have a TC equal but opposite to the TC of the base-to-emitter voltage. This is actually nothing more than the band gap voltage reference principle in thinly veiled disguise. When R2 is chosen so that the sum of the voltage across it and the V_{BE} of Q1 is close to the band gap voltage of about 1.2 V, V_{OUT} is stable over a wide range of temperatures, provided Q1 and the AD590 share the same thermal environment.

Since the average emitter current is 600 µA during each half-cycle of the square wave, a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value of R2 depends on the transistor used and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the devices shown and sine wave signals, the recommended value is 806 Ω. This resistor also serves to lower the peak current in Q1 and the 200 Hz LP filter it forms with C2 helps to minimize distortion due to ripple in V_G. Note that the output amplitude under sine wave conditions is higher than for a square wave because the average value of the current for an ideal rectifier would be 0.637 times as large, causing the output amplitude to be 1.88 V (= 1.2/0.637), or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.275 V rms.

An offset of 375 mV is applied to the inverting gain-control inputs C1LO and C2LO. Therefore, the nominal –625 mV to +625 mV range for V_G is translated upwards (at V_G') to –0.25 V for minimum gain to +1 V for maximum gain. This prevents Q1 from going into heavy saturation at low gains and leaves sufficient headroom of 4 V for the AD590 to operate correctly at high gains when using a 5 V supply.

In fact, the 6 dB interstage attenuator means that the overall gain of this AGC system actually runs from –6 dB to +74 dB. Thus, an input of 2 V rms would be required to produce a 1 V rms output at the minimum gain, which exceeds the 1 V rms maximum input specification of the AD600. The available gain range is therefore 0 dB to 74 dB (or X1 to X5000). Since the gain scaling is 15.625 mV/dB (because of the cascaded stages), the minimum value of V_G' is actually increased by 6 × +15.625 mV, or about 94 mV, to –156 mV, so the risk of saturation in Q1 is reduced.

The emitter circuit of Q1 is somewhat inductive (due its finite f_t and base resistance). Consequently, the effective value of R2 increases with frequency. This results in an increase in the stabilized output amplitude at high frequencies, but for the addition of C3, determined experimentally to be 15 pF for the 2N3904 for maximum response flatness. Alternatively, a faster transistor can be used here to reduce HF peaking. Figure 38 shows the ac response at the stabilized output level of about 1.3 rms. Figure 39 demonstrates the output stabilization for the sine wave inputs of 1 mV to 1 V rms at frequencies of 100 kHz, 1 MHz, and 10 MHz.

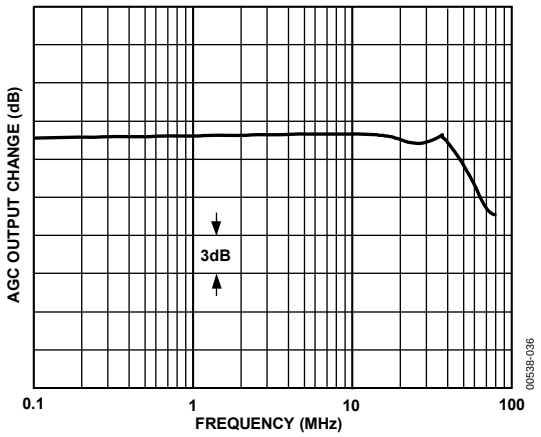


Figure 38. AC Response at the Stabilized Output Level of 1.3 V rms

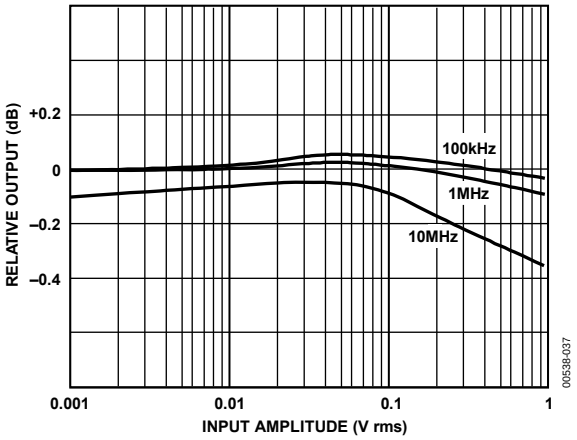


Figure 39. Output Stabilization vs. rms Input for Sine Wave Inputs at 100 kHz, 1 MHz, and 10 MHz

While the band gap principle used here sets the output amplitude to 1.2 V (for the square wave case), the stabilization point can be set to any higher amplitude, up to the maximum output of ±(V_S – 2) V that the AD600 can support. It is only necessary to split R2 into two components of appropriate ratio whose parallel sum remains close to the zero-TC value of 806 Ω. Figure 40 shows this and how the output can be raised without altering the temperature stability.

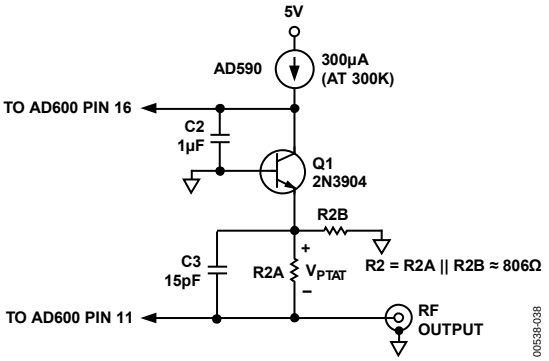


Figure 40. Modification in Detector to Raise Output to 2 V rms

A WIDE RANGE, RMS-LINEAR dB MEASUREMENT SYSTEM (2 MHz AGC AMPLIFIER WITH RMS DETECTOR)

Monolithic rms-dc converters provide an inexpensive means to measure the rms value of a signal of arbitrary waveform; they can also provide a low accuracy logarithmic (decibel-scaled) output. However, they have certain shortcomings. The first of these is their restricted dynamic range, typically only 50 dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3 dB bandwidth of 900 kHz for an input of 100 mV rms but has a bandwidth of only 100 kHz for a 10 mV rms input. Its logarithmic output is unbuffered, uncalibrated, and not stable over temperature. Considerable support circuitry, including at least two adjustments and a special high TC resistor, is required to provide a useful output.

These problems can be eliminated using an AD636 as the detector element in an AGC loop, in which the difference between the rms output of the amplifier and a fixed dc reference are nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the rms-dc converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal dependent. If the amplifier has an exactly exponential (linear-dB) gain-control law, its control voltage V_G is forced by the AGC loop to have the general form

$$V_{OUT} = V_{SCALE} \log 10 \frac{V_{IN(RMS)}}{V_{REF}} \quad (4)$$

Figure 41 shows a practical wide dynamic range rms-responding measurement system using the AD600. Note that the signal output of this system is available at A2OP, and the circuit can be used as a wideband AGC amplifier with an rms-responding detector. This circuit can handle inputs from 100 µV to 1 V rms with a constant measurement bandwidth of 20 Hz to 2 MHz, limited primarily by the AD636 rms converter. Its logarithmic output is a loadable voltage accurately calibrated to 100 mV/dB or 2 V per decade, which simplifies the interpretation of the reading when using a DVM and is arranged to be –4 V for an input of 100 µV rms input, zero for 10 mV, and +4 V for a 1 V rms input. In terms of Equation 4, V_{REF} is 10 mV and V_{SCALE} is 2 V.

Note that the peak log output of ±4 V requires the use of ±6 V supplies for the dual op amp U3 (AD712) although lower supplies would suffice for the AD600 and AD636. If only ±5 V supplies are available, it is necessary to either use a reduced value for V_{SCALE} (say 1 V, in which case the peak output would be only ±2 V) or restrict the dynamic range of the signal to about 60 dB.

As in the previous case, the two amplifiers of the AD600 are used in cascade. However, the 6 dB attenuator and low-pass filter found in Figure 21 are replaced by a unity gain buffer amplifier U3A, whose 4 MHz bandwidth eliminates the risk of instability at the highest gains. The buffer also allows the use of a high impedance coupling network (C1/R3) that introduces a high-pass corner at about 12 Hz. An input attenuator of 10 dB (X0.316) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 Ω. The adjustment provides exact calibration of the logarithmic intercept V_{REF} in critical applications, but R1 and R2 can be replaced by a fixed resistor of 215 Ω if very close calibration is not needed, because the input resistance of the AD600 (and all other key parameters of it and the AD636) is already laser trimmed for accurate operation. This attenuator allows inputs as large as ±4 V to be accepted, that is, signals with an rms value of 1 V combined with a crest factor of up to 4.

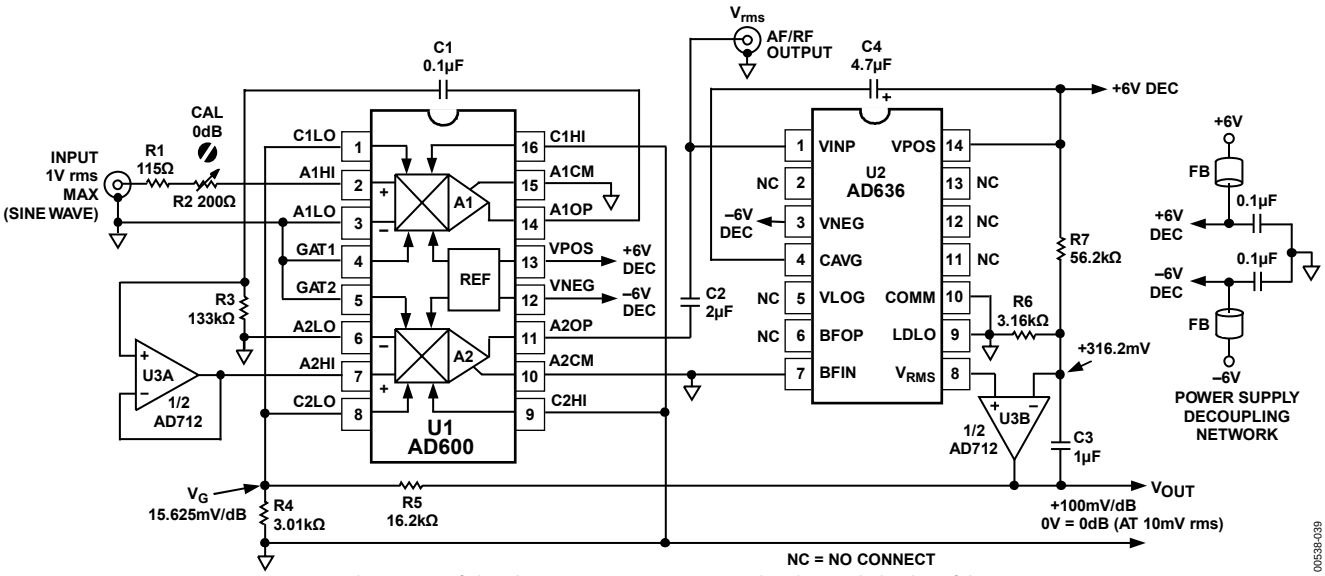


Figure 41. The Output of This Three-IC Circuit Is Proportional to the Decibel Value of the rms Input

The output of A2 is ac-coupled via another 12 Hz high-pass filter formed by C2 and the 6.7 kΩ input resistance of the AD636. The averaging time constant for the rms-dc converter is determined by C4. The unbuffered output of the AD636 (at Pin 8) is compared with a fixed voltage of 316 mV set by the positive supply voltage of 6 V and Resistors R6 and R7. V_{REF} is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply dependent reference with a more stable source.

Any difference in these voltages is integrated by the op amp U3B, with a time constant of 3 ms formed by the parallel sum of R6/R7 and C3. Now, if the output of the AD600 is too high, V rms is greater than the setpoint of 316 mV, causing the output of U3B—that is, V_{OUT}—to ramp up (note that the integrator is noninverting). A fraction of V_{OUT} is connected to the inverting gain-control inputs of the AD600, so causing the gain to be reduced, as required, until V rms is exactly equal to 316 mV, at which time the ac voltage at the output of A2 is forced to be exactly 316 mV rms. This fraction is set by R4 and R5 such that a 15.625 mV change in the control voltages of A1 and A2—which would change the gain of the cascaded amplifiers by 1 dB—requires a change of 100 mV at V_{OUT}. Notice here that since A2 is forced to operate at an output level well below its capacity, waveforms of high crest factor can be tolerated throughout the amplifier.

To check the operation, assume an input of 10 mV rms is applied to the input, which results in a voltage of 3.16 mV rms at the input to A1, due to the 10 dB loss in the attenuator. If the system operates as claimed, V_{OUT} (and hence V_G) should be 0. This being the case, the gain of both A1 and A2 is 20 dB and the output of the AD600 is therefore 100 times (40 dB) greater than its input, which evaluates to 316 mV rms, the input required at the AD636 to balance the loop. Finally, note that unlike most AGC circuits that need strong temperature compensation for the internal kT/q scaling, these voltages, and thus the output of this measurement system, are temperature stable, arising directly from the fundamental and exact exponential attenuation of the ladder networks in the AD600.

Typical results are presented for a sine wave input at 100 kHz. Figure 42 shows that the output is held close to the setpoint of 316 mV rms over an input range in excess of 80 dB.

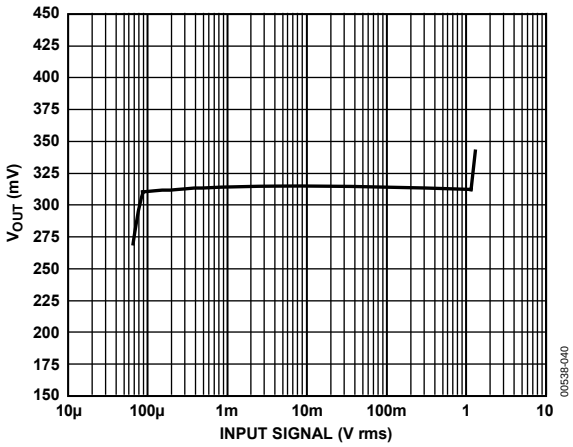


Figure 42. RMS Output of A2 Held Close to the Setpoint 316 mV for an Input Range of over 80 dB

This system can, of course, be used as an AGC amplifier in which the rms value of the input is leveled. Figure 43 shows the decibel output voltage. More revealing is Figure 44, which shows that the deviation from the ideal output predicted by Equation 1 over the input range 80 μV to 500 mV rms is within ±0.5 dB, and within ±1 dB for the 80 dB range from 80 μV to 800 mV. By suitable choice of the input attenuator R1 + R2, this can be centered to cover any range from a low of 25 mV to 250 mV to a high of 1 mV to 10 V, with appropriate correction to the value of V_{REF}. Note that V_{SCALE} is not affected by the changes in the range. The gain ripple of ±0.2 dB seen in this curve is the result of the finite interpolation error of the X-AMP. Note that it occurs with a periodicity of 12 dB, twice the separation between the tap points (because of the two cascaded stages).

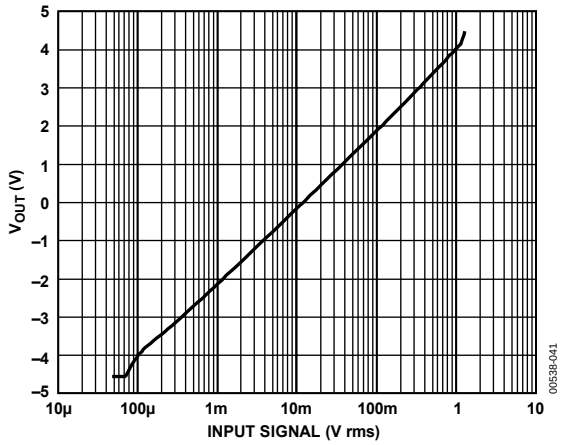


Figure 43. The dB Output of Figure 41's Circuit is Linear over an 80 dB Range

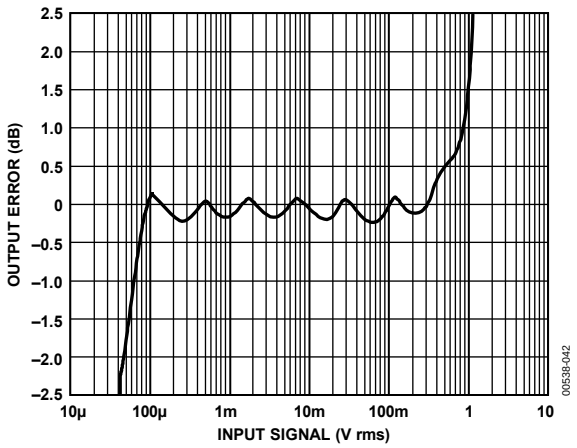


Figure 44. Data from Figure 42 Presented as the Deviation from the Ideal Output Given in Equation 4

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a 3 dB offset between the two pairs of control voltages. A simple means to achieve this is shown in Figure 45: the voltages at C1HI and C2HI are split by ±46.875 mV, or ±1.5 dB. Alternatively, either one of these pins can be individually offset by 3 dB and a 1.5 dB gain adjustment made at the input attenuator (R1 + R2).

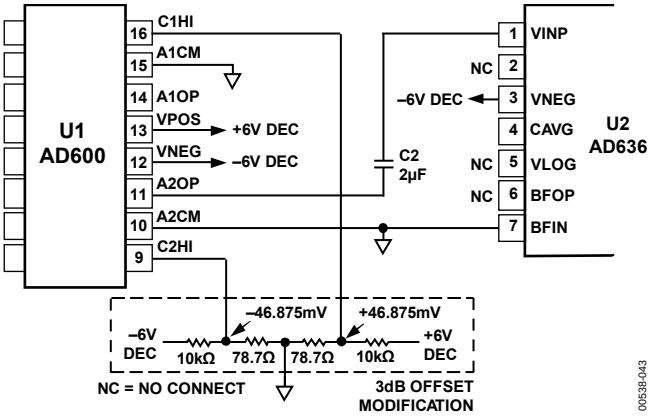


Figure 45. Reducing the Gain Error Ripple

The error curve shown in Figure 46 demonstrates that over the central portion of the range the output voltage can be maintained close to the ideal value. The penalty for this modification is the higher errors at the extremities of the range. The next two applications show how three amplifier sections can be cascaded to extend the nominal conversion range to 120 dB, with the inclusion of simple LP filters of the type shown in Figure 37. Very low errors can then be maintained over a 100 dB range.

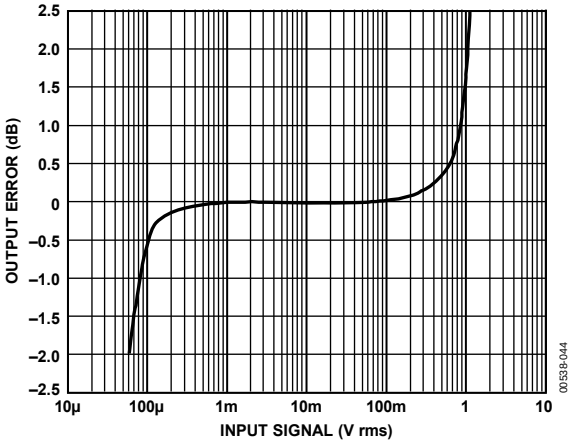


Figure 46. Using a 3 dB Offset Network Reduces Ripple

100 dB TO 120 dB RMS RESPONDING CONSTANT BANDWIDTH AGC SYSTEMS WITH HIGH ACCURACY dB OUTPUTS

The next two applications double as both AGC amplifiers and measurement systems. In both, precise gain offsets are used to achieve either a high gain linearity of ±0.1 dB over the full 100 dB range or the optimal SNR at any gain.

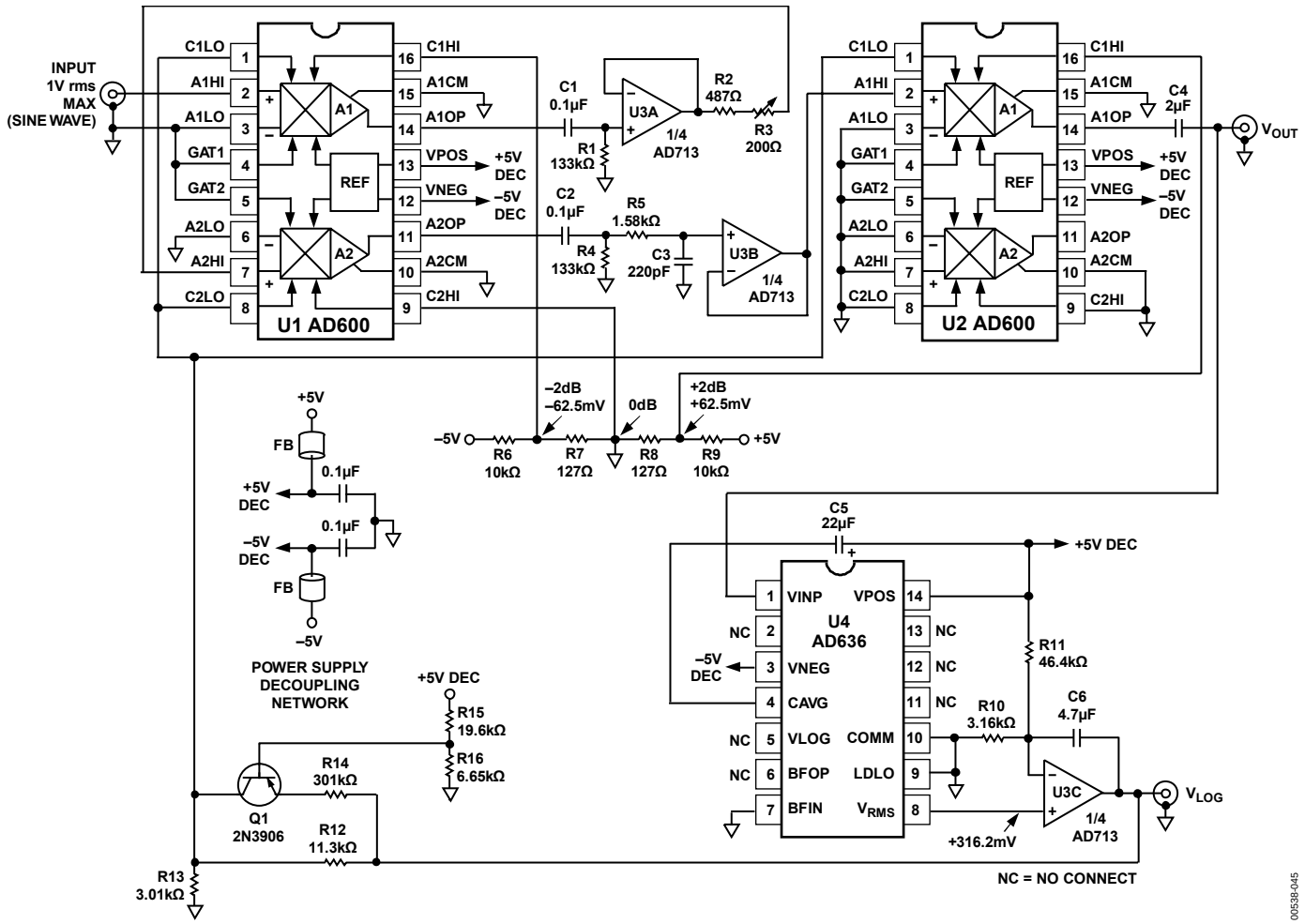


Figure 47. RMS Responding AGC Circuit with 100 dB Dynamic Range

A 100 dB RMS/AGC SYSTEM WITH MINIMAL GAIN ERROR (PARALLEL GAIN WITH OFFSET)

Figure 47 shows an rms-responding AGC circuit that can be used equally well as an accurate measurement system. It accepts inputs of 10 µV to 1 V rms (−100 dBV to 0 dBV) with generous overrange. Figure 48 shows the logarithmic output, V_{LOG}, which is accurately scaled 1 V per decade, that is, 50 mV/dB, with an intercept (V_{LOG} = 0) at 3.16 mV rms (−50 dBV). Gain offsets of ±2 dB were introduced between the amplifiers, provided by the ±62.5 mV introduced by R6 to R9. These offsets cancel a small gain ripple that arises in the X-AMP from its finite interpolation error, which has a period of 18 dB in the individual VCA sections. The gain ripple of all three amplifier sections without this offset (in which case, the gain errors simply add) is shown in Figure 49; it is still a remarkably low ±0.25 dB over the 108 dB range from 6 µV to 1.5 V rms. However, with the gain offsets connected, the gain linearity remains under ±0.1 dB over the specified 100 dB range (see Figure 50).

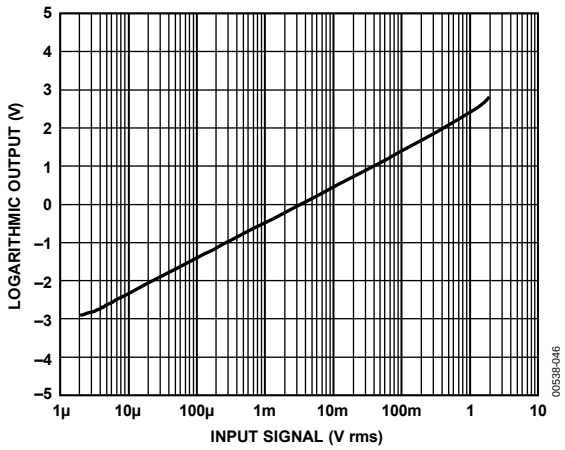


Figure 48. V_{LOG} Plotted vs. V_{IN} for Figure 47's Circuit Showing 120 dB AGC Range

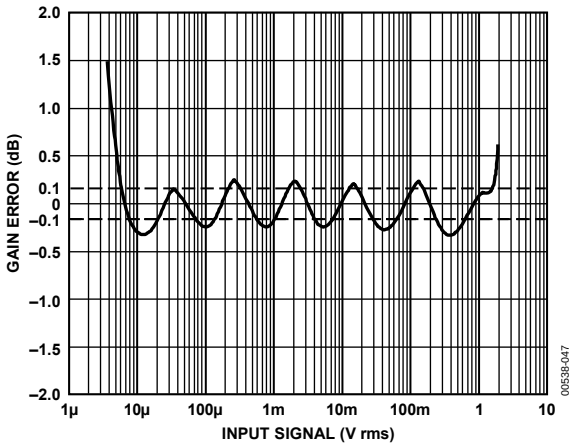


Figure 49. Gain Error for Figure 41 Without the 2 dB Offset Modification

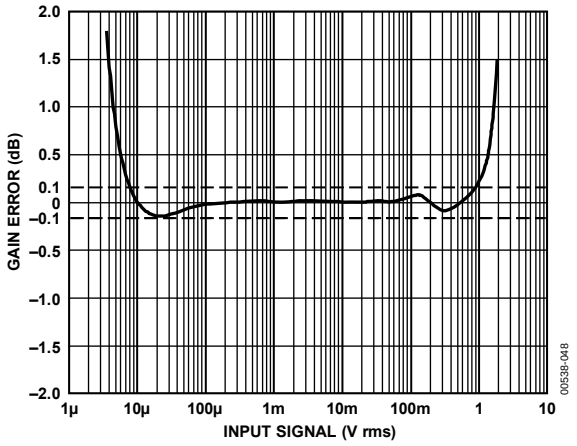


Figure 50. Adding the 2 dB Offsets Improves the Linearization

The maximum gain of this circuit is 120 dB. If no filtering was used, the noise spectral density of the AD600 (1.4 nV/√Hz) would amount to an input noise of 8.28 µV rms in the full bandwidth (35 MHz). At a gain of one million, the output noise would dominate. Consequently, some reduction of bandwidth is mandatory, and in the circuit of Figure 47, it is due mostly to a single-pole, low-pass filter R5/C3, which provides a –3 dB frequency of 458 kHz, which reduces the worst-case output noise (at V_{AGC}) to about 100 mV rms at a gain of 100 dB. Of course, the bandwidth (and therefore the output noise) could be further reduced, for example, in audio applications, merely by increasing C3. The value chosen for this application is optimal in minimizing the error in the V_{LOG} output for small input signals.

The AD600 is dc-coupled, but even miniscule offset voltages at the input would overload the output at high gains; thus, high-pass filtering is also needed. To provide operation at low frequencies, two simple 0s at about 12 Hz are provided by R1/C1 and R4/C2; op amp sections U3A and U3B (AD713) are used to provide impedance buffering, because the input resistance of the AD600 is only 100 Ω. A further 0 at 12 Hz is provided by C4 and the 6.7 kΩ input resistance of the AD636 rms converter.

The rms value of V_{LOG} is generated at Pin 8 of the AD636; the averaging time for this process is determined by C5, and the value shown results in less than 1% rms error at 20 Hz. The slowly varying V rms is compared with a fixed reference of 316 mV, derived from the positive supply by R10/R11. Any difference between these two voltages is integrated in C6, in conjunction with Op Amp U3C, the output of which is V_{LOG}. A fraction of this voltage, determined by R12 and R13, is returned to the gain control inputs of all AD600 sections. An increase in V_{LOG} lowers the gain because this voltage is connected to the inverting polarity control inputs.

In this case, the gains of all three VCA sections are being varied simultaneously, so the scaling is not 32 dB/V but 96 dB/V or 10.42 mV/dB. The fraction of V_{LOG} required to set its scaling to 50 mV/dB is therefore 10.42/50 or 0.208. The resulting full-scale range of V_{LOG} is nominally ±2.5 V. This scaling allows the circuit to operate from ±5 V supplies.

Optionally, the scaling can be altered to 100 mV/dB, which would be more easily interpreted when V_{LOG} is displayed on a DVM by increasing R12 to 25.5 kΩ. The full-scale output of ±5 V then requires the use of supply voltages of at least ±7.5 V.

A simple attenuator of 16.6 ± 1.25 dB is formed by R2/R3 and the 100 Ω input resistance of the AD600. This allows the reference level of the decibel output to be precisely set to 0 for an input of 3.16 mV rms, and thus center the 100 dB range between 10 µV and 1 V. In many applications, R2/R3 can be replaced by a fixed resistor of 590 Ω. For example, in AGC applications, neither the slope nor the intercept of the logarithmic output is important.

A few additional components (R14 to R16 and Q1) improve the accuracy of V_{LOG} at the top end of the signal range (that is, for small gains). The gain starts rolling off when the input to the first amplifier, U1A, reaches 0 dB. To compensate for this nonlinearity, Q1 turns on at V_{LOG} ~ 1.5 V and increases the feedback to the control inputs of the AD600s, thereby needing a smaller voltage at V_{LOG} to maintain the input to the AD636 to the setpoint of 316 mV rms.

A 120 dB RMS/AGC SYSTEM WITH OPTIMAL SNR (SEQUENTIAL GAIN)

In the last case, all gains were adjusted simultaneously, resulting in an output SNR that is always less than optimal. The use of sequential gain control results in a major improvement in SNR, with only a slight penalty in the accuracy of V_{LOG}, and no penalty in the stabilization accuracy of V_{AGC}. The idea is to increase the gain of the earlier stages first (as the signal level decreases) and maintain the highest SNR throughout the amplifier chain. This can be easily achieved with the AD600 because its gain is accurate even when the control input is overdriven. That is, each gain control window of 1.25 V is used fully before moving to the next amplifier to the right.

Figure 51 shows the circuit for the sequential control scheme. R6 to R9 with R16 provide offsets of 42.14 dB between the individual amplifiers to ensure smooth transitions between the gain of each successive X-AMP, with the sequence of gain increase being U1A, then U1B, and then U2A. The adjustable attenuator provided by R3 + R17 and the 100 Ω input resistance of U1A, as well as the fixed 6 dB attenuation provided by R2 and the input resistance of U1B, are included both to set V_{LOG} to read 0 dB when V_{IN} is 3.16 mV rms and to center the 100 dB range between 10 µV rms and 1 V rms input. R5 and C3 provide a 3 dB noise bandwidth of 30 kHz. R12 to R15 change the scaling from 625 mV/decade at the control inputs to 1 V/decade at the output. At the same time, R12 to R15 center the dynamic range at 60 dB, which occurs if the V_G of U1B is equal to 0. These arrangements ensure that the V_{LOG} still fits within the ±6 V supplies.

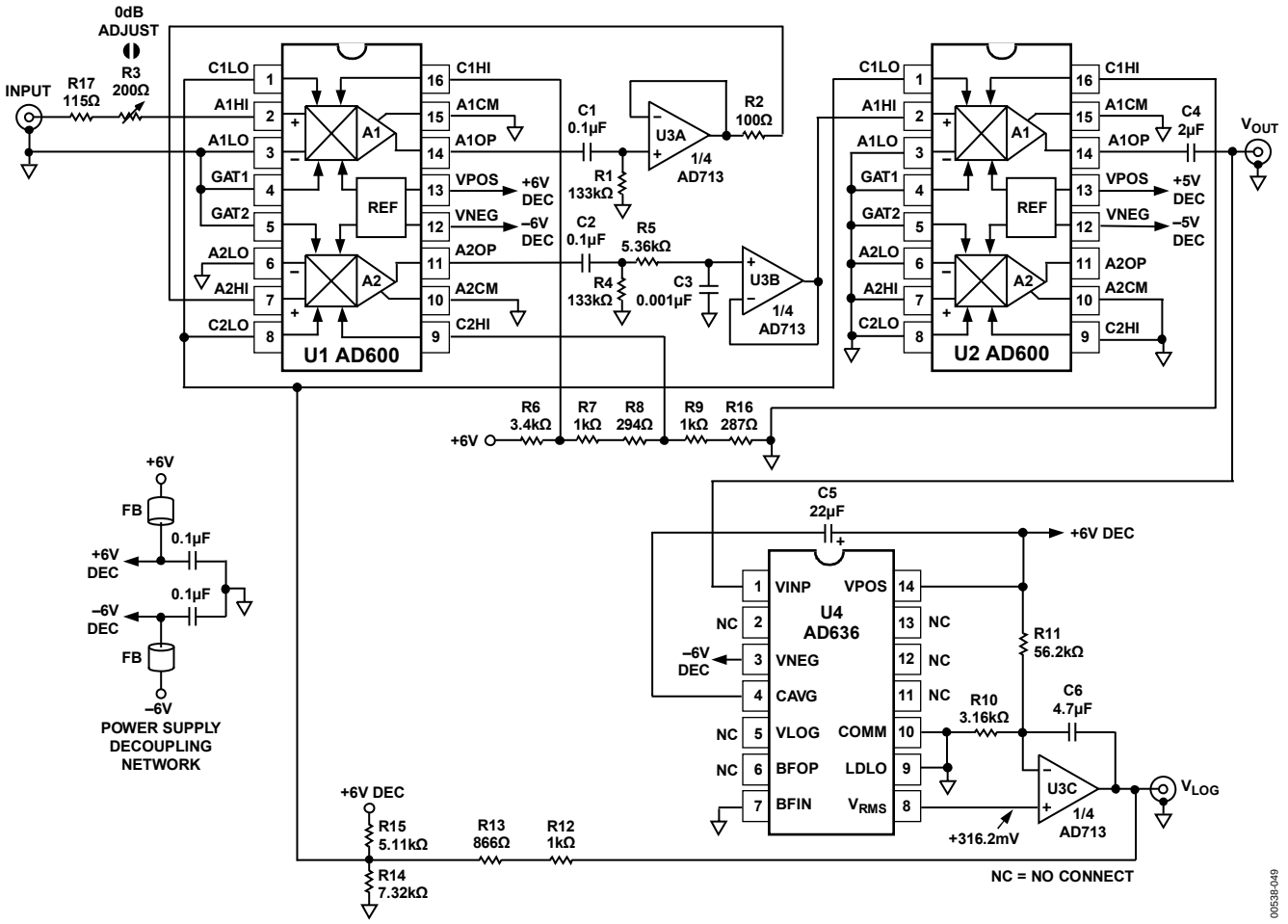


Figure 51. 120 dB Dynamic Range RMS Responding Circuit Optimized for SNR

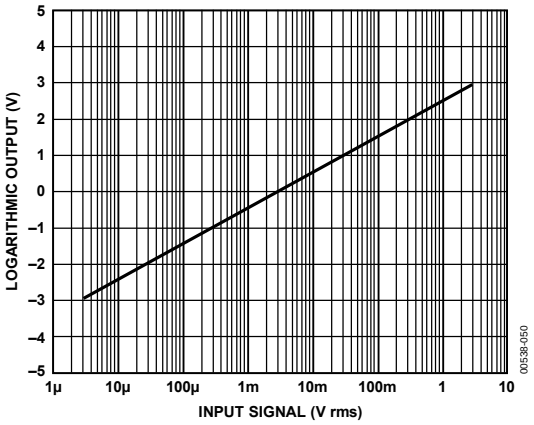


Figure 52. V_{LOG} Is Linear over the Full 120 dB Range

Figure 52 shows V_{LOG} to be linear over a full 120 dB range. Figure 53 shows the error ripple due to the individual gain functions bounded by ±0.2 dB (dotted lines) from 6 μV to 2 V. The small perturbations at about 200 μV and 20 mV, caused by the impracticality of matching the gain functions perfectly, are the only sign that the gains are now sequential. Figure 54 is a plot of V_{AGC} that remains very close to its set value of 316 mV rms over the full 120 dB range.

To compare the SNRs in the simultaneous and sequential modes of operation more directly, all interstage attenuation was eliminated (R2 and R3 in Figure 47 and R2 in Figure 51), the input of U1A was shorted, R5 was selected to provide a 20 kHz bandwidth (R5 = 7.87 kΩ), and only the gain control was varied, using an external source. The rms value of the noise was then measured at V_{OUT} and expressed as an SNR relative to 0 dBV, which is almost the maximum output capability of the AD600. Results for the simultaneous mode can be seen in Figure 55. The SNR degrades uniformly as the gain is increased. Note that since the inverting gain control was used, the gain in this curve and in Figure 56 decreases for more positive values of the gain-control voltage.

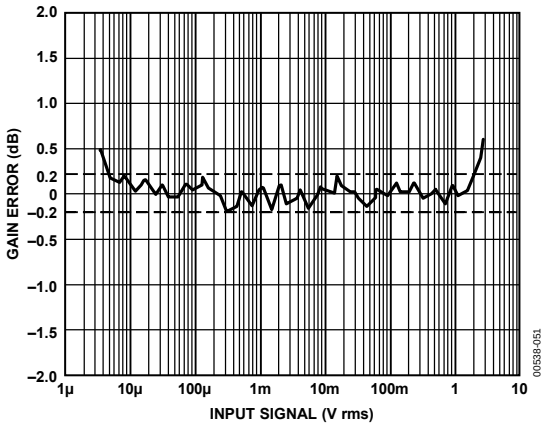


Figure 53. Error Ripple due to the Individual Gain Functions

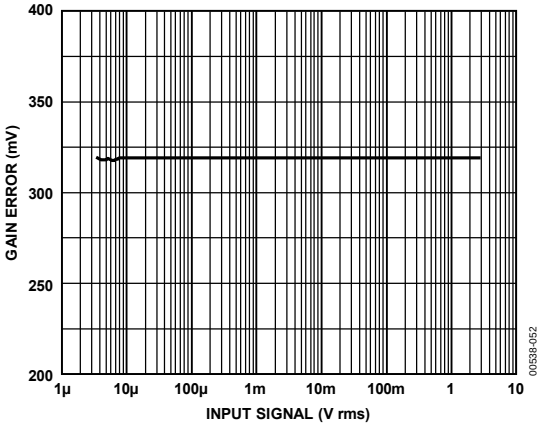


Figure 54. V_{AGC} Remains Close to Its Setpoint of 316 mV rms over the Full 120 dB Range

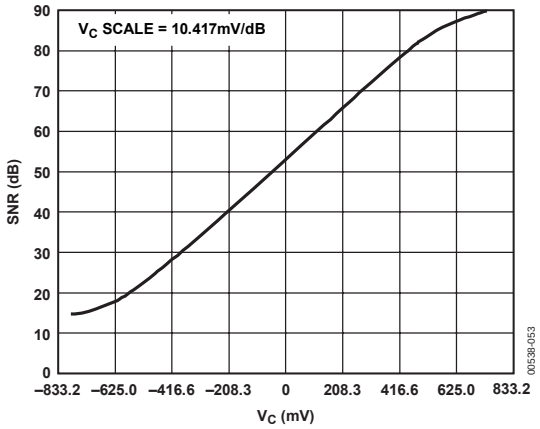


Figure 55. SNR vs. Control Voltage for Parallel Gain Control (See Figure 47)

In contrast, the SNR for the sequential mode is shown in Figure 56. U1A always acts as a fixed noise source; varying its gain has no influence on the output noise. This is a feature of the X-AMP technique. Therefore, for the first 40 dB of control range (actually slightly more, as is explained later), when only this VCA section has its gain varied, the SNR remains constant. During this time, the gains of U1B and U2A are at their minimum value of −1.07 dB.

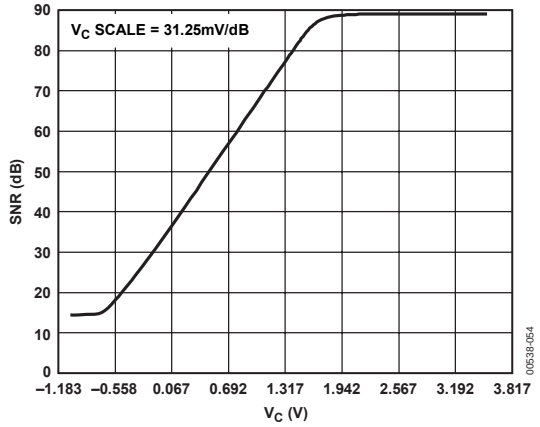


Figure 56. SNR vs. Control Voltage for Sequential Gain Control (See Figure 51)

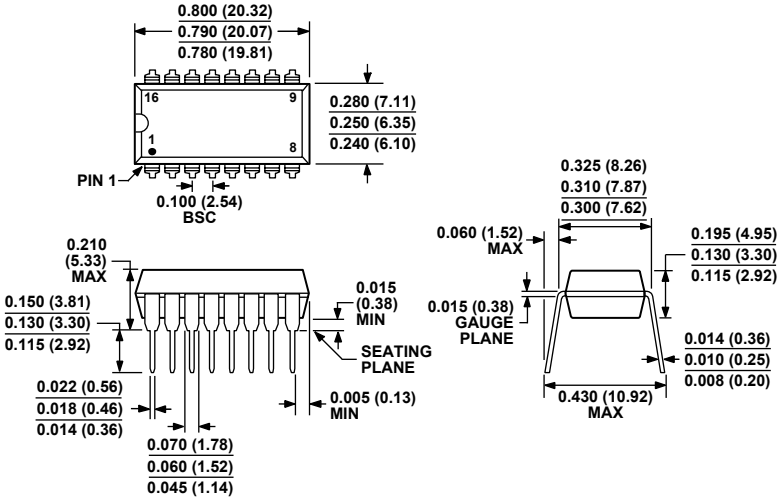
For the next 40 dB of control range, the gain of U1A remains fixed at its maximum value of 41.07 dB and only the gain of U1B is varied, while that of U2A remains at its minimum value of −1.07 dB. In this interval, the fixed output noise of U1A is amplified by the increasing gain of U1B and the SNR progressively decreases.

Once U1B reaches its maximum gain of 41.07 dB, its output also becomes a gain independent noise source; this noise is presented to U2A. As the control voltage is further increased, the gains of both U1A and U1B remain fixed at their maximum value of 41.07 dB, and the SNR continues to decrease. Figure 56 clearly shows this, because the maximum SNR of 90 dB is extended for the first 40 dB of input signal before it starts to roll off.

This arrangement of staggered gains can be easily implemented because when the control inputs of the AD600 are overdriven, the gain limits to its maximum or minimum values without side effects. This eliminates the need for awkward nonlinear shaping circuits that have previously been used to break up the gain range of multistage AGC amplifiers. The precise values of the AD600's maximum and minimum gain (not 0 dB and +40 dB but −1.07 dB and +41.07 dB) explain the rather odd values of the offset values that are used.

The optimization of the output SNR is of obvious value in AGC systems. However, in applications where these circuits are considered for their wide range logarithmic measurement capabilities, the inevitable degradation of the SNR at high gains need not seriously impair their utility. In fact, the bandwidth of the circuit shown in Figure 47 was specifically chosen to improve measurement accuracy by altering the shape of the log error curve at low signal levels (see Figure 53).

OUTLINE DIMENSIONS



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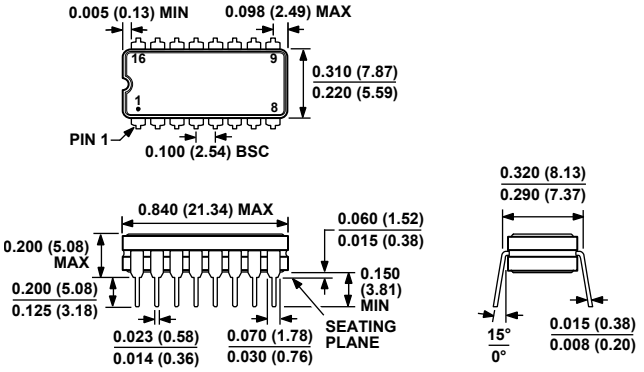
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 57. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body (N-16)
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 58. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)

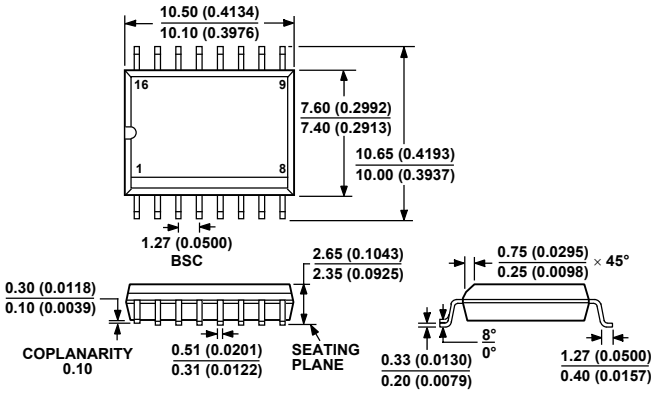


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Figure 59. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Gain Range	Temperature Range	Package Description	Package Option
AD600AQ	0 dB to 40 dB	−40°C to +85°C	16-Lead CERDIP	Q-16
AD600AR	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600AR-REEL	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600AR-REEL7	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600ARZ[1]	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600ARZ-R7[1]	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600ARZ-RL[1]	0 dB to 40 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD600JN	0 dB to 40 dB	0°C to 70°C	16-Lead PDIP	N-16
AD600JNZ[1]	0 dB to 40 dB	0°C to 70°C	16-Lead PDIP	N-16
AD600JR	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600JR-REEL	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600JR-REEL7	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600JRZ[1]	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600JRZ-R7[1]	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600JRZ-RL[1]	0 dB to 40 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD600SQ/883B[2]	0 dB to 40 dB	−55°C to +125°C	16-Lead CERDIP	Q-16
AD602AQ	−10 dB to +30 dB	−40°C to +85°C	16-Lead CERDIP	Q-16
AD602AR	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602AR-REEL	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602AR-REEL7	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602ARZ[1]	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602ARZ-R7[1]	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602ARZ-RL[1]	−10 dB to +30 dB	−40°C to +85°C	16-Lead SOIC_W	RW-16
AD602JCHIPS			DIE	
AD602JN	−10 dB to +30 dB	0°C to 70°C	16-Lead PDIP	N-16
AD602JNZ[1]	−10 dB to +30 dB	0°C to 70°C	16-Lead PDIP	N-16
AD602JR	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602JR-REEL	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602JR-REEL7	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602JRZ[1]	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602JRZ-R7[1]	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602JRZ-RL[1]	−10 dB to +30 dB	0°C to 70°C	16-Lead SOIC_W	RW-16
AD602SQ/883B[3]	−10 dB to +30 dB	−55°C to +150°C	16-Lead CERDIP	Q-16

[1] Z = Pb-free part.
[2] Refer to AD600/AD602 military data sheet. Also available as 5962-9457201MEA.
[3] Refer to AD600/AD602 military data sheet. Also available as 5962-9457202MEA.

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C00538-0-1/06(E)

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