

PowerPSoC® Intelligent LED Driver

1. Features

■ Integrated power peripherals

- Four internal 32 V low side N-Channel power FETs
 - $R_{DS(ON)} = 0.5 \Omega$ for 1.0 A devices
 - Up to 2 MHz configurable switching frequency
- Four hysteretic controllers
 - Independently programmable upper and lower thresholds
 - Programmable minimum ON/OFF timers
- Four low side gate drivers with programmable drive strength
- Four precision high side current sense amplifiers
- Three 16-bit LED dimming modulators: PrISM, DMM, and PWM
- Six fast response (100 ns) voltage comparators
- Six 8-bit reference DACs
- Built-in switching regulator eliminates external 5 V supply
- Multiple topologies including floating load buck, floating load buck-boost, and boost

■ M8C CPU core

- Processor speeds up to 24 MHz

■ Advanced peripherals (PSoC® Blocks)

- Capacitive sensing application capability
- DMX512 interface
- I²C master or slave
- Full-duplex UARTs
- Multiple SPI masters or slaves
- Integrated temperature sensor
- Up to 12-bit ADCs
- 6 to 12-bit incremental ADCs

- Up to 9-bit DACs
- Programmable gain amplifiers
- Programmable filters and comparators
- 8 to 32-bit timers and counters
- Complex peripherals by combining blocks
- Configurable to all GPIO pins

■ Programmable pin configurations

- 25 mA sink, 10 mA source on all GPIO and function pins
- Pullup, pull down, high Z, strong, or open drain drive modes on all GPIO and function pins
- Up to 10 analog inputs on GPIO
- Two 30 mA analog outputs on GPIO
- Configurable interrupt on all GPIO

■ Flexible on-chip memory

- 16 K Flash program storage 50,000 erase and write cycles
- 1 K SRAM data storage
- In-System Serial Programming (ISSP)
- Partial Flash updates
- Flexible protection modes
- EEPROM emulation in Flash

■ Complete development tools

- Free development software: PSoC Designer™
- Full featured, In-Circuit Emulator and Programmer
- Full speed emulation
- Complex breakpoint structure
- 128 kbytes trace memory

■ Applications

- Stage LED lighting
- Architectural LED lighting
- General purpose LED lighting
- Automotive and emergency vehicle LED lighting
- Landscape LED lighting
- Display LED lighting
- Effects LED lighting
- Signage LED lighting

■ Device options

- CY8CLED04D0x
 - Four internal FETs with 0.5 A and 1.0 A options
 - Four external gate drivers
- CY8CLED04G01
 - Four external gate drivers
- CY8CLED03D0x
 - Three internal FETs with 0.5 A and 1.0 A options
 - Three external gate drivers
- CY8CLED03G01
 - Three external gate drivers
- CY8CLED02D01
 - Two 1.0 A internal FETs
 - Two external gate drivers
- CY8CLED01D01
 - One 1.0 A internal FET
 - One external gate driver

■ 56-pin QFN package

Figure 1-1. PowerPSoC Architectural Block Diagram



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3. Logic Block Diagrams

Figure 3-1. CY8CLED04D0x Logic Block Diagram



Figure 3-2. CY8CLED04G01 Logic Block Diagram

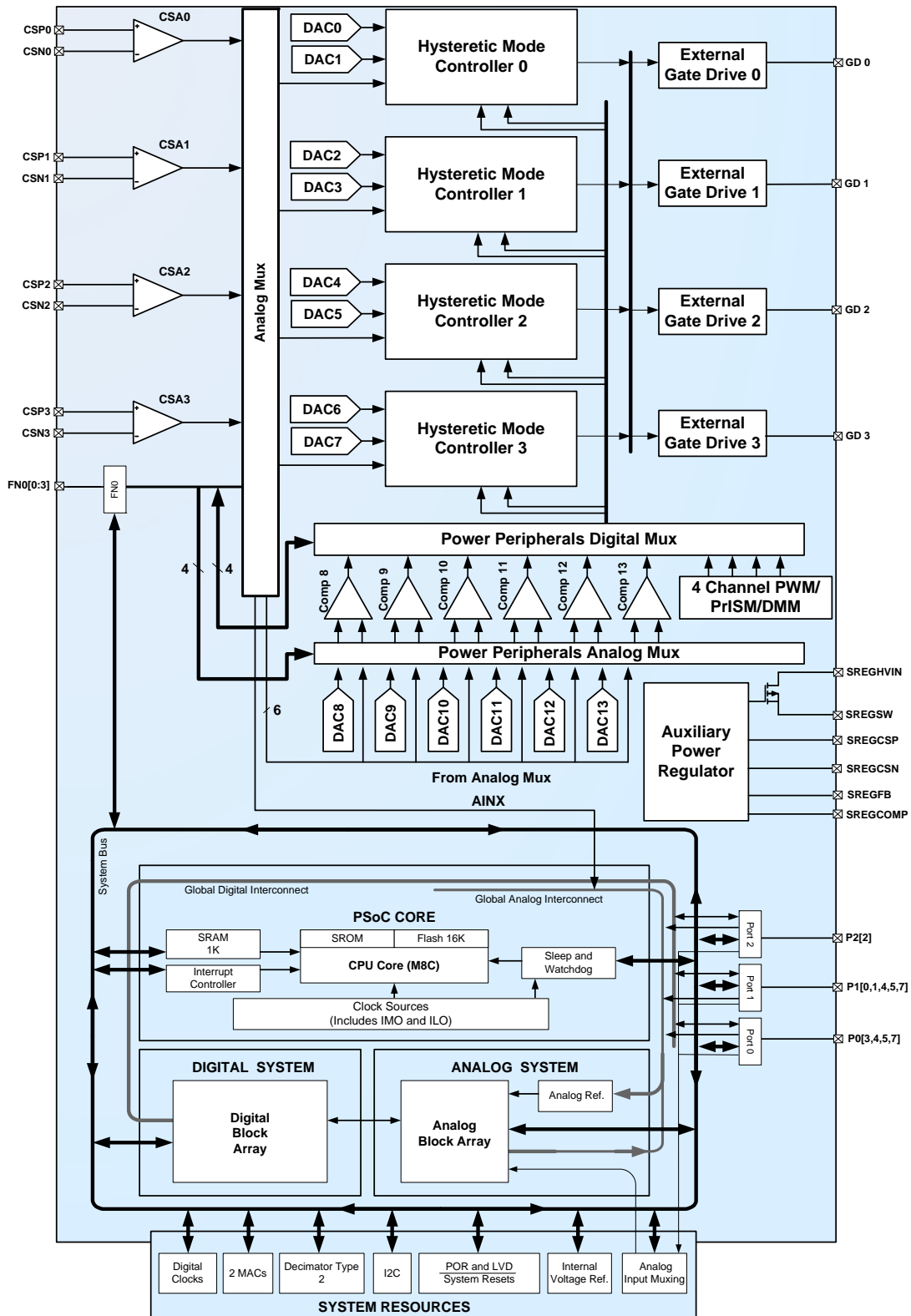


Figure 3-3. CY8CLED03D0x Logic Block Diagram

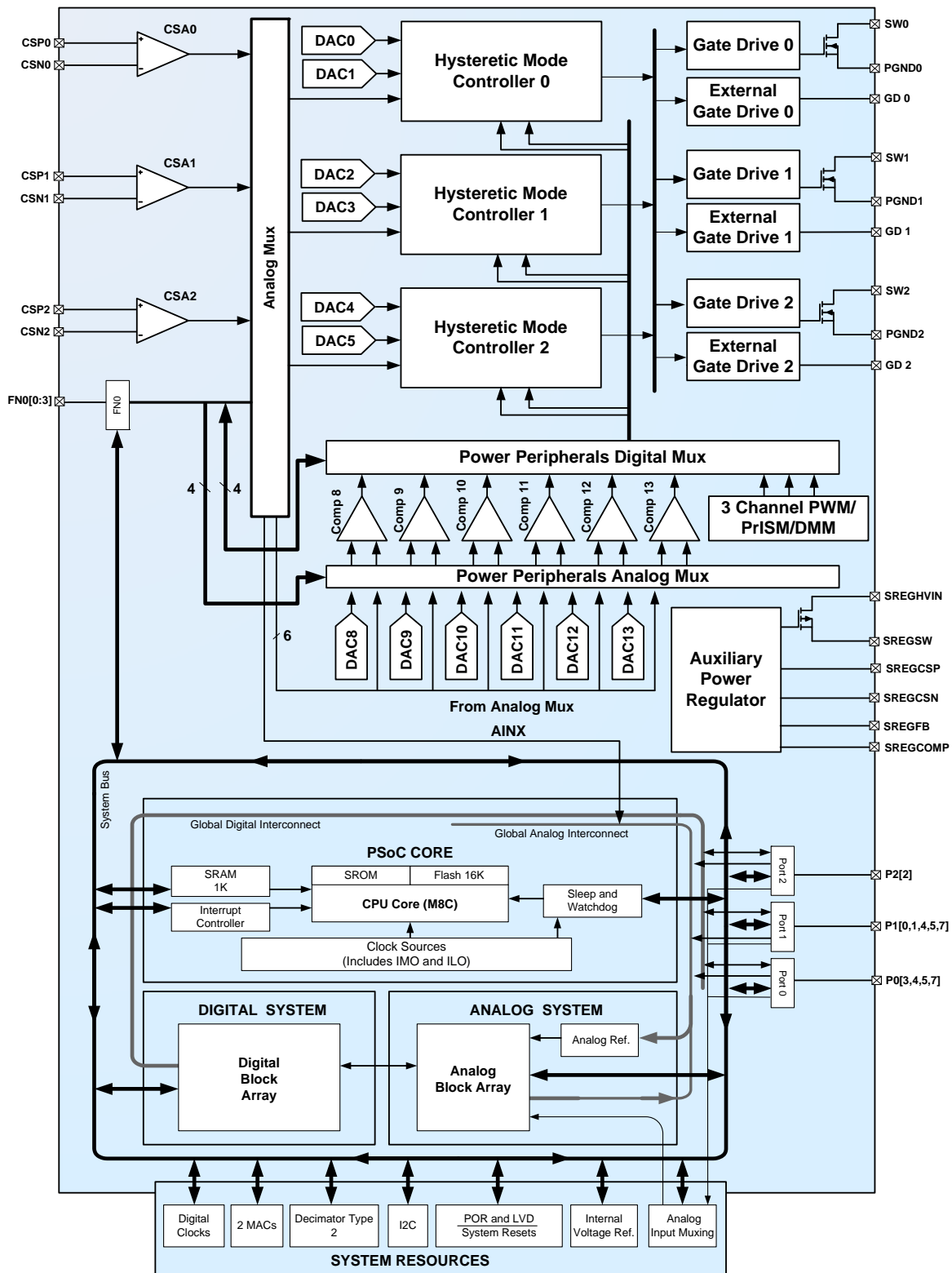


Figure 3-4. CY8CLED03G01 Logic Block Diagram

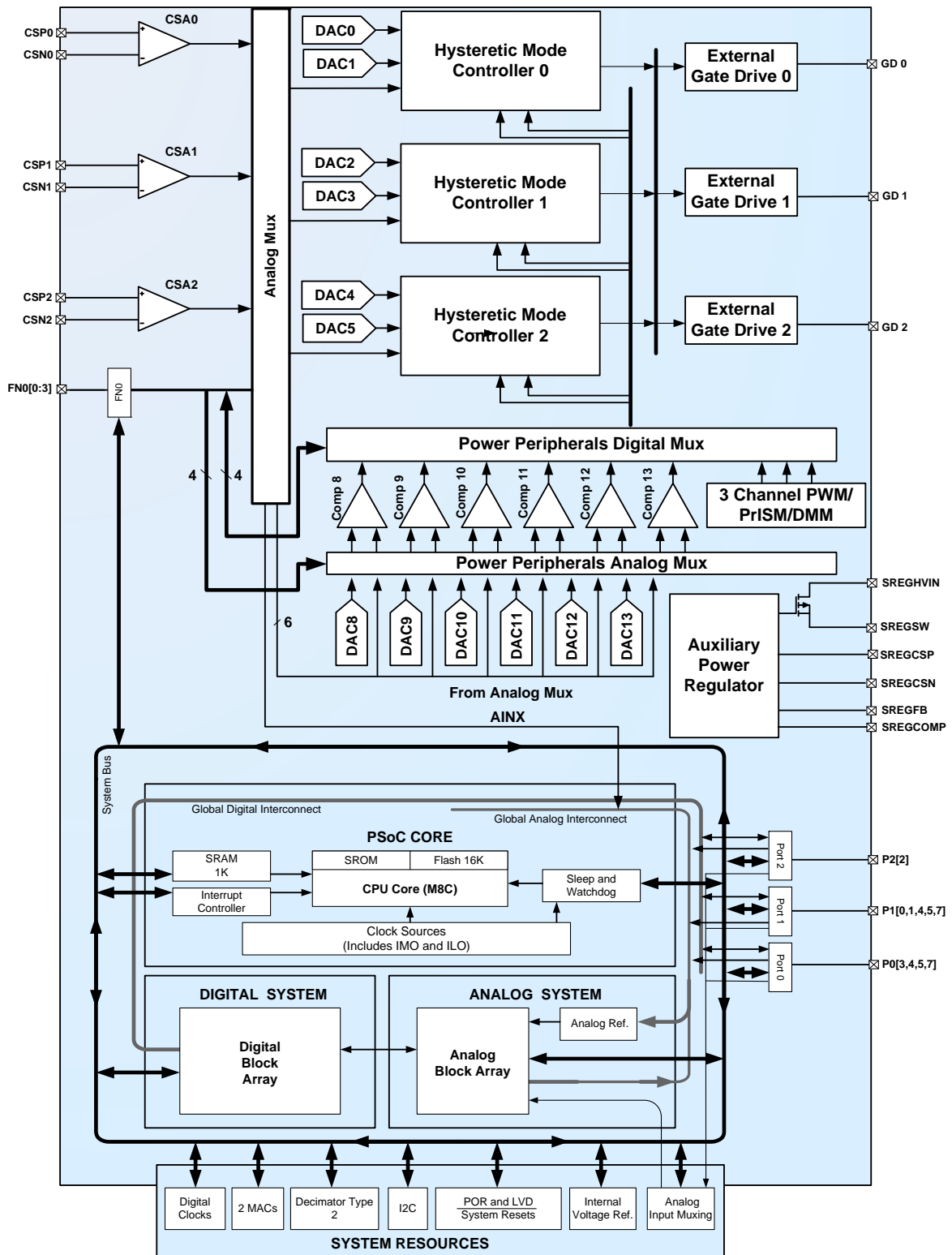


Figure 3-5. CY8CLED02D01 Logic Block Diagram

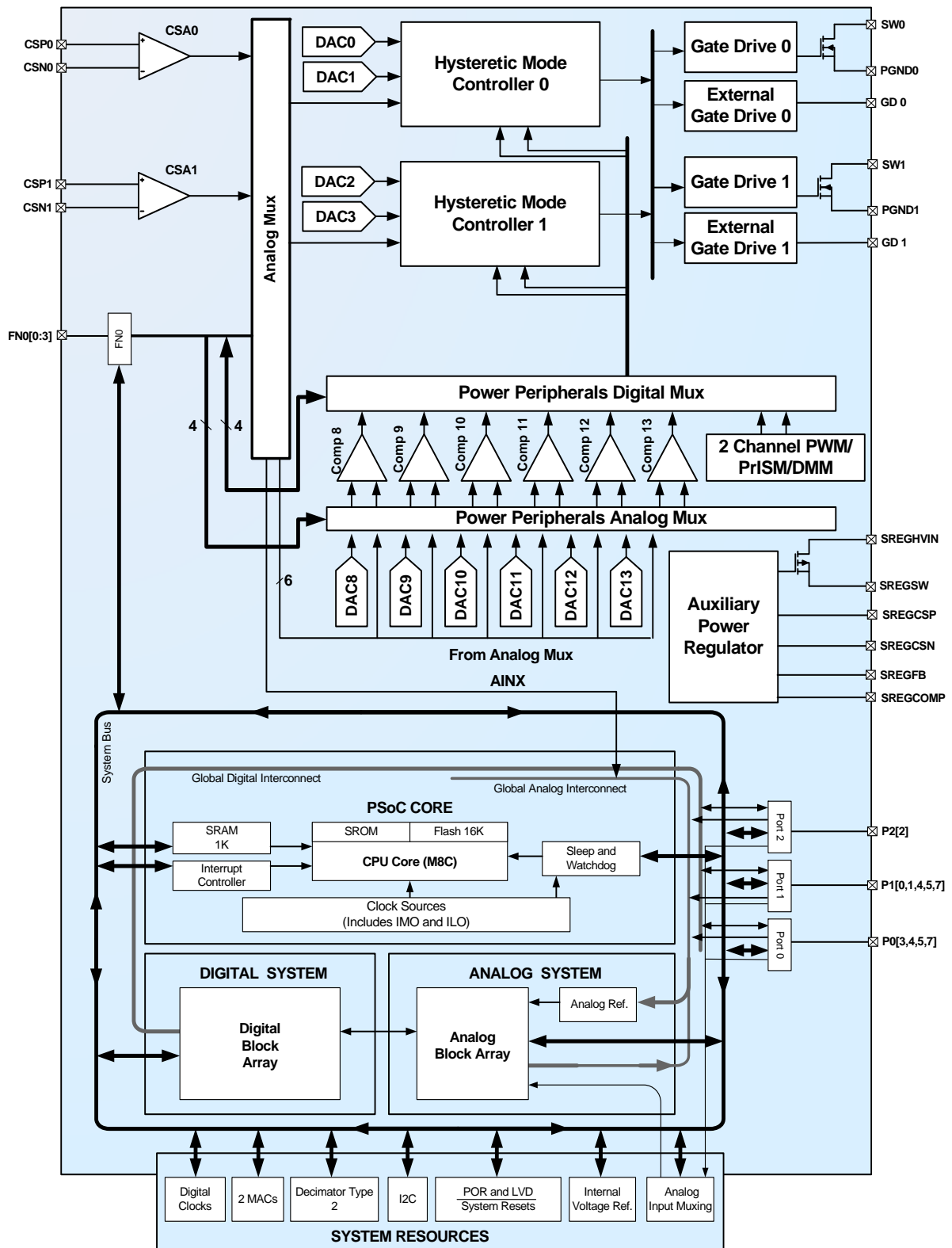
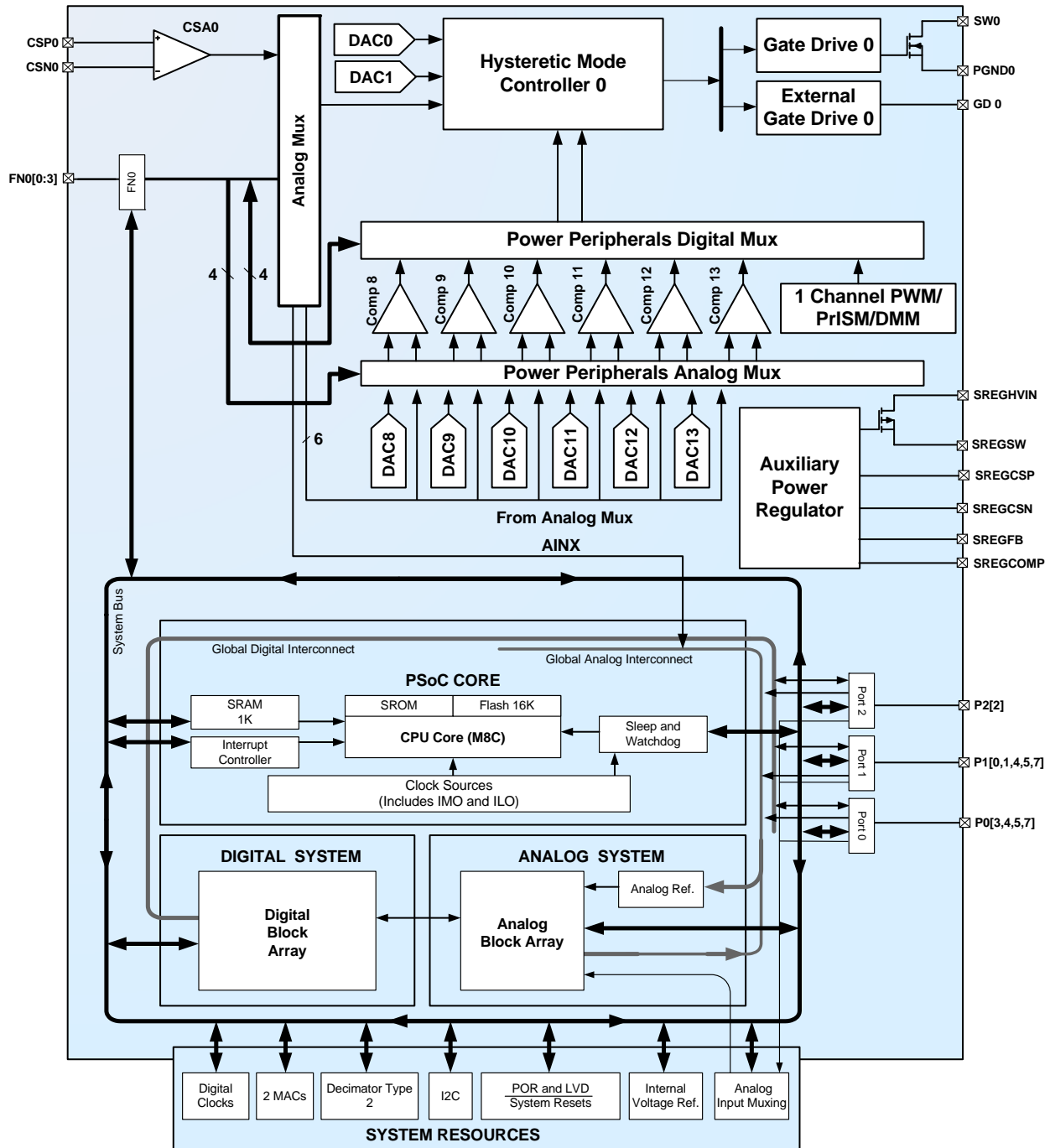


Figure 3-6. CY8CLED01D01 Logic Block Diagram



4. PowerPSoC® Functional Overview

The PowerPSoC family incorporates programmable system-on-chip technology with the best in class power electronics controllers and switching devices to create easy to use power-system-on-chip solutions for lighting applications.

All PowerPSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. PowerPSoC devices feature high performance power electronics including 1 ampere 2 MHz power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators to create a complete power electronics solution for LED power management. Configurable power, analog, digital, and interconnect circuitry enables a high level of integration in a host of industrial, commercial, and consumer LED lighting applications.

This architecture integrates programmable analog and digital blocks to enable you to create customized peripheral configurations that match the requirements of each individual application. Additionally, the device includes a 24 MHz CPU, Flash program memory, SRAM data memory, and configurable I/O in a range of convenient pinouts and packages.

The PowerPSoC architecture, as illustrated in the block diagrams, comprises five main areas: PSoC core, digital system, analog system, system resources, and power peripherals, which include power FETs, hysteretic controllers, current sense amplifiers, and PrISM/PWM modulators. Configurable global busing combines all the device resources into a complete custom system. The PowerPSoC family of devices have 10-port I/Os that connect to the global digital and analog interconnects, providing access to eight digital blocks and six analog blocks.

5. Power Peripherals

PowerPSoC is designed to operate at voltages from 7 V to 32 V, drive up to 1 ampere of current using internal MOSFET switches, and over 1 ampere with external MOSFETs.

This family of devices (CY8CLED0xD/G0y) combines up to four independent channels of constant current drivers. These drivers feature hysteretic controllers with the Programmable System-on-Chip (PSoC) that contains an 8-bit microcontroller, configurable digital and analog peripherals, and embedded flash memory.

The CY8CLED0xD/G0y is the first product in the PowerPSoC family to integrate power peripherals to add further integration for your power electronics applications. The PowerPSoC family of intelligent power controller ICs are used in lighting applications that need traditional MCUs and discrete power electronics support. The power peripherals of the CY8CLED0xD/G0y include up to four 32 volt power MOSFETs with current ratings up to 1 ampere each. It also integrates gate drivers that enable applications to drive external MOSFETs for higher current and voltage capabilities. The controller is a programmable threshold hysteretic controller, with user-selectable feedback paths that uses the IC in current mode floating load buck, floating load buck-boost, and boost configurations.

5.1 Hysteretic Controllers

The PowerPSoC contains four hysteretic controllers. There is one hysteretic controller for each channel of the device.

The hysteretic controllers provide cycle by cycle switch control with fast transient response, which simplifies system design by requiring no external compensation. The hysteretic controllers include the following key features:

- Four independent channels
- DAC configurable thresholds
- Wide switching frequency range from 20 kHz to 2 MHz
- Programmable minimum on and off time
- Floating load buck, floating load buck-boost and boost topology controller

The reference inputs (REF_A and REF_B in Figure 5-1.) of the hysteretic controller are provided by the reference DACs as illustrated in the top level block diagram (see Figure 3-1. on page 3).

The hysteretic control function output is generated by comparing the feedback value to two thresholds. Going below the lower threshold turns the switch ON and exceeding the upper threshold turns the switch OFF as shown in Figure 5-1. The output current waveforms are shown in Figure 5-2.

The hysteretic controller also controls the minimum on-time and off-time. This circuit prevents oscillation at very high frequencies, which can be very destructive to output switches.

The output to the gate drivers is gated by the Trip, DIM and Enable signals. The Enable signal is a direct result of the enable bit in the control register for the hysteretic controller.

The Trip signal can be any digital signal that follows TTL logic (logic high and logic low). It is an active high input.

The DIM Modulation signal is the output of the dedicated modulators that are present in the power peripherals, or any other digital modulation signal.

Figure 5-1. Generating Hysteretic Control Function Output



Figure 5-2. Current Waveforms



The minimum on-time and off-time circuits in the PowerPSoC prevent oscillations at very high frequencies, which can be very destructive to output switches.

5.2 Low Side N-Channel FETs

The internal low side N-Channel FETs are designed to enhance system integration. The low side N-Channel FETs include the following key features:

- Drive capability up to 1 A
- Switching times of 20 ns (rise and fall times) to ensure high efficiency (more than 90%)
- Drain source voltage rating 32 V
- Low $R_{DS(ON)}$ to ensure high efficiency
- Switching frequency up to 2 MHz

5.3 External Gate Drivers

These gate drivers enable the use of external FETs with higher current capabilities or lower $R_{DS(ON)}$. The external gate drivers directly drive MOSFETs that are used in switching applications. The gate driver provides multiple programmable drive strength steps to enable improved EMI management. The external gate drivers include the following key features:

- Programmable drive strength options (25%, 50%, 75%, 100%) for EMI management
- Rise and fall times at 55 ns with 4 nF load

5.4 Dimming Modulation Schemes

There are three dimming modulation schemes available with the PowerPSoC. The configurable modulation schemes are:

- Precise Intensity Signal Modulation (PrISM)
- Delta Sigma Modulation Mode (DMM)
- Pulse Width Modulation (PWM)

5.4.1 PrISM Mode Configuration

- High resolution operation up to 16 bits
- Dedicated PrISM module enables customers to use core PSoc digital blocks for other needs
- Clocking up to 48 MHz
- Selectable output signal density
- Reduced EMI

The PrISM mode compares the output of a pseudo-random counter with a signal density value. The comparator output asserts when the count value is less than or equal to the value in the signal density register.

5.4.2 DMM Mode Configuration

- High resolution operation up to 16 bits
- Configurable output frequency and delta sigma modulator width to trade off repeat rates versus resolution
- Dedicated DMM module enables customers to use PSoc digital blocks for other uses
- Clocking up to 48 MHz

The DMM modulator consists of a 12-bit PWM block and a 4-bit Delta Sigma Modulator (DSM) block. The width of the PWM, the width of the DMM, and the clock defines the output frequency. The duty cycle of the PWM output is dithered by using the DSM block which has a user-selectable resolution up to 4 bits.

5.4.3 PWM Mode Configuration

- High resolution operation up to 16 bits
- User programmable period from 1 to 65535 clocks
- Dedicated PWM module enables customers to use core PSoc digital blocks for other use
- Interrupt on rising edge of the output or terminal count
- Precise PWM phase control to manage system current edges
- Phase synchronization among the four channels
- PWM output can be aligned to left, right, or center

The PWM features a down counter and a pulse width register. A comparator output is asserted when the count value is less than or equal to the value in the pulse width register.

5.5 Current Sense Amplifier

The high side current sense amplifiers provide a differential sense capability to sense the voltage across current sense resistors in lighting systems. The current sense amplifier includes the following key features:

- Operation with high common mode voltage to 32 V
- High common mode rejection ratio
- Programmable bandwidth to optimize system noise immunity

An off-chip resistor R_{sense} is used for high side current measurement as shown in Figure 5-3, on page 11. The output of the current sense amplifier goes to the power peripherals analog multiplexer where, you select the hysteretic controller to which

the routing is done. Table 5-1 illustrates example values of R_{sense} for different currents.

The method to calculate the R_{sense} value for a desired average current is explained in the application note, [Floating Load Buck Topology for HB-LEDs - AN52699](#)

Table 5-1. R_{sense} Values for Different Currents

| Max Load Current (mA) | Typical R_{sense} (m Ω) |
|-----------------------|-----------------------------------|
| 1000 | 100 |
| 750 | 130 |
| 500 | 200 |
| 350 | 300 |

Figure 5-3. High Side Current Measurement



5.6 Voltage Comparators

There are six comparators that provide high speed comparator operation for over voltage, over current, and various other system event detections. For example, the comparators may be used for zero crossing detection for an AC input line or monitoring total DC bus current. Programmable internal analog routing enables these comparators to monitor various analog signals. These comparators include the following key features:

- High speed comparator operation: 100 ns response time
- Programmable interrupt generation
- Low input offset voltage and input bias currents

Six precision voltage comparators are available. The differential positive and negative inputs of the comparators are routed from the analog multiplexer and the output goes to the digital multiplexer. A programmable inverter is used to select the output polarity. User-selectable hysteresis can be enabled or disabled to trade-off noise immunity versus comparator sensitivity.

5.7 Reference DACs

The reference DACs are used to generate set points for various analog modules such as Hysteretic controllers and comparators. The reference DACs include the following key features:

- 8-bit resolution
- Guaranteed monotonic operation

- Low gain errors
- 10 us settling time

These DACs are available to provide programmable references for the various analog and comparator functions and are controlled by memory mapped registers.

DAC[0:7] are embedded in the hysteretic controllers and are required to set the upper and lower thresholds for channel 0 to 3.

DAC [8:13] are connected to the Power Peripherals Analog Multiplexer and provide programmable references to the comparator bank. These are used to set trip points which enable over voltage, over current, and other system event detection.

5.8 Built-in Switching Regulator

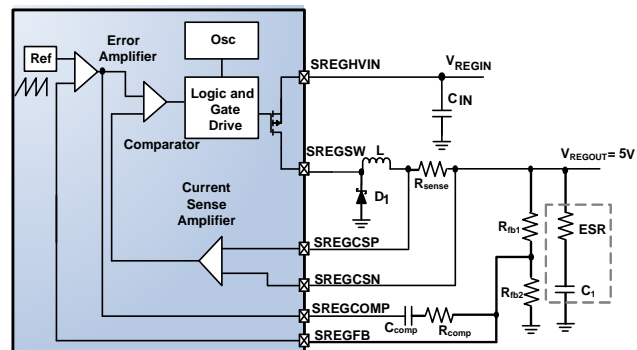
The switching regulator is used to power the low voltage (5 V) portion of the PowerPSoC from the input line. This regulator is based upon a peak current control loop which can support up to 250 mA of output current. The current not being consumed by PowerPSoC is used to power additional system peripherals. The key features of the built-in switching regulator include:

- Ability to self power device from input line
- Small filter component sizes
- Fast response to transients

Refer to Table 16-20 for component values.

The 'Ref' signal that forms the reference to the Error Amplifier is internally generated and there is no user control over it.

Figure 5-4. Built-in Switching Regulator



5.9 Analog Multiplexer

The PowerPSoC family's analog MUX is designed to route signals from the CSA output, function I/O pins and the DACs to comparator inputs and the current sense inputs of the hysteretic controllers. Additionally, CSA outputs can be routed to the AINX block using this MUX.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

The CPU configures the Power Peripherals Analog Multiplexer connections using memory mapped registers. The analog multiplexer includes the following key features:

- Signal integrity for minimum signal corruption

5.10 Digital Multiplexer

The PowerPSoC family's digital MUX is a configurable switching matrix that connects the power peripheral digital resources.

For a full matrix representation of all possible routing using this MUX, refer to the PowerPSoC Technical Reference Manual.

This Power Peripheral Digital Multiplexer is independent of the main PSoC digital buses or global interconnect of the PSoC core. The digital multiplexer includes the following key features:

- Connect signals to ensure needed flexibility

5.11 Function Pins (FN0[0:3])

The function I/O pins are a set of dedicated control pins used to perform system level functions with the power peripheral blocks of the PowerPSoC. These pins are dynamically configurable, enabling them to perform a multitude of input and output functions. These I/Os have direct access to the input and output of the voltage comparators, input of the hysteretic controller, and output of the digital PWM blocks for the device. The function I/O pins are register mapped. The microcontroller can control and read the state of these pins and the interrupt function.

Some of the key system benefits of the function I/O are:

- Enabling an external higher voltage current-sense amplifier as shown in [Figure 5-5](#).
- Synchronizing dimming of multiple PowerPSoC controllers as shown in [Figure 5-6](#).
- Programmable fail-safe monitor and dedicated shutdown of hysteretic controller as shown in [Figure 5-7](#).

Along with these functions, these I/Os also provide interrupt functionality, enabling intelligent system responses to power control lighting system status.

Figure 5-5. External CSA and FET Application

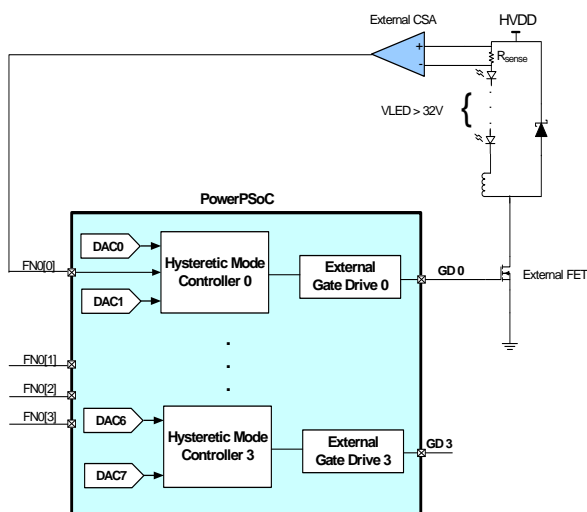


Figure 5-6. PowerPSoC in Master/Slave Configuration

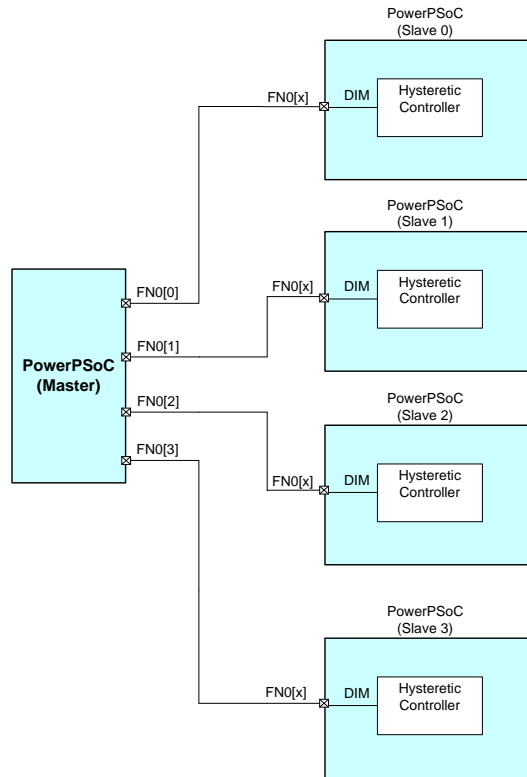
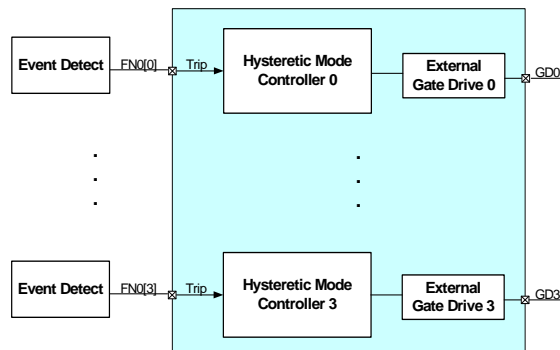


Figure 5-7. Event Detection



6. PSoC Core

The PSoC core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable General Purpose I/O (GPIO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors to simplify programming of real time embedded events. The program execution is timed and protected using the included Sleep and Watchdog Timers (WDT) time and protect program execution.

Memory encompasses 16 K of Flash for program storage, 1K of SRAM for data storage, and up to 2 K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz internal main oscillator (IMO) accurate to 4 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz internal low speed oscillator (ILO) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a system resource), provide the flexibility to integrate almost any timing requirement into the PowerPSoC device.

PowerPSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

6.1 Digital System

The digital system contains eight digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Digital peripheral configurations include:

- DMX512
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I²C master, slave, and multi-master
- Cyclical redundancy checker/generator (8 to 32 bit)
- IrDA
- Pseudo random sequence generators (8 to 32 bit)

Note The DALI interface is supported through the use of a combination of the above mentioned user modules. For more details on the exact configuration and an example project, refer to the application note, [Implementing a DALI Receiver System Using PowerPSoC™ - AN52525](#).

The digital blocks can be connected to any GPIO through a series of global buses that route any signal to any pin. The buses

also allow signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

There are four digital blocks in each row. This allows optimum choice of system resources for your application.

Figure 6-1. Digital System Block Diagram



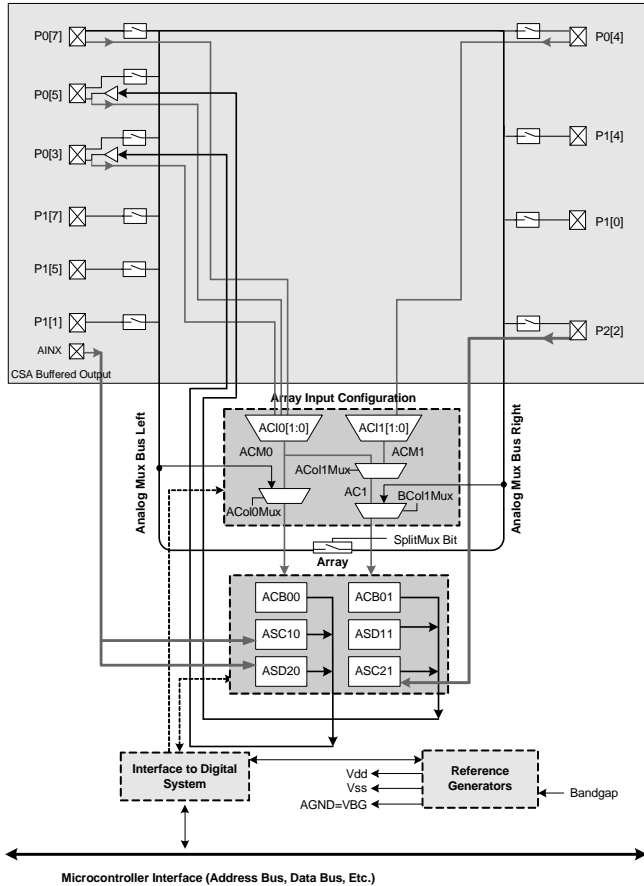
6.2 Analog System

The analog system contains six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PowerPSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (up to 2, with 6 to 12-bit resolution, selectable as incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6 to 9-bit resolution)
- Multiplying DACs (up to 2, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC core resource)
- 1.3 V reference (as a system resource)
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are arranged in two columns of three blocks each, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 6-2. on page 14.

Figure 6-2. Analog System Block Diagram



6.3 Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0 to 2. Pins can be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. It can be split into two sections for simultaneous dual-channel processing. An additional analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive

measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Crosspoint connection between any I/O pin combinations

Like other PSoC devices, PowerPSoC has specific pins allocated to the reference capacitor (Ref Cap) and modulation resistor (Mod resistor). These are indicated in the device pin outs (Section 13). For more details on Capacitive Sensing, refer to the application notes AN2394 - CapSense Best Practices, AN2292 - Capacitance Sensing Layout Guidelines for PSoC CapSense and AN47456 - Design Guide CapSense buttons with CSD. Apart from these, there are a number of application notes on Capacitive Sensing on the Cypress webbiest. The PowerPSoC Technical Reference Manual provides details on the analog system configuration that enables all I/Os in the device to be CapSense inputs.

6.4 Additional System Resources

System resources provide additional capability useful in complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- A decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. The designer can generate additional clocks using digital PSoC blocks as clock dividers.
- The I²C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master applications are supported.
- An internal 1.3 V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

7. Applications

The following figures show examples of applications in which the PowerPSoC family of devices adds intelligent power control for power applications.

Figure 7-1. LED Lighting with RRGB Color Mixing Configured as Floating Load Buck Converter



Figure 7-2. LED Lighting with RGBA Color Mixing Driving External MOSFETS as Floating Load Buck Converter

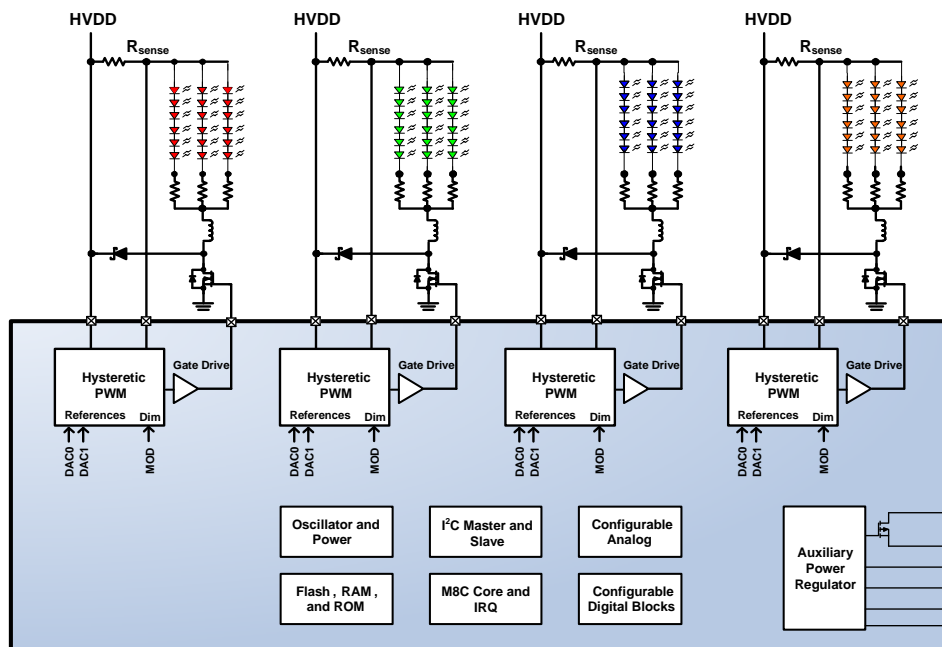


Figure 7-3. LED Lighting with a Single Channel Boost Driving Three Floating Load Buck Channels



8. PowerPSoC Device Characteristics

There are two major groups of devices in the PowerPSoC family. One group is a 4-channel 56-pin QFN and the other is a 3-channel 56-pin QFN. These are summarized in the following table.

Table 8-1. PowerPSoC Device Characteristics

| Device Group | Internal Power FETs | External Gate Drivers | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size |
|---------------------|---------------------|-----------------------|-------------|--------------|----------------|---------------|----------------|----------------|---------------|-----------|------------|
| CY8CLED04D01-56LTXI | 4X1.0 A | 4 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED04D02-56LTXI | 4X0.5 A | 4 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED04G01-56LTXI | 0 | 4 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED03D01-56LTXI | 3X1.0 A | 3 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED03D02-56LTXI | 3X0.5 A | 3 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED03G01-56LTXI | 0 | 3 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED02D01-56LTXI | 2X1.0 A | 2 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED01D01-56LTXI | 1X1.0 A | 1 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |
| CY8CLED01D01-56LTXQ | 1X1.0 A | 1 | 14 | 2 | 8 | 14 | 2 | 2 | 6 | 1 K | 16 K |

9. Getting Started

The quickest way to understand the PowerPSoC device is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PowerPSoC integrated circuit and presents specific pin, register, and electrical specifications. For in depth information, along with detailed programming information, refer to the *PowerPSoC Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PowerPSoC device datasheets on the web at www.cypress.com.

9.1 Application Notes

Application notes are an excellent introduction to a wide variety of possible PowerPSoC designs. Layout Guidelines, Thermal Management and Firmware Design Guidelines are some of the topics covered. To view the PowerPSoC application notes, go to <http://www.cypress.com/powerpsoc> and click on the Application Notes link.

9.2 Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store contains development kits, C compilers, and all accessories for PowerPSoC development. For more information on the kits or to purchase a kit from the Cypress web site, go to <http://www.cypress.com/powerpsoc> and click on the Development Kits link.

9.3 Training

Free PowerPSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

9.4 CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PowerPSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

9.5 Technical Support

PowerPSoC application engineers take pride in fast and accurate response. They can be reached with a 24-hour guaranteed response at <http://www.cypress.com/support/>. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

10. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP, Windows Vista, or Windows 7.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PowerPSoC family.

10.1 PSoC Designer Software Subsystems

10.1.1 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PowerPSoC blocks. Examples of user modules are Current Sense Amplifiers, PrISM, PWM, DMM, Floating Load Buck, and Boost. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

10.1.2 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PowerPSoC family of devices. The products allow you to create complete C programs for the PowerPSoC family of devices.

The optimizing C compilers provide all the features of C tailored to the PowerPSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

10.1.3 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PowerPSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

10.1.4 Online Help System

The online help system displays online, context-sensitive help for you. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

10.2 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

11. Designing with User Modules

The development process for the PowerPSoC device differs from that of a traditional fixed function microprocessor. The configurable power, analog, and digital hardware blocks give the PowerPSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PowerPSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PowerPSOC development process can be summarized in the following four steps:

1. Select Components
2. Configure Components
3. Organize and Connect
4. Generate, Verify and Debug

Select Components. In the chip-level view the components are called “user modules”. User modules make selecting and implementing peripheral devices simple and come in power, analog, digital, and mixed signal varieties. The standard user module library contains over 50 common peripherals such as Current Sense Amplifiers, PrISM, PWM, DMM, Floating Buck, Boost, ADCs, DACs, Timers, Counters, UARTs, and other not so common peripherals such as DTMF generators and Bi-Quad analog filter sections.

Configure Components. Each of the components selected establishes the basic register settings that implement the selected function. They also provide parameters allowing precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSOC blocks, one for each 8 bits of resolution. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

The chip-level user modules are documented in datasheets that are viewed directly in PSoC Designer. These datasheets explain the internal operation of the component and provide performance specifications. Each datasheet describes the use

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PowerPSoC devices.

of each user module parameter and other information needed to successfully implement your design.

Organize and Connect. Signal chains can be built at the chip level by interconnecting user modules to each other and the I/O pins. In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug. When ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the high level user module API functions.

The chip-level designs generate software based on your design. The chip-level view provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows development and customization of your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.

12. Pin Information

12.1 CY8CLED04D0x 56-Pin Part Pinout (without OCD)

The CY8CLED04D01 and CY8CLED04D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-1. CY8CLED04D0x 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|----------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ISSP SDATA |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/Analog Output (Column 0) |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/Analog Output (Column 1)/Capsense Ref Cap |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/Capsense Ref Cap |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCL (Secondary)/ISSP SCLK |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) |
| 9 | | | | V _{SS} | Digital Ground |
| 10 | | | | NC | No Connect |
| 11 | | | | NC | No Connect |
| 12 | | | | NC | No Connect |
| 13 | | | | NC | No Connect |
| 14 | I | | | XRES | External Reset |
| 15 | | | | V _{DD} | Digital Power Supply |
| 16 | | | | V _{SS} | Digital Ground |
| 17 | | | | AV _{SS} | Analog Ground |
| 18 | | | | AV _{DD} | Analog Power Supply |
| 19 | | | I | CSN2 | Current Sense Negative Input - CSA2 |
| 20 | | | | CSP2 | Current Sense Positive Input and Power Supply - CSA2 |
| 21 | | | | CSP3 | Current Sense Positive Input and Power Supply - CSA3 |
| 22 | | | I | CSN3 | Current Sense Negative Input 3 |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply |
| 30 | | | | GDV _{SS} | Gate Driver Ground |
| 31 | | | | PGND3 ^[1] | Power FET Ground 3 |
| 32 | | | O | GD3 | External Low Side Gate Driver 3 |
| 33 | | | | SW3 | Power Switch 3 |
| 34 | | | | PGND2 ^[1] | Power FET Ground 2 |
| 35 | | | O | GD2 | External Low Side Gate Driver 2 |
| 36 | | | | SW2 | Power Switch 2 |
| 37 | | | | SW1 | Power Switch 1 |
| 38 | | | O | GD1 | External Low Side Gate Driver 1 |
| 39 | | | | PGND1 ^[1] | Power FET Ground 1 |
| 40 | | | | SW0 | Power Switch 0 |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 |
| 42 | | | | PGND0 ^[1] | Power FET Ground 0 |
| 43 | | | | GDV _{SS} | Gate Driver Ground |
| Pin No. | Type | | | Name | Description |
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply |
| 45 | | | O | FN0[0] | Function I/O |
| 46 | | | I/O | FN0[1] | Function I/O |
| 47 | | | I/O | FN0[2] | Function I/O |
| 48 | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output |
| 54 | | | | V _{DD} | Digital Power Supply |
| 55 | | | | V _{SS} | Digital Ground |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input |

Figure 12-1. CY8CLED04D0x 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Note

1. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

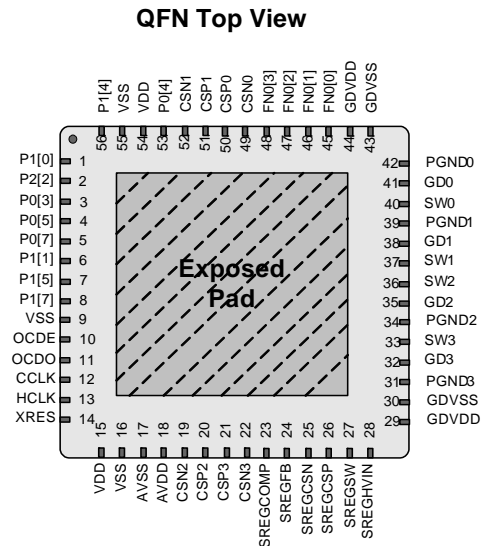
12.3 CY8CLEDD04DOCD1 56-Pin Part Pinout (with OCD)

The CY8CLEDD04DOCD1 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-3. CY8CLEDD04DOCD1 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|----------------------|---|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ ISSP SDA |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/ Analog Output (Column 0) |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/ Analog Output (Column 1) / Capsense Ref Cap |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/ Capsense Ref Cap |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCL (Secondary)/ ISSP SCLK |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) |
| 9 | | | | V _{SS} | Digital Ground |
| 10 | I/O | | | OCDE | On Chip Debugger Port |
| 11 | I/O | | | OCDO | On Chip Debugger Port |
| 12 | I/O | | | CCLK | On Chip Debugger Port |
| 13 | I/O | | | HCLK | On Chip Debugger Port |
| 14 | I | | | XRES | External Reset |
| 15 | | | | V _{DD} | Digital Power Supply |
| 16 | | | | V _{SS} | Digital Ground |
| 17 | | | | AV _{SS} | Analog Ground |
| 18 | | | | AV _{DD} | Analog Power Supply |
| 19 | | | I | CSN2 | Current Sense Negative Input 2 |
| 20 | | | | CSP2 | Current Sense Positive Input and Power Supply - CSA2 |
| 21 | | | | CSP3 | Current Sense Positive Input and Power Supply - CSA3 |
| 22 | | | I | CSN3 | Current Sense Negative Input 3 |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply |
| 30 | | | | GDV _{SS} | Gate Driver Ground |
| 31 | | | | PGND3 ^[4] | Power FET Ground 3 |
| 32 | | | O | GD3 | External Low Side Gate Driver 3 |
| 33 | | | | SW3 | Power Switch 3 |
| 34 | | | | PGND2 ^[4] | Power FET Ground 2 |
| 35 | | | O | GD2 | External Low Side Gate Driver 2 |
| 36 | | | | SW2 | Power Switch 2 |
| 37 | | | | SW1 | Power Switch 1 |
| 38 | | | O | GD1 | External Low Side Gate Driver 1 |
| 39 | | | | PGND1 ^[4] | Power FET Ground 1 |
| 40 | | | | SW0 | Power Switch 0 |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 |
| 42 | | | | PGND0 ^[4] | Power FET Ground 0 |
| 43 | | | | GDV _{SS} | Gate Driver Ground |

Figure 12-3. CY8CLEDD04DOCD1 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|-------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply |
| 45 | | | I/O | FN0[0] | Function I/O |
| 46 | | | I/O | FN0[1] | Function I/O |
| 47 | | | I/O | FN0[2] | Function I/O |
| 48 | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output |
| 54 | | | | V _{DD} | Digital Power Supply |
| 55 | | | | V _{SS} | Digital Ground |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input |

Note

4. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.4 CY8CLED03D0x 56-Pin Part Pinout (without OCD)

The CY8CLED03D01 and CY8CLED03D02 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-4. CY8CLED03D0x 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description | |
|---------|--------------|----------------|-------------------|----------------------|--|--------------|
| | Digital Rows | Analog Columns | Power Peripherals | | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ ISSP SDATA | |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection | |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/ Analog Output (Column 0) | |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap | |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/ Capsense Ref Cap | |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCL (Secondary)/ ISSP SCLK | |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) | |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) | |
| 9 | | | | V _{SS} | Digital Ground | |
| 10 | | | | NC | No Connect | |
| 11 | | | | NC | No Connect | |
| 12 | | | | NC | No Connect | |
| 13 | | | | NC | No Connect | |
| 14 | I | | | XRES | External Reset | |
| 15 | | | | V _{DD} | Digital Power Supply | |
| 16 | | | | V _{SS} | Digital Ground | |
| 17 | | | | AV _{SS} | Analog Ground | |
| 18 | | | | AV _{DD} | Analog Power Supply | |
| 19 | | | I | CSN2 | Current Sense Negative Input - CSA2 | |
| 20 | | | | CSP2 | Current Sense Positive Input and Power Supply - CSA2 | |
| 21 | | | | DNC ^[5] | Do Not Connect | |
| 22 | | | | DNC ^[5] | Do Not Connect | |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp | |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node | |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative | |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive | |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT | |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN | |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply | |
| 30 | | | | GDV _{SS} | Gate Driver Ground | |
| 31 | | | | PGND3 ^[6] | Power FET Ground 3 | |
| 32 | | | | DNC ^[5] | Do Not Connect | |
| 33 | | | | DNC ^[5] | Do Not Connect | |
| 34 | | | | PGND2 ^[6] | Power FET Ground 2 | |
| 35 | | | O | GD2 | External Low Side Gate Driver 2 | |
| 36 | | | | SW2 | Power Switch 2 | |
| 37 | | | | SW1 | Power Switch 1 | |
| 38 | | | O | GD1 | External Low Side Gate Driver 1 | |
| 39 | | | | PGND1 ^[6] | Power FET Ground 1 | |
| 40 | | | | SW0 | Power Switch 0 | |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 | |
| 42 | | | | PGND0 ^[6] | Power FET Ground 0 | |
| 43 | | | | GDV _{SS} | Gate Driver Ground | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply | |
| 45 | | | | I/O | FN0[0] | Function I/O |
| 46 | | | | I/O | FN0[1] | Function I/O |
| 47 | | | | I/O | FN0[2] | Function I/O |
| 48 | | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 | |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 | |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 | |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 | |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output | |
| 54 | | | | V _{DD} | Digital Power Supply | |
| 55 | | | | V _{SS} | Digital Ground | |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input | |

Figure 12-4. CY8CLED03D0x 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

| Pin No. | Type | | | Name | Description | |
|---------|--------------|----------------|-------------------|-------------------|--|--------------|
| | Digital Rows | Analog Columns | Power Peripherals | | | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply | |
| 45 | | | | I/O | FN0[0] | Function I/O |
| 46 | | | | I/O | FN0[1] | Function I/O |
| 47 | | | | I/O | FN0[2] | Function I/O |
| 48 | | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 | |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 | |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 | |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 | |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output | |
| 54 | | | | V _{DD} | Digital Power Supply | |
| 55 | | | | V _{SS} | Digital Ground | |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input | |

Notes

5. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
6. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.5 CY8CLED03G01 56-Pin Part Pinout (without OCD)

The CY8CLED03G01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-5. CY8CLED03G01 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|----------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ ISSP SDATA |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/ Analog Output (Column 0) |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/ Capsense Ref Cap |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCL (Secondary)/ ISSP SCLK |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) |
| 9 | | | | V _{SS} | Digital Ground |
| 10 | | | | NC | No Connect |
| 11 | | | | NC | No Connect |
| 12 | | | | NC | No Connect |
| 13 | | | | NC | No Connect |
| 14 | I | | | XRES | External Reset |
| 15 | | | | V _{DD} | Digital Power Supply |
| 16 | | | | V _{SS} | Digital Ground |
| 17 | | | | AV _{SS} | Analog Ground |
| 18 | | | | AV _{DD} | Analog Power Supply |
| 19 | | | I | CSN2 | Current Sense Negative Input 2 |
| 20 | | | I | CSP2 | Current Sense Positive Input and Power Supply - CSA2 |
| 21 | | | | DNC ^[1] | Do Not Connect |
| 22 | | | | DNC ^[1] | Do Not Connect |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply |
| 30 | | | | GDV _{SS} | Gate Driver Ground |
| 31 | | | | PGND3 ^[8] | Power FET Ground 3 |
| 32 | | | | DNC ^[1] | Do Not Connect |
| 33 | | | | DNC ^[1] | Do Not Connect |
| 34 | | | | PGND2 ^[8] | Power FET Ground 2 |
| 35 | | | O | GD2 | External Low Side Gate Driver 2 |
| 36 | | | | DNC ^[1] | Do Not Connect |
| 37 | | | | DNC ^[1] | Do Not Connect |
| 38 | | | O | GD1 | External Low Side Gate Driver 1 |
| 39 | | | | PGND1 ^[8] | Power FET Ground 1 |
| 40 | | | | DNC ^[1] | Do Not Connect |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 |
| 42 | | | | PGND0 ^[8] | Power FET Ground 0 |
| 43 | | | | GDV _{SS} | Gate Driver Ground |
| Pin No. | Type | | | Name | Description |
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply |
| 45 | | | | FN0[0] | Function I/O |
| 46 | | | | FN0[1] | Function I/O |
| 47 | | | | FN0[2] | Function I/O |
| 48 | | | | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output |
| 54 | | | | V _{DD} | Digital Power Supply |
| 55 | | | | V _{SS} | Digital Ground |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input |

Figure 12-5. CY8CLED03G01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Notes

- Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
- All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

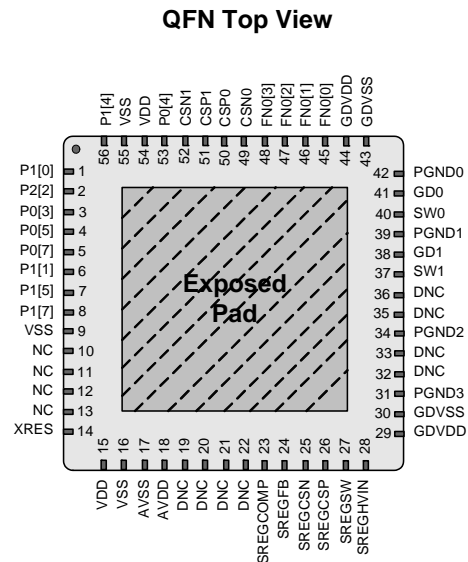
12.6 CY8CLED02D01 56-Pin Part Pinout (without OCD)

The CY8CLED02D01 PowerPSoC devices are available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-6. CY8CLED02D01 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|-----------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ ISSP SDA |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/ Analog Output (Column 0) |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/ Capsense Ref Cap |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCLK (Secondary)/ ISSP SCLK |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) |
| 9 | | | | V _{SS} | Digital Ground |
| 10 | | | | NC | No Connect |
| 11 | | | | NC | No Connect |
| 12 | | | | NC | No Connect |
| 13 | | | | NC | No Connect |
| 14 | I | | | XRES | External Reset |
| 15 | | | | V _{DD} | Digital Power Supply |
| 16 | | | | V _{SS} | Digital Ground |
| 17 | | | | AV _{SS} | Analog Ground |
| 18 | | | | AV _{DD} | Analog Power Supply |
| 19 | | | | DNC ^[9] | Do Not Connect |
| 20 | | | | DNC ^[9] | Do Not Connect |
| 21 | | | | DNC ^[9] | Do Not Connect |
| 22 | | | | DNC ^[9] | Do Not Connect |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply |
| 30 | | | | GDV _{SS} | Gate Driver Ground |
| 31 | | | | PGND3 ^[10] | Power FET Ground 3 |
| 32 | | | | DNC ^[9] | Do Not Connect |
| 33 | | | | DNC ^[9] | Do Not Connect |
| 34 | | | | PGND2 ^[10] | Power FET Ground 2 |
| 35 | | | | DNC ^[9] | Do Not Connect |
| 36 | | | | DNC ^[9] | Do Not Connect |
| 37 | | | | SW1 | Power Switch 1 |
| 38 | | | O | GD1 | External Low Side Gate Driver 1 |
| 39 | | | | PGND1 ^[10] | Power FET Ground 1 |
| 40 | | | | SW0 | Power Switch 0 |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 |
| 42 | | | | PGND0 ^[10] | Power FET Ground 0 |
| 43 | | | | GDV _{SS} | Gate Driver Ground |
| Pin No. | Digital Rows | Analog Columns | Power Peripherals | Name | Description |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply |
| 45 | | | I/O | FN0[0] | Function I/O |
| 46 | | | I/O | FN0[1] | Function I/O |
| 47 | | | I/O | FN0[2] | Function I/O |
| 48 | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 |
| 51 | | | | CSP1 | Current Sense Positive Input and Power Supply - CSA1 |
| 52 | | | I | CSN1 | Current Sense Negative Input 1 |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output |
| 54 | | | | V _{DD} | Digital Power Supply |
| 55 | | | | V _{SS} | Digital Ground |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input |

Figure 12-6. CY8CLED02D01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

Notes

- 9. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
- 10. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

12.7 CY8CLED01D01 56-Pin Part Pinout (without OCD)

The CY8CLED01D01 PowerPSoC device is available with the following pinout information. Every port pin (labeled with a “P” and “FN0”) is capable of Digital I/O.

Table 12-7. CY8CLED01D01 56-Pin Part Pinout (QFN)

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|-----------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 1 | I/O | I | | P1[0] | GPIO/I ² C SDA (Secondary)/ ISSP SDATA |
| 2 | I/O | I | | P2[2] | GPIO/Direct Switch Cap connection |
| 3 | I/O | I/O | | P0[3] | GPIO/Analog Input (Column 0)/ Analog Output (Column 0) |
| 4 | I/O | I/O | | P0[5] | GPIO/Analog Input (Column 0)/ Analog Output (Column 1)/ Capsense Ref Cap |
| 5 | I/O | I | | P0[7] | GPIO/Analog Input (Column 0)/ Capsense Ref Cap |
| 6 | I/O | I | | P1[1] | GPIO/I ² C SCLK (Secondary)/ ISSP SCLK |
| 7 | I/O | I | | P1[5] | GPIO/I ² C SDA (Primary) |
| 8 | I/O | I | | P1[7] | GPIO/I ² C SCL (Primary) |
| 9 | | | | V _{SS} | Digital Ground |
| 10 | | | | NC | No Connect |
| 11 | | | | NC | No Connect |
| 12 | | | | NC | No Connect |
| 13 | | | | NC | No Connect |
| 14 | I | | | XRES | External Reset |
| 15 | | | | V _{DD} | Digital Power Supply |
| 16 | | | | V _{SS} | Digital Ground |
| 17 | | | | AV _{SS} | Analog Ground |
| 18 | | | | AV _{DD} | Analog Power Supply |
| 19 | | | | DNC ^[1] | Do Not Connect |
| 20 | | | | DNC ^[1] | Do Not Connect |
| 21 | | | | DNC ^[1] | Do Not Connect |
| 22 | | | | DNC ^[1] | Do Not Connect |
| 23 | | | | SREGCOMP | Voltage Regulator Error Amp Comp |
| 24 | | | I | SREGFB | Regulator Voltage Mode Feedback Node |
| 25 | | | I | SREGCSN | Current Mode Feedback Negative |
| 26 | | | I | SREGCSP | Current Mode Feedback Positive |
| 27 | | | O | SREGSW | Switch Mode Regulator OUT |
| 28 | | | | SREGHVIN | Switch Mode Regulator IN |
| 29 | | | | GDV _{DD} | Gate Driver Power Supply |
| 30 | | | | GDV _{SS} | Gate Driver Ground |
| 31 | | | | PGND3 ^[12] | Power FET Ground 3 |
| 32 | | | | DNC ^[1] | Do Not Connect |
| 33 | | | | DNC ^[1] | Do Not Connect |
| 34 | | | | PGND2 ^[12] | Power FET Ground 2 |
| 35 | | | | DNC ^[1] | Do Not Connect |
| 36 | | | | DNC ^[1] | Do Not Connect |
| 37 | | | | DNC ^[1] | Do Not Connect |
| 38 | | | | DNC ^[1] | Do Not Connect |
| 39 | | | | PGND1 ^[12] | Power FET Ground 1 |
| 40 | | | | SW0 | Power Switch 0 |
| 41 | | | O | GD0 | External Low Side Gate Driver 0 |
| 42 | | | | PGND0 ^[12] | Power FET Ground 0 |
| 43 | | | | GDV _{SS} | Gate Driver Ground |

Figure 12-7. CY8CLED01D01 56-Pin PowerPSoC Device



*** Connect Exposed Pad to PGNDx**

| Pin No. | Type | | | Name | Description |
|---------|--------------|----------------|-------------------|--------------------|--|
| | Digital Rows | Analog Columns | Power Peripherals | | |
| 44 | | | | GDV _{DD} | Gate Driver Power Supply |
| 45 | | | I/O | FN0[0] | Function I/O |
| 46 | | | I/O | FN0[1] | Function I/O |
| 47 | | | I/O | FN0[2] | Function I/O |
| 48 | | | I/O | FN0[3] | Function I/O |
| 49 | | | I | CSN0 | Current Sense Negative Input 0 |
| 50 | | | | CSP0 | Current Sense Positive Input and Power Supply - CSA0 |
| 51 | | | | DNC ^[1] | Do Not Connect |
| 52 | | | | DNC ^[1] | Do Not Connect |
| 53 | I/O | I | | P0[4] | GPIO/Analog Input (Column 1) / Bandgap Output |
| 54 | | | | V _{DD} | Digital Power Supply |
| 55 | | | | V _{SS} | Digital Ground |
| 56 | I/O | I | | P1[4] | GPIO / External Clock Input |

Notes

11. Do Not Connect (DNC) pins must be left unconnected, or floating. Connecting these pins to power or ground may cause improper operation or failure of the device.
12. All PGNDx pins must be connected to the ground plane on the PCB irrespective of whether the corresponding PowerPSoC channel is used or not.

13. Register General Conventions

13.1 Abbreviations Used

The register conventions specific to this section are listed in [Table 13-1](#).

Table 13-1. Register Conventions

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

13.2 Register Naming Conventions

The register naming convention specific to the PSoC core section of PowerPSoC blocks and their registers is:

<Prefix>mn<Suffix>

where m = row index, n = column index

Therefore, ASD13CR3 is a register for an analog PowerPSoC block in row 1 column 3.

The register naming convention specific to the power peripheral section of PowerPSoC blocks and their registers is:

<Prefix>x<Suffix>

where x = number of channel

Therefore, CSA0_CR is a register for a power peripheral PowerPSoC block in for Current Sense Amplifier, channel 0.

13.3 Register Mapping Tables

The PowerPSoC device has a total register address space of 512 bytes. The register space is also referred to as I/O space and is broken into two parts. The XIO bit in the Flag register (CPU_F) determines which bank you are currently in. When the XIO bit is set, you are said to be in the “extended” address space or the “configuration” registers.

More detailed description of the Registers are found in the PowerPSoC TRM. The TRM can be found at <http://www.cypress.com/powerpsoc> and clicking on the Technical Reference Manual link.



CY8CLED04D01, CY8CLED04D02, CY8CLED04G01 CY8CLED03D01, CY8CLED03D02, CY8CLED03G01 CY8CLED02D01, CY8CLED01D01

13.4 Register Map Bank 0 Table

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|-----------|--------------|--------|------------|--------------|--------|-----------|--------------|--------|-----------|--------------|--------|
| PRT0DR | 00 | RW | DPWM0PCF | 40 | RW | ASC10CR0 | 80 | RW | VDAC0_CR | C0 | RW |
| PRT0IE | 01 | RW | DPWM0PDH | 41 | RW | ASC10CR1 | 81 | RW | VDAC0_DR0 | C1 | RW |
| PRT0GS | 02 | RW | DPWM0PDL | 42 | RW | ASC10CR2 | 82 | RW | VDAC0_DR1 | C2 | RW |
| PRT0DM2 | 03 | RW | DPWM0PWH | 43 | RW | ASC10CR3 | 83 | RW | | C3 | |
| PRT1DR | 04 | RW | DPWM0PWL | 44 | RW | ASD11CR0 | 84 | RW | VDAC1_CR | C4 | RW |
| PRT1IE | 05 | RW | DPWM0PCH | 45 | RW | ASD11CR1 | 85 | RW | VDAC1_DR0 | C5 | RW |
| PRT1GS | 06 | RW | DPWM0PCL | 46 | RW | ASD11CR2 | 86 | RW | VDAC1_DR1 | C6 | RW |
| PRT1DM2 | 07 | RW | DPWM0GCFG | 47 | RW | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | DPWM1PCF | 48 | RW | | 88 | | VDAC2_CR | C8 | RW |
| PRT2IE | 09 | RW | DPWM1PDH | 49 | RW | | 89 | | VDAC2_DR0 | C9 | RW |
| PRT2GS | 0A | RW | DPWM1PDL | 4A | RW | | 8A | | VDAC2_DR1 | CA | RW |
| PRT2DM2 | 0B | RW | DPWM1PWH | 4B | RW | | 8B | | | CB | |
| FN0DR | 0C | RW | DPWM1PWL | 4C | RW | | 8C | | VDAC3_CR | CC | RW |
| FN0IE | 0D | RW | DPWM1PCH | 4D | RW | | 8D | | VDAC3_DR0 | CD | RW |
| FN0GS | 0E | RW | DPWM1PCL | 4E | RW | | 8E | | VDAC3_DR1 | CE | RW |
| FN0DM2 | 0F | RW | DPWM1GCFG | 4F | RW | | 8F | | | CF | |
| | 10 | | DPWM2PCF | 50 | RW | ASD20CR0 | 90 | RW | CUR_PP | D0 | RW |
| | 11 | | DPWM2PDH | 51 | RW | ASD20CR1 | 91 | RW | STK_PP | D1 | RW |
| | 12 | | DPWM2PDL | 52 | RW | ASD20CR2 | 92 | RW | | D2 | |
| | 13 | | DPWM2PWH | 53 | RW | ASD20CR3 | 93 | RW | IDX_PP | D3 | RW |
| | 14 | | DPWM2PWL | 54 | RW | ASC21CR0 | 94 | RW | MVR_PP | D4 | RW |
| | 15 | | DPWM2PCH | 55 | RW | ASC21CR1 | 95 | RW | MVW_PP | D5 | RW |
| | 16 | | DPWM2PCL | 56 | RW | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| | 17 | | DPWM2GCFG | 57 | RW | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| PDMUX_S1 | 18 | RW | DPWM3PCF | 58 | RW | | 98 | | I2C_DR | D8 | RW |
| PDMUX_S2 | 19 | RW | DPWM3PDH | 59 | RW | | 99 | | I2C_MSCR | D9 | # |
| PDMUX_S3 | 1A | RW | DPWM3PDL | 5A | RW | | 9A | | INT_CLR0 | DA | RW |
| PDMUX_S4 | 1B | RW | DPWM3PWH | 5B | RW | | 9B | | INT_CLR1 | DB | RW |
| PDMUX_S5 | 1C | RW | DPWM3PWL | 5C | RW | VDAC6_CR | 9C | RW | INT_CLR2 | DC | RW |
| PDMUX_S6 | 1D | RW | DPWM3PCH | 5D | RW | VDAC6_DR0 | 9D | RW | INT_CLR3 | DD | RW |
| | 1E | | DPWM3PCL | 5E | RW | VDAC6_DR1 | 9E | RW | INT_MSK3 | DE | RW |
| CHBOND_CR | 1F | RW | DPWM3GCFG | 5F | RW | | 9F | | INT_MSK2 | DF | RW |
| DBB0DR0 | 20 | # | AMX_IN | 60 | RW | VDAC4_CR | A0 | RW | INT_MSK0 | E0 | RW |
| DBB0DR1 | 21 | W | AMUX_CFG | 61 | RW | VDAC4_DR0 | A1 | RW | INT_MSK1 | E1 | RW |
| DBB0DR2 | 22 | RW | | 62 | | VDAC4_DR1 | A2 | RW | INT_VC | E2 | RC |
| DBB0CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB0DR0 | 24 | # | CMP_CR0 | 64 | # | VDAC5_CR | A4 | RW | DEC_DH | E4 | RC |
| DBB0DR1 | 25 | W | ASY_CR | 65 | # | VDAC5_DR0 | A5 | RW | DEC_DL | E5 | RC |
| DBB0DR2 | 26 | RW | CMP_CR1 | 66 | RW | VDAC5_DR1 | A6 | RW | DEC_CR0 | E6 | RW |
| DBB0CR0 | 27 | # | PAMUX_S1 | 67 | RW | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | PAMUX_S2 | 68 | RW | MUL1_X | A8 | W | MUL0_X | E8 | W |
| DCB02DR1 | 29 | W | PAMUX_S3 | 69 | RW | MUL1_Y | A9 | W | MUL0_Y | E9 | W |
| DCB02DR2 | 2A | RW | PAMUX_S4 | 6A | RW | MUL1_DH | AA | R | MUL0_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | MUL1_DL | AB | R | MUL0_DL | EB | R |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | ACC1_DR1 | AC | RW | ACC0_DR1 | EC | RW |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | ACC1_DR0 | AD | RW | ACC0_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | ACC1_DR3 | AE | RW | ACC0_DR3 | EE | RW |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | ACC1_DR2 | AF | RW | ACC0_DR2 | EF | RW |
| DBB10DR0 | 30 | # | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10DR1 | 31 | W | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10DR2 | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBB10CR0 | 33 | # | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11DR0 | 34 | # | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11DR1 | 35 | W | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11DR2 | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBB11CR0 | 37 | # | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12DR0 | 38 | # | DPWM0PCFG | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12DR1 | 39 | W | DPWM1PCFG | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12DR2 | 3A | RW | DPWM2PCFG | 7A | RW | RDI1IS | BA | RW | | FA | |
| DCB12CR0 | 3B | # | DPWM3PCFG | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13DR0 | 3C | # | DPWMINTFLG | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13DR1 | 3D | W | DPWMINTMSK | 7D | RW | RDI1RO0 | BD | RW | DAC_D | FD | RW |
| DCB13DR2 | 3E | RW | DPWMSYNC | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCB13CR0 | 3F | # | | 7F | | | BF | | CPU_SCR0 | FF | # |



**CY8CLED04D01, CY8CLED04D02, CY8CLED04G01
CY8CLED03D01, CY8CLED03D02, CY8CLED03G01
CY8CLED02D01, CY8CLED01D01**

13.5 Register Map Bank 1 Table: User Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---------|--------------|--------|-----------|--------------|--------|----------|--------------|--------|-------------|--------------|--------|
| PRT0DM0 | 00 | RW | CSA0_CR | 40 | RW | ASC10CR0 | 80 | RW | CMPCH0_CR | C0 | RW |
| PRT0DM1 | 01 | RW | | 41 | | ASC10CR1 | 81 | RW | CMPCH2_CR | C1 | RW |
| PRT0IC0 | 02 | RW | | 42 | | ASC10CR2 | 82 | RW | CMPCH4_CR | C2 | RW |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | CMPCH6_CR | C3 | RW |
| PRT1DM0 | 04 | RW | CSA1_CR | 44 | RW | ASD11CR0 | 84 | RW | CMPBNK8_CR | C4 | RW |
| PRT1DM1 | 05 | RW | | 45 | | ASD11CR1 | 85 | RW | CMPBNK9_CR | C5 | RW |
| PRT1IC0 | 06 | RW | | 46 | | ASD11CR2 | 86 | RW | CMPBNK10_CR | C6 | RW |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | CMPBNK11_CR | C7 | RW |
| PRT2DM0 | 08 | RW | CSA2_CR | 48 | RW | | 88 | | CMPBNK12_CR | C8 | RW |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | CMPBNK13_CR | C9 | RW |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| FN0DM0 | 0C | RW | CSA3_CR | 4C | RW | | 8C | | | CC | |
| FN0DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| FN0IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| FN0IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | ASC21CR0 | 94 | RW | HYSCTLR0CR | D4 | RW |
| | 15 | | | 55 | | ASC21CR1 | 95 | RW | HYSCTLR1CR | D5 | RW |
| | 16 | | | 56 | | ASC21CR2 | 96 | RW | HYSCTLR2CR | D6 | RW |
| | 17 | | | 57 | | ASC21CR3 | 97 | RW | HYSCTLR3CR | D7 | RW |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | | DB | |
| | 1C | | | 5C | | | 9C | | SREG_TST | DC | RW |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | DEC_CR2 | E7 | RW |
| DCB02FN | 28 | RW | ALT_CR1 | 68 | RW | | A8 | | IMO_TR | E8 | RW |
| DCB02IN | 29 | RW | CLK_CR2 | 69 | RW | | A9 | | ILO_TR | E9 | RW |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | | EB | |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | AMUX_CLK | AF | RW | | EF | |
| DBB10FN | 30 | RW | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10IN | 31 | RW | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10OU | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11FN | 34 | RW | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB01IN | 35 | RW | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB01OU | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12FN | 38 | RW | | 78 | | RDI1RI | B8 | RW | | F8 | |
| DCB12IN | 39 | RW | GDRV0_CR | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12OU | 3A | RW | | 7A | | RDI1IS | BA | RW | | FA | |
| | 3B | | GDRV1_CR | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13FN | 3C | RW | | 7C | | RDI1LT1 | BC | RW | | FC | |
| DCB13IN | 3D | RW | GDRV2_CR | 7D | RW | RDI1RO0 | BD | RW | DAC_CR | FD | RW |
| DCB13OU | 3E | RW | | 7E | | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| | 3F | | GDRV3_CR | 7F | RW | | BF | | CPU_SCR0 | FF | # |

14. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 of the PowerPSoC device family. For the most up to date electrical specifications, confirm that you have the most recent datasheet by going to the web at <http://www.cypress.com/powerpsoc>. Specifications for Industrial rated devices are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, $T_J \leq 115\text{ }^{\circ}\text{C}$ and for Extended Temperature rated devices for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$, $T_J \leq 125\text{ }^{\circ}\text{C}$, except where noted.

14.1 Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. Not all user guidelines are production tested.

Table 14-1. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|--|----------------|-----|----------------|--|--|
| T_{STG} | Storage temperature | -55 | - | +115 | $^{\circ}\text{C}$ | Higher storage temperatures reduces data retention time. Recommended storage temperature is $0\text{ }^{\circ}\text{C}$ to $50\text{ }^{\circ}\text{C}$. |
| T_A | Ambient temperature with power applied | -40 -40 | - | +85 +105 | $^{\circ}\text{C}$ $^{\circ}\text{C}$ | $T_J \leq 115\text{ }^{\circ}\text{C}$ (Industrial rated) $T_J \leq 125\text{ }^{\circ}\text{C}$ (Extended Temperature rated) |
| V_{DD} , AV_{DD} , GDV_{DD} | Supply voltage on V_{DD} , AV_{DD} , and GDV_{DD} | -0.5 | - | +6.0 | V | Relative to V_{SS} , AV_{SS} , and GDV_{SS} respectively |
| V_{IO} | DC input voltage | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | Applies only to GPIO and FNO pins |
| V_{IO2} | DC voltage applied to tristate | $V_{SS} - 0.5$ | - | $V_{DD} + 0.5$ | V | |
| V_{FET} | Maximum voltage from power Switch (SWx) to Power FET Ground (PGNDx) | - | - | $36^{[13]}$ | V | PGNDx is connected to GDV_{SS} |
| V_{REGIN} | Maximum voltage on SREGHVIN Pin relative to V_{SS} | - | - | $36^{[13]}$ | V | |
| V_{CSP}, V_{CSN} | Maximum voltage applied to CSA pins relative to V_{SS} | -0.5 | - | $36^{[13]}$ | V | |
| V_{SENSE} | Maximum input differential voltage across CSA input | -1.0 | - | 1.0 | V | |
| I_{MAIO} | Maximum current into any port pin configured as analog driver | -50 | - | +50 | mA | |
| I_{MIO} | Maximum current into any port and function pin | -25 | - | +50 | mA | |
| LU | Latch up current | 200 | - | - | mA | JESD78A Conformal |
| ESD | Electrostatic Discharge Voltage | 2000 | - | - | V | Human Body Model ESD. |
| SR_{REGIN} | Ramp Rate for the SREGHVIN pin | - | - | 32 | V/ μs | |
| SR_{CSP} | Ramp Rate for the CSPx pins | - | - | 3.2 | V/ μs | |
| $SR_{HV_{DD-FLB}}$ | High Voltage Supply Ramp Rate for Floating Load Buck Configuration | - | - | 15 | V/ms | For other topologies, to enable operation with faster ramp rates, or if the LED string voltage is $< 6.5\text{ V}$, see the <i>PowerPSoC Technical Reference Manual</i> . |
| $SR_{V_{DD-EXT}}$ | External V_{DD} Supply Ramp Rate (V_{DD} , AV_{DD} , and GDV_{DD} pins) | - | - | 0.2 | V/ μs | Applies only when powered by a source other than the Built-in Switching Regulator |

Note

13. Stresses beyond the "Absolute Maximum Ratings" on page 29 may cause permanent damage to the device. You must ensure that the Absolute Maximum Ratings are NEVER exceeded. Functional operation is not implied under any conditions beyond the "Electrical Characteristics" on page 30 onwards. Extended exposure to "Absolute Maximum Ratings" on page 29 may affect reliability of the device.

14.2 Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|--|
| T _A | Ambient Temperature | -40 | - | +85 | °C | T _J ≤ 115 °C (Industrial rated) T _J ≤ 125 °C (Extended Temperature rated) |
| | | -40 | - | +105 | °C | |
| T _J | Junction Temperature | -40 | - | +115 | °C | Industrial rated Extended Temperature rated |
| | | -40 | - | +125 | °C | |

15. Electrical Characteristics

15.1 System Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, T_J ≤ 115 °C for Industrial rated devices and 4.75 V to 5.25 V, T_J ≤ 125 °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-1. System Level Operating Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|---|------|-----|-----|-------|--|
| f _{SW} | Circuit switching frequency range for hysteretic control loop | 0.02 | - | 2 | MHz | |
| t _{D,MAX} | Maximum Delay Time from CSA input to FET state change | - | - | 100 | ns | HV _{DD} = 24 V, I _D = 1 A, f _{SW} = 2 MHz (Industrial rated) HV _{DD} = 24 V, I _D = 1 A, f _{SW} = 2 MHz (Extended Temperature rated) |
| | | - | - | 115 | ns | |
| D | Output duty cycle for hysteretic controllers | 5 | - | 95 | % | f _{SW} < 0.25 MHz |
| E | Power converter efficiency | 90 | 95 | - | % | HV _{DD} = 24 V, I _D = 1 A, f _{SW} = 2 MHz |

15.2 Chip Level

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, T_J ≤ 115 °C for Industrial rated devices and 4.75 V to 5.25 V, T_J ≤ 125 °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note See the *PowerPSoC Technical Reference Manual* for more information on the DPWMxPCF register

Table 15-2. Chip Level DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--|---|------|-----|------|-------|--|
| V _{DD} , AV _{DD} , GDV _{DD} | Digital, analog, and gate driver supply voltage range | 4.75 | - | 5.25 | V | All should be powered from the same source. |
| HV _{DD} | Power converter high voltage supply range | 7 | - | 32 | V | |
| HV _{PINS} | Voltage range for the CSPx and SREGHVIN pins | 7 | - | 32 | V | Not all pins need to be at the same voltage level. |
| I _{VDD} | Supply current (V _{DD} pins), IMO = 24 MHz | - | 16 | 50 | mA | Conditions are V _{DD} = 5 V, T _J = 25 °C, CPU = 3 MHz, SYSClk doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off. |
| I _{AVDD} | Supply current (AV _{DD} pin) | - | - | 25 | mA | Conditions are V _{DD} = 5 V, T _J = 25 °C, |

Table 15-2. Chip Level DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|---|--------|----------|-----------|----------|---|
| $I_{GD}V_{DD}$ | Supply current per channel (GDV _{DD} pins) | – – | – – | 25 100 | mA mA | Internal Power FET at 2 MHz External Gate Driver at 1 MHz, C _L = 4 nF at V _{DD} = 5 V |
| I_{SB} | Sleep (mode) current with POR, LVD, sleep timer, and WDT. | – – | 18 30 | 25 550 | μA μA | T _J = 25 °C, Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = off T _J = 115 °C (Industrial rated) and T _J = 125 °C (Extended Temperature rated), Built-in Switching Regulator disabled, DPWMxPCF = 0, Power Peripherals disabled, analog power = OFF |

Table 15-3. Chip Level AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------------|---|-------|-----|-----------------------|-------|---|
| f_{IMO24} | Internal main oscillator frequency for 24 MHz | 23.04 | 24 | 24.96 | MHz | |
| f_{CPU1} | CPU frequency | 0.093 | 24 | 24.96 | MHz | |
| f_{BLK} | Digital PSoC Block frequency | 0 | 48 | 49.92 ^[14] | MHz | Refer to “PSoC Core Digital Block Specifications” on page 48. |
| f_{32K1} | Internal low-speed oscillator frequency | 15 | 32 | 64 | kHz | |
| f_{32K_U} | Internal low speed oscillator (ILO) untrimmed frequency | 5 | – | – | kHz | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PowerPSoC Technical Reference Manual for details on timing this. |
| DC _{ILO} | Internal low speed oscillator duty cycle | 20 | 50 | 80 | % | |
| Jitter _{32K} | 32 kHz period jitter | – | 100 | – | ns | |
| Jitter _{24M1} | 24 MHz period jitter (IMO) peak-to-peak | – | 600 | – | ps | |
| $t_{POWERUP}$ | Time from end of POR to CPU executing code | – | 30 | 100 | ms | Power up from 0 V. See the System Resets section of the PowerPSoC Technical Reference Manual. |

Figure 15-1. 24 MHz Period Jitter (IMO) Timing Diagram



Note

14. See the individual user module datasheets for information on maximum frequencies for user modules.

15.3 Power Peripheral Low Side N-Channel FET

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25°C . These are for design guidance only.

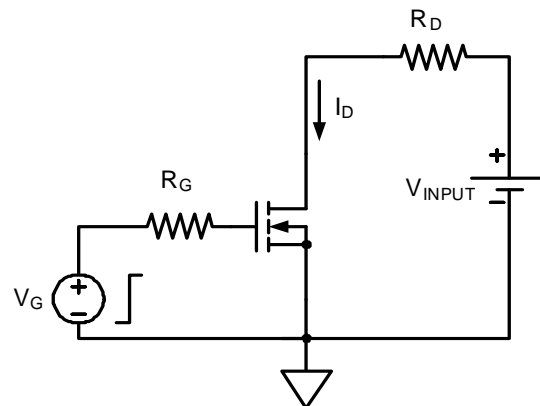
Table 15-4. Low Side N-Channel FET DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|---|-----|-----|-----------|--------------------------------|---|
| V_{DS} | Operating drain to source voltage | – | – | 32 | V | |
| $V_{DS,INST}$ | Instantaneous drain source voltage | – | – | 36 | V | |
| I_D | Average drain current | – | – | 1 0.5 | A A | CY8CLED04/3/2/1D01 devices CY8CLED04/3D02 devices |
| $I_{D,MAX}$ | Maximum instantaneous repetitive pulsed current | – | – | 3 1.5 | A A | Less than 33% duty cycle for an average current of 1 A, $f_{SW} = 0.1$ MHz. CY8CLED04/3/2/1D01 devices Less than 33% duty cycle for an average current of 0.5 A, $f_{SW} = 0.1$ MHz. CY8CLED04/3D02 devices |
| $R_{DS(ON)}$ | Drain to source ON resistance | – | – | 0.5 1 | Ω Ω | $I_D = 1$ A, $GDV_{DD} = 5$ V, $T_J = 25^\circ\text{C}$ CY8CLED04/3/2/1D01 devices $I_D = 0.5$ A, $GDV_{DD} = 5$ V, $T_J = 25^\circ\text{C}$ CY8CLED04/3D02 devices |
| I_{DSS} | Switching node to PGND leakage | – | – | 10 250 | μA μA | $T_J = 25^\circ\text{C}$ $T_J = 115^\circ\text{C}$ (Industrial rated) and $T_J = 125^\circ\text{C}$ (Extended Temperature rated) |
| I_{SFET} | Supply current per channel - FET (internal gate driver) | – | – | 6.25 | mA | $f_{SW} = 2$ MHz |

Table 15-5. Low Side N-Channel FET AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------|-------------|-----|-----|-----|-------|--------------------------------|
| t_R | Rise time | – | – | 20 | ns | $I_D = 1$ A, $R_D = 32 \Omega$ |
| t_F | Fall time | – | – | 20 | ns | $I_D = 1$ A, $R_D = 32 \Omega$ |

Figure 15-2. Low Side N-Channel FET Test Circuit for I_{DSS} , t_R , and t_F



15.4 Power Peripheral External Power FET Driver

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115\text{ }^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125\text{ }^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-6. Power FET Driver DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|--|------------------------------------|-----|-------------|--------|---|
| V_{OHN} | N-channel FET driver output voltage -drive high | $V_{DD} - 0.45$ $V_{DD} - 0.10$ | – | – | V V | $I_{OH} = 100\text{ mA}$ $I_{OH} = 10\text{ mA}$ |
| V_{OLN} | N-channel FET driver output voltage -drive low | – | – | 0.45 0.1 | V V | $I_{OL} = 100\text{ mA}$ $I_{OL} = 10\text{ mA}$ |
| $I_{SFETDRV}$ | Supply current per channel - external FET driver | – | – | 25 | mA | $C_L = 4\text{ nF}$ $F_{SW} = 1\text{ MHz}$ |

Table 15-7. Power FET Driver AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|---------------------------------|-----|-----|-----|-------|---------------------|
| t_R | Rise time | – | 45 | 55 | ns | $C_L = 4\text{ nF}$ |
| t_F | Fall time | – | 45 | 55 | ns | |
| $t_{P(LH)}$ | Propagation delay (low-to-high) | – | – | 10 | ns | |
| $t_{P(HL)}$ | Propagation delay (high-to-low) | – | – | 10 | ns | |

15.5 Power Peripheral Hysteretic Controller

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115\text{ }^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125\text{ }^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-8. Hysteretic Controller DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------|--|-----|-----|-----------------|----------------|---|
| V_{IO} | Comparator input offset voltage | – | – | 7.5 10 15 | mV mV mV | $1\text{ V} \leq V_{ICM} \leq 3\text{ V}$ (Industrial rated) $1\text{ V} \leq V_{ICM} \leq 3\text{ V}$ (Extended Temperature rated) $0\text{ V} \leq V_{ICM} \leq V_{DD}$ |
| V_{ICM} | Input common mode voltage range | 0 | – | V_{DD} | V | |
| V_{HYS} | Hysteresis voltage | 4.5 | – | 11 13 | mV mV | $1.5\text{ V} \leq V_{ICM} \leq 2.5\text{ V}$ (Industrial rated) $1.5\text{ V} \leq V_{ICM} \leq 2.5\text{ V}$ (Extended Temperature rated) |
| I_{SHYST} | Supply current - hysteretic controller | – | 2 | – | mA | Includes two Power Peripheral Comparators and one Reference DAC, $f_{SW} = 2\text{ MHz}$ |

Table 15-9. Hysteretic Controller AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|----------------------|-----|-----|-----|-------|-------|
| t_{ON} / t_{OFF} | Minimum ON/OFF timer | | | | | |

Table 15-9. Hysteretic Controller AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------|--------------------|-----|-----|-----|-------|-----------------|
| | MONOSHOT<1:0> = 00 | 10 | – | 30 | ns | |
| | MONOSHOT<1:0> = 01 | 20 | – | 60 | ns | |
| | MONOSHOT<1:0> = 10 | 40 | – | 110 | ns | |
| | MONOSHOT<1:0> = 11 | – | – | – | ns | Timers Disabled |

15.6 Power Peripheral Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

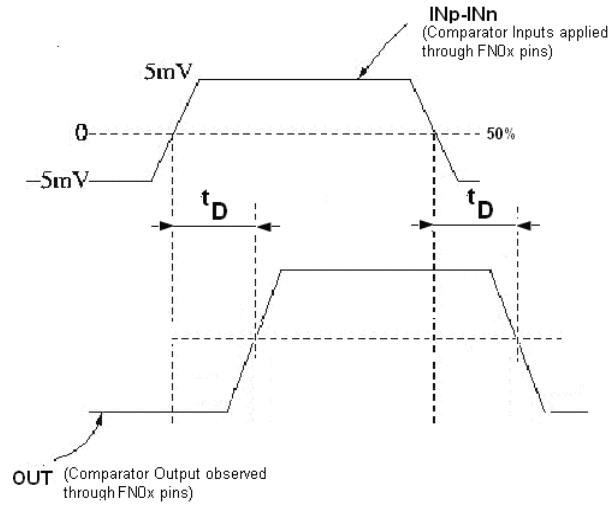
Table 15-10. Comparator DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|--|-----|-----|----------|---------------|---|
| V_{IN} | Input voltage range | 0 | – | V_{DD} | V | |
| V_{IO} | Comparator input offset voltage | – | – | 7.5 | mV | $1\text{ V} \leq V_{ICM} \leq 3\text{ V}$ (Industrial rated) $1\text{ V} \leq V_{ICM} \leq 3\text{ V}$ (Extended Temperature rated) $0\text{ V} \leq V_{ICM} \leq V_{DD}$ |
| | | – | – | 10 | mV | |
| | | – | – | 15 | mV | |
| V_{HYS} | Hysteresis voltage | 2.5 | – | 30 | mV | $0\text{ V} < V_{ICM} < V_{DD}$ $1.5\text{ V} \leq V_{ICM} \leq 2.5\text{ V}$ (Industrial rated) $1.5\text{ V} \leq V_{ICM} \leq 2.5\text{ V}$ (Extended Temperature rated) |
| | | 4.5 | – | 11 | mV | |
| | | 4.5 | – | 13 | mV | |
| V_{OVDV} | Overdrive voltage | 5 | – | – | mV | |
| I_{SCOMP} | Supply current - comparator | – | – | 650 | μA | |
| $V_{ICM,COMP}$ | Comparator input common mode voltage range | 0 | – | V_{DD} | V | |

Table 15-11. Comparator AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------|--|-----|-----|-----|-------|--|
| t_D | Comparator delay time (FN0[x] pin to FN0[x] pin) | – | 150 | – | ns | $V_{OVDV} = 5\text{ mV}$, $C_L = 10\text{ pF}$ at $V_{DD} = 5\text{ V}$ |

Figure 15-3. Comparator Timing Diagram



15.7 Power Peripheral Current Sense Amplifier

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to V_{DD} of 5 V and HV_{DD} of 32 V at 25°C . These are for design guidance only.

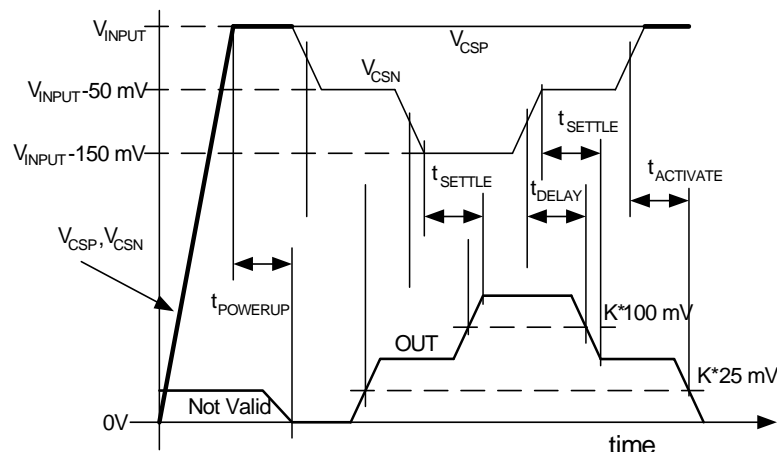
Table 15-12. Current Sense Amplifier DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------------|---|------|-----|------|---------------|---|
| V_{ICM} | Input common mode voltage operating range | 7 | – | 32 | V | Either terminal of the amplifier must not exceed this range for functionality |
| $V_{ICM(\text{Tolerant})}$ | Non functional operating range | 0 | – | 32 | | Absolute maximum rating for V_{SENSE} should never be exceeded. See Absolute Maximum Ratings on page 29 |
| V_{SENSE} | Input differential voltage range | 0 | – | 150 | mV | |
| $I_{S,CSA}$ | Supply current - CSA | – | – | 1 | mA | Enabling CSA causes an incremental draw of 1 mA on the AV_{DD} rail. |
| I_{BIASP} | Input bias current (+) | – | – | 600 | μA | |
| I_{BIASN} | Input bias current (-) | – | – | 1 | μA | |
| PSR_{HV} | Power supply rejection (CSP pin) | – | – | -25 | dB | $f_{SW} < 2\text{ MHz}$ |
| K | Gain | 19.7 | 20 | 20.3 | V/V | $V_{SENSE} = 50\text{ mV to }130\text{ mV}$ (Industrial rated) |
| | | 19.4 | 20 | 20.6 | V/V | $V_{SENSE} = 50\text{ mV to }130\text{ mV}$ (Extended Temperature rated) |
| V_{IOS} | Input offset | – | 2 | 4 | mV | $V_{SENSE} = 50\text{ mV to }130\text{ mV}$ |
| C_{IN_CSP} | CSP input capacitance | – | – | 5 | pF | |
| C_{IN_CSN} | CSN input capacitance | – | – | 2 | pF | |

Table 15-13. Current Sense Amplifier AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|---|-----|-----|-----|---------------|-------|
| t_{SETTLE} | Output settling time to 1% of final value | – | – | 5 | μs | |
| $t_{POWERUP}$ | Power up time to 1% of final value | – | – | 5 | μs | |

Figure 15-4. Current Sense Amplifier Timing Diagram



15.8 Power Peripheral PWM/PrISM/DMM Specification Table

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only. See the *PowerPSoC Technical Reference Manual* for more information on PWM/PrISM/DMM.

Table 15-14. PWM/PrISM/DMM DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|-------------------------------------|-----|-----|-----|-------|-------|
| $I_{S,Modulation}$ | Supply current - PWM, PrISM, or DMM | – | – | 5 | mA | |

Table 15-15. PWM/PrISM/DMM AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-------------------------------------|-----|------------------------------------|-------|---|
| PWM Mode | | | | | | |
| $f_{RANGE16}$ | PWM output frequency range 16-bit period | $24,000,000/(256*2^{16})$ | – | $48,000,000/2^{16}$ | Hz | Period Value = $2^{16} - 1$, Min: N = 255, Max: N = 0 |
| f_{RANGE8} | PWM output frequency range 8-bit period | $24,000,000/(256*2^8)$ | – | $48,000,000/2^8$ | Hz | Period Value = $2^8 - 1$, Min: N = 255, Max: N = 0 |
| PrISM Mode | | | | | | |
| f_{RANGE} | PrISM output frequency range | $24,000,000/(256*(2^M-1))$ | – | $48,000,000/2$ | Hz | Min: N = 255, Max: N = 0, M = 2 to 16 |
| DMM Mode | | | | | | |
| $f_{RANGE,Dimming}$ | DMM dimming frequency range | $24,000,000/(256*Max\ DMM\ Period)$ | – | $48,000,000/(Min\ DMM\ Period)$ | Hz | Min DMM Period: 2 (Right Aligned), 3 (Center Aligned), 4 (Left Aligned) Max DMM Period: 2^{12} (Right Aligned), 8190 (Center Aligned), 2^{12} (Left Aligned) |
| $f_{RANGE,Dither}$ | DMM dither frequency range | $(1/16)*(Min\ f_{RANGE,Dimming})$ | – | $(15/16)*(Max\ f_{RANGE,Dimming})$ | Hz | |

15.9 Power Peripheral Reference DAC Specification

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-16. Reference DAC DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|------|-----|------|---------------|-----------------------------|
| I_{SDAC} | Supply current - reference DAC | – | – | 600 | μA | Mode 0 and Mode1 |
| INL | Integral non linearity | –1 | – | 1 | LSB | Mode 0 |
| | | –1.5 | – | 1.5 | LSB | Mode 1 |
| DNL | Differential non linearity | –0.5 | – | 0.5 | LSB | Mode 0 and Mode1 |
| A_{ERROR} | Gain error | –5 | – | 5 | LSB | Mode 0 |
| | | –7 | – | 7 | LSB | Mode 1 |
| OS_{ERROR} | Offset error | – | – | 1 | LSB | Mode 0 and Mode1 |
| V_{DACFS} | Fullscale voltage - reference DAC | – | – | 2.6 | LSB | Mode 0 |
| | | – | – | 1.3 | LSB | Mode 1 |
| V_{DACMM} | Fullscale voltage mismatch (pair of reference DACs - even and odd) | – | – | 9 | LSB | Mode 0 (DAC0 through DAC7) |
| | | – | – | 14 | LSB | Mode 1 (DAC0 through DAC7) |
| | | – | – | 10.5 | LSB | Mode 0 (DAC8 through DAC13) |
| | | – | – | 15.5 | LSB | Mode 1 (DAC8 through DAC13) |

Table 15-17. Reference DAC AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|--|-----|-----|------|---------------|------------------|
| t_{SETTLE} | Output settling time to 0.5 LSB of final value | – | – | 10 | μs | Mode 0 and Mode1 |
| $t_{STARTUP}$ | Startup time to within 0.5 LSB of final value | – | – | 10.5 | μs | Mode 0 and Mode1 |

15.10 Power Peripheral Built-in Switching Regulator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-18. Built-in Switching Regulator DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|------|-----|-----|---------------|--|
| V_{REGIN} | Input supply voltage range | 7 | – | 32 | V | Industrial rated Extended Temperature rated See Absolute Maximum Ratings on page 29 |
| | | 8 | – | 32 | V | |
| V_{REGOUT} | Output voltage range | 4.8 | 5.0 | 5.2 | V | Does not include V_{RIPPLE} |
| V_{RIPPLE} | Output ripple | – | – | 100 | mV | |
| V_{UVLO} | Under voltage lockout voltage | 5.5 | – | 6.5 | V | $V_{REGIN} < V_{UVLO}$: Power down mode $V_{REGIN} > V_{UVLO}$: Active mode |
| I_{LOAD} | DC output current -active mode | 0.01 | – | 250 | mA | |
| $I_{S,BSR}$ | Supply current - built-in switching regulator | – | – | 4 | mA | |
| $I_{SB,HV}$ | Standby current (high voltage) | – | – | 250 | μA | |
| I_{INRUSH} | Inrush current | – | – | 1.2 | A | $V_{REGIN} = 32\text{ V}$, $SR_{REGIN} = 32\text{ V/ms}$ (Industrial rated) $V_{REGIN} = 32\text{ V}$, $SR_{REGIN} = 32\text{ V/ms}$ (Extended Temperature rated) |
| | | – | – | 1.5 | A | |
| $R_{DS(ON),PFET}$ | PFET drain to source ON resistance | – | 2.5 | – | Ω | |
| $Line_{REG}$ | Line regulation | – | 1 | – | mV | $I_{LOAD} = 250\text{ mA}$, $V_{REGIN} = 7\text{ V to }32\text{ V}$ |

Table 15-18. Built-in Switching Regulator DC Specifications

| | | | | | | |
|---------------------|---|----|-----|---|----|---|
| Load _{REG} | Load regulation | – | 1 | – | mV | V _{REGIN} = 24 V, I _{LOAD} = 2.5 mA to 250 mA |
| PSRR | Power supply rejection ratio | – | –60 | – | dB | V _{RIPPLE} = 0.2 * V _{REGIN} , f _{RIPPLE} = 1 kHz to 10 kHz |
| E _{BSR} | Built-in switching regulator efficiency | 80 | – | – | % | V _{REGIN} = 24 V, I _{LOAD} = 250 mA |

Table 15-19. Built-in Switching Regulator AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-------|-----|------|-------|---|
| f _{SW} | Switching frequency | 0.956 | 1 | 1.04 | MHz | |
| t _{RESP} | Response time to within 0.5% of final value | – | 10 | – | μs | |
| t _{SU} | Startup time | – | – | 1 | ms | |
| t _{PD} | Power down time | – | – | 100 | μs | |
| t _{PD_ACT} | Time from power down to active mode | – | – | 1 | ms | |
| t _{ACT_PD} | Time from active mode to power down mode | – | – | 50 | μs | |
| SR _{REGIN} | Ramp rate for the SREGHVIN pin | – | – | 32 | V/μs | See Absolute Maximum Ratings on page 29 |

Table 15-20. Built-in Switching Regulator Recommended Components

| Component Name | Value | Unit | Notes |
|--------------------|-------|------|---|
| R _{fb1} | 2 | kΩ | Tolerance 1% or better |
| R _{fb2} | 0.698 | kΩ | Tolerance 1% or better |
| C _{comp} | 2200 | pF | Tolerance 20% or better |
| R _{comp} | 20 | kΩ | Tolerance 5% or better |
| L | 47 | μH | Tolerance 20% or better, Saturation current rating of 1.5 A or higher |
| R _{sense} | 0.5 | Ω | Tolerance 1% or better |
| C ₁ | 10 | μF | Ceramic, X7R grade, Minimum ESR of 0.1Ω |
| C _{in} | 1 | μF | Ceramic, X7R grade |

Note If the built-in switching regulator is not being used in a design, it must be configured as per the following instructions to ensure it is disabled in a safe state.

SREGFB: 5 V

SREGCSN: 5 V

SREGCSP: 5 V

SREGCOMP: Floating

SREGHVIN: ≥ VDD rail

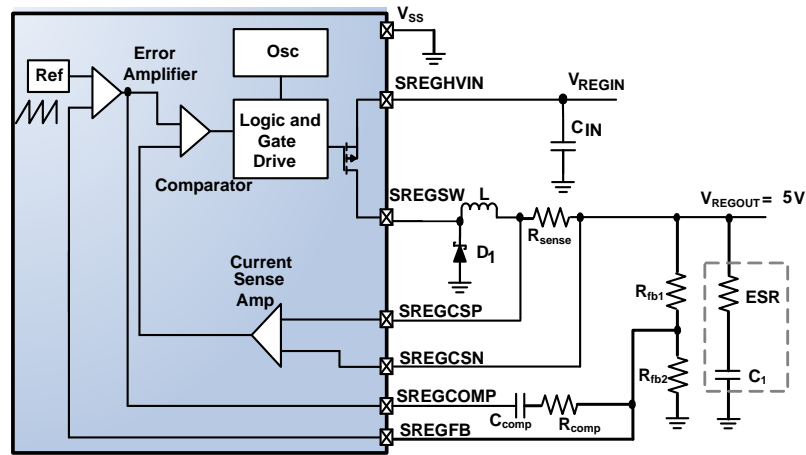
SREGSW: Floating/Tie to SREGHVIN

If the switching regulator is disabled through wiring its input pins (as previously explained) then it must be disabled through software as well (bit SREG_TST[0] = 1), which is set in the Global Resources in the Interconnect View of PSoC Designer.

Figure 15-5. Built-in Switching Regulator Timing Diagram



Figure 15-6. Built-in Switching Regulator



15.11 General Purpose I/O / Function Pin I/O

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

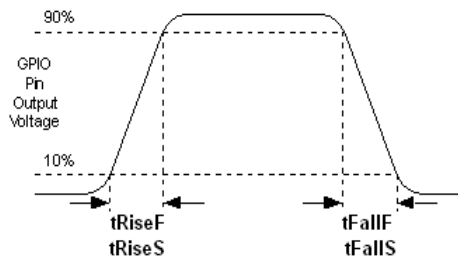
Table 15-21. GPIO/FN0 Pin I/O DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|------------|---|
| R _{PU} | Pull-up resistor | 4 | 5.6 | 8 | k Ω | |
| R _{PD} | Pull-down resistor | 4 | 5.6 | 8 | k Ω | |
| V _{OH} | High output level | V _{DD} - 1.0 | - | - | V | I _{OH} = 10 mA, 80 mA maximum combined I _{OH} budget |
| V _{OL} | Low output level | - | - | 0.75 | V | I _{OL} = 25 mA, 200 mA maximum combined I _{OL} budget |
| I _{OH} | High level source current | 10 | - | - | mA | V _{OH} = V _{DD} - 1.0 V, see the limitations of the total current in the note for V _{OH} |
| I _{OL} | Low level sink current | 25 | - | - | mA | V _{OL} = 0.75 V, see the limitations of the total current in the note for V _{OL} |
| V _{IL} | Input low level | - | - | 0.8 | V | |
| V _{IH} | Input high level | 2.1 | - | - | V | |
| V _H | Input hysteresis | - | 60 | - | mV | |
| I _{IL} | Input leakage (absolute value) | - | 1 | - | nA | Gross tested to 1 μA |
| C _{IN} | Capacitive load on pins as input | - | 3.5 | 10 | pF | T _J = 25 °C. |
| C _{OUT} | Capacitive load on pins as output | - | 3.5 | 10 | pF | T _J = 25 °C. |

Table 15-22. GPIO/FN0 Pin I/O AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|--|-----|-----|-----|-------|--------------------|
| f _{GPIO} | GPIO operating frequency | 0 | - | 12 | MHz | Normal strong mode |
| t _{RiseF} | Rise time, normal strong mode, Cload = 50 pF | 3 | - | 18 | ns | 10% - 90% |
| t _{FallF} | Fall time, normal strong mode, Cload = 50 pF | 2 | - | 18 | ns | |
| t _{RiseS} | Rise time, slow strong mode, Cload = 50 pF | 10 | 27 | - | ns | |
| t _{FallS} | Fall time, slow strong mode, Cload = 50 pF | 10 | 22 | - | ns | |

Figure 15-7. GPIO/Function I/O Timing Diagram



15.12 PSoC Core Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25°C . These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 15-23. Operational Amplifier DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|---|----------------|------|----------------|--------------------------------|---|
| V_{OSOA} | Input offset voltage (absolute value) Power = low, opamp bias = high | – | 1.6 | 10 | mV | Industrial rated |
| | | – | 1.6 | 15 | mV | Extended Temperature rated |
| | Power = medium, opamp bias = high | – | 1.3 | 8 | mV | Industrial rated |
| | | – | 1.3 | 13 | mV | Extended Temperature rated |
| | Power = high, opamp bias = high | – | 1.2 | 7.5 | mV | Industrial rated |
| | | – | 1.2 | 12 | mV | Extended Temperature rated |
| TCV_{OSOA} | Average input offset voltage drift | – | 7.0 | 35.0 | $\mu\text{V} / ^\circ\text{C}$ | |
| I_{EBOA} | Input leakage current (Port 0 analog pins) | – | 20 | – | pA | Gross tested to 1 μA . |
| C_{INOA} | Input capacitance (Port 0 analog pins) | – | 4.5 | 9.5 | pF | $T_J = 25^\circ\text{C}$. |
| V_{CMOA} | Common mode voltage range | 0.0 | – | V_{DD} | V | The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer. |
| | Common mode voltage range (high power or high opamp bias) | 0.5 | – | $V_{DD} - 0.5$ | V | |
| G_{OLOA} | Open loop gain | | | | | |
| | Power = low, opamp bias = high | 60 | – | – | dB | |
| | Power = medium, opamp bias = high | 60 | – | – | dB | |
| | Power = high, opamp bias = high | 80 | – | – | dB | |
| $V_{OHIGHOA}$ | High output voltage swing (internal signals) | | | | | |
| | Power = low, opamp bias = high | $V_{DD} - 0.2$ | – | – | V | |
| | Power = medium, opamp bias = high | $V_{DD} - 0.2$ | – | – | V | |
| | Power = high, opamp bias = high | $V_{DD} - 0.5$ | – | – | V | |
| V_{OLOWA} | Low output voltage swing (internal signals) | | | | | |
| | Power = low, opamp bias = high | – | – | 0.2 | V | |
| | Power = medium, opamp bias = high | – | – | 0.2 | V | |
| | Power = high, opamp bias = high | – | – | 0.5 | V | |
| I_{SOA} | Supply current (including associated analog output buffer) | | | | | |
| | Power = low, opamp bias = low | – | 400 | 800 | μA | |
| | Power = low, opamp bias = high | – | 500 | 900 | μA | |
| | Power = medium, opamp bias = low | – | 800 | 1000 | μA | |
| | Power = medium, opamp bias = high | – | 1200 | 1600 | μA | |
| | Power = high, opamp bias = low | – | 2400 | 3200 | μA | |
| | Power = high, opamp bias = high | – | 4600 | 6400 | μA | |
| $PSRR_{OA}$ | Supply voltage rejection ratio | 52 | 80 | – | dB | $V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25 \text{ V}) \leq V_{IN} \leq V_{DD}$. |

Table 15-24. Operational Amplifier AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|------|-----|------|---------|-------|
| t _{ROA} | Rising settling time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) | | | | | |
| | Power = low, opamp bias = low | – | – | 3.9 | μs | |
| | Power = medium, opamp bias = high | – | – | 0.72 | μs | |
| t _{SOA} | Falling settling time from 20% of ΔV to 0.1% of ΔV (10 pF load, unity gain) | | | | | |
| | Power = low, opamp bias = low | – | – | 5.9 | μs | |
| | Power = medium, opamp bias = high | – | – | 0.92 | μs | |
| SR _{ROA} | Rising slew rate (20% to 80%) (10 pF load, unity gain) | | | | | |
| | Power = low, opamp bias = low | 0.15 | – | – | V/μs | |
| | Power = medium, opamp bias = high | 1.7 | – | – | V/μs | |
| SR _{FOA} | Falling slew rate (20% to 80%) (10 pF load, unity gain) | | | | | |
| | Power = low, opamp bias = low | 0.01 | – | – | V/μs | |
| | Power = medium, opamp bias = high | 0.5 | – | – | V/μs | |
| BW _{OA} | Gain bandwidth product | | | | | |
| | Power = low, opamp bias = low | 0.75 | – | – | MHz | |
| | Power = medium, opamp bias = high | 3.1 | – | – | MHz | |
| E _{NOA} | Noise at 1 kHz (power = medium, opamp bias = high) | | | | | |
| | Power = high, opamp bias = high | 5.4 | – | – | MHz | |
| E _{NOA} | Noise at 1 kHz (power = medium, opamp bias = high) | – | 100 | – | nV/r-Hz | |

15.13 PSoC Core Low Power Comparator

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, T_J ≤ 115 °C for Industrial rated devices and 4.75 V to 5.25 V, T_J ≤ 125 °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-25. Low Power Comparator DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|---------------------|-------|-------|
| V _{REFLPC} | Low power comparator (LPC) reference voltage range | 0.2 | – | V _{DD} – 1 | V | |
| I _{SLPC} | LPC supply current | – | 10 | 40 | μA | |
| V _{OSLPC} | LPC voltage offset | – | 2.5 | 40 | mV | |

Table 15-26. Low Power Comparator AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|-------------------|-----|-----|-----|-------|---|
| t _{RLPC} | LPC response time | – | – | 50 | μs | ≥ 50 mV overdrive comparator reference set within V _{REFLPC} . |

15.14 PSoC Core Analog Output Buffer

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-27. Analog Output Buffer DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|---|---------------------------|-----|---------------------------|------------------------------|--|
| V_{OSOB} | Input offset voltage (absolute value) | – | 3 | 12 | mV | Industrial rated Extended Temperature rated |
| | | – | 3 | 18 | mV | |
| TCV_{OSOB} | Average input offset voltage drift | – | +6 | – | $\mu\text{V}/^\circ\text{C}$ | |
| V_{CMOB} | Common-mode input voltage range | 0.5 | – | $V_{DD} - 1.0$ | V | |
| R_{OUTOB} | Output resistance Power = low Power = high | – | 0.6 | – | Ω | |
| | | – | 0.6 | – | Ω | |
| $V_{OHIGHOB}$ | High output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high | $0.5 \times V_{DD} + 1.1$ | – | – | V | |
| | | $0.5 \times V_{DD} + 1.1$ | – | – | V | |
| | | $0.5 \times V_{DD} + 1.1$ | – | – | V | |
| V_{LOWOB} | Low output voltage swing (load = 32 ohms to $V_{DD}/2$) Power = low Power = high | – | – | $0.5 \times V_{DD} - 1.3$ | V | |
| | | – | – | $0.5 \times V_{DD} - 1.3$ | V | |
| | | – | – | $0.5 \times V_{DD} - 1.3$ | V | |
| I_{SOB} | Supply current including bias cell (no load) Power = low Power = high | – | 1.1 | 5.1 | mA | |
| | | – | 2.6 | 8.8 | mA | |
| $PSRR_{OB}$ | Supply voltage rejection ratio | 52 | 64 | – | dB | $(0.5 \times V_{DD} - 1.3) \leq V_{OUT} \leq (V_{DD} - 2.3)$. |

Table 15-28. Analog Output Buffer AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------|---|-----|-----|-----|---------------|-------|
| t_{ROB} | Rising settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high | – | – | 2.5 | μs | |
| | | – | – | 2.5 | μs | |
| t_{SOB} | Falling settling time to 0.1%, 1 V Step, 100 pF load Power = low Power = high | – | – | 2.2 | μs | |
| | | – | – | 2.2 | μs | |

Table 15-28. Analog Output Buffer AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------|--|--------------|--------|--------|--------------------------|-------|
| SR _{ROB} | Rising slew rate (20% to 80%), 1 V step, 100 pF load Power = low Power = high | 0.65 0.65 | – – | – – | V/ μ s V/ μ s | |
| SR _{FOB} | Falling slew rate (80% to 20%), 1 V step, 100 pF load Power = low Power = high | 0.65 0.65 | – – | – – | V/ μ s V/ μ s | |
| BW _{OBSS} | Small signal bandwidth, 20 mV _{pp} , 3 dB BW, 100 pF load Power = low Power = high | 0.8 0.8 | – – | – – | MHz MHz | |
| BW _{OBLs} | Large signal bandwidth, 1 V _{pp} , 3 dB BW, 100 pF load Power = low Power = high | 300 300 | – – | – – | kHz kHz | |

15.15 PSoC Core Analog Reference

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 15-29. Analog Reference DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------|--|--|--|--|--------|--|
| BG | Bandgap voltage reference | 1.28 1.27 | 1.30 1.30 | 1.32 1.33 | V V | Industrial rated Extended Temperature rated |
| – | AGND = $V_{DD}/2$ ^[15] | $V_{DD}/2 - 0.04$ $V_{DD}/2 - 0.02$ | $V_{DD}/2 - 0.01$ $V_{DD}/2$ | $V_{DD}/2 + 0.007$ $V_{DD}/2 + 0.02$ | V V | Industrial rated Extended Temperature rated |
| – | AGND = 2 x BandGap ^[15] | 2 x BG – 0.048 | 2 x BG – 0.030 | 2 x BG + 0.024 | V | |
| – | AGND = BandGap ^[15] | BG – 0.009 | BG + 0.008 | BG + 0.016 | V | |
| – | AGND = 1.6 x BandGap ^[15] | 1.6 x BG – 0.022 | 1.6 x BG – 0.010 | 1.6 x BG + 0.018 | V | |
| – | AGND Block to Block Variation (AGND = $V_{DD}/2$) ^[15] | –0.034 | 0.000 | 0.034 | V | |
| – | RefHi = $V_{DD}/2 + \text{BandGap}$ | $V_{DD}/2 + \text{BG} - 0.10$ | $V_{DD}/2 + \text{BG}$ | $V_{DD}/2 + \text{BG} + 0.10$ | V | |
| – | RefHi = 3 x BandGap | 3 x BG – 0.06 | 3 x BG | 3 x BG + 0.06 | V | |
| – | RefHi = 3.2 x BandGap | 3.2 x BG – 0.112 | 3.2 x BG | 3.2 x BG + 0.076 | V | |
| – | RefLo = $V_{DD}/2 - \text{BandGap}$ | $V_{DD}/2 - \text{BG} - 0.04$ $V_{DD}/2 - \text{BG} - 0.06$ | $V_{DD}/2 - \text{BG} + 0.024$ $V_{DD}/2 - \text{BG}$ | $V_{DD}/2 - \text{BG} + 0.04$ $V_{DD}/2 - \text{BG} + 0.06$ | V V | Industrial rated Extended Temperature rated |
| – | RefLo = BandGap | BG – 0.06 | BG | BG + 0.06 | V | |

15.16 PSoC Core Analog Block

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-30. Analog Block DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------|---|-----|------|-----|-------|-------|
| R _{CT} | Resistor unit value (continuous time) | – | 12.2 | – | kΩ | |
| C _{SC} | Capacitor unit value (switched capacitor) | – | 80 | – | fF | |

Notes

15. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3 V ± 0.02 V.

15.17 PSoC Core POR and LVD

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Note The bits PORLEV and VM in the following table refer to bits in the VLT_CR register. See the *PowerPSoC Technical Reference Manual* for more information on the VLT_CR register.

Table 15-31. POR and LVD DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------------------|---|--------------|--------------|--------------|--------|-------|
| V_{PPOR2} | V_{DD} Value for PPOR Trip PORLEV[1:0] = 10b | – | 4.55 | 4.70 | V | |
| V_{LVD6} V_{LVD7} | V_{DD} Value for LVD Trip VM[2:0] = 110b VM[2:0] = 111b | 4.62 4.71 | 4.73 4.81 | 4.83 4.95 | V V | |

15.18 PSoC Core Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115^\circ\text{C}$ for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125^\circ\text{C}$ for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-32. Programming DC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|----------------|-----|-----------------|-------|--------------------------------------|
| I_{DDP} | Supply current during programming or verify | – | 15 | 30 | mA | |
| V_{ILP} | Input low voltage during programming or verify | – | – | 0.8 | V | |
| V_{IHP} | Input high voltage during programming or verify | 2.1 | – | – | V | |
| I_{ILP} | Input current when applying V_{ilp} to P1[0] or P1[1] during programming or verify | – | – | 0.2 | mA | Driving internal pull down resistor. |
| I_{IHP} | Input current when applying V_{ihp} to P1[0] or P1[1] during programming or verify | – | – | 1.5 | mA | Driving internal pull down resistor. |
| V_{OLV} | Output low voltage during programming or verify | – | – | $V_{SS} + 0.75$ | V | |
| V_{OHV} | Output high voltage during programming or verify | $V_{DD} - 1.0$ | – | V_{DD} | V | |
| Flash _{ENPB} | Flash endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | Flash endurance (total) ^[16] | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash data retention ^[17] | 10 | – | – | Years | |

Notes

16. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 x 1 blocks of 50,000 maximum cycles each, 36 x 2 blocks of 25,000 maximum cycles each, or 36 x 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 x 50,000 and that no single block ever sees more than 50,000 cycles)

17. Guaranteed for $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ for Industrial rated devices and $-40^\circ\text{C} \leq T_A \leq 105^\circ\text{C}$ for Extended Temperature rated devices.

Table 15-33. Programming AC Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------|--|-----|-----|---------------------|-------|--|
| t _{RSCLK} | Rise time of SCLK | 1 | – | 20 | ns | |
| t _{FSCLK} | Fall time of SCLK | 1 | – | 20 | ns | |
| t _{SSCLK} | Data set up time to falling edge of SCLK | 40 | – | – | ns | |
| t _{HSCLK} | Data hold time from falling edge of SCLK | 40 | – | – | ns | |
| f _{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | |
| t _{ERASEB} | Flash erase time (block) | – | 10 | – | ms | |
| t _{WRITE} | Flash block write time | – | 40 | – | ms | |
| t _{DSCLK} | Data out delay from falling edge of SCLK | – | – | 50 | ns | |
| t _{ERASEALL} | Flash erase time (bulk) | – | 40 | – | ms | Erase all blocks and protection fields immediately |
| t _{PROGRAM_HOT} | Flash block erase + flash block write time | – | – | 100 ^[18] | ms | 0 °C ≤ T _j ≤ 100 °C |
| t _{PROGRAM_COLD} | Flash block erase + flash block write time | – | – | 200 ^[18] | ms | –40 °C ≤ T _j ≤ 0 °C |

15.19 PSoC Core Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, T_j ≤ 115 °C for Industrial rated devices and 4.75 V to 5.25 V, T_j ≤ 125 °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-34. Digital Block AC Specifications

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|--------------------|-----|-------|-------|---|
| Timer | Capture pulse width | 50 ^[19] | – | – | ns | |
| | Maximum frequency, no capture | – | – | 49.92 | MHz | |
| | Maximum frequency, with capture | – | – | 24.96 | MHz | |
| Counter | Enable pulse width | 50 ^[19] | – | – | ns | |
| | Maximum frequency, no enable input | – | – | 49.92 | MHz | |
| | Maximum frequency, enable input | – | – | 24.96 | MHz | |
| Dead Band | Kill pulse width: | | | | | |
| | Asynchronous restart mode | 20 | – | – | ns | |
| | Synchronous restart mode | 50 ^[19] | – | – | ns | |
| | Disable mode | 50 ^[19] | – | – | ns | |
| | Maximum Frequency | – | – | 49.92 | MHz | |
| CRCPRS (PRS Mode) | Maximum input clock frequency | – | – | 49.92 | MHz | |
| CRCPRS (CRC Mode) | Maximum input clock frequency | – | – | 24.96 | MHz | |
| SPIM | Maximum input clock frequency | – | – | 8.32 | MHz | Maximum data rate at 4.1 MHz due to 2 x over clocking. |
| SPIS | Maximum input clock frequency | – | – | 4.16 | MHz | |
| | Width of SS_ Negated between transmissions | 50 ^[19] | – | – | ns | |
| Transmitter | Maximum input clock frequency | – | – | 24.96 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| | Maximum input clock frequency with V _{DD} ≥ 4.75 V, 2 stop bits | – | – | 49.92 | MHz | Maximum data rate at 6.15 MHz due to 8 x over clocking. |

Notes

- 18. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.
- 19. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 15-34. Digital Block AC Specifications

| | | | | | | |
|----------|--|---|---|-------|-----|--|
| Receiver | Maximum input clock frequency | - | - | 24.96 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. Maximum data rate at 6.15 MHz due to 8 x over clocking. |
| | Maximum input clock frequency with $V_{DD} \geq 4.75$ V, 2 stop bits | - | - | 49.92 | MHz | |

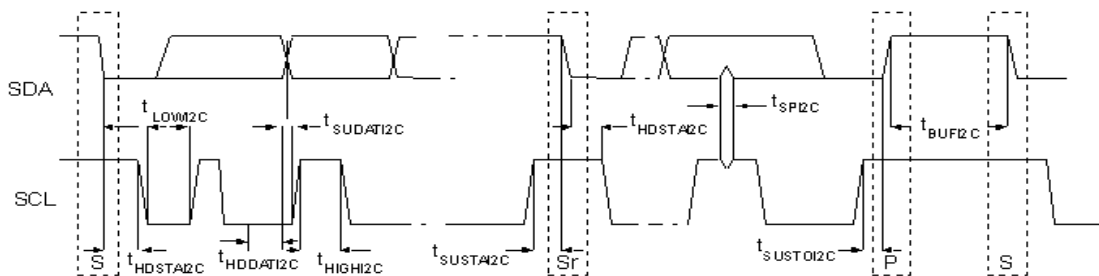
15.20 PSoC Core I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V, $T_J \leq 115$ °C for Industrial rated devices and 4.75 V to 5.25 V, $T_J \leq 125$ °C for Extended Temperature rated devices. Typical parameters apply to 5 V at 25 °C. These are for design guidance only.

Table 15-35. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|----------------|--|---------------|-----|---------------------|-----|---------|-------|
| | | Min | Max | Min | Max | | |
| f_{SCL2C} | SCL clock frequency | 0 | 100 | 0 | 400 | kHz | |
| $t_{HDSTA2C}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0 | - | 0.6 | - | μ s | |
| t_{LOW2C} | LOW period of the SCL clock | 4.7 | - | 1.3 | - | μ s | |
| t_{HIGH2C} | HIGH period of the SCL clock | 4.0 | - | 0.6 | - | μ s | |
| $t_{SUSTA2C}$ | Setup time for a repeated START condition | 4.7 | - | 0.6 | - | μ s | |
| $t_{HDDAT2C}$ | Data hold time | 0 | - | 0 | - | μ s | |
| $t_{SUDAT2C}$ | Data setup time | 250 | - | 100 ^[20] | - | ns | |
| $t_{SUSTOI2C}$ | Setup time for STOP condition | 4.0 | - | 0.6 | - | μ s | |
| t_{BUF2C} | Bus free time between a STOP and START condition | 4.7 | - | 1.3 | - | μ s | |
| t_{SPI2C} | Pulse width of spikes are suppressed by the input filter. | - | - | 0 | 50 | ns | |

Figure 15-8. Definition of Timing for Fast/Standard Mode on the I²C Bus



Note

20. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SUDAT2C} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{max} + t_{SUDAT2C} = 1000 + 250 = 1250$ ns (according to the standard mode I²C bus specification) before the SCL line is released.



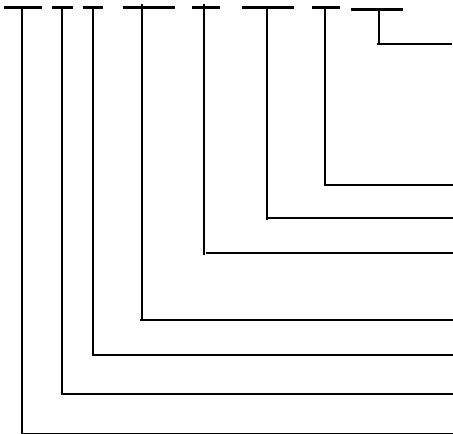
16. Ordering Information

Table 16-1. Device Key Features and Ordering Information

| PowerPSoC Part Number | No. of Pins | Package | Channels | Voltage | Internal FETs | Gate Drivers for External Low Side N-FETs |
|-----------------------|-------------|-------------|----------|---------|---------------|---|
| CY8CLED04D01-56LTXI | 56 QFN | 8 mm X 8 mm | 4 | 32 V | 4 X 1.0 A | 4 |
| CY8CLED04D02-56LTXI | 56 QFN | 8 mm X 8 mm | 4 | 32 V | 4 X 0.5 A | 4 |
| CY8CLED04G01-56LTXI | 56 QFN | 8 mm X 8 mm | 4 | 32 V | 0 | 4 |
| CY8CLED04DOCD1-56LTXI | 56 QFN | 8 mm X 8 mm | 4 | 32 V | 4 X 1.0 A | 4 |
| CY8CLED03D01-56LTXI | 56 QFN | 8 mm X 8 mm | 3 | 32 V | 3 X 1.0 A | 3 |
| CY8CLED03D02-56LTXI | 56 QFN | 8 mm X 8 mm | 3 | 32 V | 3 X 0.5 A | 3 |
| CY8CLED03G01-56LTXI | 56 QFN | 8 mm X 8 mm | 3 | 32 V | 0 | 3 |
| CY8CLED02D01-56LTXI | 56 QFN | 8 mm X 8 mm | 2 | 32 V | 2 X 1.0 A | 2 |
| CY8CLED01D01-56LTXI | 56 QFN | 8 mm X 8 mm | 1 | 32 V | 1 X 1.0 A | 1 |
| CY8CLED01D01-56LTXQ | 56 QFN | 8 mm X 8 mm | 1 | 32 V | 1 X 1.0 A | 1 |

16.1 Ordering Code Definitions

CY 8 C LED0x xxx (xxxx) - xx xxxx



Package Type:
LTX=QFN Pb-free

Thermal Rating:
I = Industrial
Q = Extended Temperature

Pin Count
OCD1 = On Chip Debugger

Part Number: D01 = Internal 1.0 A FETs, D02 = Internal 0.5 A FETs,
G01 = No Internal FETs

Family Code: 4 = 4 Channel, 3 = 3 Channel, 2 = 2 Channel, 1 = 1 Channel

Technology Code: C = CMOS

Marketing Code: 8 = Cypress PSoC

Company ID: CY = Cypress

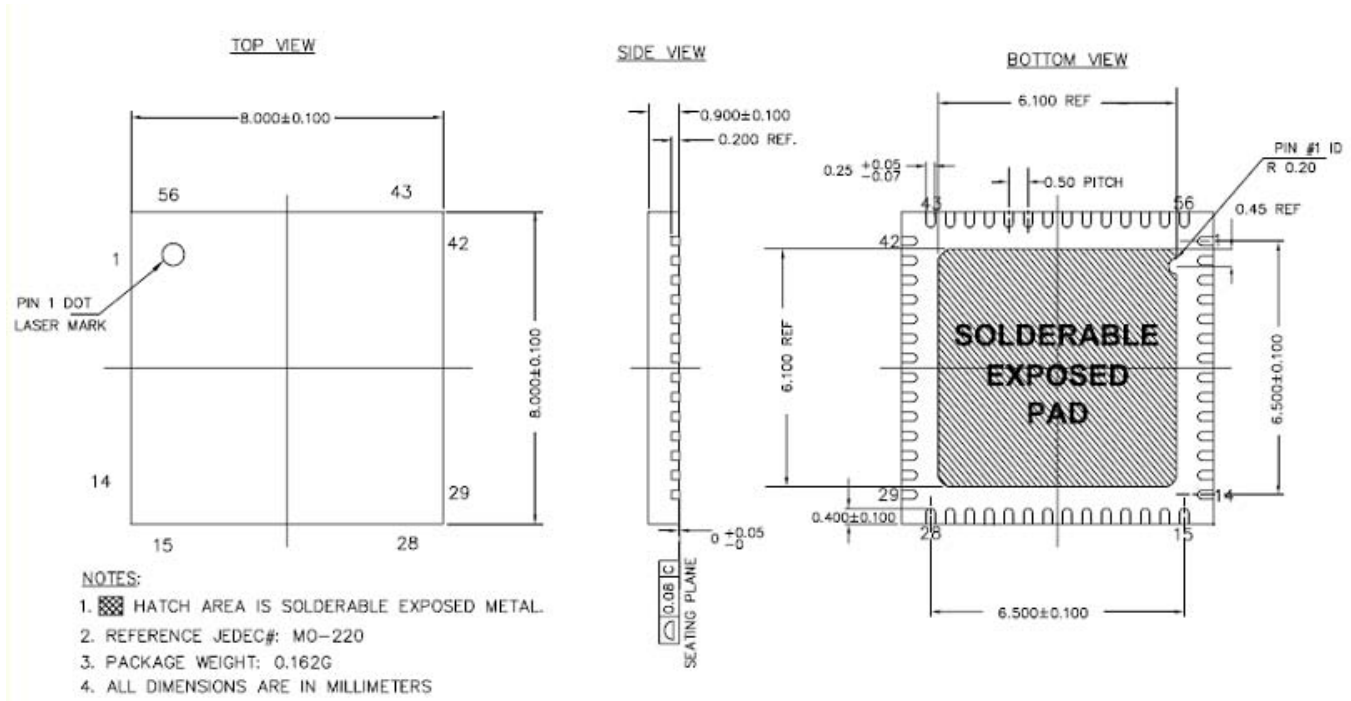
17. Packaging Information

Packaging Dimensions

This section illustrates the package specification for the CY8CLED04D0X, CY8CLED04G01, CY8CLED03D0X, CY8CLED03G01, CY8CLED02D01, and CY8CLED01D01 along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Figure 17-1. 56-Pin (8x8 mm) QFN



51-85187 *E

17.1 Thermal Impedance

| Package | Typical θ_{JA} [21] |
|-------------|----------------------------|
| 56 QFN [22] | 16.6 °C/W |

17.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

| Package | Minimum Peak Temperature [23] | Maximum Peak Temperature |
|---------|-------------------------------|--------------------------|
| 56 QFN | 240 °C | 260 °C |

Notes

21. $T_J = T_A + \text{POWER} \times \theta_{JA}$

22. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

18. Acronyms

| Acronym | Description |
|-----------|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CSA | current sense amplifier |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DALI | digital addressable lighting interface |
| DC | direct current |
| DMM | delta sigma modulation mode |
| DMX | digital multiplexing |
| DSM | delta sigma modulator |
| DTMF | dual-tone multi frequency |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| FAQ | frequently asked questions |
| FET | field effect transistor |
| FSR | full scale range |
| GPIO | general purpose i/o |
| GUI | graphical user interface |
| HBM | human body model |
| IC | integrated circuit |
| ICE | in-circuit emulator |
| IDE | integrated development environment |
| ILO | internal low-speed oscillator |
| IMO | internal main oscillator |
| ISSP | in-system serial programming |
| I/O | input/output |
| IPOR | imprecise power on reset |
| LED | light emitting diode |
| LSB | least-significant bit |
| LVD | low voltage detect |
| MCU | microcontroller |
| MOSFET | metal-oxide-semiconductor field effect transistor |
| MSB | most-significant bit |
| OCD | on chip debugger |
| PC | program counter |
| POR | power on reset |
| PPOR | precision power on reset |
| PowerPSoC | power programmable system-on-chip™ |

| Acronym | Description |
|---------|---|
| PrISM | precise intensity signal modulation |
| PSoC | programmable system-on-chip™ |
| PWM | pulse width modulator |
| QFN | quad flat no leads package |
| RGBA | red, green, blue, amber |
| RGGB | red, green, green, blue |
| SAR | successive approximation register |
| SC | switched capacitor |
| SCL | serial I ² C |
| SCLK | serial issp clock |
| SDA | serial i ² c data |
| SDATA | serial issp data |
| SPI | serial peripheral interface |
| SRAM | static random access memory |
| TRM | technical reference manual |
| UART | universal asynchronous receiver/transmitter |
| USB | universal serial bus |
| WDT | watch dog timer |

19. Document Conventions

19.1 Units of Measure

| Symbol | Unit of Measure |
|--------|------------------------------|
| °C | degrees Celsius |
| dB | decibels |
| Hz | Hertz |
| pp | peak-to-peak |
| σ | sigma:one standard deviation |
| V | volts |
| Ω | ohms |
| KB | 1024 bytes |
| ppm | parts per million |
| sps | samples per second |
| W | watts |
| A | amperes |
| Kbit | 1024 bits |
| KHz | kilohertz |
| KΩ | kilohms |
| MHz | megahertz |
| MΩ | megaohms |
| μA | microamperes |
| μF | microfarads |
| μH | microhenrys |
| μs | microseconds |
| μV | microvolts |
| μVrms | microvolts root-mean-square |

| Symbol | Unit of Measure |
|---------------|-----------------|
| μW | microwatts |
| mA | milliampere |
| ms | millisecond |
| mV | millivolts |
| mW | milliwatts |
| nA | nanoamperes |
| ns | nanoseconds |
| nV | nanovolts |
| pA | picoamperes |
| pF | picofarads |
| ps | picoseconds |
| fF | femtofarads |

20. Document History Page

| Document Title: CY8CLED04D01, CY8CLED04D02, CY8CLED04G01, CY8CLED03D01, CY8CLED03D02, CY8CLED03G01, CY8CLED02D01, CY8CLED01D01 PowerPSoc® Intelligent LED Driver Document Number: 001-46319 | | | | |
|--|---------|-----------------|-----------------|--|
| Revision | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 2506500 | ANWA/DSG | 05/20/08 | New datasheet. |
| *A | 2575708 | ANWA/AESA | 10/01/08 | 1) Updated Logic Block Diagram with AINX label and SREGFB pin. 2) Updated Current Sense Amplifier Specification Table. 3) Updated External Gate Driver Specification Table. 4) Updated Register Table. |
| *B | 2662774 | KJV | 02/19/09 | Extensive changes made to content and electrical specifications. |
| *C | 2665155 | KJV/PYRS | 02/25/09 | Updated Notes in electrical specifications. |
| *D | 2671254 | KJV/PYRS | 03/10/09 | Updated sections 8, 9, and 10 on pages 14, 15, and 16. |
| *E | 2683506 | VED | 04/03/09 | Release to the external web site. |
| *F | 2698529 | KJV/PYRS | 04/27/09 | Updated Figure 15-2. , and Figure 15-4. |
| *G | 2735072 | KJV | 07/10/09 | Added 1 and 2 channel part information. |
| *H | 2765369 | KJV | 09/17/09 | Updated electrical specifications. |
| *I | 2870389 | FRE/PYRS | 02/01/10 | Added Table of Contents Updated Absolute Maximum Ratings, DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Added $V_{REGINMAX}$ absolute maximum specification. Modified t_{WRITE} specification. Added I_{OH} , I_{OL} , DC_{ILO} , f_{32K_U} , $t_{POWERUP}$, $t_{ERASEALL}$, $t_{PROGRAM_HOT}$ and $t_{PROGRAM_COLD}$ specifications Updated package diagram |
| *J | 2952677 | FRE/UKK | 06/15/10 | Datasheet reviewed and updated with a view to improve clarity, readability and customer-friendliness. This includes language, consistency in terminology to match software and other PowerPSoc documentation, changes to reflect major changes in software such as removal of system level design addition of links to relevant collateral such as kits, technical reference manuals and application notes. |
| *K | 3031567 | FRE/UKK | 09/16/10 | Removed DALI in Page 1 and Page 13, and added the DALI note in Page 13. Added a note to Section 15.10 after Table 15-20 on page 38. Updated as per the new Cypress Style and datasheet template. |
| *L | 3073506 | KJV | 11/08/2010 | Updated datasheet to add Extended Temperature rated device CY8CLED01D01-56LTXQ |
| *M | 3178540 | KJV | 02/28/2011 | Updated certain specifications for Extended Temperature rated device |
| *N | 3244595 | KJV | 05/04/2011 | Updated description for Symbol V_{REGIN} and V_{CSP}, V_{CSN} in Table 14-1 . Updated Figure 15-6 . |



21. Sales, Solutions, and Legal Information

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