MACH211SP-7/10/12/15

High-Performance EE CMOS In-System Programmable Logic

DISTINCTIVE CHARACTERISTICS

- JTAG-Compatible, 5-V in-system programming
- 44 Pins in PLCC and TQFP
- 64 Macrocells
- 7.5 ns t_{PD} Commercial, 10 ns t_{PD} Industrial
- 133 MHz f_{CNT}
- 32 I/Os; 2 dedicated inputs/clocks
- 64 Flip-flops; 2 clock choices
- 4 "PALCE26V16" blocks with buried macrocells
- Speed Locking™ for guaranteed fixed timing
- Bus-Friendly™ Inputs and I/Os
- Peripheral Component Interconnect (PCI) compliant (-7/-10/-12)
- Programmable power-down mode

IN-SYSTEM PROGRAMMING

In-system programming allows the MACH211SP to be programmed while soldered onto a system board. Programming the MACH211SP in-system yields numerous benefits at all stages of development: prototyping, manufacturing, and in the field. Since insertion into a programmer isn't needed, multiple handling steps and the resulting bent leads are eliminated. The design can be modified in-system for design changes and debugging while prototyping, programming boards in production, and field upgrades.

The MACH211SP offers advantages with in-system programming. MACH® devices have extensive routing resources for pin-out retention; design changes resulting in pin-out changes for many non-Vantis CPLDs cancel the advantages of in-system programming. The MACH211SP can be deployed in any JTAG (IEEE 1149.1) compliant chain.

GENERAL DESCRIPTION

The MACH211SP is a member of Vantis' high-performance EE CMOS MACH 1 & 2 families. This device has approximately six times the logic macrocell capability of the popular PALCE22V10 without loss of speed.

The MACH211SP consists of four PAL® blocks interconnected by a programmable switch matrix. The four PAL blocks are essentially "PALCE26V16" structures complete with product-term arrays and programmable macrocells, which can be programmed as high speed or low power, and buried macrocells. The switch matrix connects the PAL blocks to each other and to all input pins,

providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently.

The MACH211SP has two kinds of macrocell: output and buried. The MACH211SP output macrocell provides registered, latched, or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type or T-type to help reduce the number of product terms. The register type decision can be made by the designer or by the software. All output macrocells can be connected to an I/O cell. If a buried macrocell is desired, the internal feedback path from the macrocell can be used, which frees up the I/O pin for use as an input.

The MACH211SP has dedicated buried macrocells which, in addition to the capabilities of the output macrocell, also provide input registers or latches for use in synchronizing signals and reducing setup time requirements.

The MACH211SP is an enhanced version of the MACH211, adding the JTAG-compatible in-system programming feature.

Vantis offers software design support for MACH devices through its own development system and device fitters integrated into third-party CAE tools. Platform support extends across PCs, Sun and HP workstations under advanced operating systems such as Windows 3.1, Windows 95 and NT, SunOS and Solaris, and HPUX.

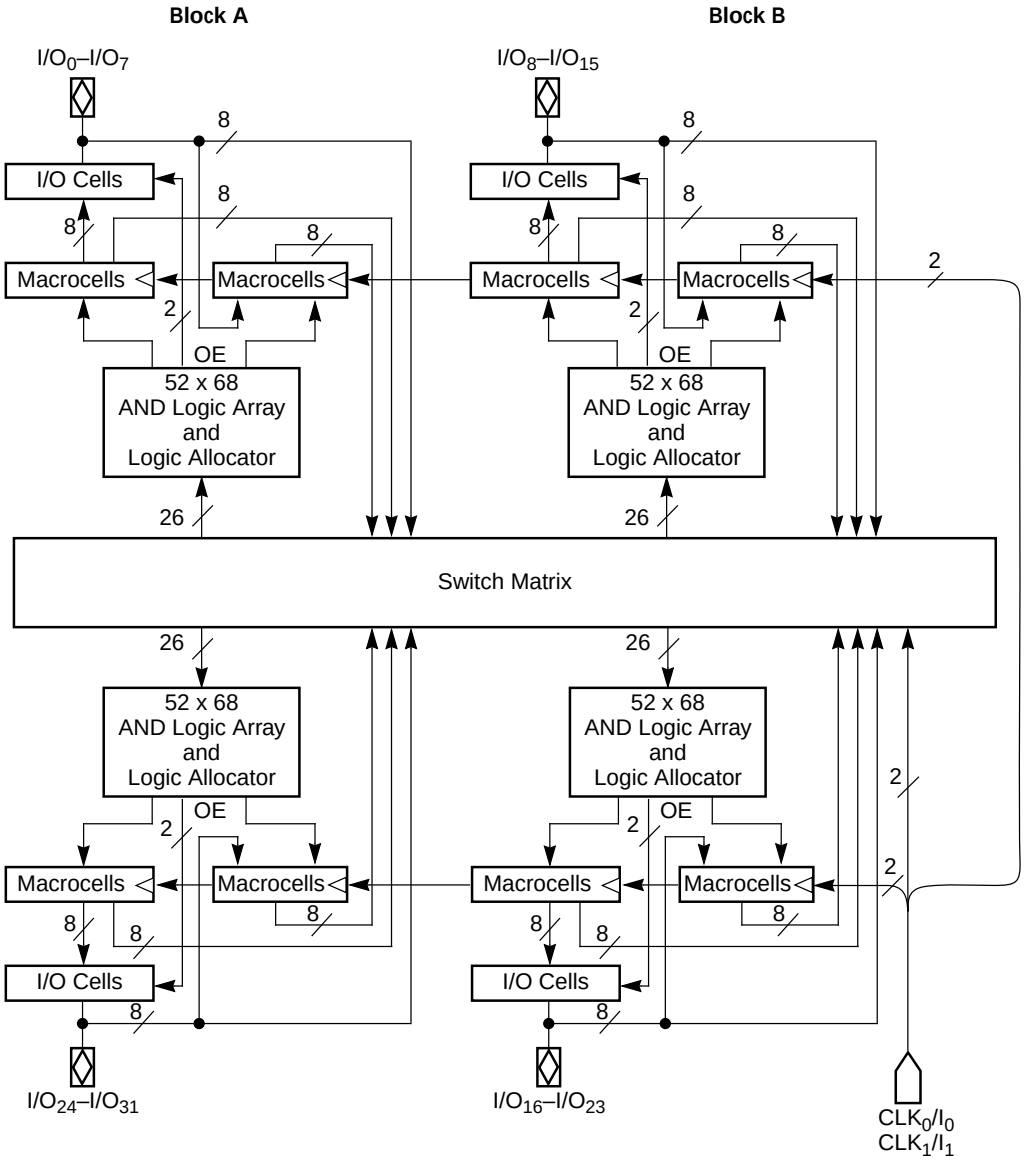
MACHXL® software is a complete development system for the PC, supporting Vantis' MACH devices. It supports design entry with Boolean and behavioral syntax, state machine syntax and truth tables. Functional simulation and static timing analysis are also included in this easy-to-use system. This development system includes high-performance device fitters for all MACH devices.

The same fitter technology included in MACHXL software is seamlessly incorporated into third-party tools from leading CAE vendors such as Synario, Viewlogic, Mentor Graphics, Cadence and MINC. Interface kits and MACHXL configurations are also available to support design entry and verification with other leading vendors such as Synopsys, Exemplar, OrCAD, Synplicity and Model Technology. These MACHXL configurations and interfaces accept EDIF 2.0.0 netlists, generate JEDEC files for MACH devices, and create industry-standard SDF, VITAL-compliant VHDL and Verilog output files for design simulation.

Vantis offers in-system programming support for MACH devices through its MACHPRO® software enabling MACH device programmability through JTAG compliant ports and easy-to-use PC interface. Additionally, MACHPRO generated vectors work seamlessly with HP3070, GenRad and Teradyne testers to program MACH devices or test them for connectivity.

All MACH devices are supported by industry standard programmers available from a number of vendors. These programmer vendors include Advin Systems, BP Microsystems, Data I/O Corporation, Hi-Lo Systems, SMS GmbH, Stag House, and System General.

BLOCK DIAGRAM



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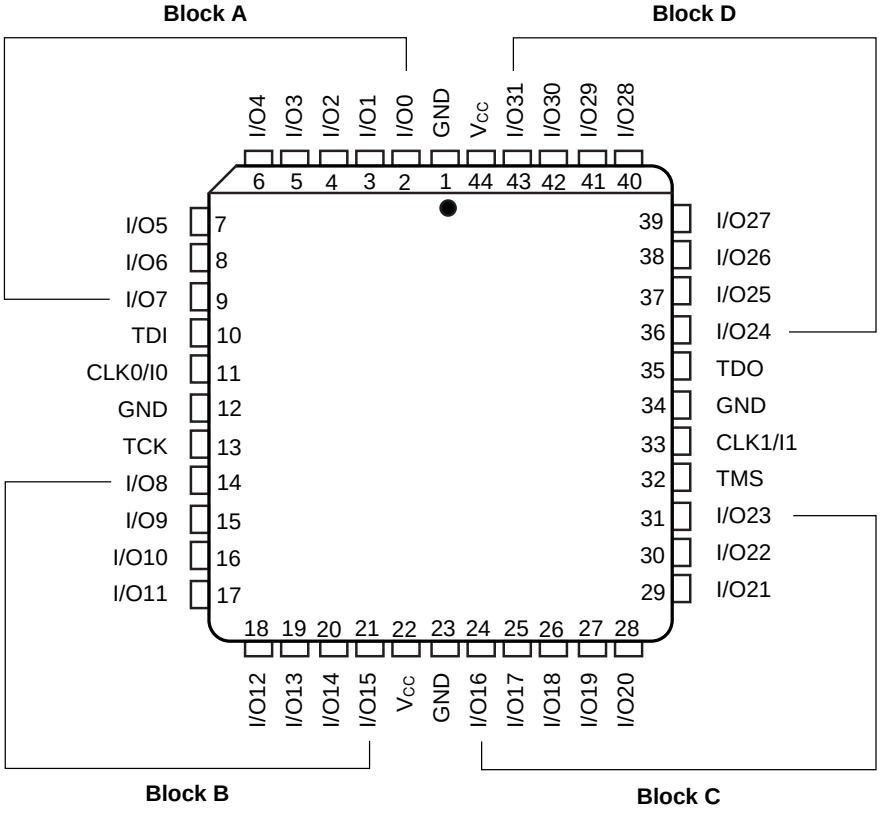
CONNECTION DIAGRAM

Top View

44-Pin PLCC



20405C-2

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

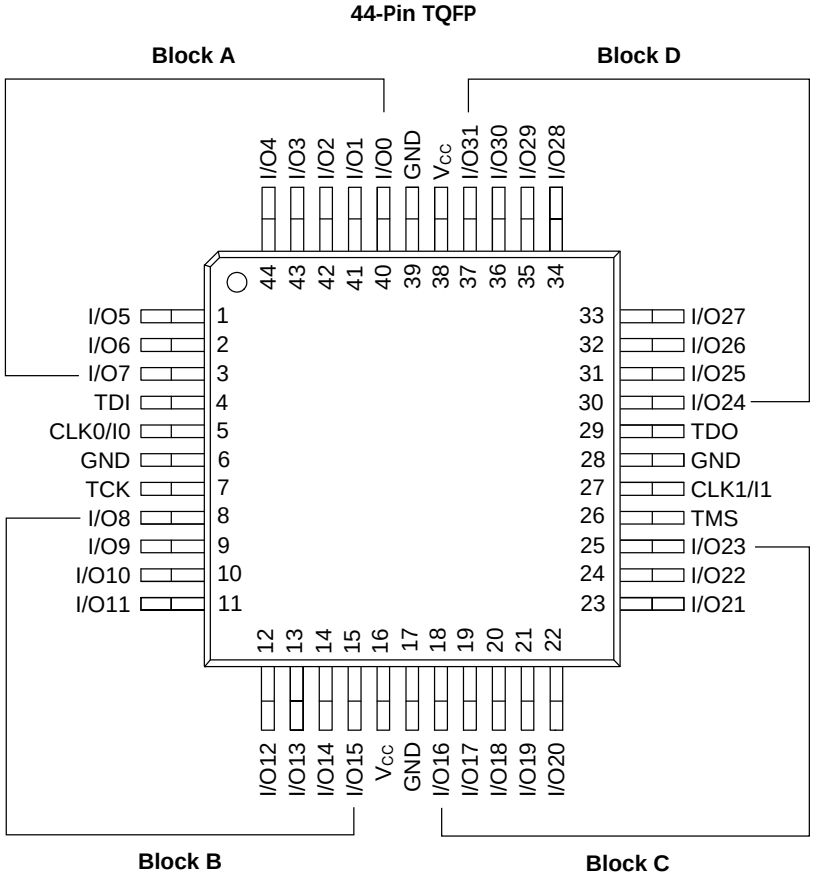
TCK = Test Clock

TMS = Test Mode Select

TDO = Test Data Out

CONNECTION DIAGRAM

Top View



20405C-3

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

TDI = Test Data In

TCK = Test Clock

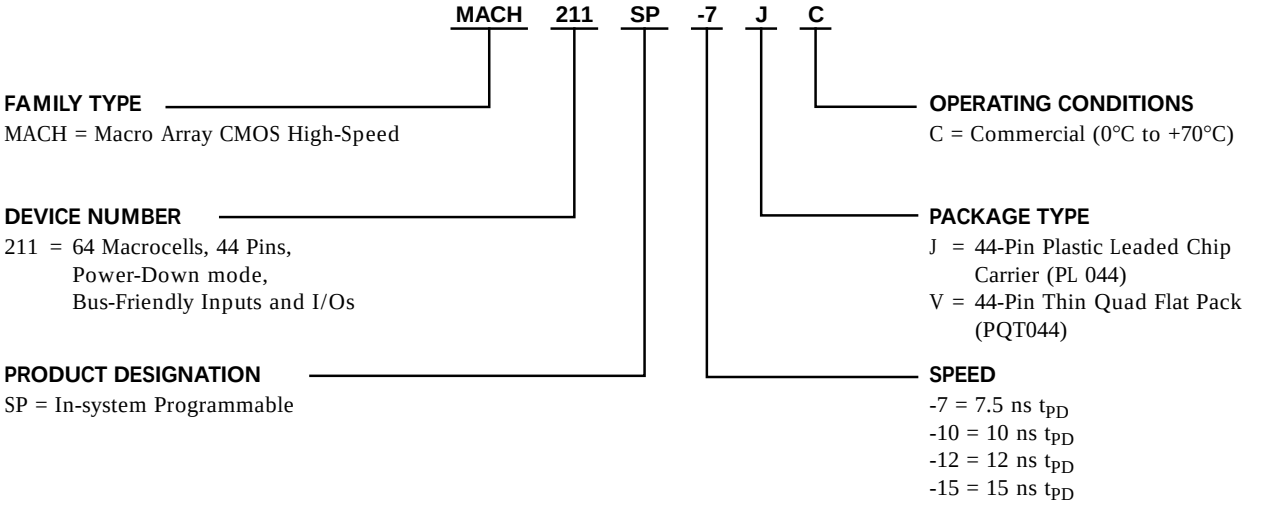
TMS = Test Mode Select

TDO = Test Data Out

ORDERING INFORMATION

Commercial Products

Vantis programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH211SP-7	JC, VC
MACH211SP-10	
MACH211SP-12	
MACH211SP-15	

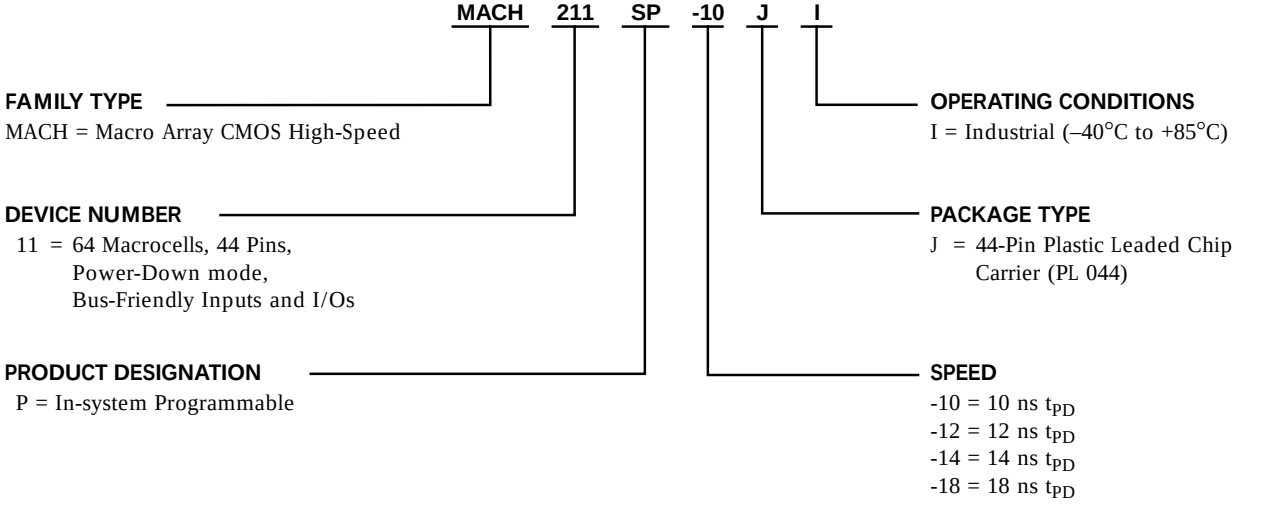
Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

Industrial Products

Vantis programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH211SP-10	JI
MACH211SP-12	
MACH211SP-14	
MACH211SP-18	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local Vantis sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH211SP consists of four PAL blocks connected by a switch matrix. There are 32 I/O pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are two clock pins that can also be used as dedicated inputs.

The PAL Blocks

Each PAL block in the MACH211SP (Figure 1) contains a 64-product-term logic array, a logic allocator, 8 output macrocells, 8 buried macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 26 inputs. This makes the PAL block look effectively like an independent "PALCE26V16" with 8 buried macrocells.

In addition to the logic product terms, two output enable product terms, an asynchronous reset product term, and an asynchronous preset product term are provided. One of the two output enable product terms can be chosen within each I/O cell in the PAL block. All flip-flops within the PAL block are initialized together.

The Switch Matrix

The MACH211SP switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH211SP product-term array consists of 64 product terms for logic use, and 4 special-purpose product terms. Two of the special-purpose product terms provide programmable output enable; one provides asynchronous reset, and one provides asynchronous preset.

The Logic Allocator

The logic allocator in the MACH211SP takes the 64 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 16 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Macrocell		Available Clusters	Macrocell		Available Clusters
Output	Buried		Output	Buried	
M_0		C_0, C_1, C_2	M_8		C_7, C_8, C_9, C_{10}
	M_1	C_0, C_1, C_2, C_3		M_9	C_8, C_9, C_{10}, C_{11}
M_2		C_1, C_2, C_3, C_4	M_{10}		$C_9, C_{10}, C_{11}, C_{12}$
	M_3	C_2, C_3, C_4, C_5		M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4		C_3, C_4, C_5, C_6	M_{12}		$C_{11}, C_{12}, C_{13}, C_{14}$
	M_5	C_4, C_5, C_6, C_7		M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6		C_5, C_6, C_7, C_8	M_{14}		C_{13}, C_{14}, C_{15}
	M_7	C_6, C_7, C_8, C_9		M_{15}	C_{14}, C_{15}

The Macrocell

The MACH211SP has two types of macrocell: output and buried. The output macrocells can be configured as either registered, latched, or combinatorial, with programmable polarity. The macrocell provides internal feedback whether configured with or without the flip-flop. The registers can be configured as D-type or T-type, allowing for product-term optimization.

The flip-flops can individually select one of two clock/gate pins, which are also available as data inputs. The registers are clocked on the LOW-to-HIGH transition of the clock signal. The latch holds its data when the gate input is HIGH, and is transparent when the gate input is LOW. The flip-flops can also be asynchronously initialized with the common asynchronous reset and preset product terms.

The buried macrocells are the same as the output macrocells if they are used for generating logic. In that case, the only thing that distinguishes them from the output macrocells is the fact that there is no I/O cell connection, and the signal is only used internally. The buried macrocell can also be configured as an input register or latch.

The I/O Cell

The I/O cell in the MACH211SP consists of a three-state output buffer. The three-state buffer can be configured in one of three ways: always enabled, always disabled, or controlled by a product term. If product term control is chosen, one of two product terms may be used to provide the control. The two product terms that are available are common to all I/O cells in a PAL block.

These choices make it possible to use the macrocell as an output, an input, a bidirectional pin, or a three-state output for use in driving a bus.

SpeedLocking for Guaranteed Fixed Timing

The unique MACH 1 & 2 architecture is designed for high performance—a metric that is met in both raw speed, but even more importantly, *guaranteed fixed* speed. Using the design of the central switch matrix, the MACH211SP product offers the SpeedLocking feature, which allows a stable fixed pin-to-pin delay, independent of logic paths, routing resources and design refits for up to 16 product terms per output. Other non-Vantis CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product-term limits. Speed *and* SpeedLocking combine for continuous, high performance required in today's demanding designs.

In-System Programming

Programming is the process where MACH devices are loaded with a pattern defined in a JEDEC file obtained from MACHXL software or third-party software. Programming is accomplished through four JTAG pins: Test Mode Select (TMS), Test Clock (TCK), Test Data In (TDI), and Test Data Out (TDO). The MACH211SP can be deployed in any JTAG (IEEE 1149.1) compliant chain. While the MACH211SP is fully JTAG compatible, it supports the BYPASS instruction, not the EXTEST and SAMPLE/PRELOAD instructions. The MACH211SP can be programmed across the commercial temperature range. Programming the MACH device after it has been placed on a circuit board is easily accomplished. Programming is initiated by placing the device into programming mode, using the MACHPRO programming software provided by Vantis. The device is bulk erased and the JEDEC file is then loaded. After the data is transferred into the device, the PROGRAM instruction is loaded.

Bus-Friendly Inputs and I/Os

The MACH211SP inputs and I/Os include two inverters in series which loop back to the input. This double inversion reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, please turn to the Input/Output Equivalent Schematics section.

PCI Compliant

The MACH211SP-7/10/12 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The MACH211SP-7/10/12's predictable timing ensures compliance with the PCI AC specifications independent of the design.

Power-Down Mode

The MACH211SP features a programmable low-power mode in which individual signal paths can be programmed as low power. These low-power speed paths will be slightly slower than the non-low-power paths. This feature allows speed critical paths to run at maximum frequency while the rest of the paths operate in the low-power mode, resulting in power savings of up to 75%. If all signals in a PAL block are low-power, then total power is reduced further.

On-Board Programming Options

Since the MACHPRO software performs these steps automatically, the following programming options are published for reference.

The configuration file, which is also known as the chain file, defines the MACH device JTAG chain. The file contains the information concerning which JEDEC file is to be placed into which device, the state which the outputs should be placed, and whether the security fuses should be programmed. The configuration file is discussed in detail in the MACHPRO software manual.

The MACH211SP devices tristate the outputs during programming. They have one security bit which inhibits program and verify. This allows the user to protect proprietary patterns and designs.

Program verification of a MACH device involves reading back the programmed pattern and comparing it with the original JEDEC file. The Vantis method of program verification performed on the MACH devices permits the verification of one device at a time.

Accidental Programming or Erasure Protection

It is virtually impossible to program or erase a MACH device inadvertently. The following conditions must be met before programming actually takes place:

- The device must be in the password-protected program mode
- The programming or bulk erase instruction must be in the instruction register

If the above conditions are not met, the programming circuitry cannot be activated.

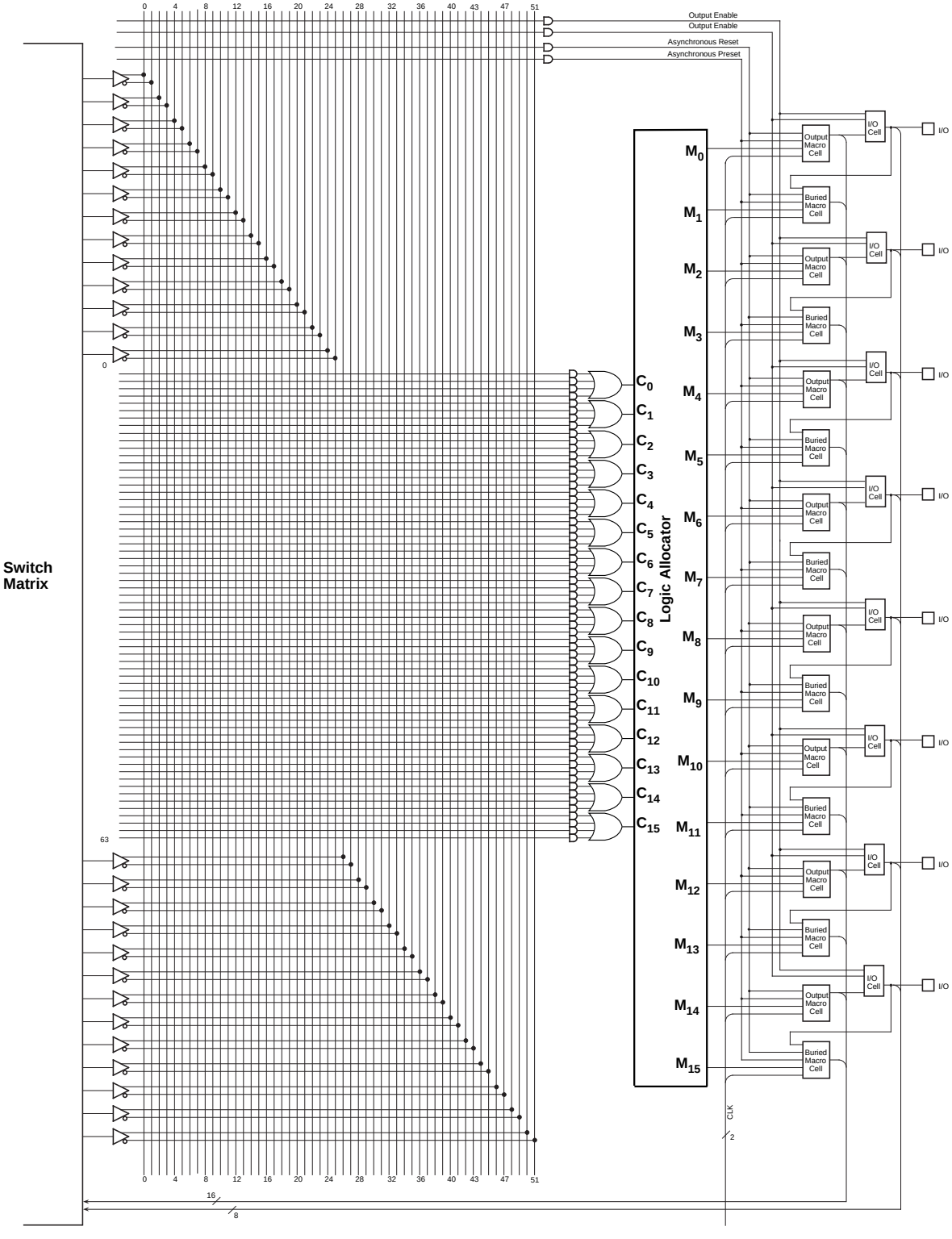


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Figure 1. MACH211SP PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to 70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		40		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-7		-10		-12		-15		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					7.5		10		12		15	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock (Note 3)			D-type	5.5		6.5		7		10		ns
				T-type	6.5		7.5		8		11		ns
t_H	Register Data Hold Time				0		0		0		0		ns
t_{CO}	Clock to Output (Note 3)					4.5		6		8		10	ns
t_{WL}	Clock Width			LOW	3		5		6		6		ns
t_{WH}				HIGH	3		5		6		6		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	100		80		66.7		50		MHz
				T-type	91		74		62.5		47.6		MHz
		Internal Feedback (f_{CNT})		D-type	133		100		83.3		66.6		MHz
				T-type	125		91		76.9		62.5		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		166.7		100		83.3		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				5.5		6.5		7		10		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		ns
t_{GO}	Gate to Output					7		7		10		11	ns
t_{GWL}	Gate Width LOW				3		5		6		6		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					9.5		12		14		17	ns
t_{SIR}	Input Register Setup Time				2		2		2		2		ns
t_{HIR}	Input Register Hold Time				2		2		2		2.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					11		13		15		18	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	9		10		12		15		ns
				T-type	10		11		13		16		ns
t_{WICL}	Input Register Clock Width			LOW	3		5		6		6		ns
t_{WICH}				HIGH	3		5		6		6		ns
f_{MAXIR}	Maximum Input Register Frequency				166.7		100		83.3		83.3		MHz
t_{SIL}	Input Latch Setup Time				2		2		2		2		ns
t_{HIL}	Input Latch Hold Time				2		2		2		2.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output					12		14		17		20	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch		14		16		19		22	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	7.5		8.5		9		12		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	10		11		13		16		ns
t_{WIGL}	Input Latch Gate Width LOW	3		5		6		6		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		12.5		14		16		19	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		9.5		15		16		20	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	5		10		12		15		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	5		10		8		10		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		9.5		15		16		20	ns
t_{APW}	Asynchronous Preset Width (Note 1)	5		10		12		15		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	5		10		8		10		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		9.5		12		15		15	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		9.5		12		15		15	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Device Junction Temperature . . . . . +150°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or
I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Temperature (T_A)
Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4		3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	–30		–160	mA
I_{CC}	Supply Current (Static)	V_{CC} = 5 V, T_A = 25°C, f = 0 MHz (Note 4)		40		mA
	Supply Current (Active)	V_{CC} = 5 V, T_A = 25°C, f = 1 MHz (Note 4)		45		mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
4. *This parameter is measured in low-power mode with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-10		-12		-14		-18		Unit
					Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					10		12		14		18	ns
t_S	Setup Time from Input, I/O, or Feedback to Clock			D-type	6.5		8		8.5		12		ns
				T-type	7.5		9		10		13.5		ns
t_H	Register Data Hold Time				0		0		0		0		ns
t_{CO}	Clock to Output (Note 3)					6		7.5		10		12	ns
t_{WL}	Clock Width			LOW	5		6		7.5		7.5		ns
t_{WH}				HIGH	5		6		7.5		7.5		ns
f_{MAX}	Maximum Frequency (Note 1)	External Feedback	$1/(t_S + t_{CO})$	D-type	80		64		53		40		MHz
				T-type	74		59		50		38		MHz
		Internal Feedback (f_{CNT})		D-type	100		80		61.5		53		MHz
				T-type	91		72.5		57		44		MHz
		No Feedback	$1/(t_{WL} + t_{WH})$		100		80		66.5		66.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Gate				6.5		8		8.5		12		ns
t_{HL}	Latch Data Hold Time				0		0		0		0		ns
t_{GO}	Gate to Output					8		8.5		12		13.5	ns
t_{GWL}	Gate Width LOW				5		6		7.5		7.5		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					12		14.5		17		20.5	ns
t_{SIR}	Input Register Setup Time				2		2.5		2.5		2.5		ns
t_{HIR}	Input Register Hold Time				2		3		3		3.5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					13		16		18		22	ns
t_{ICS}	Input Register Clock to Output Register Setup			D-type	10		12		14.5		18		ns
				T-type	11		13		16		19.5		ns
t_{WICL}	Input Register Clock Width			LOW	5		6		7.5		7.5		ns
t_{WICH}				HIGH	5		6		7.5		7.5		ns
f_{MAXIR}	Maximum Input Register Frequency		$1/(t_{WICL} + t_{WICH})$		100		80		66.5		66.5		MHz
t_{SIL}	Input Latch Setup Time				2		2.5		2.5		2.5		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

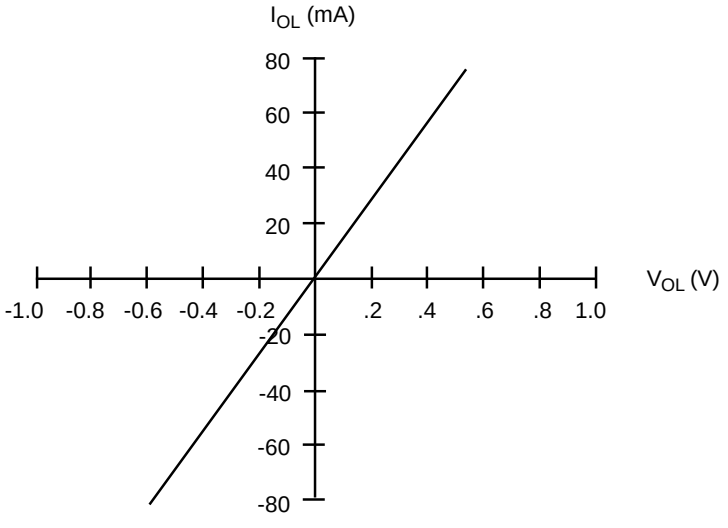
Parameter Symbol	Parameter Description	-10		-12		-14		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{HIL}	Input Latch Hold Time	2		3		3		3.5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output		14		17		20.5		24	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch		16		19.5		23		26.5	ns
t_{SLL}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Latch Gate	8.5		10.5		11		14.5		ns
t_{IGS}	Input Latch Gate to Output Latch Setup	11		13.5		16		19.5		ns
t_{WIGL}	Input Latch Gate Width LOW	5		6		7.5		7.5		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		14		17		19.5		23	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output		15		19.5		19.5		24	ns
t_{ARW}	Asynchronous Reset Width (Note 1)	10		12		14.5		18		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)	10		10		10		12		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		15		18		19.5		24	ns
t_{APW}	Asynchronous Preset Width (Note 1)	10		12		14.5		18		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)	10		10		10		12		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 1)		15		15		14.5		18	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 1)		15		15		14.5		18	ns
t_{LP}	t_{PD} Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns
t_{LPS}	t_S Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns
t_{LPCO}	t_{CO} Increase for Powered-down Macrocell (Note 3)		0		0		0		0	ns
t_{LPEA}	t_{EA} Increase for Powered-down Macrocell (Note 3)		10		10		10		10	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is powered-down, this parameter must be added to its respective high-speed parameter.*

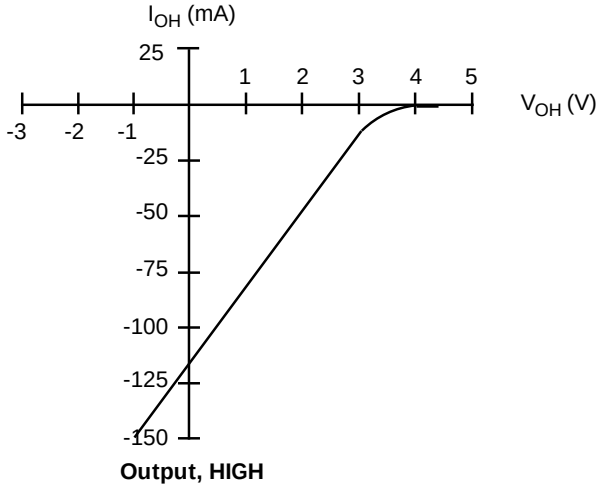
TYPICAL CURRENT vs. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



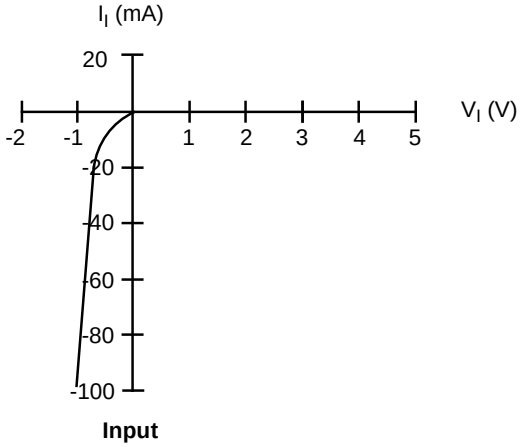
Output, LOW

20405C-5



Output, HIGH

20405C-6

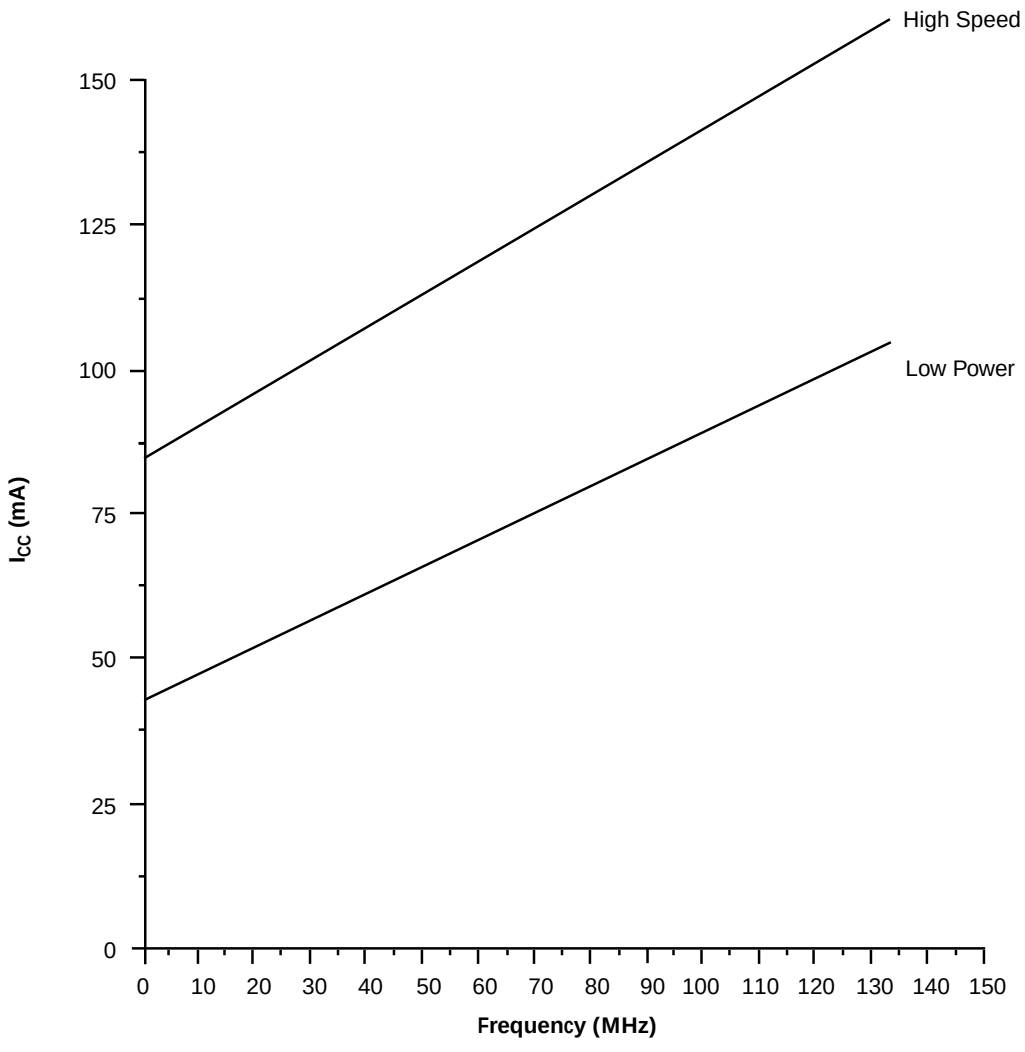


Input

20405C-7

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



20405C-8

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

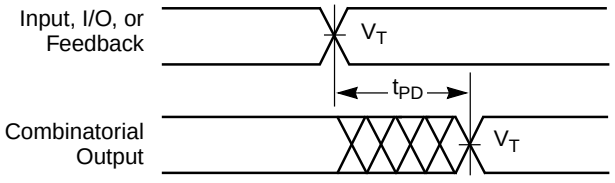
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			TQFP	PLCC	
θ_{jc}	Thermal impedance, junction to case		11	4	°C/W
θ_{ja}	Thermal impedance, junction to ambient		41	30	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	35	19	°C/W
		400 lfpm air	34	16	°C/W
		600 lfpm air	33	14	°C/W
		800 lfpm air	32	13	°C/W

Plastic θ_{jc} Considerations

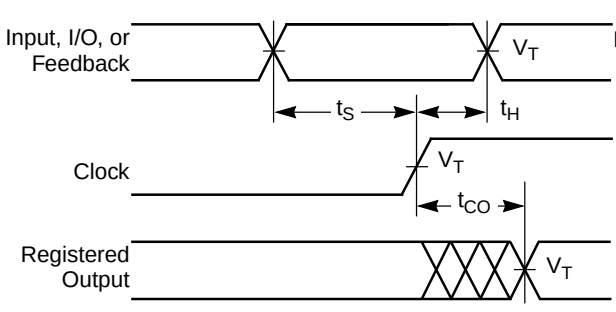
The data listed for plastic θ_{jc} are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θ_{jc} measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θ_{jc} tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment. The thermal measurements are taken with components on a six-layer printed circuit board.

SWITCHING WAVEFORMS



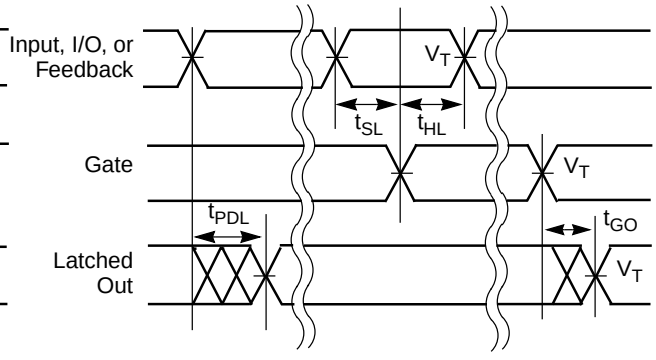
20405C-9

Combinatorial Output



20405C-10

Registered Output



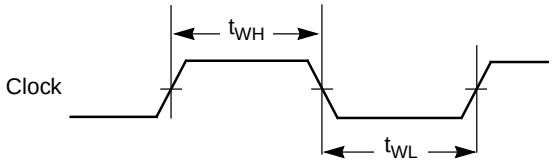
20405C-11

Latched Output

Notes:

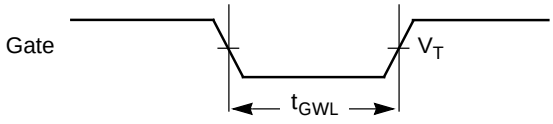
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



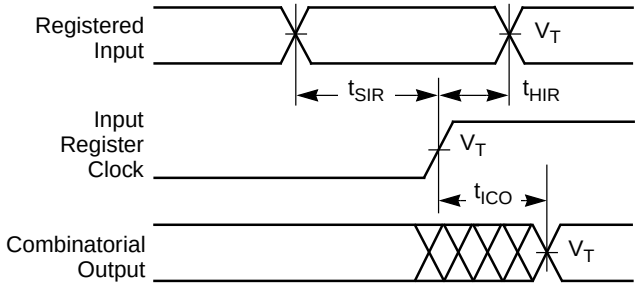
20405C-12

Clock Width



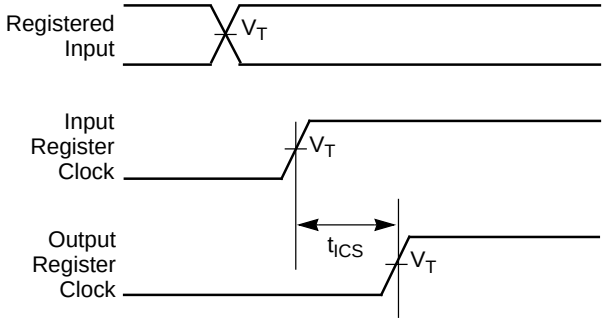
20405C-13

Gate Width



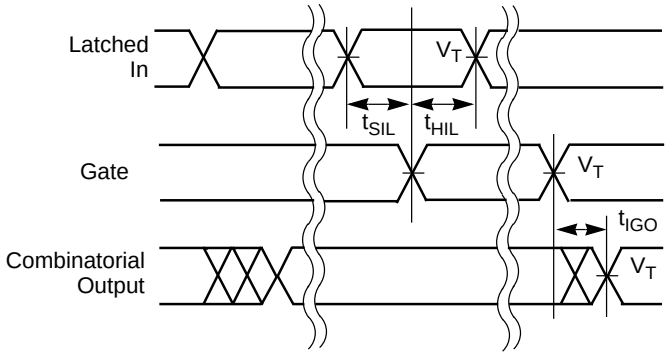
20405C-14

Registered Input



20405C-15

Input Register to Output Register Setup



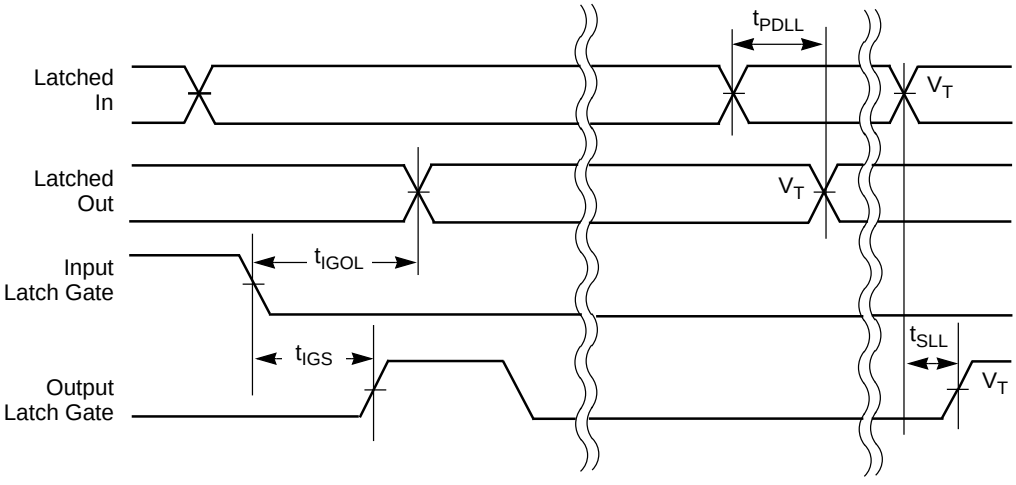
20405C-16

Latched Input

Notes:

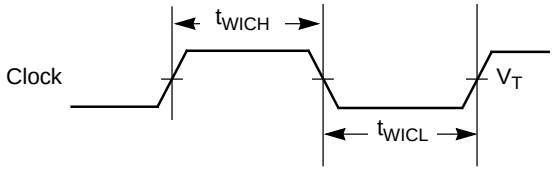
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



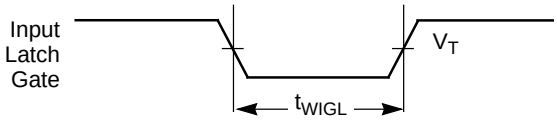
20405C-17

Latched Input and Output



20405C-18

Input Register Clock Width



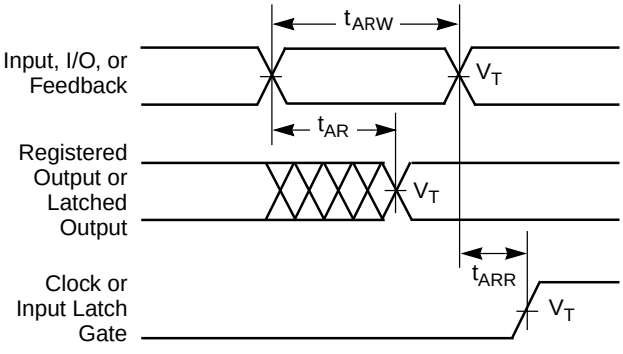
20405C-19

Input Latch Gate Width

Notes:

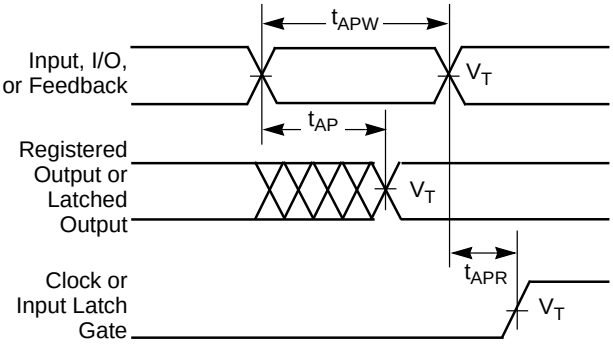
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



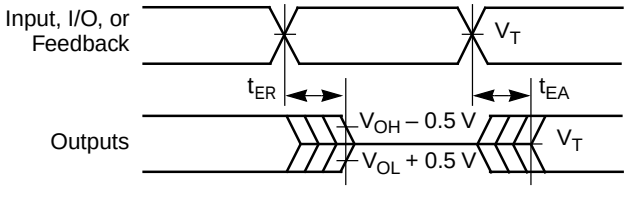
20405C-20

Asynchronous Reset



20405C-21

Asynchronous Preset



20405C-22

Output Disable/Enable

Notes:

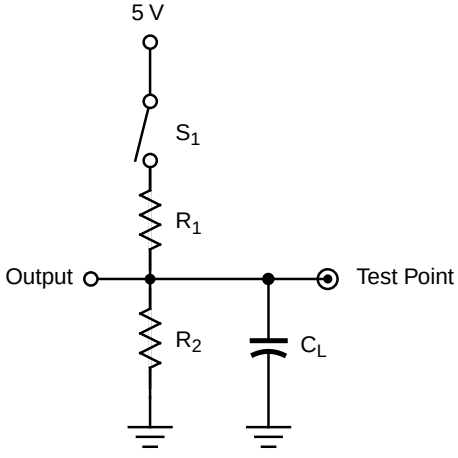
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT*



20405C-23

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

** Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

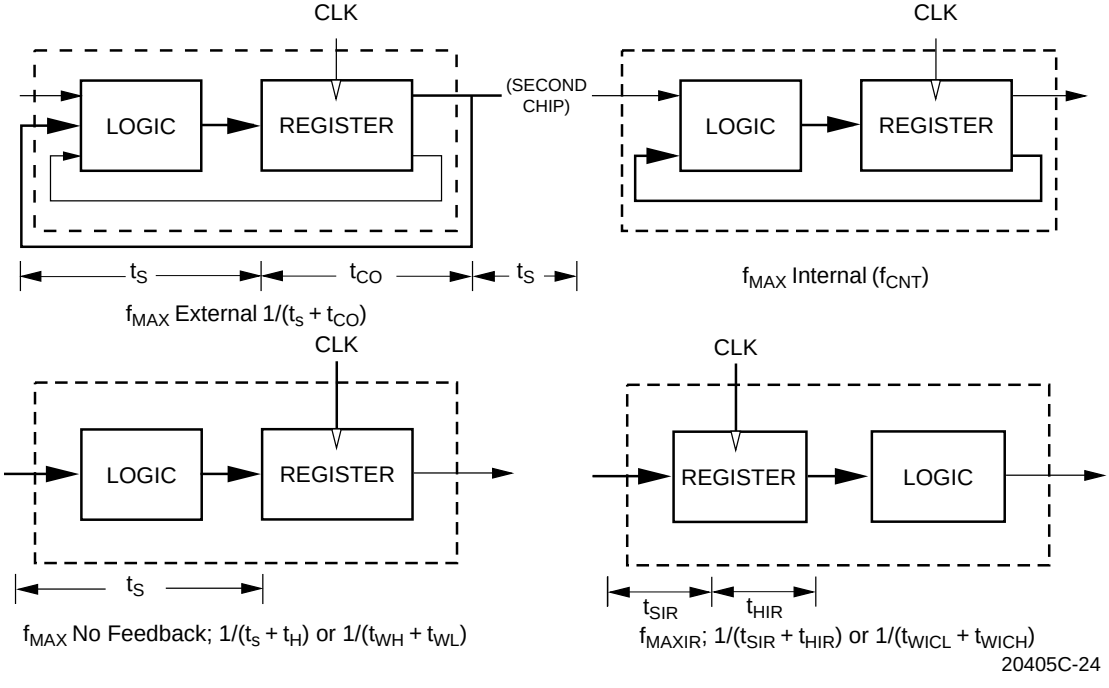
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are used in the same path, the overall frequency will be limited by t_{ICS}. All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



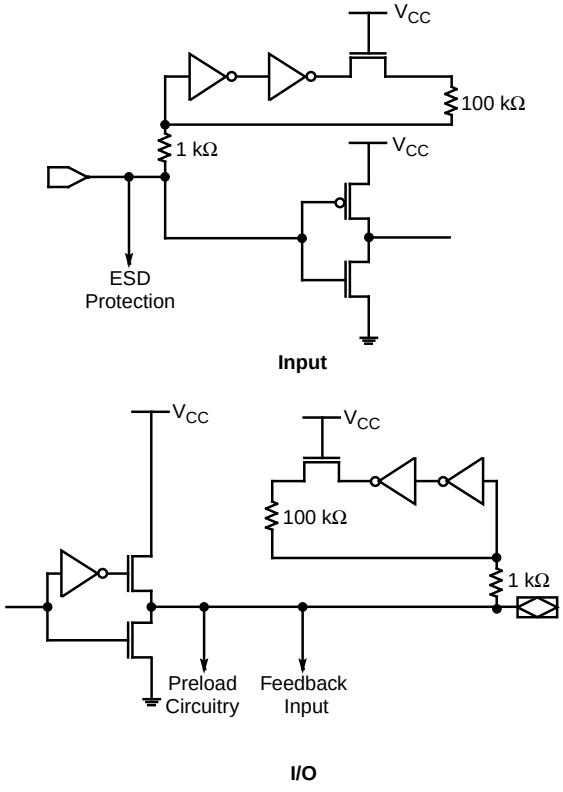
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using Vantis' advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

Endurance Characteristics

Parameter Symbol	Parameter Description		Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



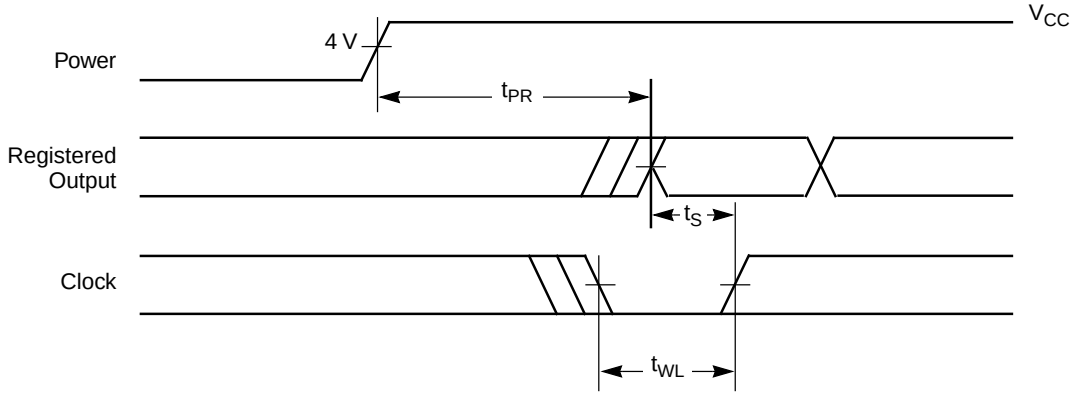
20405C-25

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



20405C-26

Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHXL Software Vantis-ABEL Software Vantis-Synario Software
Aldec, Inc. 3 Sunset Way, Suite F Henderson, NV 89014 (702) 456-1222 or (800) 487-8743	ACTIVE-CAD
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234 or (800) 746-6223	PIC Designer Concept/Composer Synergy Leapfrog/Verilog-XL
Exemplar Logic, Inc. 815 Atlantic Avenue, Suite 105 Alameda, CA 94501 (510) 337-3700	Leonardo™ Galileo™
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (800) 346-6335	SmartModel® Library
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	Design Architect, PLDSynthesis™ II Autologic II Synthesizer, QuickSim Simulator, QuickHDL Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	MicroSim Design Lab PLogic, PLSyn
MINC Inc. 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner-XL™ Software
Model Technology 8905 S.W. Nimbus Avenue, Suite 150 Beaverton, OR 97008 (503) 641-1340	V-System/VHDL
OrCAD, Inc. 9300 S.W. Nimbus Avenue Beaverton, OR 97008 (503) 671-9500 or (800) 671-9505	OrCAD Express
Synario® Design Automation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040 (415) 962-5000 or (800) 388-9125	FPGA or Design Compiler (Requires MINC PLDesigner-XL™) VSS Simulator
Synplicity, Inc. 624 East Evelyn Ave. Sunnyvale, CA 94086 (408) 617-6000	Synplify
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
VeriBest, Inc. 6101 Lookout Road, Suite A Boulder, CO 80301 (800) 837-4237	VeriBest PLD
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 873-8439 or (508) 480-0881	Viewdraw, ViewPLD, Viewsynthesis Speedwave Simulator, ViewSim Simulator, VCS Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 881-8821	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the local Vantis sales office.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 940 86 (408) 243-7000 or (800) 627-2456 BBS (408) 737-9200 Fax (408) 736-2503	Pilot-U40 Pilot-U84 MVP
BP Microsystems 1000 N. Post Oak Rd., Suite 225 Houston, TX 77055-7237 (800) 225-2102 or (713) 688-4600 BBS (713) 688-9283 Fax (713) 688-0920	BP1200 BP1400 BP2100 BP2200
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 426-1045 or (206) 881-6444 BBS (206) 882-3211 Fax (206) 882-1043	UniSite™ Model 2900 Model 3900 AutoSite
Hi-Lo Systems 4F, No. 2, Sec. 5, Ming Shoh E. Road Taipei, Taiwan (886) 2-764-0215 Fax (886) 2-756-6403 or Tribal Microsystems / Hi-Lo Systems 44388 South Grimmer Blvd. Fremont, CA 94538 (510) 623-8859 BBS (510) 623-0430 Fax (510) 623-9925	ALL-07 FLEX-700
SMS GmbH Im Grund 15 88239 Wangen Germany (49) 7522-97280 Fax (49) 7522-972850 or SMS USA 544 Weddell Dr. Suite 12 Sunnyvale, CA 94089 (408) 542-0388	Sprint Expert Sprint Optima Multisite
Stag House Silver Court Watchmead, Welwyn Garden City Herfordshire UK AL7 1LT 44-1-707-332148 Fax 44-1-707-371503	Stag Quazar

MANUFACTURER	PROGRAMMER CONFIGURATION
System General 1603A South Main Street Milpitas, CA 95035 (408) 263-6667 BBS (408) 262-6438 Fax (408) 262-9220 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Road, Shin Diau Taipei, Taiwan (886) 2-917-3005 Fax (886) 2-911-1283	Turpro-1 Turpro-1/FX Turpro-1/TX

APPROVED ADAPTER MANUFACTURERS

MANUFACTURER	PROGRAMMER CONFIGURATION
California Integration Coordinators, Inc. 656 Main Street Placerville, CA 95667 (916) 626-6168 Fax (916) 626-7740	MACH/PAL Programming Adapters
Emulation Technology, Inc. 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982-0660 Fax (408) 982-0664	Adapt-A-Socket® Programming Adapters

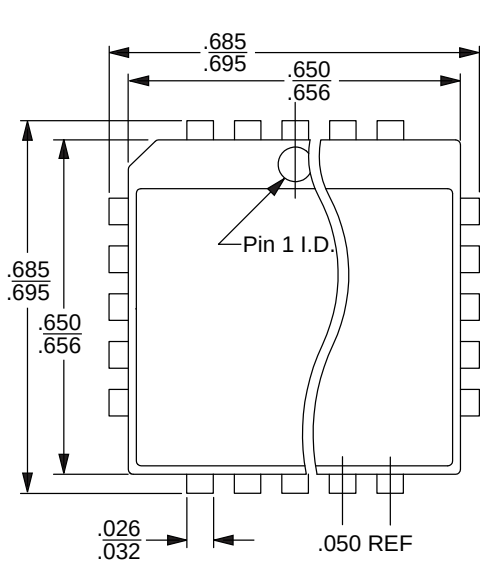
APPROVED ON-BOARD ISP PROGRAMMING TOOLS

MANUFACTURER	PROGRAMMER CONFIGURATION
Corelis, Inc. 12607 Hidden Creek Way, Suite H Cerritos, California 70703 (310) 926-6727	JTAGPROG™
Vantis Corporation P.O. Box 3755 920 DeGuigne Drive Sunnyvale, CA 94088 (408) 732-0555 or 1(888) 826-8472 (VANTIS2) http://www.vantis.com	MACHPRO®

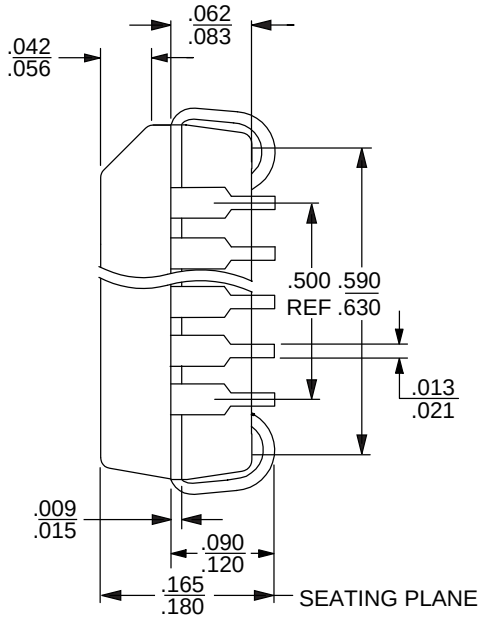
PHYSICAL DIMENSIONS

PL 044

44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW



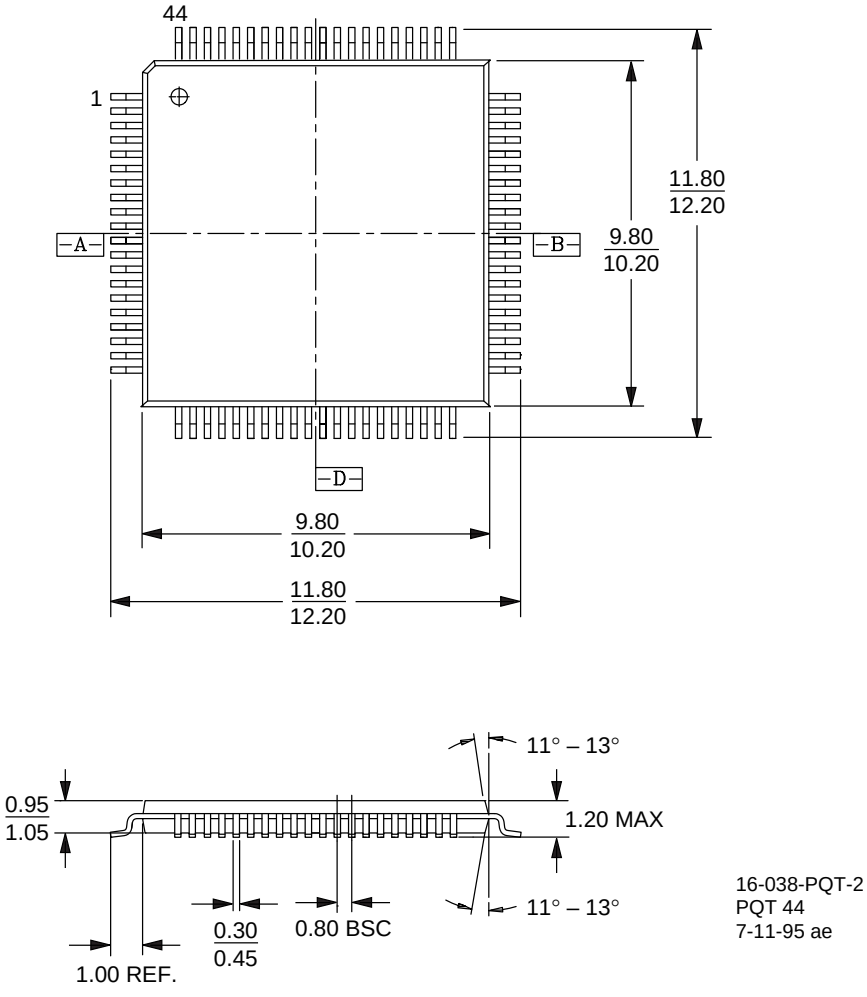
SIDE VIEW

16-038-SQ
PL 044
DA78
6-28-94 ae

PHYSICAL DIMENSIONS

PQT044

44-Pin Thin Quad Flat Pack (measured in millimeters)



16-038-PQT-2
PQT 44
7-11-95 ae

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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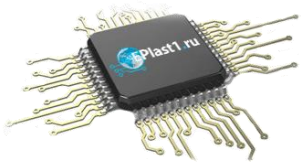
- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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