CMOS Integrated DTMF Transceiver

Features

- Advanced CMOS technology for low power consumption and increased noise immunity
- Complete DTMF Transmitter/Receiver
- Standard 6500/6800 microprocessor port
- Central office quality and performance
- Adjustable Guard Time
- Automatic Tone Burst mode
- Call Progress mode
- Single +5 volt power supply
- 20-pin DIP, 20-pin SOIC, 28-pin PLCC packages
- 2MHz microprocessor port operation
- No continuous Φ2 clock required, only strobe

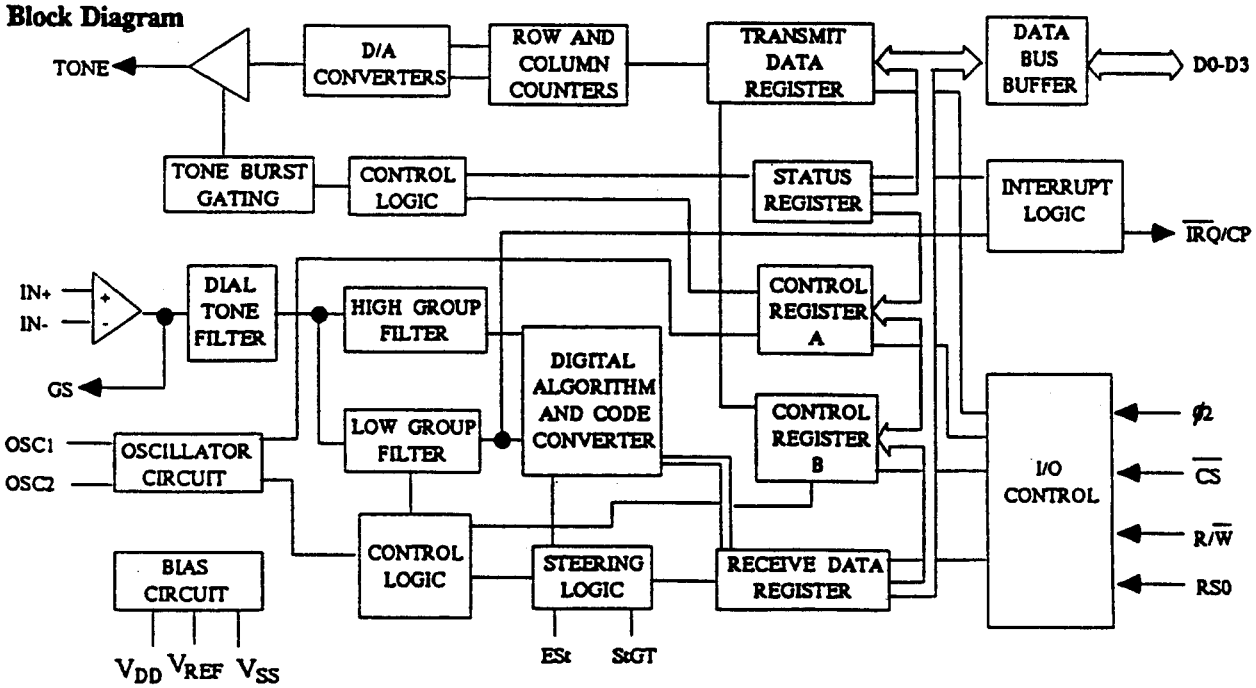
Applications

- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- PABX systems
- Computer systems
- Fax machines
- Pay telephones
- Credit card verification

General Description

The CMD CM8880 is a fully integrated DTMF Transceiver, featuring adjustable guard time, automatic tone burst mode, call progress mode and a fully compatible 6500/6800 microprocessor interface. The CM8880 is manufactured using state-of-the-art advanced CMOS technology for low power consumption and precise data handling. The CM8880 is based on the industry standard CM8870 DTMF Receiver, while the transmitter utilizes a switched-capacitor D/A converter for low distortion, highly accurate DTMF signaling. Internal counters provide an automatic tone burst mode which allows tone bursts to be transmitted with precise timing. A call progress filter can be selected by an external microprocessor for analyzing call progress tones. The CM8880-1 is functionally equivalent to the CM8880 but has input sensitivity to meet European specifications. The CM8880-2 is electrically equivalent to the CM8880 but does not include the call progress function.

Block Diagram



This is advance information and specifications are subject to change without notice.

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Absolute Maximum Ratings: (See Note)

Rating	Symbol	Value
Supply Voltage (V_{DD}-V_{SS})	V_{DD}	+6.0V Max
Voltage on any Pin	V_{dc}	-0.3V to V_{DD} +0.3V
Current on any Pin	I_{DD}	10 mA Max
Operating Temperature	T_A	-40°C to +85°C
Storage Temperature	T_S	-65°C to +150°C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating. Note: Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: All voltages referenced to V_{SS}, V_{DD} = 5.0V ± 5%, fc = 3.579545 MHz, T_A = -40°C to +85°C unless otherwise noted.

Parameter	Symbol	Min	Typ*	Max	Units
Operating Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Operating Supply Current	I_{DD}		10		mA
Power Consumption	P_O			52.5	mW
Inputs					
High Level Input Voltage OSC1	V_{IHO}	3.5			V
Low Level Input Voltage OSC1	V_{ILO}			1.5	V
Input Impedance (@1KHz) IN+, IN-	R_{IN}		10.0		MΩ
Steering Threshold Voltage (V_{DD}=5.0V)	V_{TSt}	2.2	2.3	2.5	V
Outputs					
High Level Output Voltage (No Load) OSC2	V_{OHO}	4.9			V
Low Level Output Voltage (No Load) OSC2	V_{OLO}			0.1	V
Output Leakage Current (V_{OH}=2.4V) IRQ	I_{OZ}		1.0	10.0	µA
V_{REF} Output Voltage (No Load)	V_{REF}	2.4		2.7	V
V_{REF} Output Resistance	R_{OR}			1	KΩ
Data Bus (DO-D3, Φ2, R/$\overline{W}$,, RSO, $\overline{CS}$)					
Low Level Input Voltage	V_{IL}			0.8	V
High Level Input Voltage	V_{IH}	2.0			V
Low Level Output Voltage (I_{OL}=1.6mA)	V_{OL}			0.4	V
High Level Output Voltage (I_{OH}=400µA)	V_{OH}	2.4			V
Input Leakage Current (V_{IN} = 0.4 to 2.4V)	I_{IZ}			10.0	µA

* Typical values are for use as design aids only, and are not guaranteed through production testing.

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Electrical Characteristics - Gain Setting Amplifier: All voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25°C

Parameter	Symbol	Min	Typ*	Max	Units
Input Leakage Current ($V_{SS} \le V_{IN} \le V_{DD}$)	I_{IN}		100		nA
Input Resistance	R_{IN}		10		MΩ
Input Offset Voltage	V_{OS}		25		mV
Power Supply Rejection (1 KHz)	PSRR		60		dB
Common Mode Rejection (-3.0V ≤ V_{IN} ≤ 3.0V)	CMRR		60		dB
DC Open-Loop Voltage Gain	A_{VOL}		65		dB
Unity Gain Bandwidth	BW		1.5		MHz
Output Voltage Swing ($R_L \ge$ 100KΩ to V_{SS})	V_O		4.5		V_{PP}
Maximum Capacitive Load GS	C_L		100		pF
Maximum Resistive Load GS	R_L		50		KΩ
Common Mode Range (No Load)	V_{CM}		3.0		V_{PP}

AC Characteristics: All Voltages referenced to V_{SS} unless otherwise noted. V_{DD} = 5.0V, V_{SS} = OV, fc = 3.579545 MHz

Receive Signal Conditions

Valid Input Signal Levels CM8880, CM8880-2 (Each Tone of Composite Signal; Notes 1, 2, 3, 5, 6, 9)		-29 27.5		+1 869	dBm mV_{RMS}
Valid Input Signal Levels CM8880-1 (Each Tone of Composite Signal; Notes 1, 2, 3, 5, 6, 9)		-31 21.8		+1 869	dBm mV_{RMS}
Input Signal Level Reject CM8880-1 (Each Tone of Composite Signal; Notes 1, 2, 3, 5, 6, 9)		-37 10.9			dBm mV_{RMS}
Positive Twist Accept (Notes 2, 3, 6, 9)				6	dB
Negative Twist Accept (Notes 2, 3, 6, 9)				6	dB
Freq. Deviation Accept (Notes 2, 3, 5, 9)		±1.5% ±2 Hz			Nom.
Freq. Deviation Reject (Notes 2, 3, 5)		±3.5%			Nom.
Third Tone Tolerance (Notes 2, 3, 4, 5, 9, 10)			-16		dB
Noise Tolerance (Notes 2, 3, 4, 5, 7, 9, 10)			-12		dB
Dial Tone Tolerance (Notes 2, 3, 4, 5, 8, 9, 11)			+22		dB

Call Progress (CM8880, CM8880-1)

Lower Frequency (@ -25 dBm) ACCEPT	f_{LA}		320		Hz
Upper Frequency (@ -25 dBm) ACCEPT	f_{HA}		510		Hz
Lower Frequency (@ -25 dBm) REJECT	f_{LR}		290		Hz
Upper Frequency (@ -25 dBm) REJECT	f_{HR}		540		Hz

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Receive Timing

Parameter	Symbol	Min	Typ*	Max	Units
Tone Present Detect Time	t_{DP}	5	11	14	mS
Tone Absent Detect Time	t_{DA}	0.5	4	8.5	mS
Tone Duration Accept (Ref. Fig. 9)	t_{REC}			40	mS
Tone Duration Reject (Ref. Fig. 9)	$t_{\overline{REC}}$	20			mS
Interdigit Pause Accept (Ref. Fig. 9)	t_{ID}			40	mS
Interdigit Pause Reject (Ref. Fig. 9)	t_{DO}	20			mS
Delay St to b3	t_{PStb3}		13		µS
Delay St to RX_0-RX_3	t_{PStRX}		8		µS

Transmit Timing

Tone Burst Duration (DTMF Mode)	t_{BST}	50		52	mS
Tone Pause Duration (DTMF Mode)	t_{PS}	50		52	mS
Tone Burst Duration (Extended, Call Process Mode)	t_{BSTE}	100		104	mS
Tone Pause Duration (Extended, Call Process Mode)	t_{PSE}	100		104	mS

Tone Output

High Group Output Level (R_L = 10 KΩ)	V_{HOUT}	-6.1		-2.1	dBm
Low Group Output Level (R_L = 10 KΩ)	V_{LOUT}	-8.1		-4.1	dBm
Pre-emphasis (R_L - 10KΩ)	dB_P	0	2	3	dB
Output Distortion (R_L = 10KΩ, 3.4 KHz Bandwidth)	THD		-25		dB
Frequency Deviation (f = 3.5795 MHz)	f_D		±0.7	±1.5	%
Output Load Resistance	R_{LT}	10		50	KΩ

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AC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40°C to +85°C

Microprocessor Interface

Parameter	Symbol	Min	Typ*	Max	Units
Φ2 Cycle Period	t_{CYC}	0.5			μs
Φ2 High Pulse Width	t_{CH}	200			ns
Φ2 Low Pulse Width	t_{CL}	180			ns
Φ2 Rise and Fall Time	t_R, t_F			25	ns
Address, R/$\overline{W}$ Hold Time	t_{AH}, t_{RWH}	10			ns
Address, R/$\overline{W}$ Setup Time (Prior to Φ2)	t_{AS}, t_{RWS}	23			ns
Data Hold Time (Read)	t_{DHR}	22			ns
Φ2 to Valid Data Delay (Read) (200pF load)	t_{DDR}			150	ns
Data Setup Time (Write)	t_{DSW}	45			ns
Data Hold Time (Write)	t_{DHW}	10			ns
Input Capacitance DO-D3	C_{IN}		5		pF
Output Capacitance $\overline{IRQ}$ CP	C_{OUT}		5		pF

DTMF Clock

Crystal Clock Frequency	fc	3.5759	3.5795	3.5831	MHz
Clock Input Rise Time (External Clk)	t_{LHCL}			110	ns
Clock Input Fall Time (External Clk)	t_{HLCL}			110	ns
Clock Input Duty Cycle (External Clk)	DC_{CL}	40	50	60	%
Capacitive Load OSC2	C_{LO}			30	pF

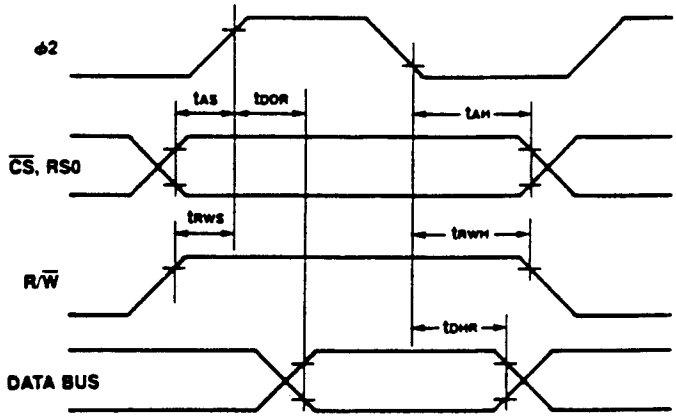
* Typical values are for use as design aids only, and are not guaranteed or subject to production testing.

Notes:

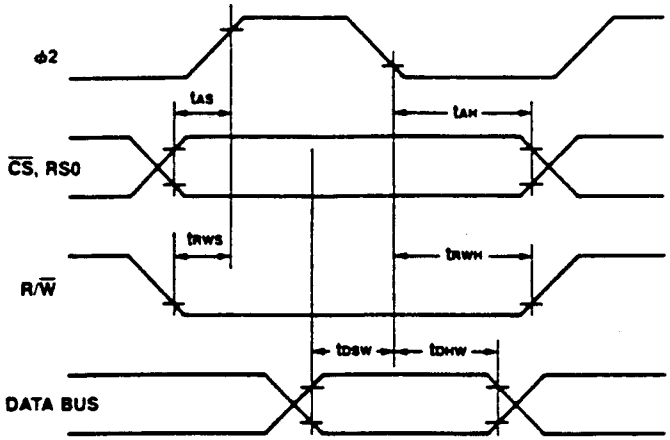
1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40 mS. Tone pause = 40 mS.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. The tone pair is deviated by ± 1.5% ± 2Hz.
7. Bandwidth limited (3 KHz) Gaussian noise.
8. The precise dial tone frequencies are 350 and 440 Hz (±2%)
9. For an error date of less than 1 in 10,000.
10. Referenced to the lowest amplitude tone in the DTMF signal.
11. Referenced to the minimum valid accept level.

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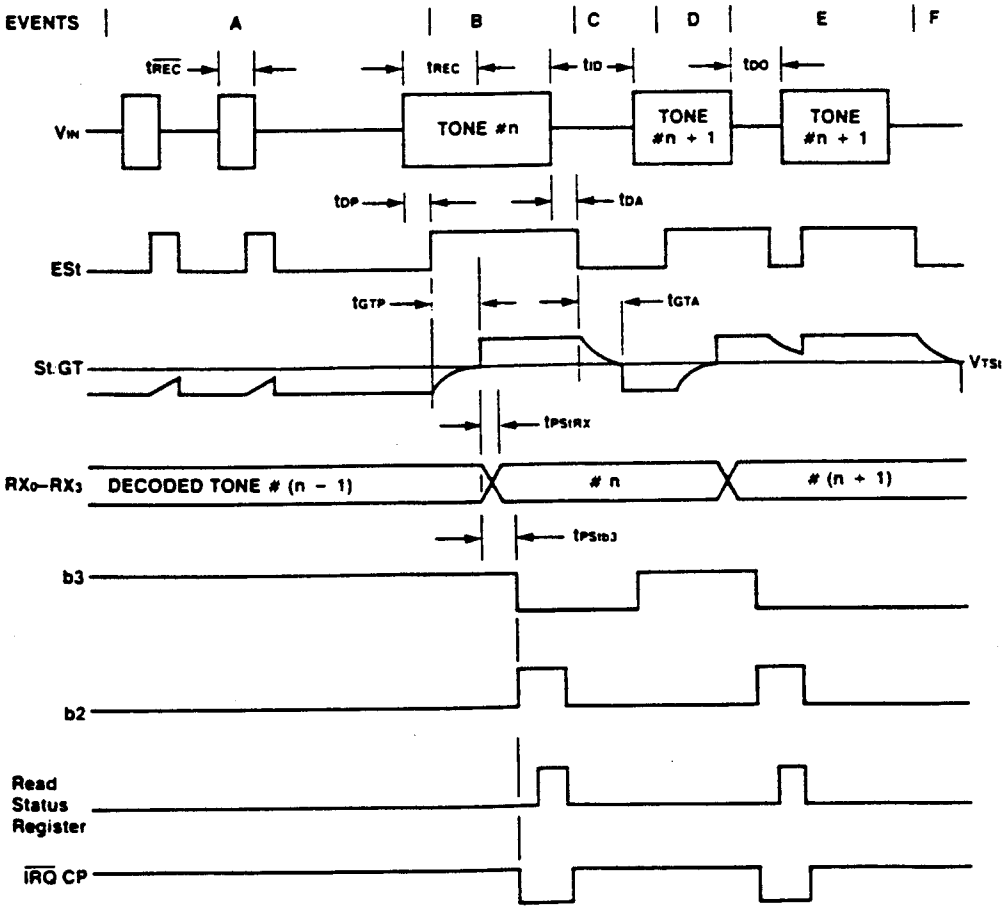
Microprocessor Read Cycle



Microprocessor Write Cycle



General Transceiver Timing



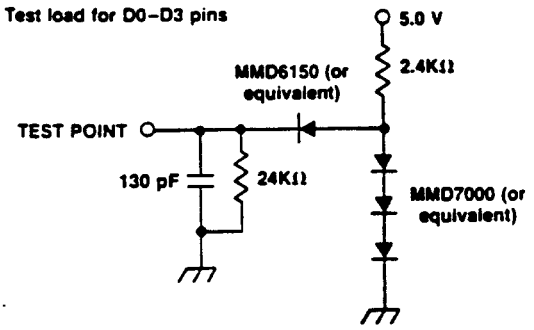
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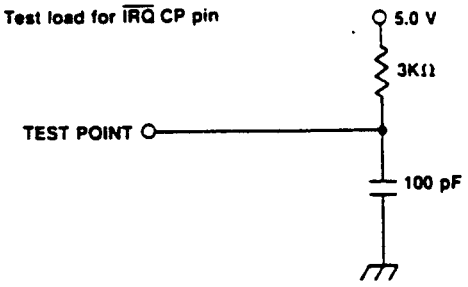
Explanation of Events

A	Tone bursts detected, tone duration invalid, RX data register not updated.
B	Tone #n detected, tone duration valid, tone decoded and latched in RX data register.
C	End of tone #n detected, tone absent duration valid, information in RX data register retained until next valid tone pair.
D	Tone #n + 1 detected, tone duration valid, tone decoded and latched in RX data register.
E	Acceptable dropout of tone #n + 1, tone absent duration invalid, data remains unchanged.
F	End of tone #n + 1 detected, tone absent duration valid, information in RX data register retained until next valid tone pair.

Explanation of Symbols

V_{IN}	DTMF composite input signal.
ESt	Early steering output. Indicates detection of valid tone frequencies.
St/GT	Steering input/guard time output. Drives external RC timing circuit.
RX_0-RX_3	4-bit decoded data in receive data register.
b3	Delayed steering. Indicates that valid frequencies have been present/absent for the required guard time thus consituting a valid signal. Active low for the duration of a valid DTMF signal.
b2	Indicates that valid data is in the receive data register. The bit is cleared after the status register is read.
IRQ/CP	Interrupt is active indicating that new data is in the R X data register. The interrupt is cleared after the status register is read.
$\overline{tREC}$	Maximum DTMF signal duration not detected as valid.
tREC	Minimum DTMF signal duration required for valid recognition.
t_{ID}	Minimum time between valid sequential DTMF signals.
t_{DO}	Maximum allowable dropout during valid DTMF signal.
t_{DP}	Time to detect valid frequencies present.
t_{DA}	Time to detect valid frequencies absent.
t_{GTP}	Guard time, tone present.
t_{GTA}	Guard time, tone absent.





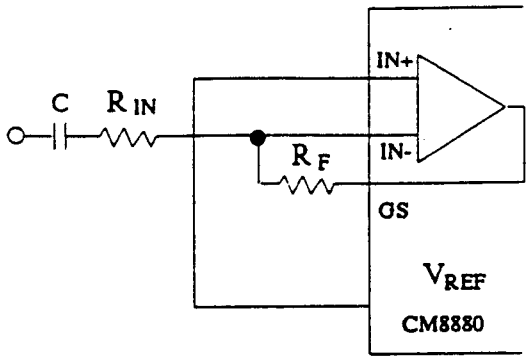
Functional Description

The CM8880 Integrated DTMF Transceiver provides the design engineer with not only low power consumption, but central office quality performance. The CM8880's internal architecture consists of a high performance DTMF receiver with an internal Gain Setting Amplifier and DTMF Generator. The DTMF Generator contains a Tone Burst Counter for generating precise tone bursts and pauses. The Call Progress mode, when selected, allows the detection of call progress tones. A standard 8051, 8086/8 series microprocessor interface allows access to an internal status register, two control registers and two data registers within the CM8880.

Input Configuration

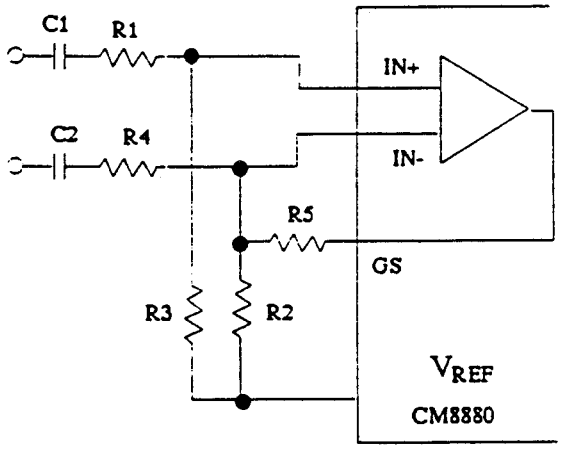
The CM8880 input arrangement consists of a differential input operational amplifier and bias sources (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the op amp output (GS) for gain adjustment. In the single-ended configuration, the input pins should be connected as shown in Figure 1, while Figure 2 shows the necessary connections for a differential input configuration.

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VOLTAGE GAIN
$(A_V) = R_F / R_{IN}$

Figure 1. Single-Ended Input Configuration



DIFFERENTIAL INPUT AMPLIFIER
C1 = C2 = 10nF
R1 = R4 = R5 = 100KΩ
R2 = 60KΩ, R3 = 37.5KΩ
R3 = (R2R5)/(R2 + R5)
VOLTAGE GAIN
(Av diff) = R5/R1
INPUT IMPEDANCE
$(Z_{IN}\ diff) = \sqrt{2\ R1^2 + (1/wC)^2}$

Figure 2. Differential Input Configuration

Receiver Section

Separation of the low and high-group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high-group frequencies as shown in Figure 5. The low-group filter incorporates notches at 350 Hz and 440 Hz for excellent dial-tone rejection. Each filter output is followed by a single-order switched capacitor filter section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparators with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full-rail logic swings at the incoming DTMF signals frequencies.

Following the filter section is a decoder which employs digital counting techniques to determine the frequencies of the incoming tones, and to verify that the incoming tones correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals (e.g. voice), while still providing tolerance to small deviations in frequency. The averaging algorithm was developed to ensure an optimum combination of immunity to talk-off, as well as a tolerance to the presence of interfering frequencies (3rd tones) and noise. When the detector recognizes the presence of two valid tones (sometimes referred to as "signal condition" in industry publications), the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as Character Recognition Condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (See Figure 3) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (See Figure 5) into the Receive Data Register. At this point the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the Delayed Steering output flag goes high, signalling that a received tone pair has been registered. It is possible to monitor the status of the Delayed Steering flag by checking the appropriate bit in the Status Register. If Interrupt Mode has been selected, the IRQ/CP pin will pull low when the Delayed Steering flag is active.

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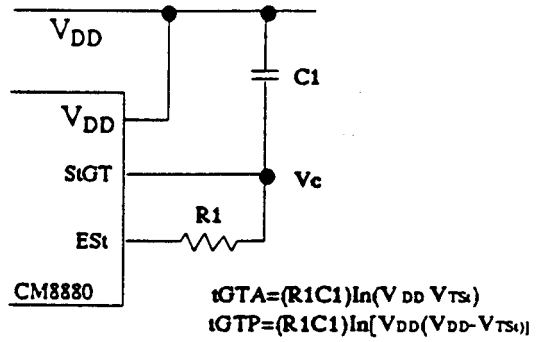


Figure 3. Basic Steering Circuit

The contents of the output latch are updated on an active Delayed Steering transition. This data is presented to the 4-bit bi-directional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

The simple steering circuit shown in Figure 3 is adequate for most applications. Component values are chosen according to the formula:

$$tREC = tDP + tGTP$$
$$tID = tDA + tGTA$$

The value of tDP is a device parameter and tREC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. Different steering arrangements may be used to select independently the guard times for tone present (tGPT) and tone absent (tGTA). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard Time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing tREC improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short tREC with a long tDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for Guard Time adjustment is shown in Figure 4.

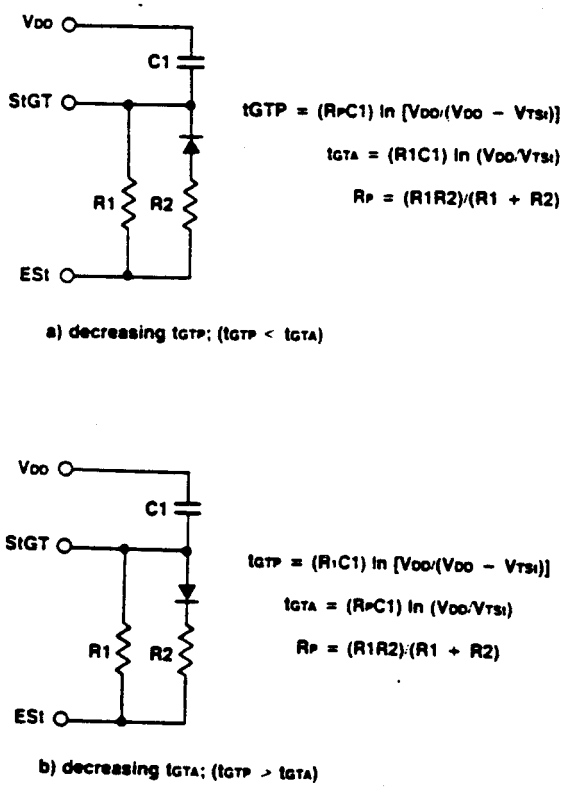


Figure 4. Guard Time Adjustment

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FLOW	FHIGH	DIGIT	D3	D2	D3	DO
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	•	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0 = LOGIC LOW, 1 = LOGIC HIGH

Figure 5. Functional Encode/Decode

Call Progress Filter (CM8880, CM8880-1)

A Call Progress (CP) Mode can be selected allowing the detection of various tones which identify the progress of a telephone call on the network. The Call Progress tone input and DTMF input are common, however, call progress tones can only be detected when the CP Mode has been selected. DTMF signals cannot be detected if the CP Mode has been selected (see Table 5). Figure 6 indicates the useful detect bandwidth of the Call Progress filter. Frequencies presented to the input (IN+ and IN-) which are within the 'accept' bandwidth limits of the filter are hard-limited by a high-gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The square wave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the Call Progress tone being detected. Frequencies which are in the 'reject' area will not be detected, and consequently there will be no activity on $\overline{IRQ}$/CP as a result of these frequencies.

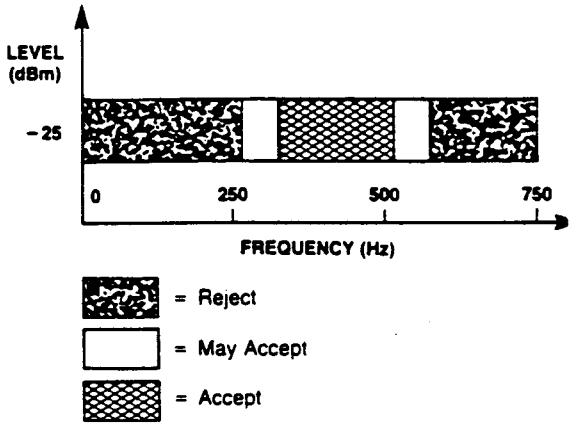


Figure 6. Call Progress Response

DTMF Generator

The DTMF transmitter employed in the CM8880 is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Figure 5 must be written to the Transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. As seen from Table 1, the Low-Group frequencies are

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697, 770, 852, and 941 Hz; the High-Group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically the High-Group to Low-Group amplitude ratio (twist) is 2dB to compensate for High-Group attenuation on long loops.

DTMF Generator Operation

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the transmit data register, 4-bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32; however, by varying the segment length as described above, the frequency can also be varied. The divider output clocks another counter which addresses the sinewave lookup ROM. The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously, thus providing a high degree of tone burst accuracy. Under conditions when there is no tone output signal, the TONE pin assumes a DC level of 2.5 volts (typ). A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 4 KHz. It can be seen from Figure 7 that the distortion products are very low in amplitude.

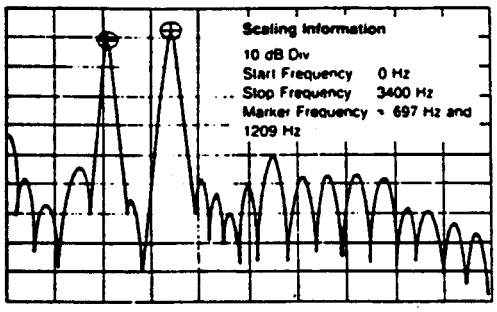


Figure 7. Spectrum Plot

ACTIVE CELL	OUTPUT FREQUENCY (Hz)		% ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1447	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 1. Actual Frequencies Versus Standard Requirements

Burst Mode

In certain telephony applications it is required that DTMF signals being generated be of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 mS ± 1 mS which is a standard interval for autodialer and central office applications. After the burst pause has been issued, the appropriate bit is set in the Status Register, indicating that the transmitter is ready for more data. The timing described above is available when the DTMF Mode has been selected. However, when CP Mode (Call Progress Mode) is selected, a secondary burst/pause time is available such that this interval is extended to 102 mS ± 2 mS. The extended interval is useful when precise tone bursts of longer than 51 mS duration and 51 mS pause are desired. Note that when CP mode and burst mode have been selected, DTMF tones may be transmitted only and not received. In certain applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

The CM8880 is initialized on power-up sequence such that DTMF mode and burst mode are selected.

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The CM8880 is initialized on power-up sequence such that DTMF mode and burst mode are selected.

Single Tone Generation

A Single Tone Mode is available whereby individual tones from the low-group or high-group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B (Table 6) description for details.

Distortion Calculations

The CM8880 is capable of producing precise tone bursts with minimal error in frequency (See Table 1). The internal summing amplifier is followed by a first-order low-pass switched-capacitor filter to minimize harmonic components and intermodulation products.

$$THD(\%) = 100\ \frac{\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + \ldots V^2_{nf}}}{V_{fundamental}}$$

Equation 1. THD(%) For a Single Tone

$$THD(\%) = 100\ \frac{\sqrt{V^2_{2L} + V^2_{3L} + \ldots V^2_{nL} + V^2_{2H} + V^2_{3H} + \ldots V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD(%) For a Dual Tone

The total harmonic distortion for a single tone can be calculated using Equation 1 which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage. The Fourier components of the tone output correspond to V2f....Vnf as measured on the output waveform. The total harmonic distortion for a dual tone can be calculated using Equation 2. V_L and V_H correspond to the low-group amplitude and high-group amplitude, respectively, and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 7.

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television color burst crystal having a resonant frequency of 3.579545 MHz. A number of CM8880 devices can be connected as shown in Figure 8 such that only one crystal is required.

Figure 8. Common Crystal Connection

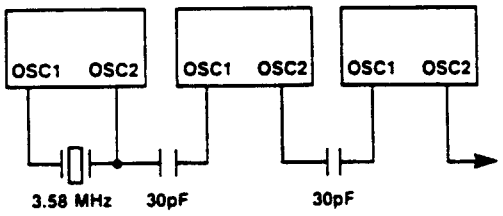


Table 2. Internal Register Functions

RSO	RD	WR	Function
0	1	0	Write to Transmitter
0	0	1	Read from Receiver
1	1	0	Write to Control Register
1	0	1	Read from Status Register

Table 3. CRA Bit Positions

b3	b2	b1	b0
RSEL	IRQ	CP $\overline{\text{DTMF}}$	TOUT

Table 4. CRB Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST

Microprocessor Interface

The CM8880 employs a microprocessor interface which allows precise control of transmitter and receiver functions. There are five internal registers associated with the microprocessor interface which can be subdivided into three categories, ie; data transfer, transceiver control and transceiver status.

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There are two registers associated with data transfer operations. The Receive Data Register contains the output code of the last valid DTMF tone pair to be decoded and is a read-only register. The data entered in the Transmit Data Register will determine which tone pair is to be generated (See Figure 5 for coding details). Data can only be written to the Transmit Data Register. Transceiver control is accomplished with two Control Registers (CRA and CRB) which occupy the same address space. A write operation to CRB can be executed by setting the appropriate bit in CRA. The following write operation to the same address will then be directed to CRB and subsequent write cycles will then be directed back to CRA. Internal reset circuitry will clear the control registers on power-up; however, as a precautionary measure the initialization software should include a routine to clear the registers. Refer to Table 5 and 6 for details concerning the Control Registers. The $\overline{IRQ}$/CP pin can be programmed such that it will provide an interrupt request signal upon validation of DTMF signals, or when the transmitter is ready for more data (Burst mode only). The $\overline{IRQ}$/CP pin is configured as an open-drain output device and as such requires a pull-up resistor (See Figure 9).

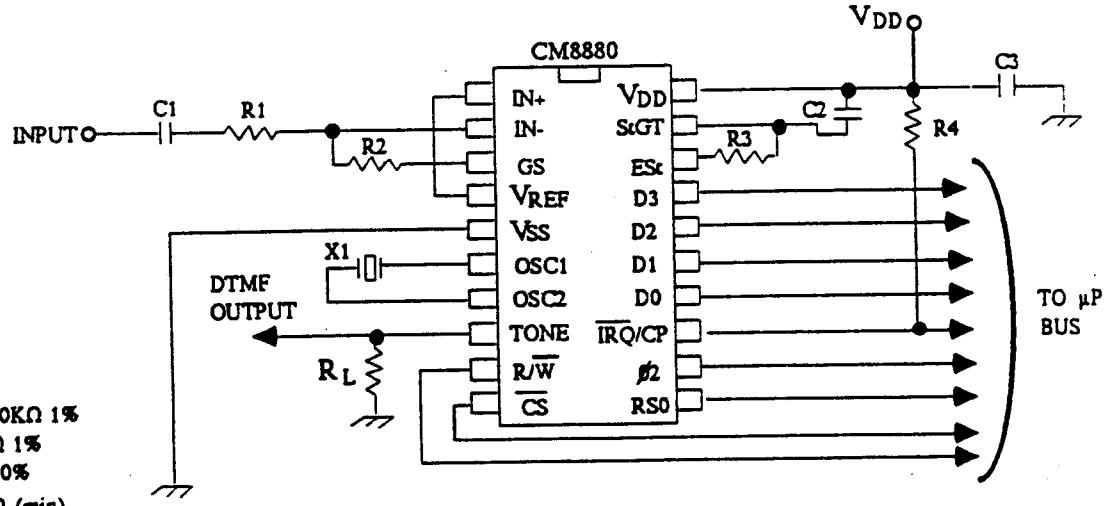
Table 5. Control Register A Description

Bit	Name	Function	Description
b0	TOUT	Tone Output	A logic '1' enables the Tone Output. This function can be implemented in either the Burst Mode or Non-Burst Mode.
b1	CP/$\overline{DTMF}$	Mode Control	In DTMF Mode (logic '0'), the device is capable of generating and receiving Dual Tone Multi-Frequency signals. When the CP (Call Progress) mode is selected (logic '1'), a 6th order bandpass filter is enabled to allow Call Progress tones to be detected. Call Progress tones which are within the specified bandwidth will be presented at the $\overline{IRQ}$/CP pin in rectangular wave format if the IRQ bit has been enabled (b2=1). Also when the CP mode and Burst Mode have both been selected, the transmitter will issue DTMF signals with a burst and pause of 102 mS (typ) duration. This signal duration is twice that obtained from the DTMF transmitter, if DTMF mode had been selected. Note that signals cannot be decoded when the CP mode of operation has been selected.
b2	IRQ	Interrupt Enable	A logic '1' enables the Interrupt Mode. When this mode is active and the DTMF Mode has been selected (b1=0), the $\overline{IRQ}$/CP pin will pull to a logic '0' condition when either 1) a validDTMF signal has been received and has been present for the guard time duration or 2) the transmitter is ready for more data (Burst Mode only).
b3	RSEL	Register Select	A logic '1' selects Control Register B on the next write cycle to the Control Register address. Subsequent write cycles to the Control Register are directed back to Control Register A.

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Table 6. Control Register B Description

Bit	Name	Function	Description
b0	BURST	Burst Mode	A logic '0' enables the Burst Mode. When this mode is selected, data corresponding to the desired DTMF tone pair can be written to the Transmit Data Register, resulting in a tone burst of a specific duration (See AC Characteristics). Subsequently, a pause of the same duration is induced. Immediately following the pause, the Status Register is updated indicating that the Transmit Data Register is ready for further instructions, and an interrupt will be generated if the Interrupt Mode has been enabled. Additionally, if Call Progress (CP) Mode has been enabled, the burst and pause duration is increased by a factor of two. When the Burst Mode is not selected (logic '1') tone bursts of any desired duration may be generated.
b1	TEST	Test Mode	By enabling the Test Mode (logic '1') the $\overline{IRQ}$/CP pin will present the delayed steering (inverted) signal from the DTMF receiver. Refer to General Transceiver Timing (b3 waverform) for details concerning the output waveform. DTMF Mode must be selected (CRA b1 = 0) before Test Mode can be implemented.
b2	S/$\overline{D}$	Single/Dual Tone Generation	A logic '0' will allow Dual Tone Multi-Frequency signals to be produced. If single-tone generation is enabled (logic '1'). either row or column tones (low-group or high-group) can be genrated depending on the state of b3 in Control Register B.
b3	C/$\overline{R}$	Column/Row Tones	When used in conjunction with b2 (above) the transmitter can be made to generate single-row or single-column frequencies. A logic '0' will select row frequencies and a logic '1' will select column frequencies.



Notes:
R1, R2 = 100KΩ 1%
R3 = 374KΩ 1%
R4 = 3KΩ 10%
R_L = 10KΩ (min)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%
X1 = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the CM8880 can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 9. Application Circuit (Single Ended Input)

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Table 7. Status Register Description

Bit	Name	Status Flag Set	Status Flag Cleared
b0	IRQ	Interrupt has occurred. Bit one (b1) and/or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	Transmit Data Register Empty (Burst Mode Only)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in Non-Burst Mode.
b2	Receive Data Register Full	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{Delayed Steering}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

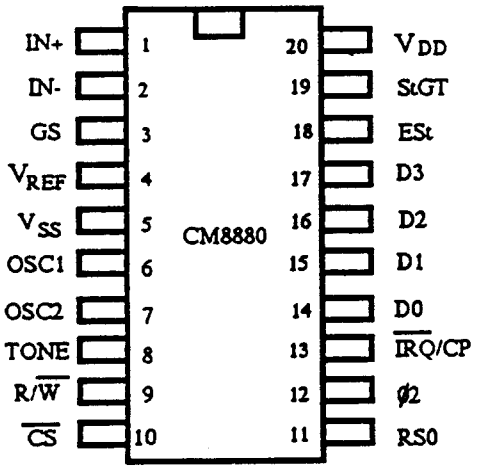
Pin Function Table

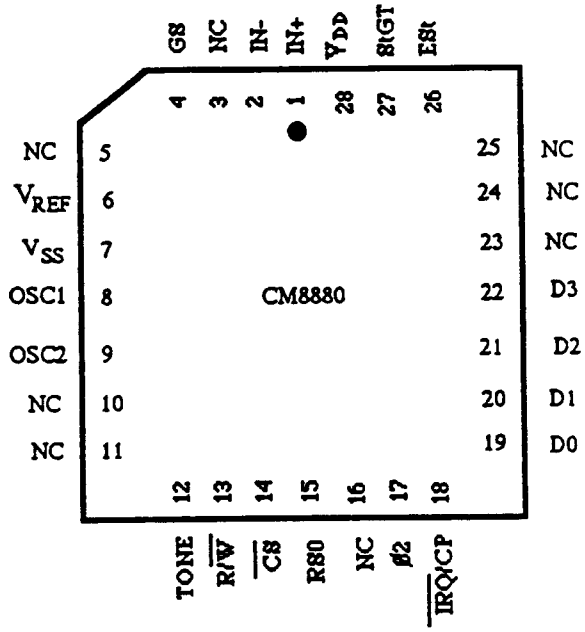
Name	Description
IN+	Non-inverting op-amp input.
IN-	Inverting op-amp input.
GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{REF}	Reference voltage output. Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see application circuit).
V_{SS}	Negative power supply input.
OSC1	DTMF clock/oscillator input.
OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
TONE	Dual Tone Multi-Frequency (DTMF) output.
R/$\overline{\text{W}}$	Read/write input. Controls the direction of data transfer to and from the microprocessor and the CM8880. TTL compatible.
CS	Chip Select. TTL input (CS = 0 to select the chip).
RSO	Register select input. See register decode table. TTL compatible.
Φ2	System clock input. May be continuous or strobed only during read or write. TTL compatible.

Name	Description
$\overline{\text{IRQ}}$/CP	Interrupt request to microprocessor (open-drain output). Also, when Call Progress (CP) Mode has been selected and Interrupt enabled the IRQ/CP pin will output a rectangular wave signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the Call Progress filter. See Filter 6.
D0-D3	Microprocessor data bus. TTL compatible.
ESt	Early Steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
StGT	Steering input/Guard Time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the extenal steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	Positive power supply input.

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Pin Configuration





Ordering Information

CM8880 P I

Product Identification Number

CM8880-2 -- Standard
CM8880 -- Standard With Call Progress Mode
CM8880-1 -- European Input Specification

Package

P -- Plastic E -- Leaded Chip Carrier S -- Small Outline
C -- Ceramic L -- Leadless Chip Carrier
D -- Cerdip X -- Dice

Temperature/Processing

I -- - 40°C to + 85°C, ± 5% P.S. Tol.

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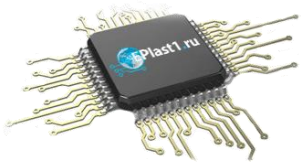
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