

# MC100LVEL32

## 3.3V ECL ÷2 Divider

### Description

The MC100LVEL32 is an integrated ÷2 divider. The LVEL32 is functionally identical to the EL32, but operates from a 3.3 V supply.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flop will attain a random state; the reset allows for the synchronization of multiple LVEL32's in a system.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

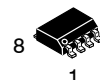
- 510 ps Propagation Delay
- 2.6 GHz Typical Maximum Frequency
- ESD Protection: Human Body Model; >4 kV, Machine Model; >200 V
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  
 $V_{CC} = 3.0$  V to 3.8 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  
 $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to  $-3.8$  V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1  
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 111 devices
- Pb-Free Packages are Available



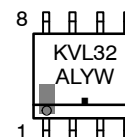
ON Semiconductor®

<http://onsemi.com>

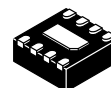
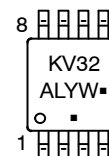
### MARKING DIAGRAMS\*



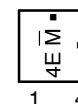
SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M̄ = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# MC100LEVEL32

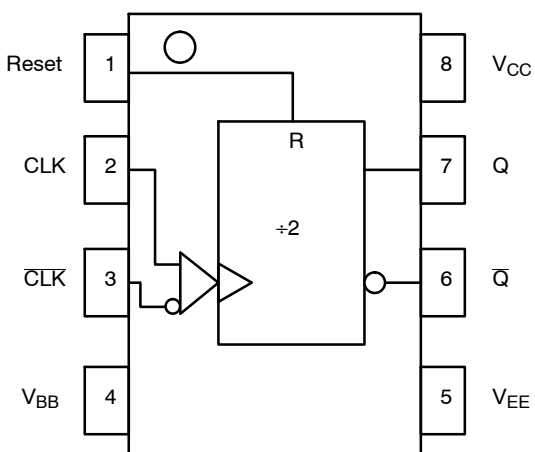


Figure 1. Logic Diagram and Pinout Assessment

Table 1. PIN DESCRIPTION

| Pin                                | Function   |
|------------------------------------|--|
| CLK*, $\overline{\text{CLK}}^{**}$ | ECL Differential Clock Inputs  |
| Q, $\overline{\text{Q}}$           | ECL Differential Data +2 Outputs   |
| Reset*                             | ECL Asynch Reset   |
| V <sub>BB</sub>                    | Reference Voltage Output   |
| V <sub>CC</sub>                    | Positive Supply  |
| V <sub>EE</sub>                    | Negative Supply  |
| EP                                 | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

\*Pin will default low when left open, per internal 75 K pull-down to V<sub>EE</sub>.

\*\* Pin will default to V<sub>CC</sub>/2 when left open per internal 75 K $\Omega$  pull-down to V<sub>EE</sub> and 75 K $\Omega$  pull-up to V<sub>CC</sub>.

Table 2. MAXIMUM RATINGS

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating            | Unit                             |
|------------------|--|--|--|-------------------|----------------------------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 8 to 0            | V                                |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | -8 to 0           | V                                |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> $\leq$ V <sub>CC</sub><br>V <sub>I</sub> $\geq$ V <sub>EE</sub> | 6 to 0<br>-6 to 0 | V<br>V                           |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> $\leq$ V <sub>CC</sub><br>V <sub>I</sub> $\geq$ V <sub>EE</sub> | 6 to 0<br>-6 to 0 | V<br>V                           |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100         | mA<br>mA                         |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |  |  | $\pm$ 0.5         | mA                               |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | -40 to +85        | $^{\circ}$ C                     |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | -65 to +150       | $^{\circ}$ C                     |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | SOIC-8<br>SOIC-8   | 190<br>130        | $^{\circ}$ C/W<br>$^{\circ}$ C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SOIC-8   | 41 to 44 $\pm$ 5% | $^{\circ}$ C/W                   |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | TSSOP-8<br>TSSOP-8   | 185<br>140        | $^{\circ}$ C/W<br>$^{\circ}$ C/W |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8  | 41 to 44 $\pm$ 5% | $^{\circ}$ C/W                   |
| $\theta_{JA}$    | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | DFN8<br>DFN8   | 129<br>84         | $^{\circ}$ C/W<br>$^{\circ}$ C/W |
| T <sub>sol</sub> | Wave Solder  | Pb<br>Pb-Free                                  | <2 to 3 sec @ 248 $^{\circ}$ C<br><2 to 3 sec @ 260 $^{\circ}$ C               | 265<br>265        | $^{\circ}$ C                     |
| $\theta_{JC}$    | Thermal Resistance (Junction-to-Case)              | (Note 1)                                       | DFN8   | 35 to 40          | $^{\circ}$ C/W                   |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board - 2S2P (2 signal, 2 power)

# MC100LEVEL32

**Table 3. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 1)

| Symbol      | Characteristic  | -40°C                   |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---|-------------------------|------|------|------|------|------|------|------|------|---------------|
|             |   | Min                     | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current  |                         | 29   | 35   |      | 29   | 35   |      | 31   | 36   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)  | 2215                    | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)   | 1470                    | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2135                    |      | 2420 | 2135 |      | 2420 | 2135 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1490                    |      | 1825 | 1490 |      | 1825 | 1490 |      | 1825 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1.92                    |      | 2.04 | 1.92 |      | 2.04 | 1.92 |      | 2.04 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | 1.2                     |      | 3.1  | 1.1  |      | 3.1  | 1.1  |      | 3.1  | V             |
|             |   | 1.4                     |      | 3.1  | 1.3  |      | 3.1  | 1.3  |      | 3.1  | V             |
| $I_{IH}$    | Input HIGH Current  |                         |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | CLK                     | 0.5  |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |
|             |   | $\overline{\text{CLK}}$ | -600 |      | -600 |      |      | -600 |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 4. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 5)

| Symbol      | Characteristic  | -40°C                   |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|---|-------------------------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |   | Min                     | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current  |                         | 29    | 35    |       | 29    | 35    |       | 31    | 36    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 6)  | -1085                   | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 6)   | -1830                   | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1165                   |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1810                   |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1.38                   |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)<br>$V_{PP} < 500\text{ mV}$<br>$V_{PP} \geq 500\text{ mV}$ | -2.1                    |       | -0.2  | -2.1  |       | -0.2  | -2.1  |       | -0.2  | V             |
|             |   | -1.9                    |       | -0.2  | -1.9  |       | -0.2  | -1.9  |       | -0.2  | V             |
| $I_{IH}$    | Input HIGH Current  |                         |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | CLK                     | 0.5   |       | 0.5   |       |       | 0.5   |       |       | $\mu\text{A}$ |
|             |   | $\overline{\text{CLK}}$ | -600  |       | -600  |       |       | -600  |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

# MC100LVEL32

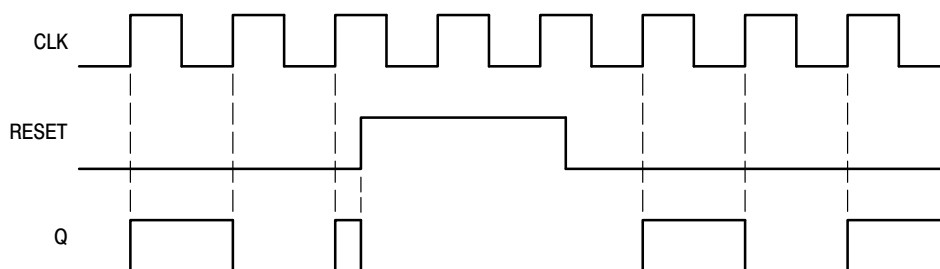
**Table 5. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 8)

| Symbol                               | Characteristic   | -40°C             |                   |                   | 25°C              |                   |                   | 85°C              |                   |                   | Unit |
|--------------------------------------|--|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------|
|                                      |  | Min               | Typ               | Max               | Min               | Typ               | Max               | Min               | Typ               | Max               |      |
| $f_{\max}$                           | Maximum Toggle Frequency   | 2.2               | 2.5               |                   | 2.4               | 2.6               |                   | 2.6               | 2.8               |                   | GHz  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay CLK to Q (Differential)<br>CLK to Q (Single-Ended)<br>Reset to Q | 350<br>300<br>440 | 500<br>500<br>555 | 530<br>580<br>640 | 370<br>320<br>450 | 510<br>510<br>540 | 550<br>600<br>650 | 410<br>360<br>480 | 540<br>540<br>580 | 590<br>640<br>680 | ps   |
| $t_{\text{RR}}$                      | Reset Recovery   | 175               | 50                |                   | 175               | 50                |                   | 175               | 50                |                   | ps   |
| $t_{\text{PW}}$                      | Minimum Pulse Width Reset  | 500               | 300               |                   | 500               | 300               |                   | 500               | 300               |                   | ps   |
| $t_{\text{JITTER}}$                  | Random Clock Jitter (RMS)  |                   | 2.0               |                   |                   | 2.0               |                   |                   | 2.0               |                   | ps   |
| $V_{\text{PP}}$                      | Input Swing (Differential Swing) (Note 9)  | 150               |                   | 1000              | 150               |                   | 1000              | 150               |                   | 1000              | mV   |
| $t_r$<br>$t_f$                       | Output Rise/Fall Times Q<br>(20% – 80%)  | 120               | 225               | 320               | 120               | 225               | 320               | 120               | 225               | 320               | ps   |

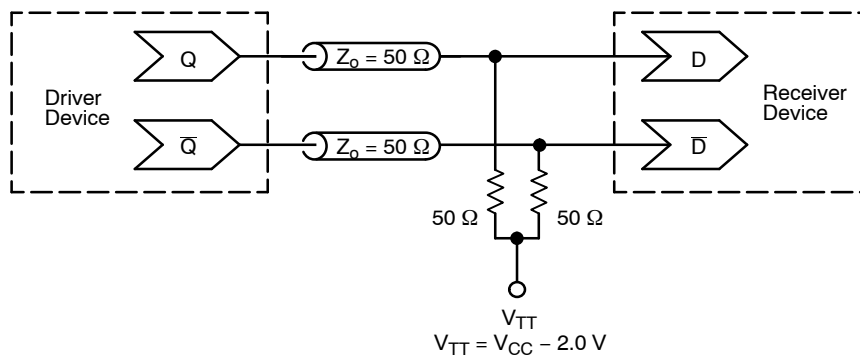
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

9.  $V_{\text{PP}}(\text{min})$  is input swing measured single-ended on each input in differential configuration.



**Figure 1. Timing Diagram**



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

## MC100LVEL32

### ORDERING INFORMATION

| Device           | Package              | Package†           |
|------------------|----------------------|--------------------|
| MC100LVEL32D     | SOIC-8               | 98 Units / Rail    |
| MC100LVEL32DG    | SOIC-8<br>(Pb-Free)  | 98 Units / Rail    |
| MC100LVEL32DR2   | SOIC-8               | 2500 / Tape & Reel |
| MC100LVEL32DR2G  | SOIC-8<br>(Pb-Free)  | 2500 / Tape & Reel |
| MC100LVEL32DT    | TSSOP-8              | 100 Units / Rail   |
| MC100LVEL32DTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail   |
| MC100LVEL32DTR2  | TSSOP-8              | 2500 / Tape & Reel |
| MC100LVEL32DTR2G | TSSOP-8<br>(Pb-Free) | 2500 / Tape & Reel |
| MC100LVEL32MNR4  | DFN8                 | 1000 / Tape & Reel |
| MC100LVEL32MNR4G | DFN8<br>(Pb-Free)    | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

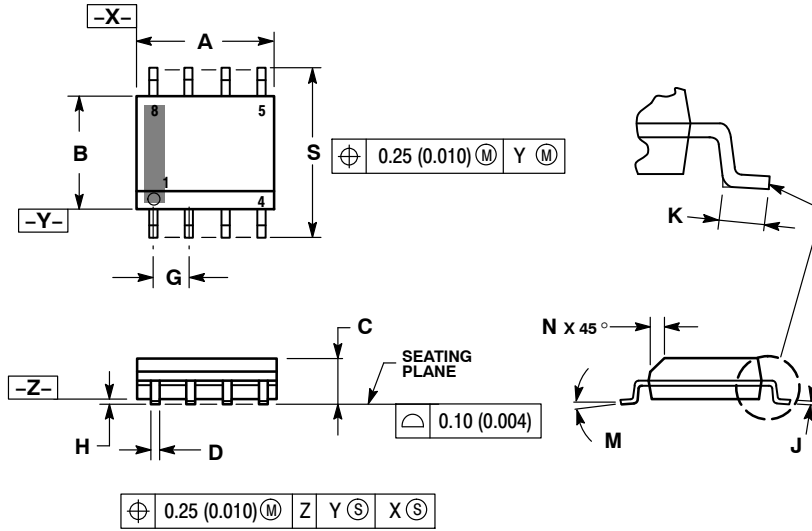
#### Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS I/O SPiCE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

# MC100LEVEL32

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

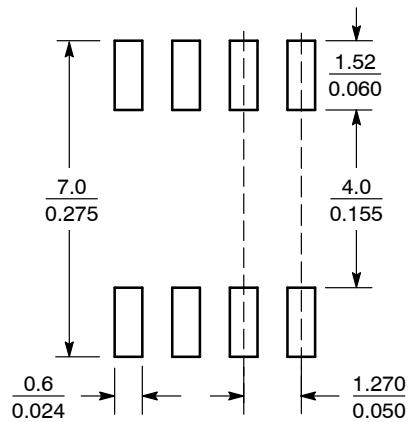


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0°          | 8°   | 0°        | 8°    |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



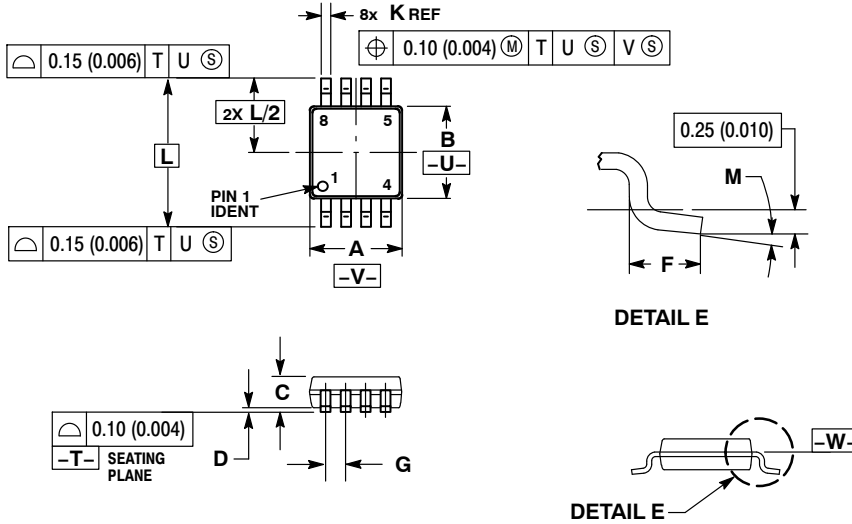
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100LVEL32

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

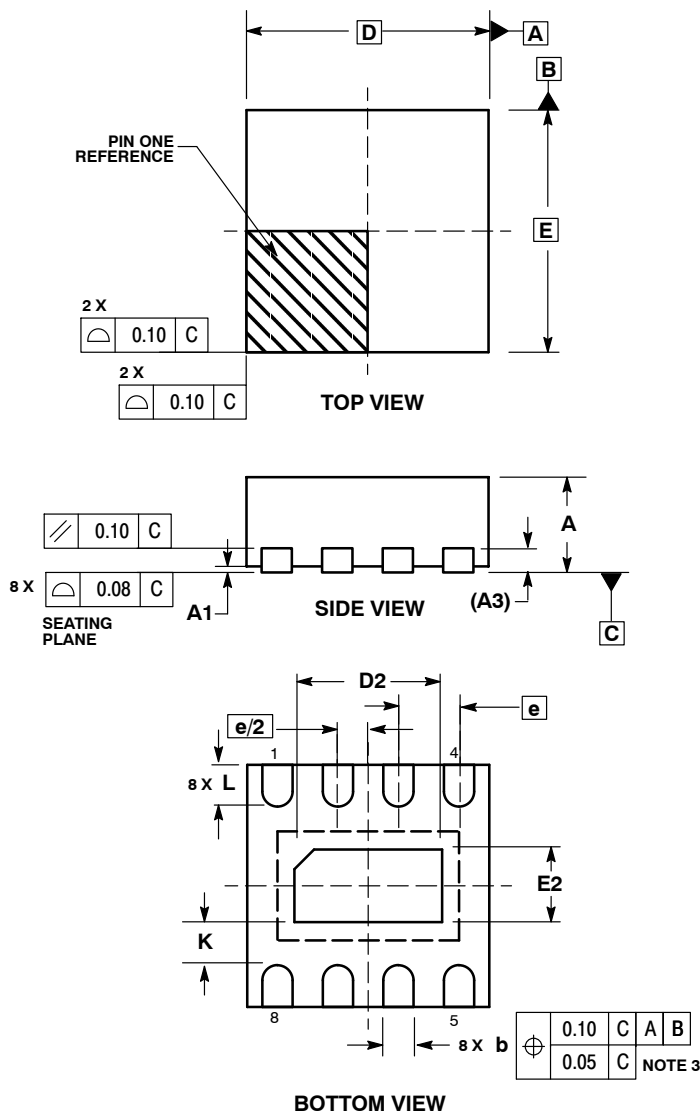
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |

# MC100LVEL32

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.80        | 1.00 |
| A1  | 0.00        | 0.05 |
| A3  | 0.20 REF    |      |
| b   | 0.20        | 0.30 |
| D   | 2.00 BSC    |      |
| D2  | 1.10        | 1.30 |
| E   | 2.00 BSC    |      |
| E2  | 0.70        | 0.90 |
| e   | 0.50 BSC    |      |
| K   | 0.20        | ---  |
| L   | 0.25        | 0.35 |

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