



The Future of Analog IC Technology®

MP5010B

3V-18V, 1A-5A Programmable-Current-Limit Switch with Over-Voltage Clamp

DESCRIPTION

The MP5010B is a protection device designed to protect circuitry on the output (source) from transients on the input (V_{CC}). It also protects the input from undesired shorts and transients coming from the source.

A small capacitor on the dv/dt pin controls the slew rate that limit the inrush current at the source. For instance, a 1nF capacitor results in a source ramp-up time of 3ms.

The maximum load at the source is current limited using a sense FET topology. An external resistor between the I-Limit pin and the Source pins controls the magnitude of the current limit.

An internal charge pump drives the gate of the power device, allowing the DMOS power FET to have a very low ON-resistance of just 40mΩ.

The MP5010B also protects the source from the input being too low or too high. Under-voltage lockout ensures that the input remains above the minimum operating threshold before the power device turns on. If the input rises above the high output threshold, the MP5010B limits the source voltage.

FEATURES

- Wide 3V-to-18V Operating Input Range
- 5.7V Output Over-Voltage Clamp
- Integrated 40mΩ Power FET
- Enable/Fault Pin
- Adjustable Output Voltage Slew Rate
- Adjustable Current Limit
- Thermal Protection

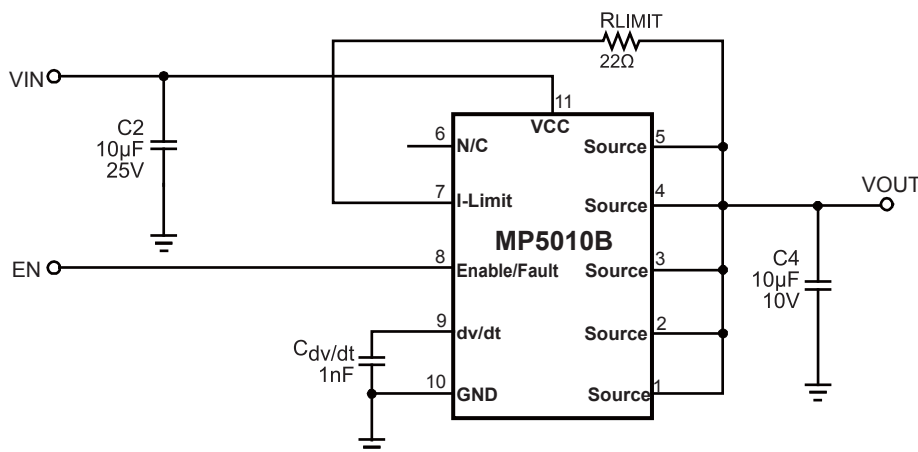
APPLICATIONS

- Hot-Swappable Devices
- Wireless Modem Data Cards
- PC Cards
- Laptops

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

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TYPICAL APPLICATION



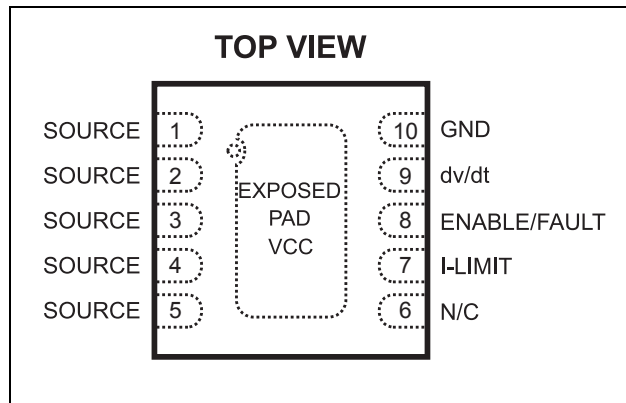
ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|--------------|-----------------|-------------|
| MP5010BDQ | QFN10 (3mm×3mm) | AFN |

* For Tape & Reel, add suffix –Z (e.g. MP5010BDQ–Z).

For RoHS compliant packaging, add suffix –LF (e.g. MP5010BDQ-LF-Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V_{CC}, SOURCE, I-LIMIT –0.3V to 22V
 dv/dt, ENABLE/FAULT –0.3V to 6V
 Storage Temperature –65°C to +155°C
 Junction Temperature +150°C
 Lead Temperature +260°C
 Continuous Power Dissipation (T_A=+25°C) ⁽²⁾
 2.5W

Recommended Operating Conditions ⁽³⁾

Input Voltage Operating Range 3V to 18V
 Operating Junction Temp. (T_J) –40°C to +125°C

Thermal Resistance ⁽⁴⁾ **θ_{JA}** **θ_{JC}**
 QFN10 (3mm×3mm) 50 12... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Reduce 0.2 Watts for every 10°C ambient temperature increasing
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V$, $R_{LIMIT} = 22\Omega$, Capacitive Load = $10\mu F$, $T_A = 25^\circ C$, unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|--------------|--|------|------|----------|------------|
| Power FET | | | | | | |
| Delay Time | τ_{DLY} | Enabling of chip to $I_D = 40mA$ with a 5Ω resistive load | | 44 | | μs |
| ON Resistance | R_{DSon} | $T_J = 25^\circ C$ | | 40 | 55 | m Ω |
| | | $T_J = 85^\circ C^{(5)}$ | | 52 | | |
| OFF-State Output Voltage | V_{OFF} | $V_{CC} = 18V$, $V_{EN} = 0V$, $R_L = 500\Omega$ | | | 120 | mV |
| Continuous Current | I_D | 0.5 in^2 pad, $T_A = 25^\circ C$ | | 4.2 | | A |
| | | minimum copper, $T_A = 80^\circ C$ | | 2.3 | | |
| Thermal Latch | | | | | | |
| Shutdown Temperature ⁽⁵⁾ | T_{SD} | | | 175 | | $^\circ C$ |
| Under/Over-Voltage Protection | | | | | | |
| Output Clamp Voltage | V_{CLAMP} | Over-Voltage Protection $V_{CC} = 8V$ | 5.5 | 5.7 | 5.9 | V |
| Under-Voltage Lockout | V_{UVLO} | Rising Edge | 2.65 | 2.8 | 2.9 | V |
| Under-Voltage Lockout (UVLO) Hysteresis | V_{HYST} | | | 0.15 | | V |
| Current Limit⁽⁶⁾ (For Direct Current-Sense, refer to typical application in Figure 5) | | | | | | |
| Hold Current | I_{LIM-SS} | 0Ω Short Resistance, $R_{LIM} = 22\Omega$ | 2.2 | 2.8 | 3.4 | A |
| Trip Current | I_{LIM-OL} | $R_{LIM} = 22\Omega$ | | 4.3 | | A |
| Current Limit⁽⁶⁾ (For Kelvin Sense, refer to typical application in Figure 4) | | | | | | |
| Hold Current | I_{LIM-SS} | 0Ω Short Resistance, $R_{LIM} = 22\Omega$ | 0.77 | 1.10 | 1.43 | A |
| Trip Current | I_{LIM-OL} | $R_{LIM} = 22\Omega$ | | 2.18 | | A |
| dv/dt Circuit | | | | | | |
| Rise Time ⁽⁷⁾ | τ_r | $C_{dv/dt} = 1nF$ | 2 | 3 | 4 | ms |
| Enable/Fault | | | | | | |
| Low-Level Input Voltage | V_{IL} | Output Disabled | | | 0.5 | V |
| Intermediate-Level Input Voltage | $V_{I(INT)}$ | Thermal Fault, Output Disabled | 0.82 | 1.4 | 1.95 | V |
| High-Level Input Voltage | V_{IH} | Output Enabled | 2.5 | | | V |
| HIGH-State Maximum Voltage | $V_{I(MAX)}$ | | | 4.95 | | V |
| Pull-Up Current (Source) | I_{IL} | $V_{ENABLE} = 0V$ | 15 | 25 | 35 | μA |
| Maximum Fanout for Fault Signal | | Maximum number of chips for simultaneous shutdown | | | 3 | Units |
| Maximum Voltage on EN ⁽⁸⁾ | V_{MAX} | | | | V_{CC} | V |

ELECTRICAL CHARACTERISTICS (continued)
 $V_{CC} = 5V$, $R_{LIMIT}=22\Omega$, Capacitive Load= $10\mu F$, $T_A=25^\circ C$, unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|------------------------------------|------------|--------------------|-----|-----|-----|---------|
| Total Device | | | | | | |
| Bias Current | I_{BIAS} | Device Operational | | 860 | 950 | μA |
| | | Thermal Shutdown | | 580 | 650 | |
| Minimum Operating Voltage for UVLO | V_{MIN} | Enable<0.5V | | | 2.5 | V |

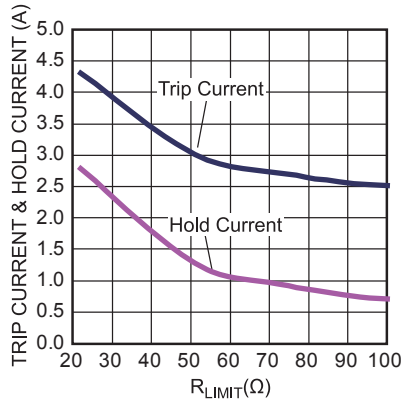
Notes:

- 5) Guaranteed by design.
- 6) Guaranteed by Characterization Test.
- 7) Measured from 10% to 90%.
- 8) Maximum Input Voltage on Enable pin to be $\leq 6V$ if $V_{CC} \geq 6V$. Maximum Input Voltage on Enable pin to be V_{CC} if $V_{CC} \leq 6V$.

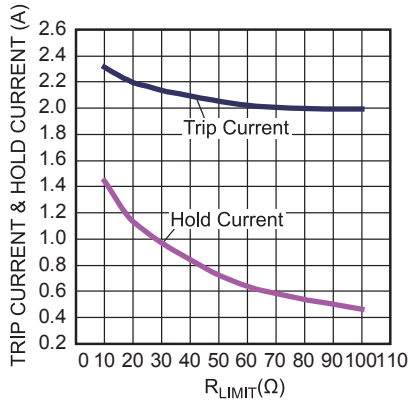
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$, $V_{EN}=5V$, $R_{LIMIT}=22\Omega$, $C_{OUT}=10\mu F$, $C_{dv/dt} = 1nF$, $T_A=25^\circ C$, unless otherwise noted.

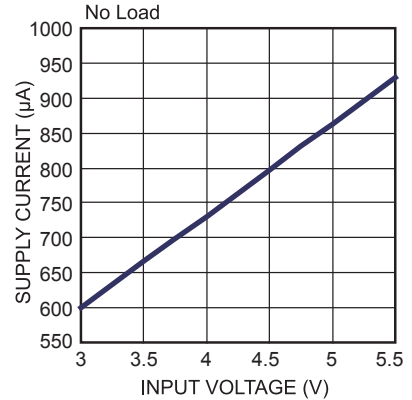
Trip Current & Hold Current vs. R_{LIMIT}
Direct Connection, $V_{IN}=5V$



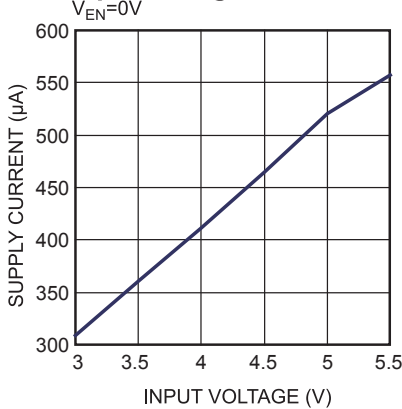
Trip Current & Hold Current vs. R_{LIMIT}
Kelvin Connection, $V_{IN}=5V$



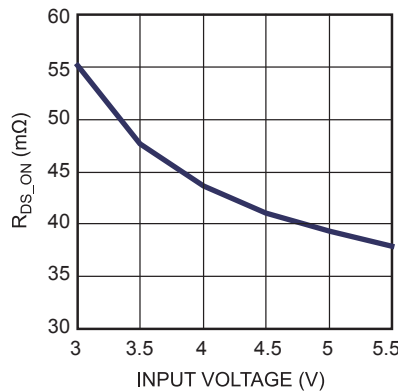
Supply Current, Output Enabled vs. Input Voltage
No Load



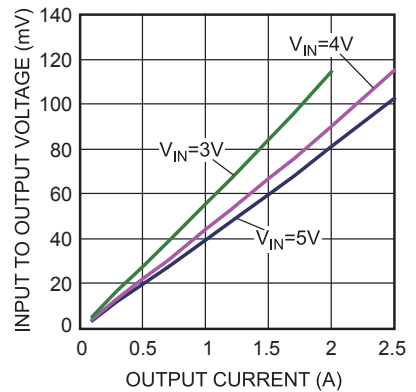
Supply Current, Output Disabled vs. Input Voltage
 $V_{EN}=0V$



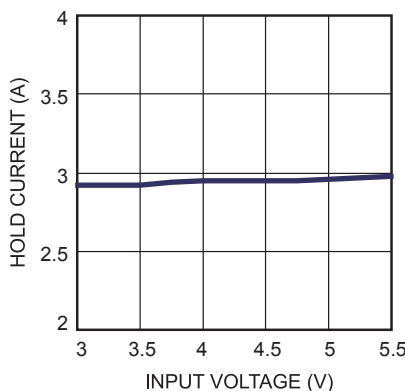
R_{DS_ON} vs. Input Voltage
 $I_{OUT}=0.5A$



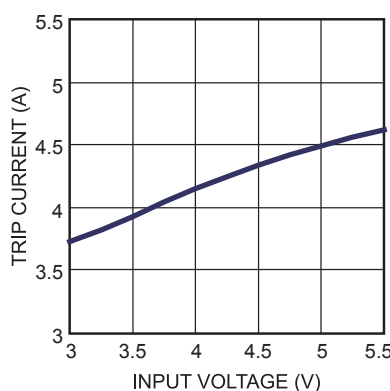
Input to Output Voltage vs. Load Current



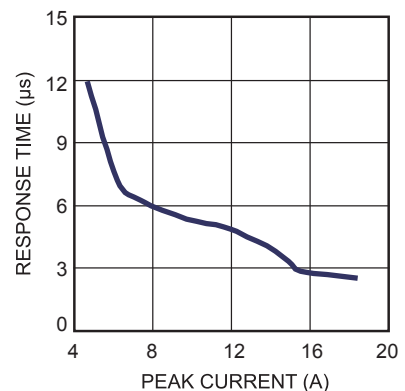
Hold Current vs. Input Voltage



Trip Current vs. Input Voltage



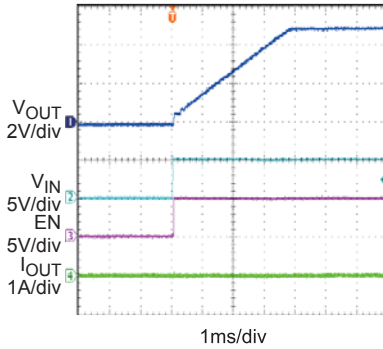
Current Limit Response vs. Peak Current

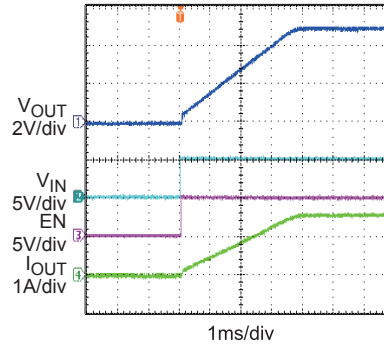


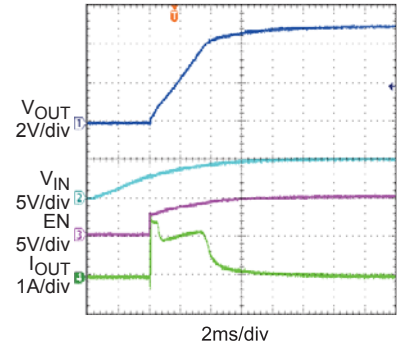
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 5V$, $V_{EN}=5V$, $R_{LIMIT}=22\Omega$, $C_{OUT}=10\mu F$, $C_{dv/dt} = 1nF$, $T_A=25^\circ C$, unless otherwise noted.

Startup through Input Voltage

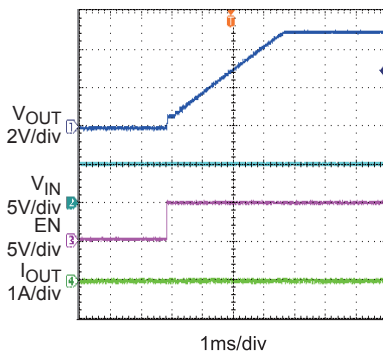
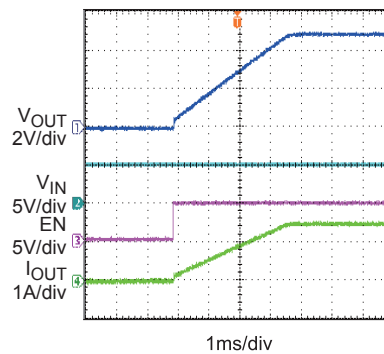
En Float, no load

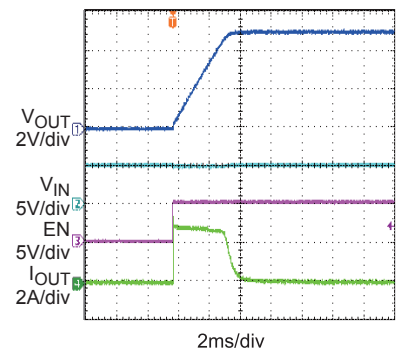

Startup through Input Voltage

 En Float, $R_{LOAD} = 3.3\Omega$

Startup through Input Voltage

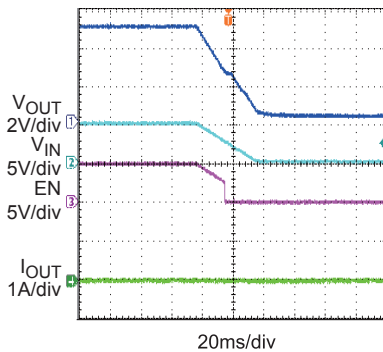
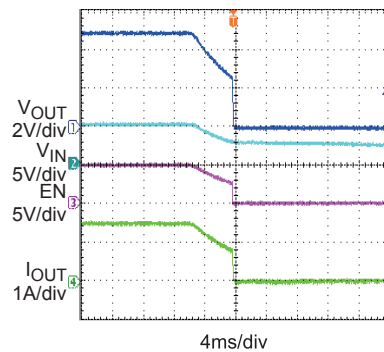
 En Float, No Load, $C_{OUT} = 2200\mu F$

Startup through Enable

No Load

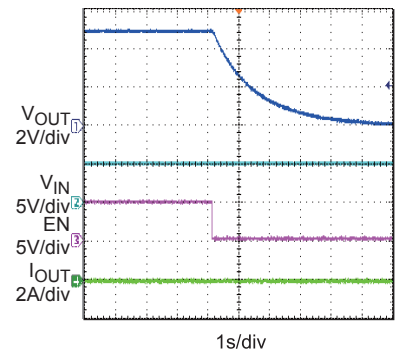

Startup through Enable
 $R_{LOAD} = 3.3\Omega$

Startup through Enable

 No Load, $C_{OUT} = 2200\mu F$

Shutdown through Input Voltage

No Load


Shutdown through Input Voltage
 $R_{LOAD} = 3.3\Omega$

Shutdown through Enable

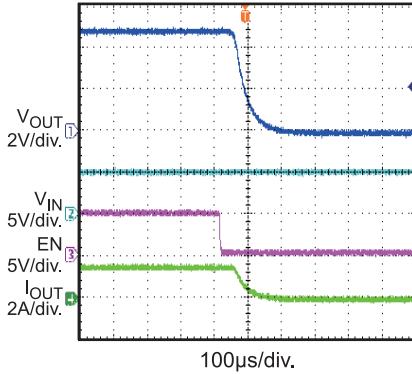
No Load



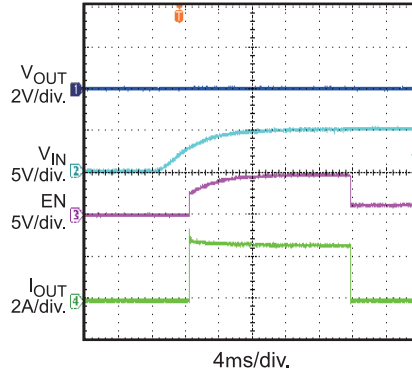
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 5V$, $V_{EN}=5V$, $R_{LIMIT}=22\Omega$, $C_{OUT}=10\mu F$, $C_{dv/dt} = 1nF$, $T_A=25^\circ C$, unless otherwise noted.

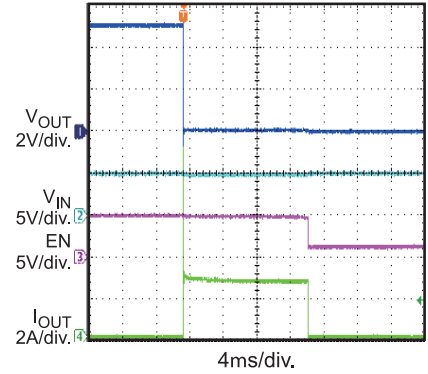
Shutdown Through Enable
 $R_{LOAD} = 3.3\Omega$



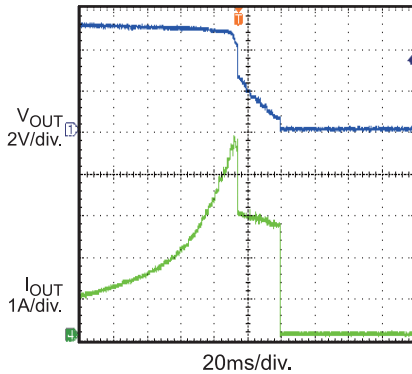
Short Circuit before Input Voltage Startup, and Thermal Shutdown



Short Circuit during Normal Operation, and Thermal Shutdown

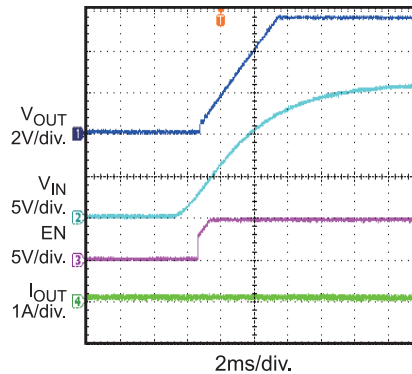


Current Limit



Start Up into OVP, no load EN float

$V_{IN} = 16V$



PIN FUNCTIONS

| Pin # | Name | Description |
|-------------------|-----------------|---|
| 1-5 | SOURCE | Source. Internal power FET source. IC output. |
| 6 | N/C | DO NOT CONNECT—leave floating. |
| 7 | I-Limit | Current Limit. Using a resistor between this pin and Source to set the overload and short-circuit current-limit levels. |
| 8 | Enable/Fault | Enable/Fault. A tri-state, bi-directional interface. Leave floating to enable the output. Pull to ground (using an open drain or open collector device) to disable the output. If a thermal fault occurs, this voltage enters an intermediate state to signal that the device is in thermal shutdown. |
| 9 | dv/dt | Slew Rate. The internal dv/dt circuit controls the slew rate of the output voltage at turn-on. |
| 10 | GND | Ground. Internal IC reference. |
| 11 Exposed Pad | V _{CC} | Input. Positive input voltage. |

BLOCK DIAGRAM

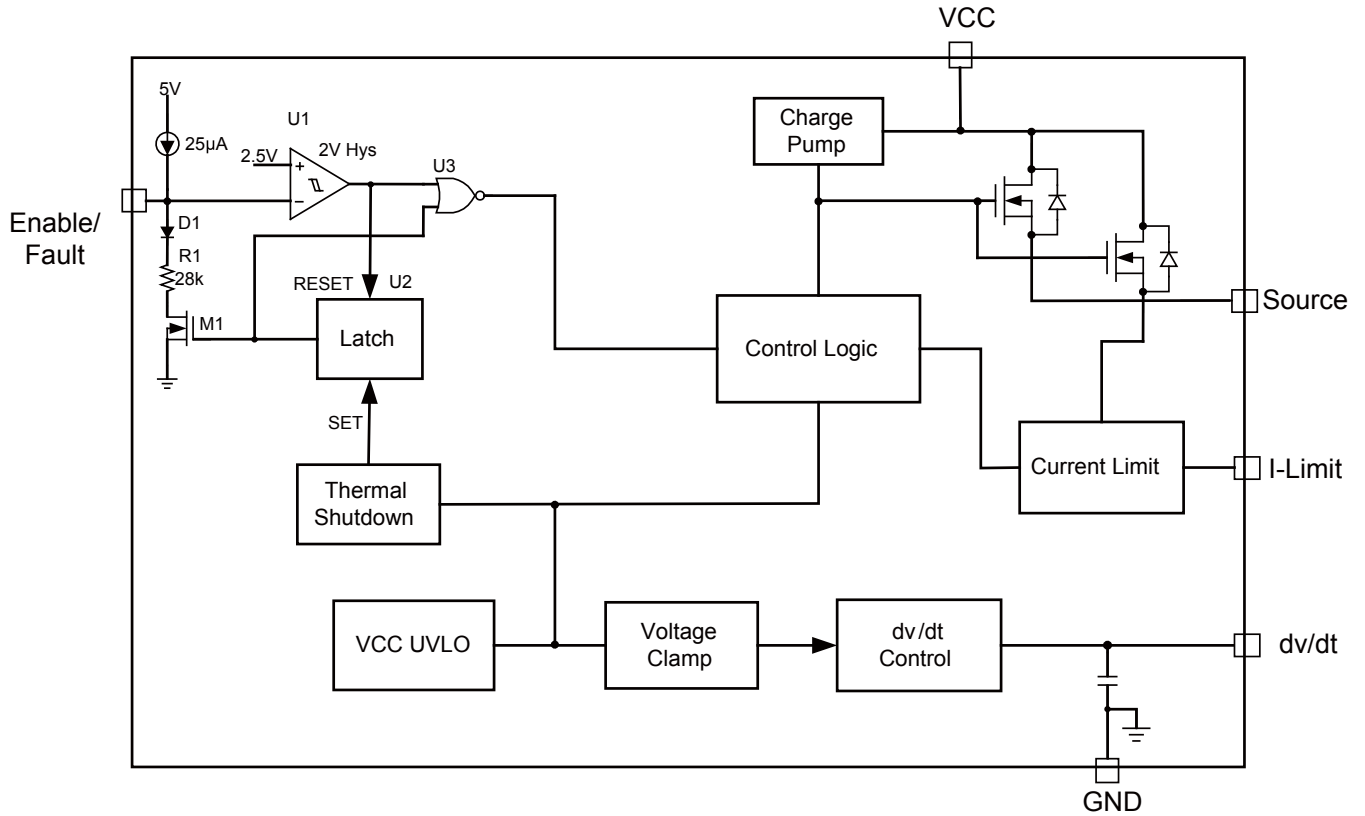


Figure 1: Functional Block Diagram

OPERATION

The MP5010B limits the inrush current to the load when a circuit card connects to a live backplane power source, thereby limiting the backplane's voltage drop and the dV/dt of the voltage to the load. It offers an integrated solution to monitor the input voltage, output voltage, output current, and die temperature, eliminating the external current-sense power resistor, power MOSFET, and thermal sensor.

Under-Voltage Lockout Operation

If the supply (input) is below the UVLO threshold, the output is disabled, and the EN/Fault line is driven low.

When the supply rises above the UVLO threshold, the output is enabled and the EN/Fault is pulled high through a $25\mu\text{A}$ current source without an external pull-up resistor. The pull-up voltage is limited to 4.95V.

Output Over-Voltage Protection

If the input voltage exceeds the over-voltage protection (OVP) threshold, the output is clamped at 5.7V (typ).

Current Limiting

When the chip is active, if load reaches the over-current protection (OCP) threshold (trip current) or a short is present, the part switches to constant-current mode (hold current). The chip shuts down only if the over-current condition eventually triggers thermal protection. However, when the part is powered up by V_{CC} or EN, the load current should be smaller than the hold current. Otherwise, the part can't be fully turned on.

In a typical application with a current-limiting resistor of 22Ω , the trip current is 2.18A for Kelvin current sensing and 4.3A for direct current sensing. If the device is in normal operation and passing 2.0A, it will only need to dissipate 160mW with the low ON resistance of $40\text{m}\Omega$. For a package dissipation of 50°C/Watt , the temperature rise is $+8^\circ\text{C}$. Given a 25°C ambient temperature, the typical package temperature is 33°C .

The MP5010B requires a heat sink during constant-current mode (such as from a short-circuit) to prevent unwanted shutdown: In constant-current mode, the chip must dissipate the power from a 5V drop. Without additional heat dissipation at 50°C/Watt , the temperature would exceed the thermal threshold ($+175^\circ\text{C}$) and the MP5010B will shutdown to force the temperature to drop below a hysteresis level. Without a heat sink, maintain the current below 600mA at $+25^\circ\text{C}$ and below 360mA at $+85^\circ\text{C}$ to prevent thermal shutdown.

Thermal Protection

If the temperature exceeds the thermal threshold, the MP5010B disables its output and drives the Enable/Fault line to the middle (MID) level (read the following Enable/Fault Pin section for more information). The thermal fault condition is latched, and the part remains OFF until the Enable/Fault line goes low. Cycling the power below the UVLO threshold will also reset the fault flag.

Fault and Enable Pin

The Enable/Fault pin is a bi-directional, three-level I/O with a weak pull-up current ($25\mu\text{A}$, typ.). The three levels are LOW, MID, and HIGH. It functions to enable/disable the part and to relay fault information.

Enable/Fault as an input:

1. LOW and MID disable the part.
2. LOW, in addition to disabling the part, clears the fault flag.
3. HIGH enables the part (if the fault flag is clear).

Enable/Fault as an output:

1. The pull-up current will allow a "wired nor" pull-up to enable the part (if not overridden).
2. An under-voltage condition will cause a LOW on the Enable/Fault pin, and will clear the fault flag.
3. A thermal fault will set a MID on the Enable/Fault pin, and will set the fault flag

The Enable/Fault line must remain above the MID level for the output to turn ON.

The fault flag is an internal flip-flop that can be set or reset under the following conditions:

1. Thermal Shutdown: set fault flag
2. Under-Voltage: reset fault flag
3. LOW on Enable/Fault pin: reset fault flag
4. MID on Enable/Fault pin: no effect

Given a fault, the Enable/Fault pin is driven to MID.

There are 4 types of faults, and each fault has a direct and indirect effect on the Enable/Fault pin and the internal fault flag. In a typical application there are one or more of the MP5010B chips in a system. The Enable/Fault lines are typically be connected together.

Table 1—Fault Function Influence in Application

| Fault description | Internal action | Effect on Fault Pin | Effect on Flag | Effect on secondary Part |
|--------------------------|--|---|-----------------------|---|
| Short/Over Current | Limit current | none | none | none |
| Under Voltage | Output turns OFF | Internally drives Enable/Fault pin to logic LOW | Flag is reset | Disables secondary output, and resets fault flag. |
| Over Voltage | Limit output voltage | None | None | None |
| Thermal Shutdown | Shutdown. The part is latched OFF until a UVLO or externally driven to ground. | Internally drives Enable/Fault pin to MID | Flag is Set | Disables secondary part output. |

APPLICATION INFORMATION

Current Limit

The current limit is a function of the external current-limit resistor. Table 2 and Table 3 list examples of current values as a function of the resistor value for both Kelvin current sensing and direct current sensing.

Rise Time

The rise time is a function of the capacitor ($C_{dv/dt}$) on the dv/dt pin. Table 4 lists typical rise times as a function of capacitance.

Table 2: Current Limit vs. Current Limit Resistor ($V_{CC}=5V$, Kelvin Current Sensing)

| | | | | | |
|--------------------------|------|------|------|------|------|
| R_{LIMIT} (Ω) | 10 | 22 | 51 | 75 | 100 |
| Trip Current (A) | 2.31 | 2.18 | 2.05 | 2.00 | 1.99 |
| Hold Current (A) | 1.45 | 1.10 | 0.71 | 0.56 | 0.47 |

Table 3: Current Limit vs. Current Limit Resistor ($V_{CC}=5V$, Direct Current Sensing)

| | | | | | |
|--------------------------|------|------|------|------|------|
| R_{LIMIT} (Ω) | 22 | 51 | 75 | 100 | 220 |
| Trip Current (A) | 4.31 | 3.10 | 2.69 | 2.52 | 2.31 |
| Hold Current (A) | 2.79 | 1.29 | 0.91 | 0.78 | 0.40 |

Table 4: Rise Time vs. $C_{dv/dt}$

| | | | | |
|----------------------|-------|-----|-------|-------|
| $C_{dv/dt}$ | 330pF | 1nF | 3.3nF | 6.8nF |
| Rise Time (typ., ms) | 1.1 | 3 | 9.4 | 19.2 |

* Notes: Rise Time = $K_{RT} \cdot (50pF + C_{dv/dt})$, $K_{RT} = 2.8E6$

The “rise time” is measured by from 10% to 90% of output voltage.

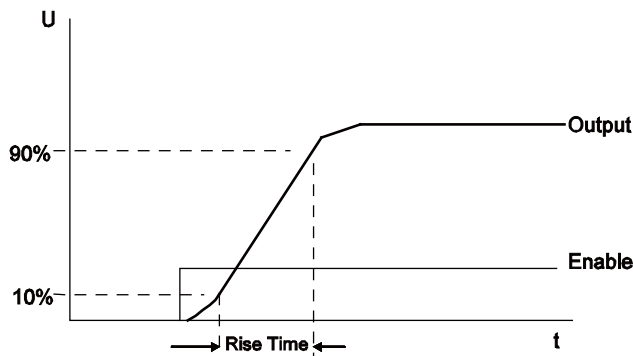


Figure 2—Rise Time

PCB Layout

PCB layout is very important to achieve stable operation. Please follow these guidelines and use Figure 3 as reference.

- Place R_{LIMIT} close to the I-limit pin
- Place $C_{dv/dt}$ close to dv/dt pin
- Place the input capacitor close to the V_{CC} pin.
- Leave the N/C pin floating.
- Place vias in the thermal pad and provide enough copper area near the V_{CC} pin and Source pin for thermal dissipation.

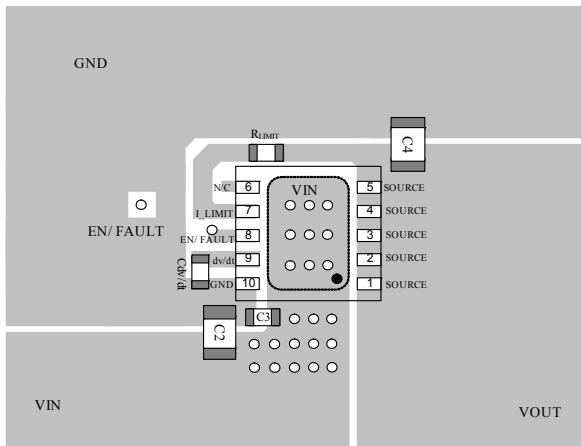
Design Example

Below is a direct-current-sensing design example following the application guidelines for the given specifications:

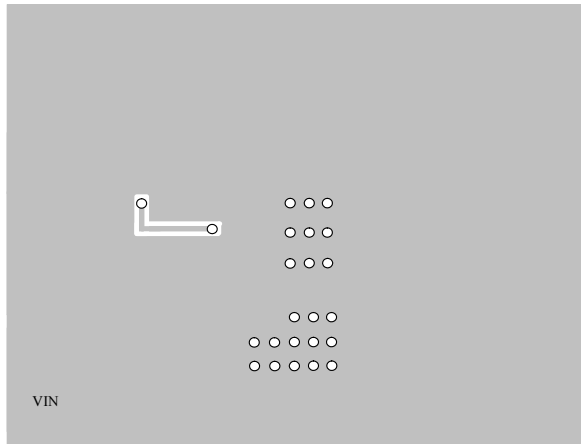
Table 5: Design Example

| | |
|--------------|------|
| V_{IN} | 5V |
| Trip Current | 4.3A |
| Hold Current | 2.8A |

Figure 5 shows the application schematic. The Typical Performance Characteristics section shows the circuit waveforms. For more device applications, please refer to the related Evaluation Board Datasheet.

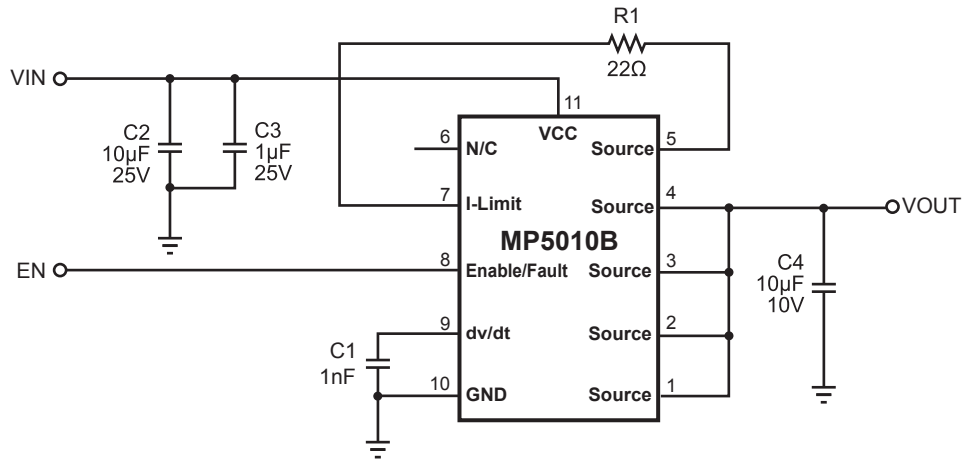
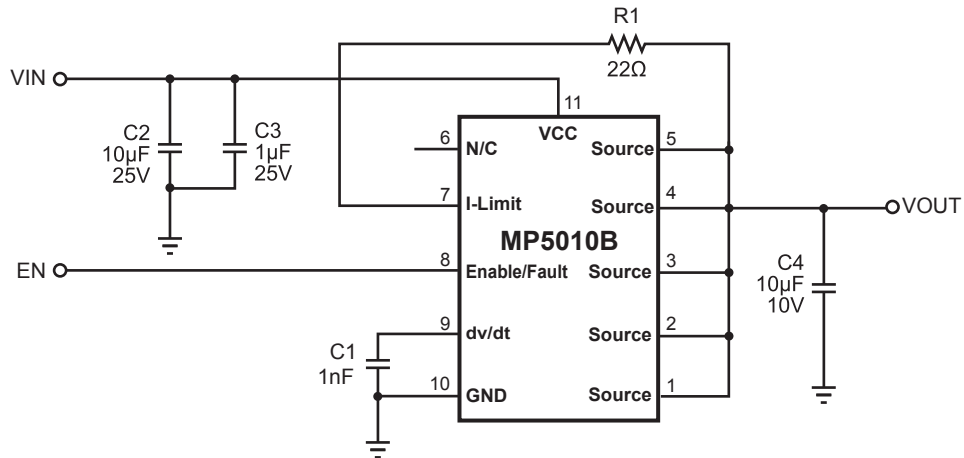


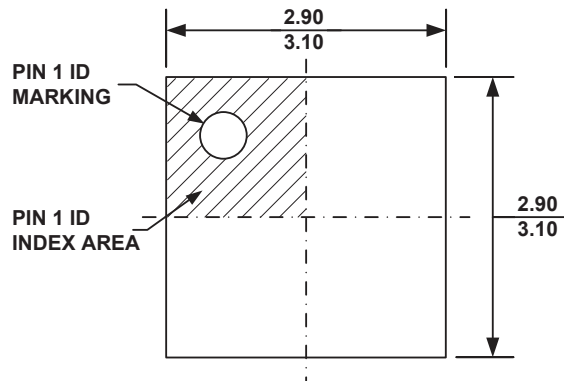
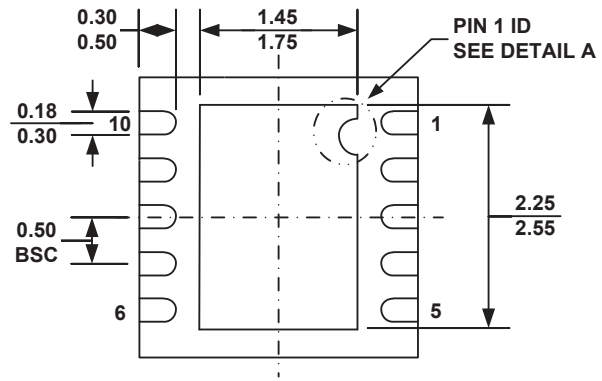
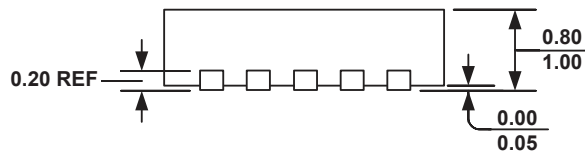
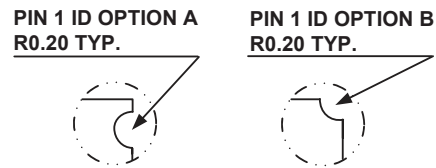
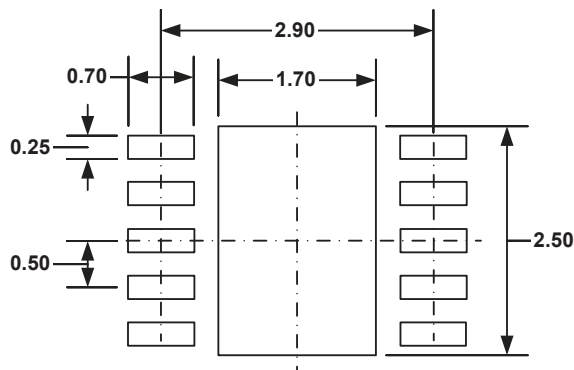
Top Layer



Bottom Layer

Figure 3: PCB Layout

TYPICAL APPLICATION CIRCUITS

Figure 4: Typical Application Schematic with Kelvin Current Sensing

Figure 5: Typical Application Schematic with Direct Current Sensing

PACKAGE INFORMATION
QFN10 (3mm × 3mm)

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

RECOMMENDED LAND PATTERN
NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
- 5) DRAWING IS NOT TO SCALE.

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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