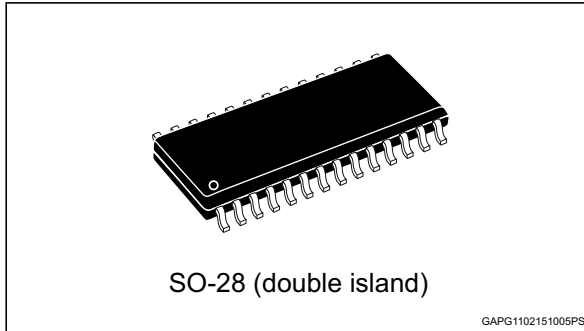


Quad channel high-side driver

Datasheet - production data



- Undervoltage shutdown
- Overvoltage clamp
- Output stuck to V_{CC} detection
- Load current limitation
- Reverse battery protection
- Electrostatic discharge protection

Description

The VNQ830P-E is a quad HSD formed by assembling two VND830P-E chips in the same SO-28 package. The VND830P-E is a monolithic device made using STMicroelectronics™ VIPower™ M0-3 technology. The VNQ830P-E is intended for driving any type of multiple load with one side connected to ground.

The active V_{CC} pin voltage clamp protects the device against low energy spikes. Active current limitation combined with thermal shutdown and automatic restart protects the device against over-load. The device detects the open-load condition in both the on and off-state.

In the off-state the device detects if the output is shorted to V_{CC} . The device automatically turns off in the case where the ground pin becomes disconnected.

Features

Type	$R_{DS(on)}$	I_{OUT}	V_{CC}
VNQ830P-E	65 m Ω ⁽¹⁾	6 A	36V

1. Per each channel.

- ECOPACK®: lead free and RoHS compliant
- Automotive Grade: compliance with AEC guidelines
- Very low standby current
- CMOS compatible input
- On-state open-load detection
- Off-state open-load detection
- Thermal shutdown protection and diagnosis

Table 1. Device summary

Package	Order codes	
	Tube	Tape and reel
SO-28	VNQ830P-E	VNQ830PTR-E

Contents

1	Block diagram and pin description	5
2	Electrical specifications	7
2.1	Absolute maximum ratings	7
2.2	Thermal data	8
2.3	Electrical characteristics	8
2.4	Electrical characteristics curves	14
3	Application information	17
3.1	GND protection network against reverse battery	17
3.1.1	Solution 1: a resistor in the ground line (RGND only)	17
3.1.2	Solution 2: a diode (D_{GND}) in the ground line	18
3.2	Load dump protection	18
3.3	MCU I/O protection	18
3.4	Open-load detection in off-state	19
3.5	Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)	20
4	Package and PCB thermal data	21
4.1	SO-28 thermal data	21
5	Package information	24
5.1	SO-28 package information	24
5.2	SO-28 packing information	26
6	Revision history	27

List of tables

Table 1.	Device summary	1
Table 2.	Suggested connections for unused and not connected pins	6
Table 3.	Absolute maximum ratings	7
Table 4.	Thermal data (per island)	8
Table 5.	Power	8
Table 6.	Protections	9
Table 7.	V _{CC} - output diode	9
Table 8.	Switching (V _{CC} = 13V; T _j = 25°C)	10
Table 9.	Logic inputs.	10
Table 10.	Status pin	10
Table 11.	Open-load detection	11
Table 12.	Truth table.	12
Table 13.	Electrical transient requirements.	12
Table 14.	Thermal calculation according to the PCB heatsink area	21
Table 15.	Thermal parameters	23
Table 16.	SO-28 mechanical data	24
Table 17.	Document revision history.	27

List of figures

Figure 1.	Block diagram	5
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current and voltage conventions	8
Figure 4.	Status timings	11
Figure 5.	Switching characteristics	11
Figure 6.	Waveforms	13
Figure 7.	Off-state output current	14
Figure 8.	High level input current	14
Figure 9.	Input clamp voltage	14
Figure 10.	Turn-on voltage slope	14
Figure 11.	Overshoot shutdown	14
Figure 12.	Turn-off voltage slope	14
Figure 13.	I_{LIM} vs T_{case}	15
Figure 14.	On-state resistance vs V_{CC}	15
Figure 15.	Input high level	15
Figure 16.	Input hysteresis voltage	15
Figure 17.	On-state resistance vs T_{case}	15
Figure 18.	Input low level	15
Figure 19.	Status leakage current	16
Figure 20.	Status low output voltage	16
Figure 21.	Status clamp voltage	16
Figure 22.	[Figure title]	16
Figure 23.	Open-load off-state voltage detection threshold	16
Figure 24.	Application schematic	17
Figure 25.	Open-load detection in off-state	19
Figure 26.	Maximum turn-off current versus load inductance	20
Figure 27.	SO-28 PC board	21
Figure 28.	$R_{thj-amb}$ vs PCB copper area in open box free air condition	22
Figure 29.	SO-28 thermal impedance junction ambient single pulse	22
Figure 30.	Thermal fitting model of a quad channel HSD in SO-28	23
Figure 31.	SO-28 package outline	24
Figure 32.	SO-28 tube shipment (no suffix)	26
Figure 33.	SO-28 tape and reel shipment (suffix "TR")	26

1 Block diagram and pin description

Figure 1. Block diagram

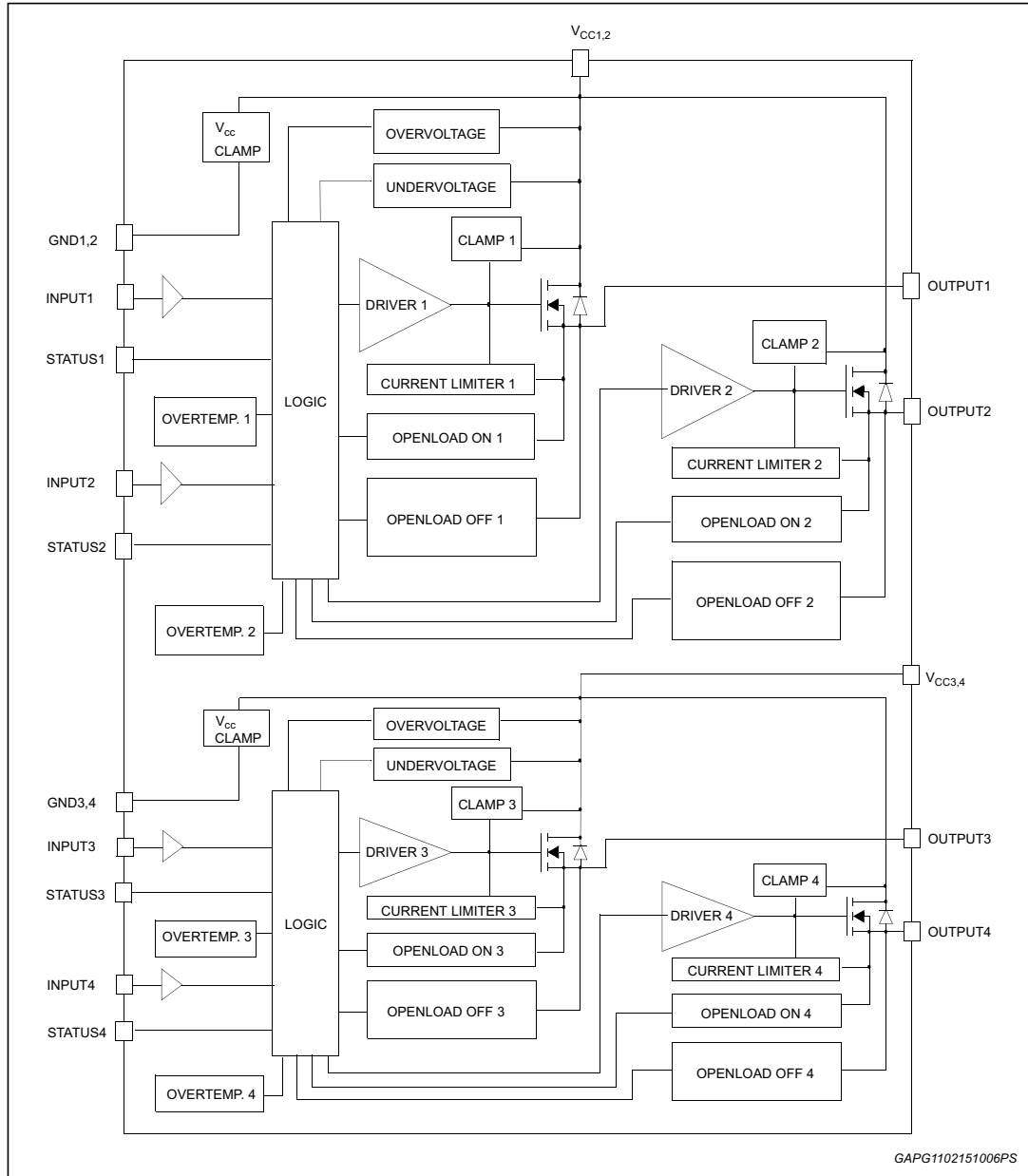


Figure 2. Configuration diagram (top view)

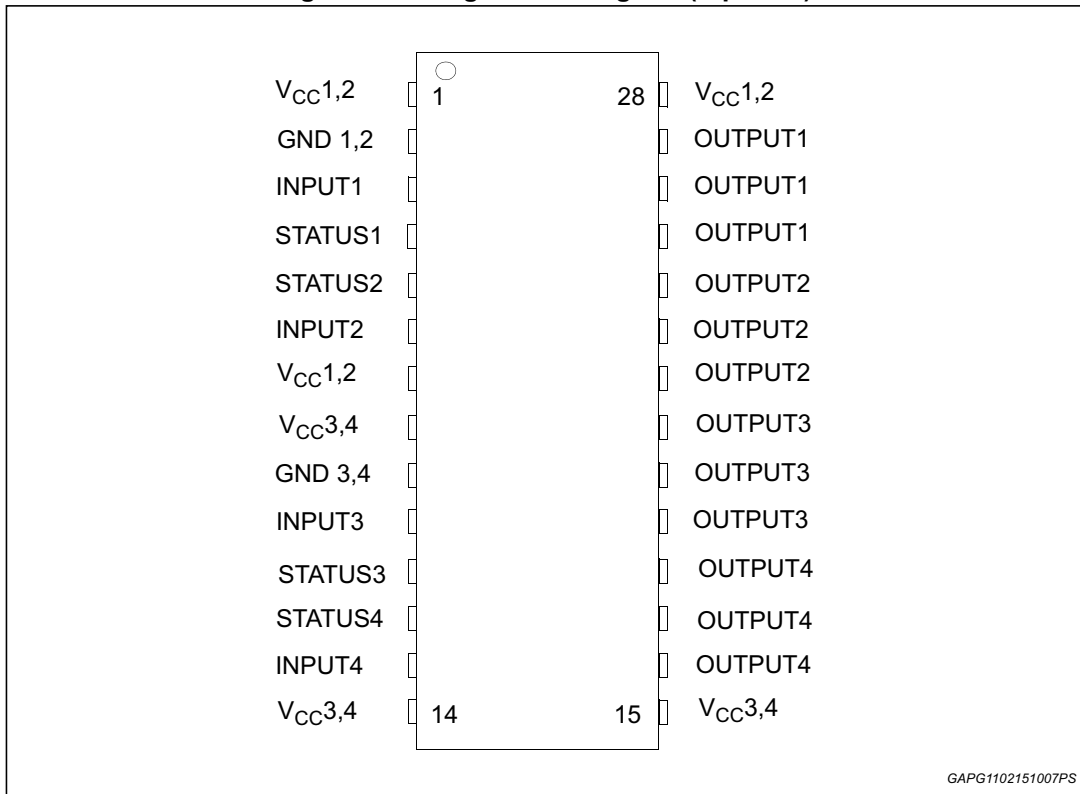


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Status	N.C.	Output	Input
Floating	X	X	X	X
To ground		X		Through 10 KΩ resistor

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-6	A
I_{IN}	DC input current	± 10	mA
I_{STAT}	DC status current	± 10	mA
V_{ESD}	Electrostatic discharge (Human Body Model: R=1.5 K Ω ; C = 100 pF)		
	– INPUT	4000	V
	– STATUS	4000	V
	– OUTPUT	5000	V
	– V_{CC}	5000	V
E_{MAX}	Maximum switching energy (L = 1.5 mH; R _L = 0 Ω ; V _{bat} = 13.5 V; T _{jstart} = 150 °C; I _L = 9 A)	140	mJ
P_{tot}	Power dissipation (per island) at T _{lead} = 25 °C	6.25	W
T_j	Junction operating temperature	Internally limited	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data (per island)

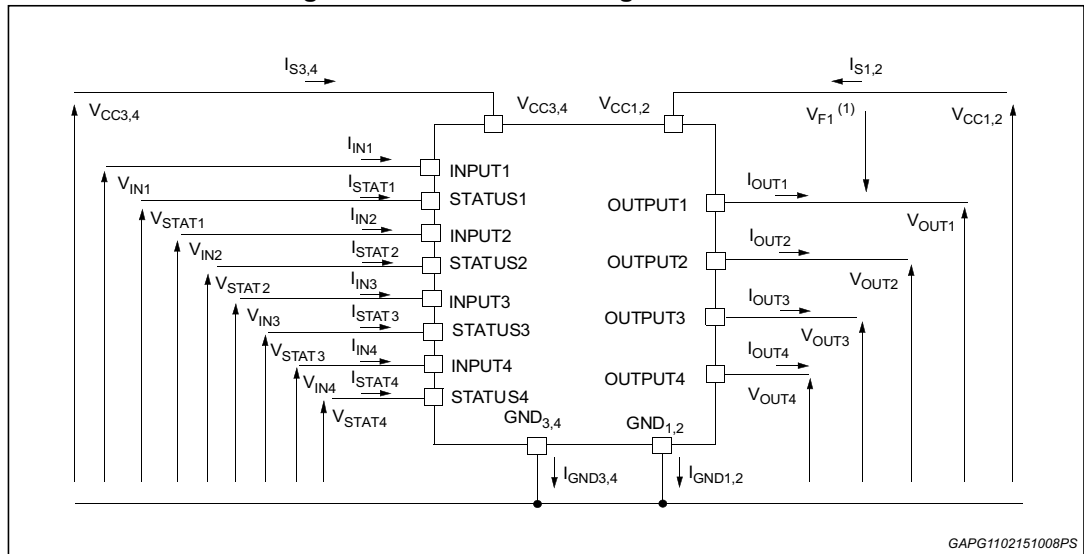
Symbol	Parameter	Value		Unit
$R_{thj-lead}$	Thermal resistance junction-lead	15		°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (one chip ON)	60 ⁽¹⁾	44 ⁽²⁾	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (two chips ON)	46 ⁽¹⁾	31 ⁽²⁾	°C/W

1. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.
2. When mounted on a standard single-sided FR-4 board with 6cm² of Cu (at least 35 μm thick) connected to all V_{CC} pins. Horizontal mounting and no artificial air flow.

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise stated.

Figure 3. Current and voltage conventions



1. $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

Table 5. Power

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		5.5	13	36	V
V _{USD}	Undervoltage shutdown		3	4	5.5	V
V _{OV}	Overvoltage shutdown		36			V

Table 5. Power (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R _{ON}	On-state resistance	I _{OUT} = 2 A; T _j = 25°C			65	mΩ
		I _{OUT} = 2 A; V _{CC} > 8 V			130	mΩ
I _S	Supply current	Off-state; V _{CC} = 13 V; V _{IN} = V _{OUT} = 0 V		12	40	μA
		Off-state; V _{CC} = 13 V; V _{IN} = V _{OUT} = 0 V; T _j = 25°C		12	25	μA
		On-state; V _{CC} = 13 V; V _{IN} = 5 V; I _{OUT} = 0 A		5	7	mA
I _{L(off1)}	Off-state output current	V _{IN} = V _{OUT} = 0 V	0		50	μA
I _{L(off2)}	Off-state output current	V _{IN} = 0V; V _{OUT} = 3.5 V	-75		0	μA
I _{L(off3)}	Off-state output current	V _{IN} = V _{OUT} = 0V; V _{CC} = 13 V; T _j = 125°C			5	μA
I _{L(off4)}	Off-state output current	V _{IN} = V _{OUT} = 0 V; V _{CC} = 13 V; T _j = 25°C			3	μA

Table 6. Protections

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{TSD}	Shutdown temperature		150	175	200	°C
T _R	Reset temperature		135			°C
T _{hyst}	Thermal hysteresis		7	15		°C
t _{SDL}	Status delay in overload conditions	T _j > T _{TSD}			20	μs
I _{lim}	Current limitation	V _{CC} = 13 V	6	9	15	A
		5.5 V < V _{CC} < 36 V			15	A
V _{demag}	Turn-off output clamp voltage	I _{OUT} = 2 A; L = 6 mH	V _{CC} - 41	V _{CC} - 48	V _{CC} - 55	V

Note: To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 7. V_{CC} - output diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _F	Forward on voltage	- I _{OUT} = 1.2 A; T _j = 150°C	—	—	0.6	V

Table 8. Switching ($V_{CC} = 13V$; $T_j = 25^\circ C$)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$R_L = 6.5 \Omega$ from V_{IN} rising edge to $V_{OUT} = 1.3 V$ (see Figure 5)	—	30	—	μs
$t_{d(off)}$	Turn-off delay time	$R_L = 6.5 \Omega$ from V_{IN} falling edge to $V_{OUT} = 11.7 V$ (see Figure 5)	—	30	—	μs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	$R_L = 6.5 \Omega$ from $V_{OUT} = 1.3 V$ to $V_{OUT} = 10.4 V$ (see Figure 5)	—	See Figure 10	—	$V/\mu s$
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	$R_L = 6.5 \Omega$ from $V_{OUT} = 11.7 V$ to $V_{OUT} = 1.3 V$ (see Figure 5)	—	See Figure 12	—	$V/\mu s$

Table 9. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level				1.25	V
I_{IL}	Low level input current	$V_{IN} = 1.25 V$	1			μA
V_{IH}	Input high level		3.25			V
I_{IH}	High level input current	$V_{IN} = 3.25 V$			10	μA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	$I_{IN} = 1 mA$	6	6.8	8	V
		$I_{IN} = -1 mA$		-0.7		V

Table 10. Status pin

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status low output voltage	$I_{STAT} = 1.6 mA$			0.5	V
I_{LSTAT}	Status leakage current	Normal operation; $V_{STAT} = 5 V$			10	μA
C_{STAT}	Status pin input capacitance	Normal operation; $V_{STAT} = 5 V$			100	pF
V_{SCL}	Status clamp voltage	$I_{STAT} = 1 mA$	6	6.8	8	V
		$I_{STAT} = -1 mA$		-0.7		V

Table 11. Open-load detection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{OL}	Open-load on-state detection threshold	$V_{IN} = 5\text{ V}$	50	100	200	mA
$t_{DOL(on)}$	Open-load on-state detection delay	$I_{OUT} = 0\text{ A}$			200	μs
V_{OL}	Open-load off-state voltage detection threshold	$V_{IN} = 0\text{ V}$	1.5	2.5	3.5	V
$t_{DOL(off)}$	Open-load detection delay at turn-off				1000	μs

Figure 4. Status timings

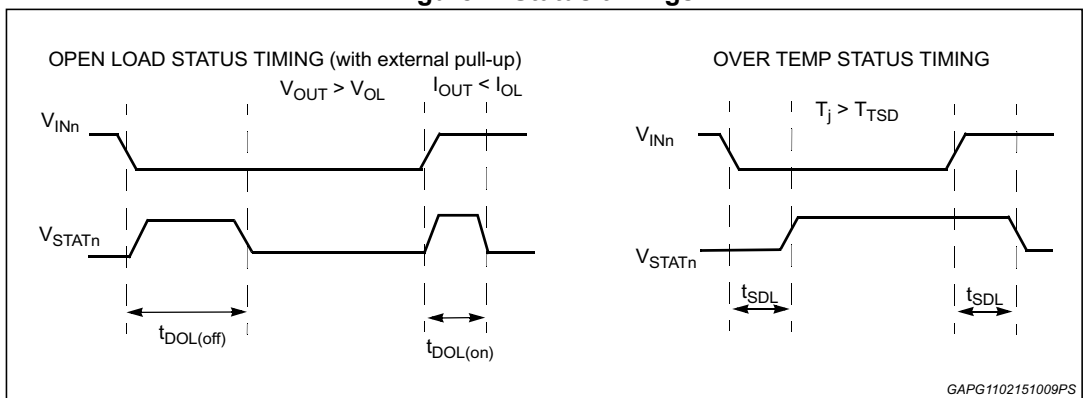


Figure 5. Switching characteristics

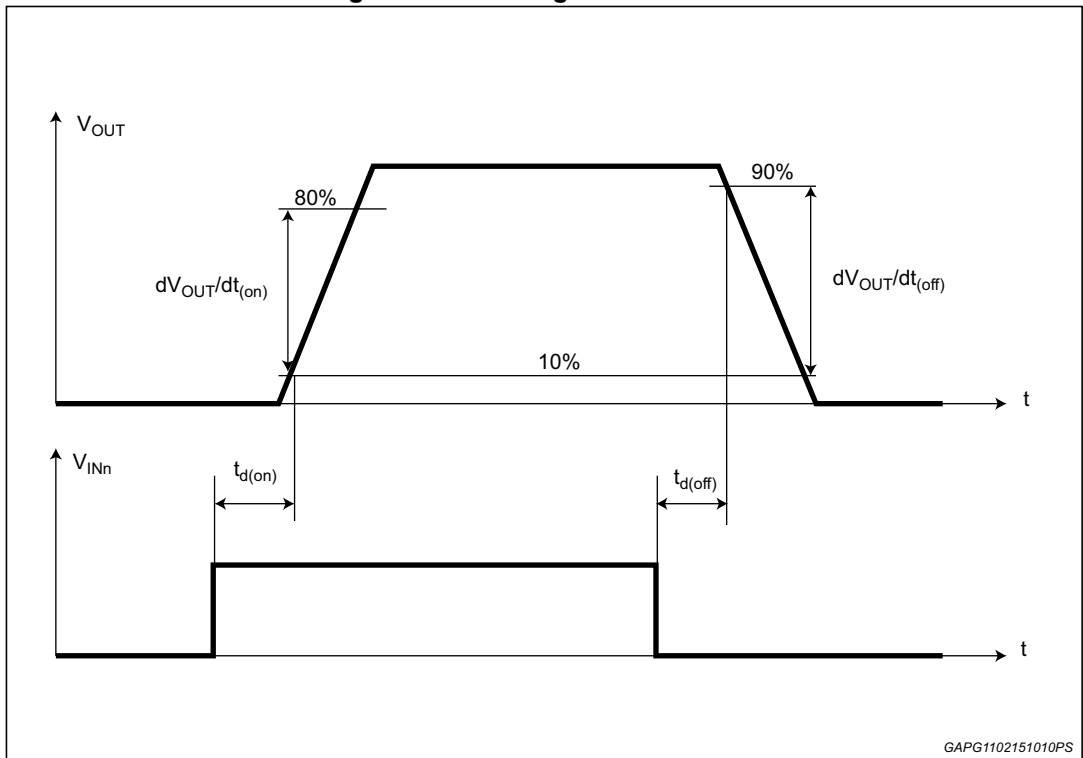


Table 12. Truth table

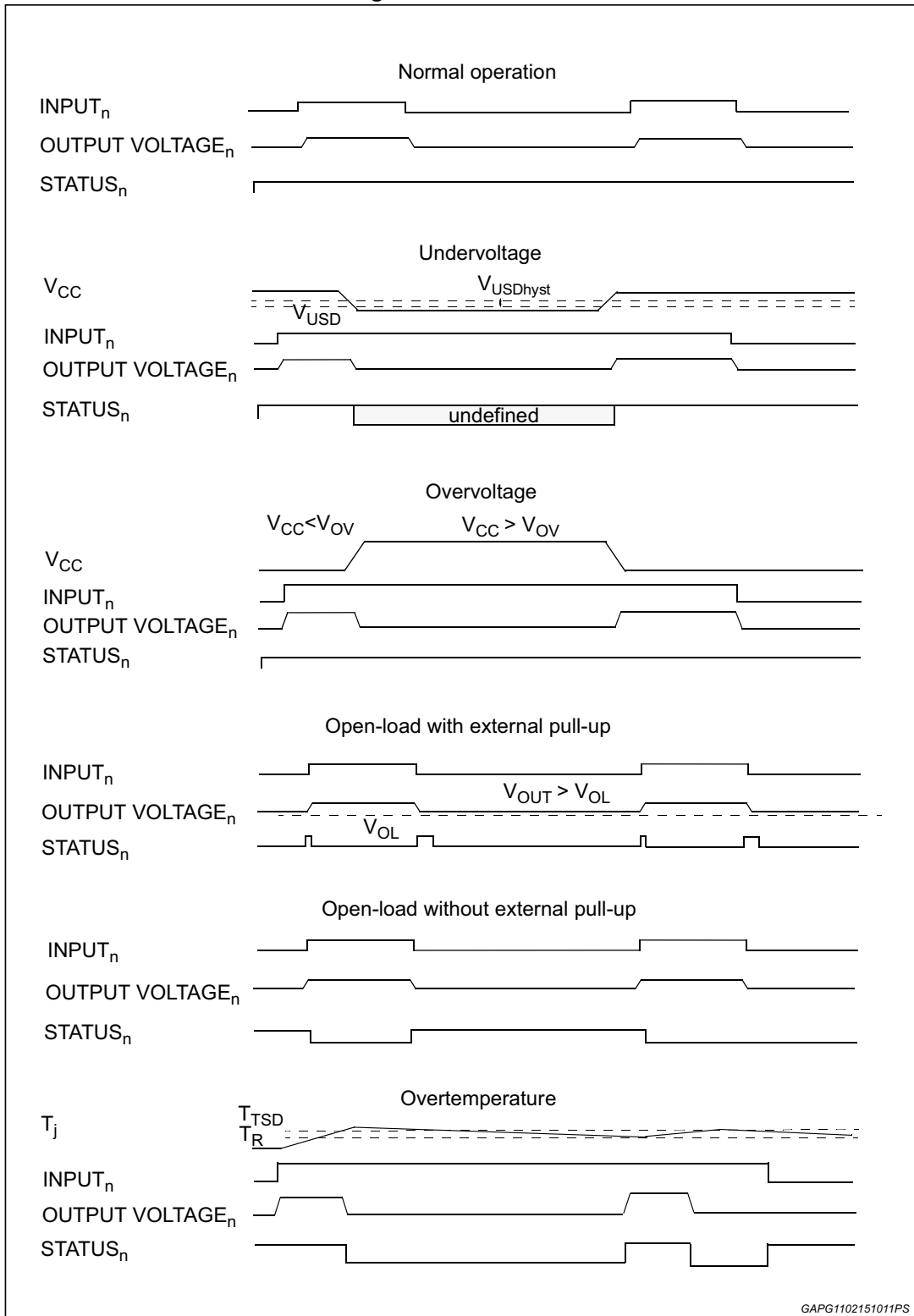
Conditions	Input	Output	Status
Normal operation	L	L	H
	H	H	H
Current limitation	L	L	H
	H	X	($T_j < T_{TSD}$) H
	H	X	($T_j > T_{TSD}$) L
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Overvoltage	L	L	H
	H	L	H
Output voltage > V_{OL}	L	H	L
	H	H	H
Output current < I_{OL}	L	L	H
	H	H	L

Table 13. Electrical transient requirements

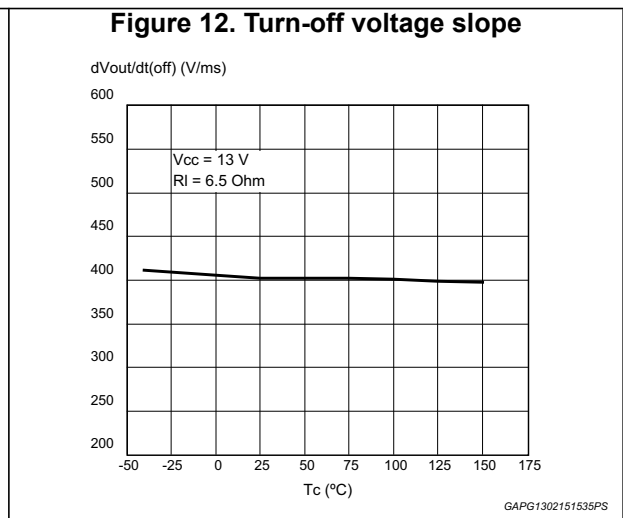
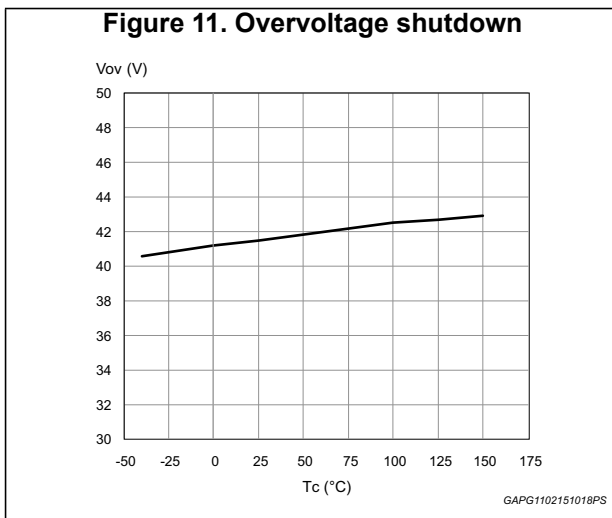
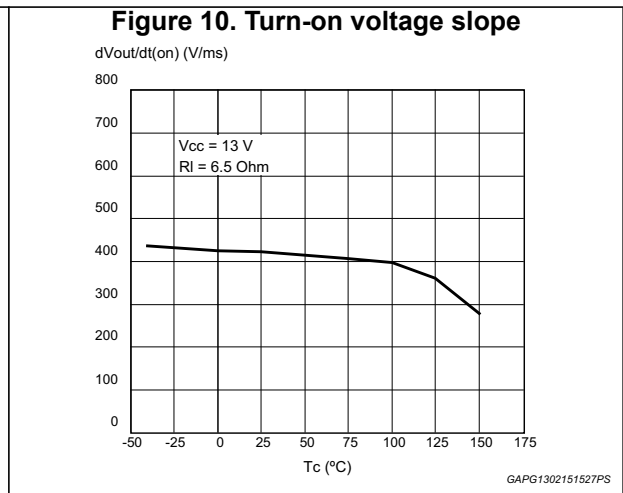
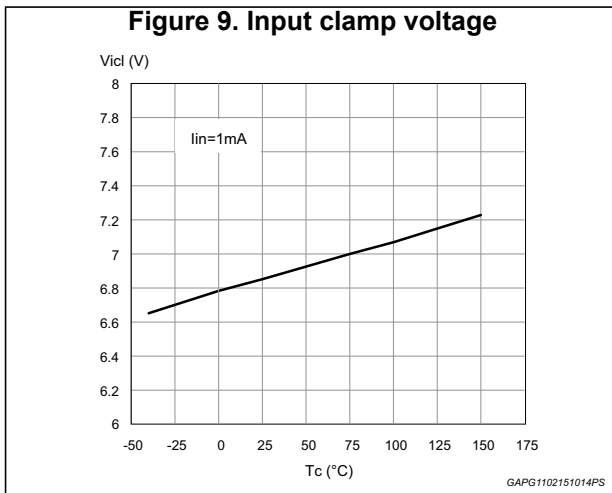
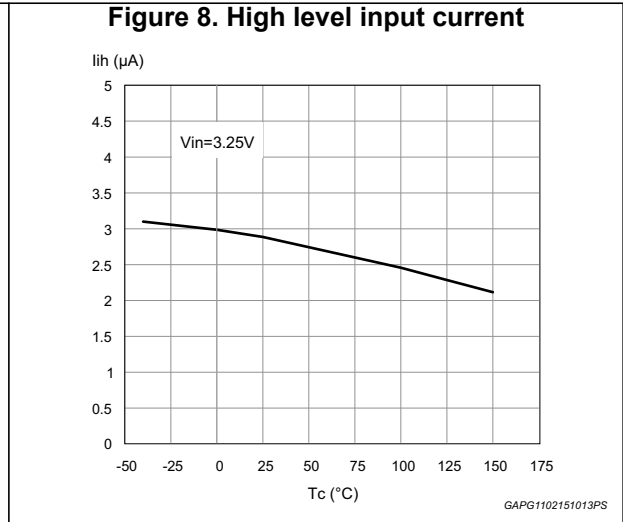
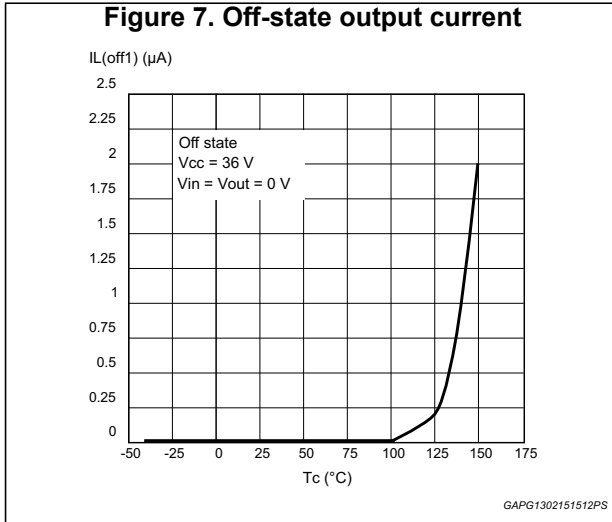
ISO T/R 7637/1 test pulse	Test level				Delays and impedance
	I	II	III	IV	
1	-25 V ⁽¹⁾	-50 V ⁽¹⁾	-75 V ⁽¹⁾	-100 V ⁽¹⁾	2 ms, 10 Ω
2	+25 V ⁽¹⁾	+50 V ⁽¹⁾	+75 V ⁽¹⁾	+100 V ⁽¹⁾	0.2 ms, 10 Ω
3a	-25 V ⁽¹⁾	-50 V ⁽¹⁾	-100 V ⁽¹⁾	-150 V ⁽¹⁾	0.1 μs, 50 Ω
3b	+25 V ⁽¹⁾	+50 V ⁽¹⁾	+75 V ⁽¹⁾	+100 V ⁽¹⁾	0.1 μs, 50 Ω
4	-4 V ⁽¹⁾	-5 V ⁽¹⁾	-6 V ⁽¹⁾	-7 V ⁽¹⁾	100 ms, 0.01 Ω
5	+26.5 V ⁽¹⁾	+46.5 V ⁽²⁾	+66.5 V ⁽²⁾	+86.5 V ⁽²⁾	400 ms, 2 Ω

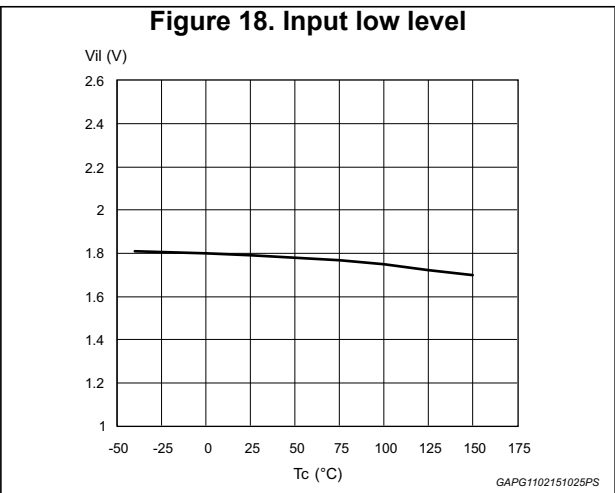
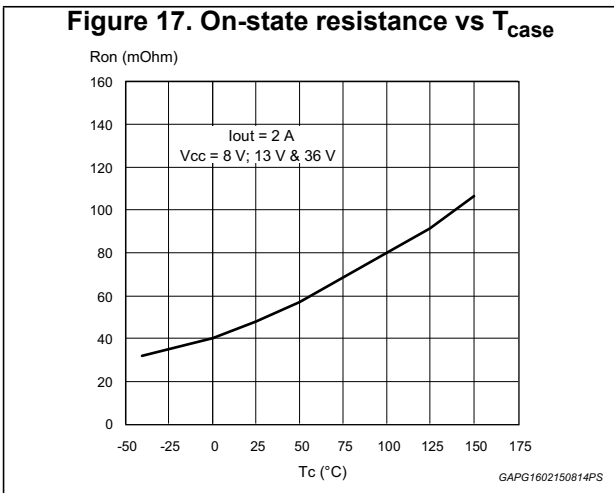
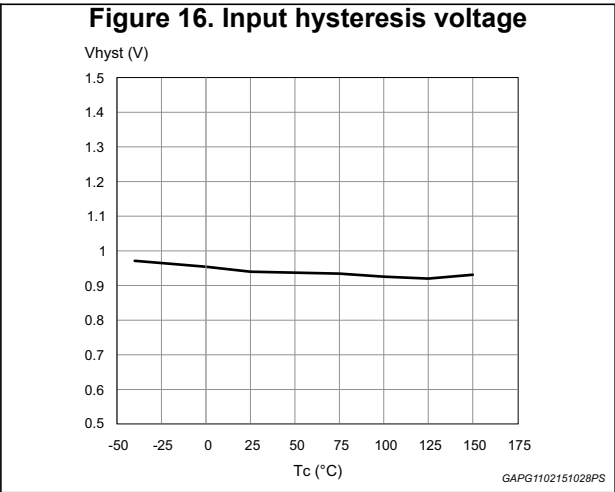
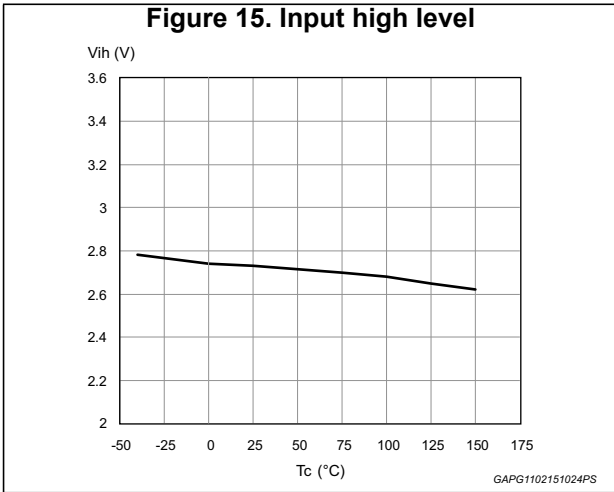
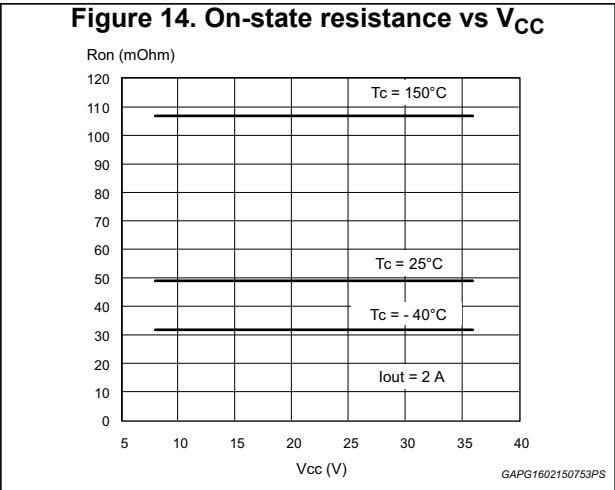
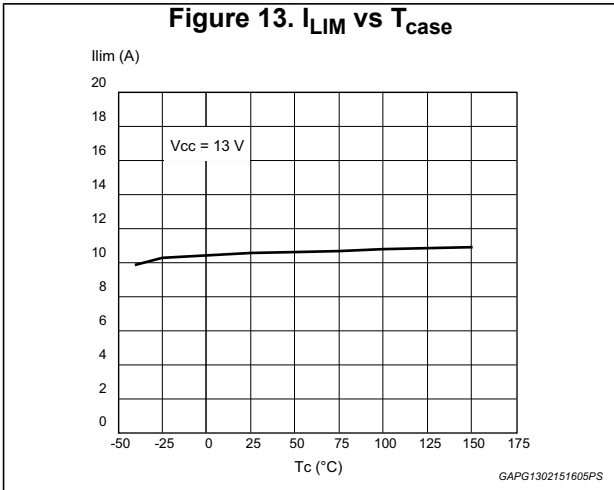
1. All functions of the device are performed as designed after exposure to disturbance.
2. One or more functions of the device is not performed as designed after exposure and cannot be returned to proper operation without replacing the device.

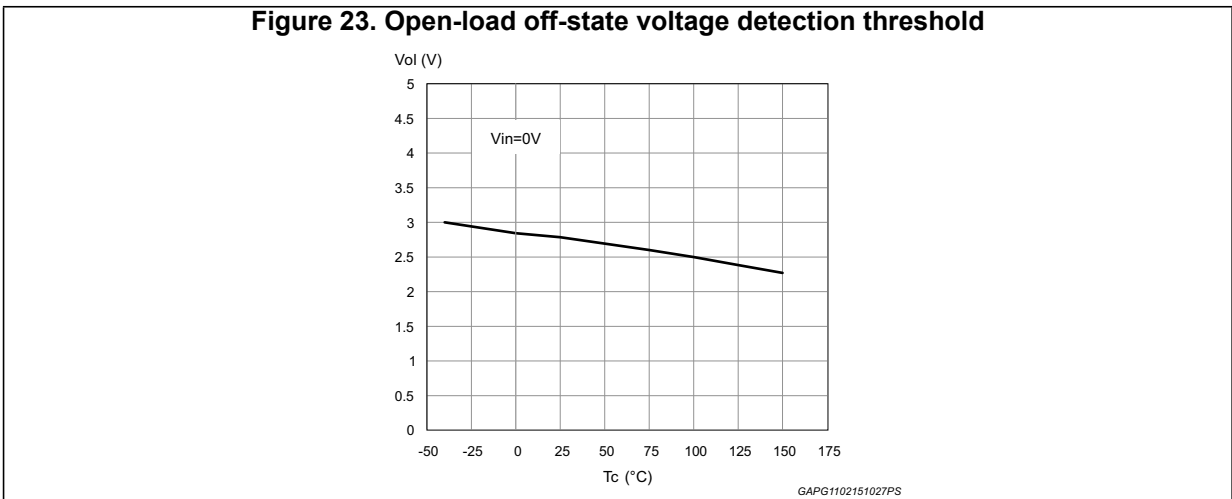
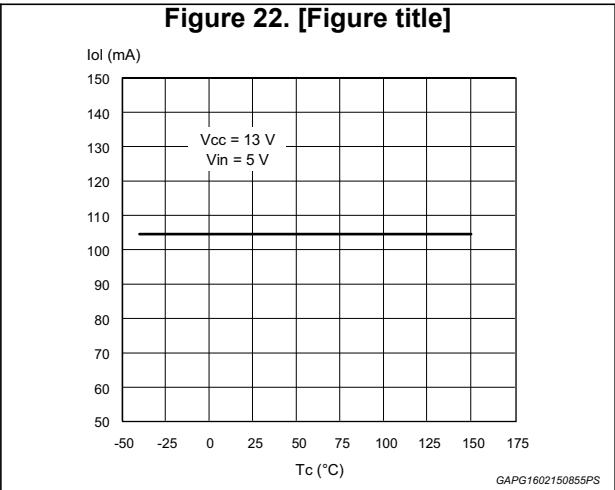
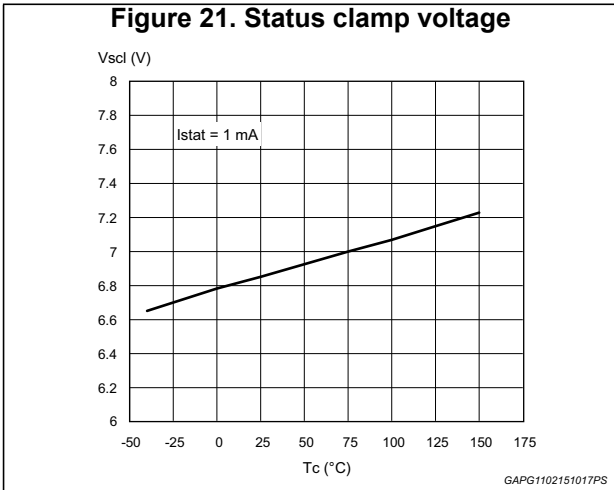
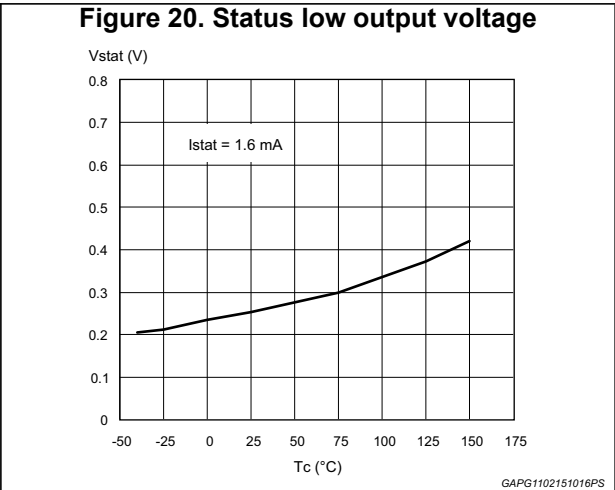
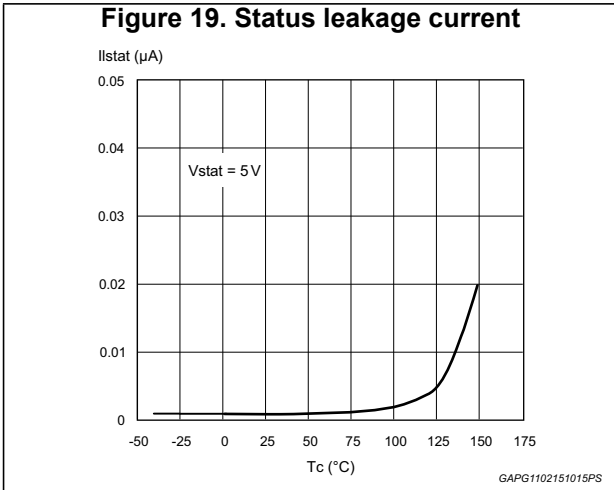
Figure 6. Waveforms



2.4 Electrical characteristics curves

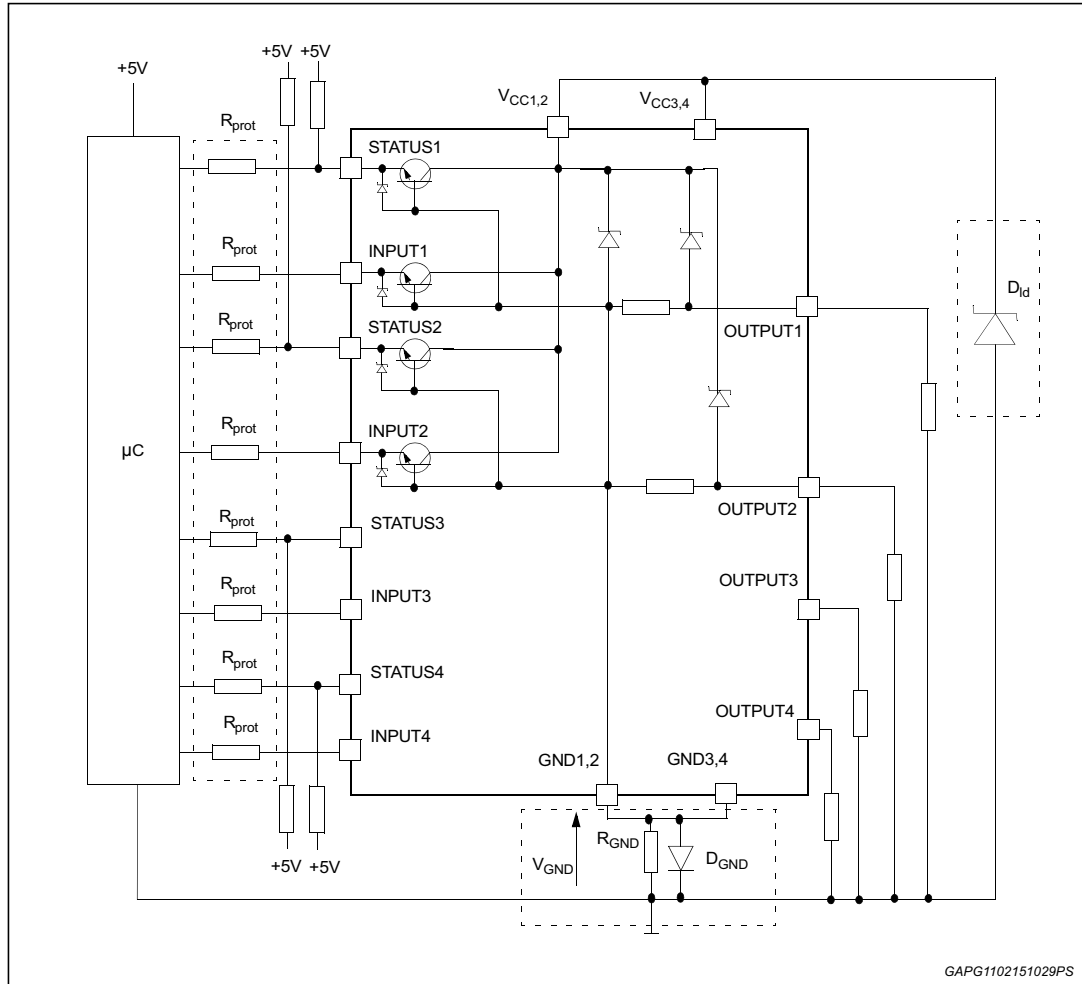






3 Application information

Figure 24. Application schematic



GAPG1102151029PS

Note: Channels 3 & 4 have the same internal circuit as channel 1 & 2.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: a resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following show how to dimension the R_{GND} resistor:

1. $R_{GND} \leq 600 \text{ mV} / 2 (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$ during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that, if the microprocessor ground is not shared by the device ground, then the R_{GND} produces a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high-side drivers sharing the same R_{GND} .

If the calculated power dissipation requires the use of a large resistor, or several devices have to share the same resistor, then ST suggests using solution 2 below.

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND} = 1 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device is driving an inductive load. This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network produces a shift ($\sim 600\text{mV}$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift not varies if more than one HSD shares the same diode/resistor network. Series resistor in INPUT and STATUS lines are also required to prevent that, during battery voltage transient, the current exceeds the Absolute Maximum Rating. Safest configuration for unused INPUT and STATUS pin is to leave them unconnected.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} maximum DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than those shown in [Table 13](#).

3.3 MCU I/O protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins are pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Example

For the following conditions:

$$V_{CCpeak} = - 100 \text{ V}$$

$$I_{latchup} \geq 20 \text{ mA}$$

$$V_{OH\mu C} \geq 4.5 \text{ V}$$

$$5 \text{ k}\Omega \leq R_{prot} \leq 65 \text{ k}\Omega.$$

Recommended values are:

$$R_{prot} = 10 \text{ k}\Omega$$

3.4 Open-load detection in off-state

Off-state open-load detection requires an external pull-up resistor (R_{PU}) connected between OUTPUT pin and a positive supply voltage (V_{PU}) like the +5 V line used to supply the microprocessor.

The external resistor has to be selected according to the following requirements:

1. No false open load indication when load is connected: in this case we have to avoid V_{OUT} to be higher than V_{OLmin} ; this results in the following condition:

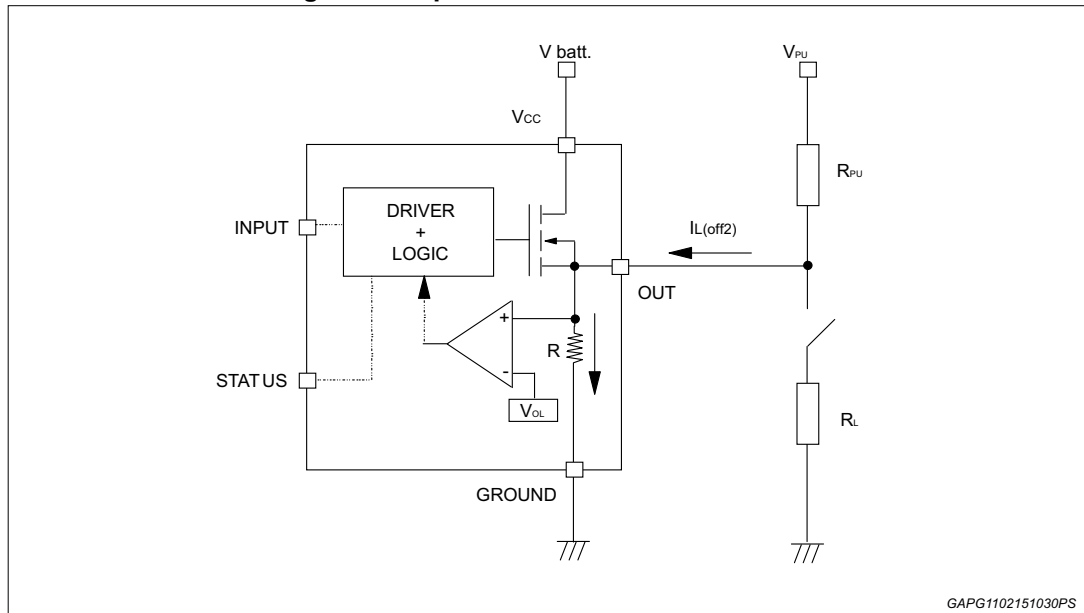
$$V_{OUT} = (V_{PU} / (R_L + R_{PU}))R_L < V_{OLmin}.$$

2. No misdetection when load is disconnected: in this case the V_{OUT} has to be higher than V_{OLmax} ; this results in the following condition:

$$R_{PU} < (V_{PU} - V_{OLmax}) / I_{L(off2)}.$$

Because $I_{s(OFF)}$ may significantly increase if V_{out} is pulled high (up to several mA), the pull-up resistor R_{PU} should be connected to a supply that is switched OFF when the module is in standby.

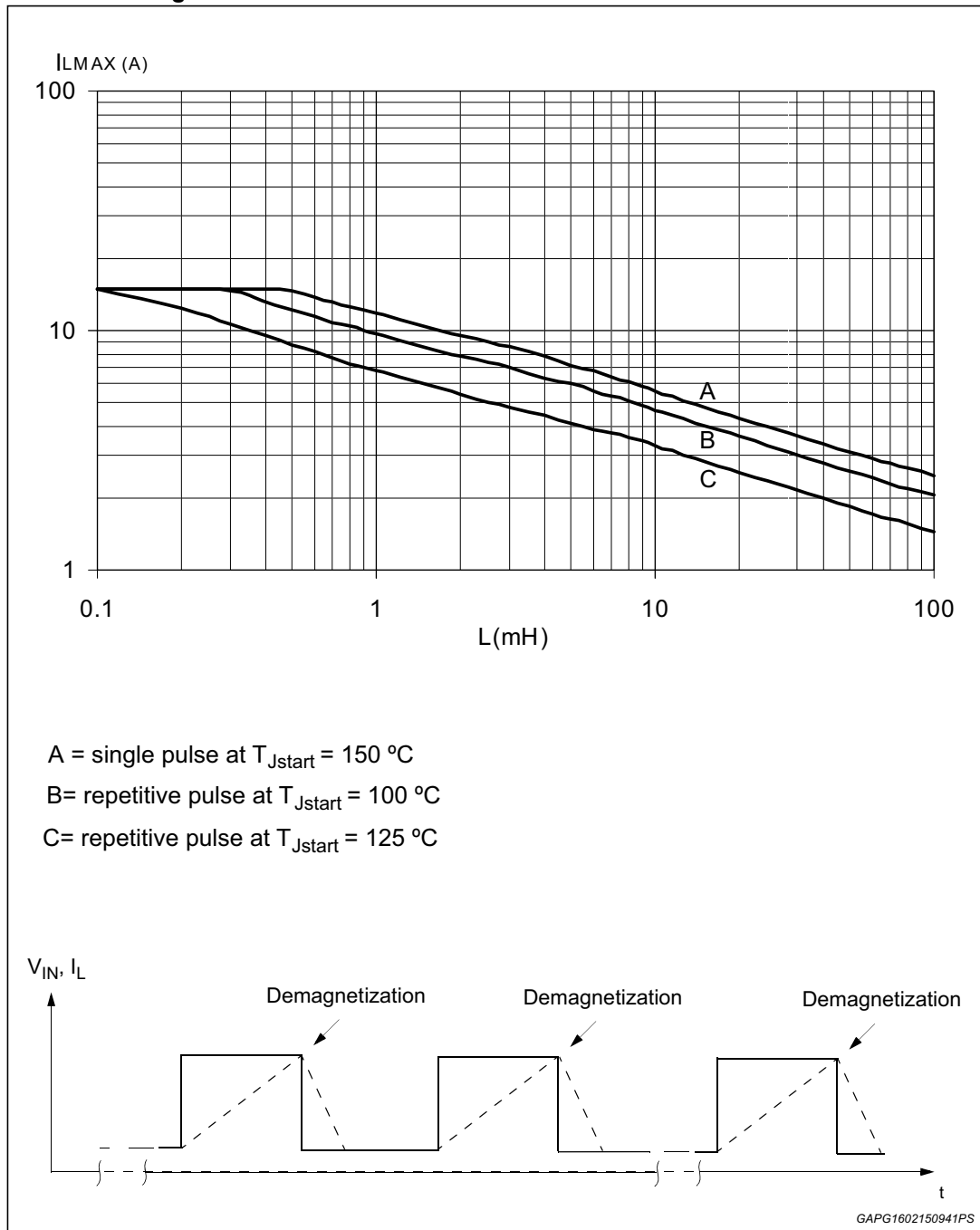
Figure 25. Open-load detection in off-state



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3.5 Maximum demagnetization energy ($V_{CC} = 13.5\text{ V}$)

Figure 26. Maximum turn-off current versus load inductance

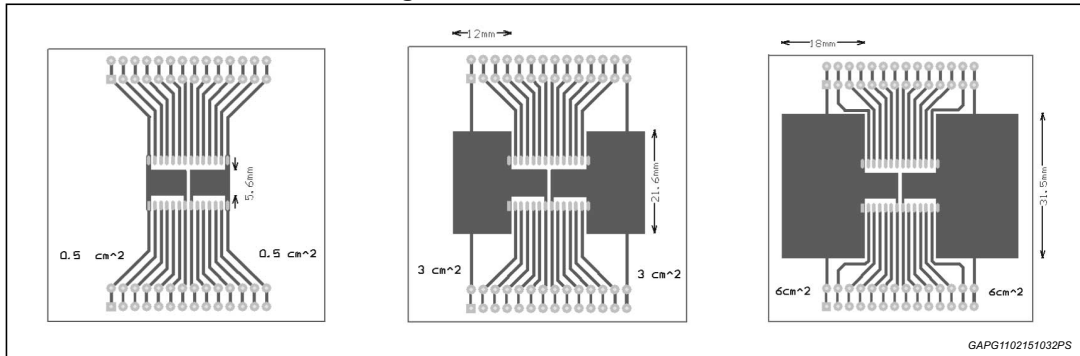


Note: Values are generated with $R_L = 0\ \Omega$.
 In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

4 Package and PCB thermal data

4.1 SO-28 thermal data

Figure 27. SO-28 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness = 2 mm, Cu thickness = 35 μ m, Copper areas: 0.5 cm², 3 cm², 6 cm²).

Table 14. Thermal calculation according to the PCB heatsink area

Chip 1	Chip 2	T_{jchip1}	T_{jchip2}	Note
ON	OFF	$R_{thA} \times P_{dchip1} + T_{amb}$	$R_{thC} \times P_{dchip1} + T_{amb}$	
OFF	ON	$R_{thC} \times P_{dchip2} + T_{amb}$	$R_{thA} \times P_{dchip2} + T_{amb}$	
ON	ON	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$R_{thB} \times (P_{dchip1} + P_{dchip2}) + T_{amb}$	$P_{dchip1} = P_{dchip2}$
ON	ON	$(R_{thA} \times P_{dchip1}) + R_{thC} \times P_{dchip2} + T_{amb}$	$(R_{thA} \times P_{dchip2}) + R_{thC} \times P_{dchip1} + T_{amb}$	$P_{dchip1} \neq P_{dchip2}$

R_{thA} = thermal resistance junction to ambient with one chip ON

R_{thB} = thermal resistance junction to ambient with both chips ON and $P_{dchip1} = P_{dchip2}$

R_{thC} = mutual thermal resistance

Figure 28. $R_{thj-amb}$ vs PCB copper area in open box free air condition

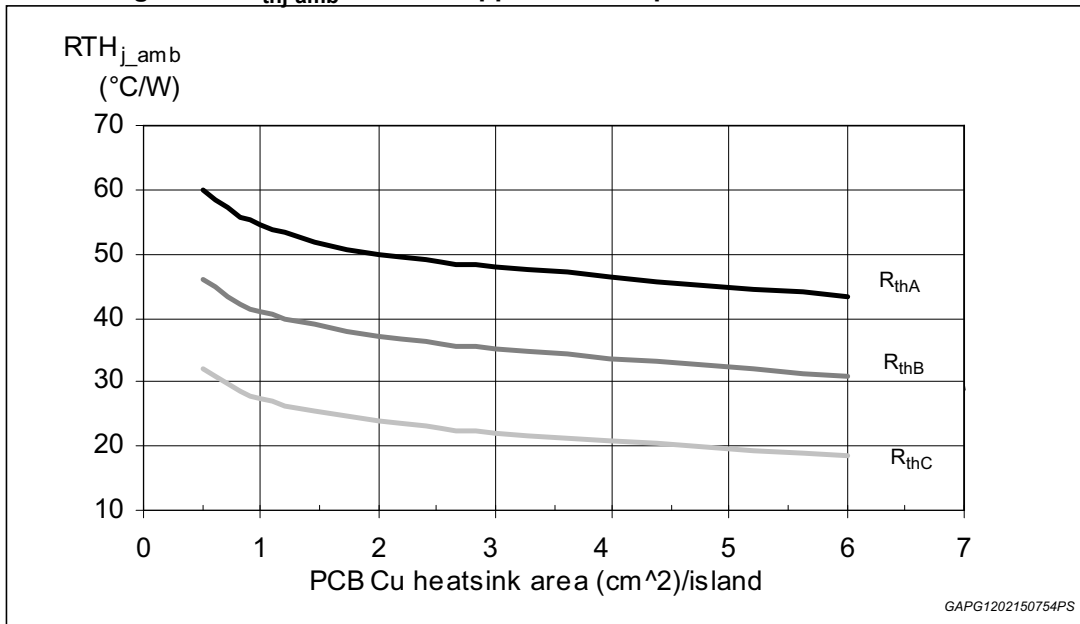
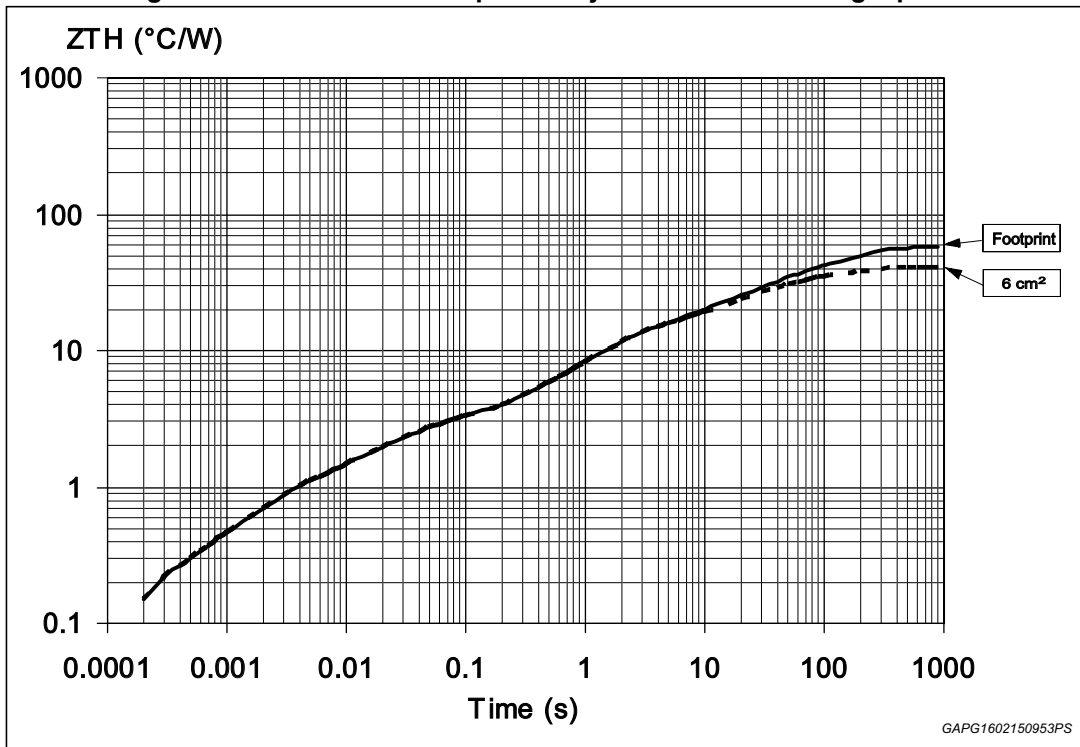


Figure 29. SO-28 thermal impedance junction ambient single pulse

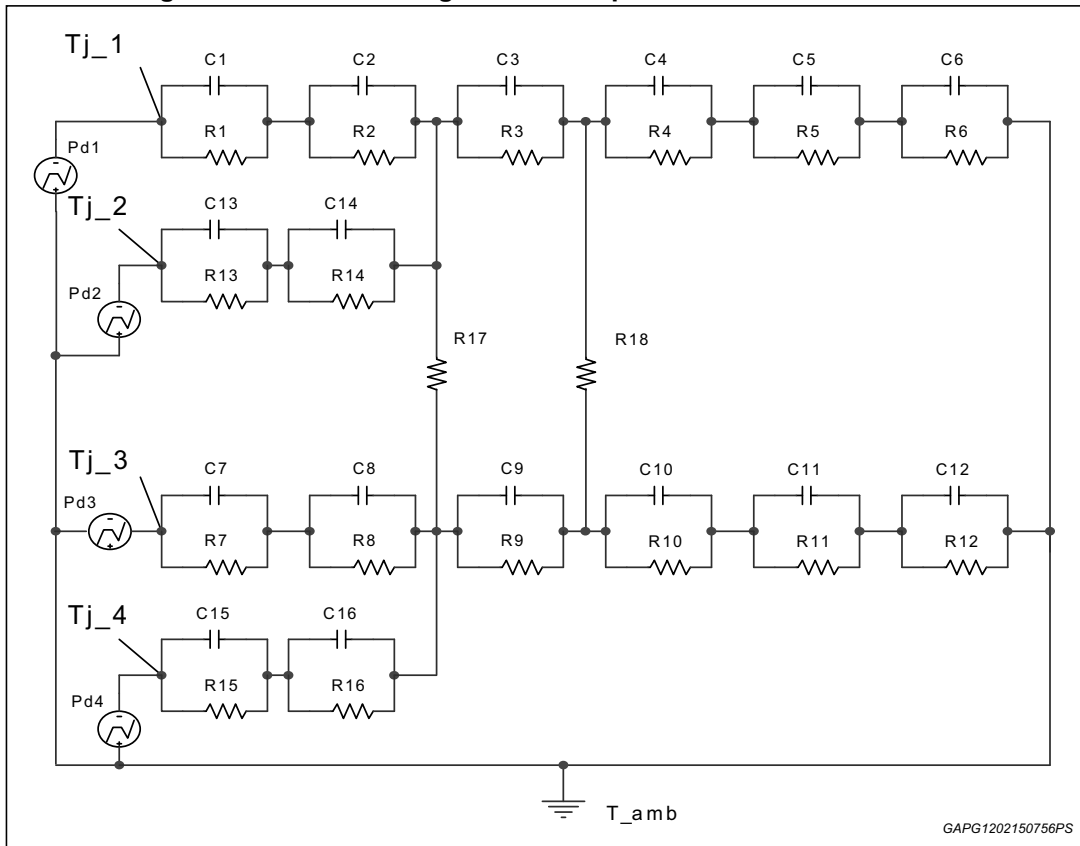


Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Figure 30. Thermal fitting model of a quad channel HSD in SO-28



GAPG1202150756PS

Table 15. Thermal parameters

Area / island (cm ²)	Footprint	6
R1 = R7 = R13 = R15 (°C/W)	0.15	
R2 = R8 = R14 = R16 (°C/W)	0.7	
R3 = R9 (°C/W)	1.8	
R4 = R10 (°C/W)	10	
R5 = R11 (°C/W)	15	
R6 = R12 (°C/W)	30	13
C1 = C7 = C13 = C15 (W.s/°C)	0.0005	
C2 = C8 = C14 = C16 (W.s/°C)	3E-03	
C3 = C9 (W.s/°C)	1.50E-02	
C4 = C10 (W.s/°C)	0.15	
C5 = C11 (W.s/°C)	1.5	
C6 = C12 (W.s/°C)	5	8
R17 = R18 (°C/W)	150	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 SO-28 package information

Figure 31. SO-28 package outline

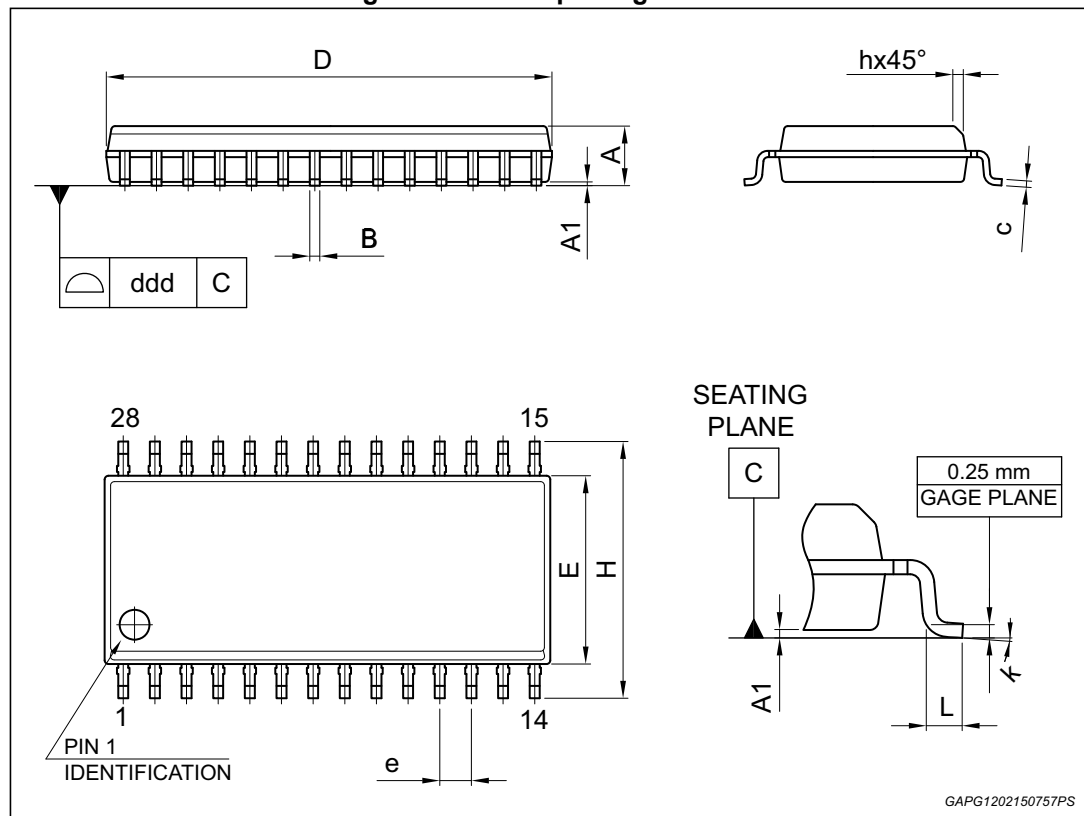


Table 16. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D ⁽¹⁾	17.70		18.10

Table 16. SO-28 mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
E	7.40		7.60
e		1.27	
H	10.0		10.65
h	0.25		0.75
L	0.40		1.27
k	0°		8°
ddd			0.10

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

5.2 SO-28 packing information

Figure 32. SO-28 tube shipment (no suffix)

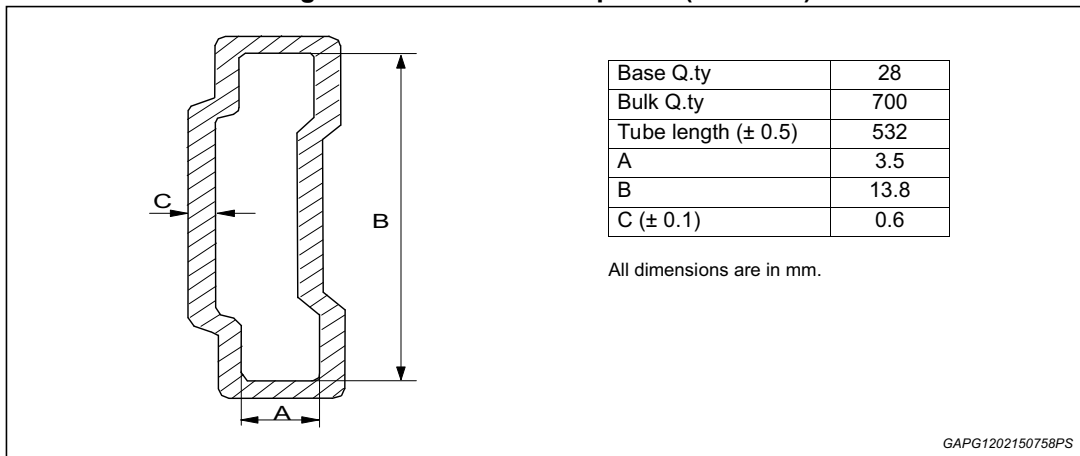
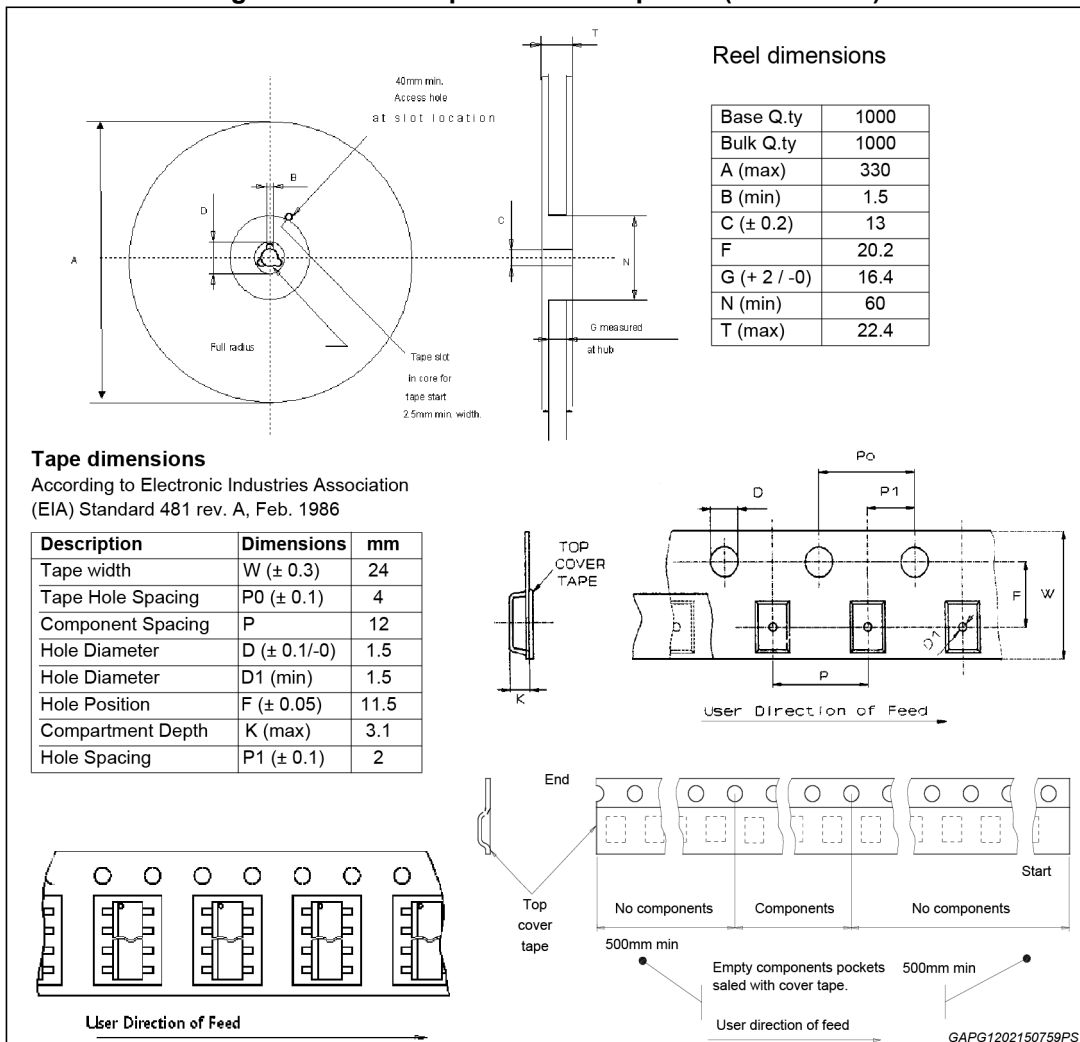


Figure 33. SO-28 tape and reel shipment (suffix "TR")



6 Revision history

Table 17. Document revision history

Date	Revision	Changes
03-May-2006	1	Initial release.
18-Dec-2008	2	Document reformatted and restructured. Added contents, list of tables and figures. Added <i>ECOPACK[®] packages</i> information.
03-May-2010	3	Changed <i>Features</i> list. Replaced VND830P-E to VND830-E.
07-Feb-2011	4	<i>Table 3: Absolute maximum ratings</i> – E _{MAX} : updated value Updated <i>Figure 5: Switching characteristics</i> Updated <i>Table 15: Thermal parameters</i>
19-Sep-2013	5	Updated Disclaimer.
16-Feb-2015	6	Updated: – <i>Section 5.1: SO-28 package information</i> ; – Tape dimensions in <i>Figure 33: SO-28 tape and reel shipment (suffix "TR") on page 26</i> .

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