LNK64x4-64x8
LinkSwitch-3 Family

Energy-Efficient, Accurate Primary-Side Regulation CV/CC Switcher for Adapters and Chargers

Product Highlights

Dramatically Simplifies CV/CC Converters
- Eliminates optocoupler and all secondary CV/CC control circuitry
- Eliminates all control loop compensation circuitry

Advanced Performance Features
- Compensates for transformer inductance tolerances
- Compensates for input line voltage variations
- Compensates for cable voltage drop
- Compensates for external component temperature variations
- Very accurate IC parameter tolerances using test trimming technology
- Frequency jittering greatly reduces EMI filter cost
- Programmable switching frequency up to 85 kHz to reduce transformer size
- Minimum operation frequency fixed to improve transient load response

Advanced Protection/Safety Features
- Auto-restart protection reduces power delivered by >90% for output short-circuit and control loop faults (open and shorted components)
- Hysteretic thermal shutdown – automatic recovery reduces power supply returns from the field
- Meets high-voltage creepage requirements between DRAIN and all other pins both on the PCB and at the package

EcoSmart™– Energy Efficient
- Easily meets all global energy efficiency regulations with no added components
- No-load consumption at 230 VAC input with bias winding <10 mW for LNK64x4-LNK64x6 and <30 mW for LNK64x7-LNK64x8
- ON/OFF control provides constant efficiency down to very light loads – ideal for CEC regulations
- No current sense resistors – maximizes efficiency

Green Package
- Halogen free and RoHS compliant package

Applications
- Chargers for cell/cordless phones, PDAs, MP3/portable audio devices, adapters, etc.

Description

The LinkSwitch™-3 family of ICs dramatically simplifies low power CV/CC charger designs by eliminating an optocoupler and secondary control circuitry. The device introduces a revolutionary control technique to provide very accurate output voltage and current regulation, compen-sating for transformer and internal parameter tolerances along with input voltage variations.

The device incorporates a 725 V power MOSFET, a novel ON/OFF control state machine, a high-voltage switched current source for self biasing, frequency jittering, cycle-by-cycle current limit and hysteretic thermal shutdown circuitry onto a monolithic IC.

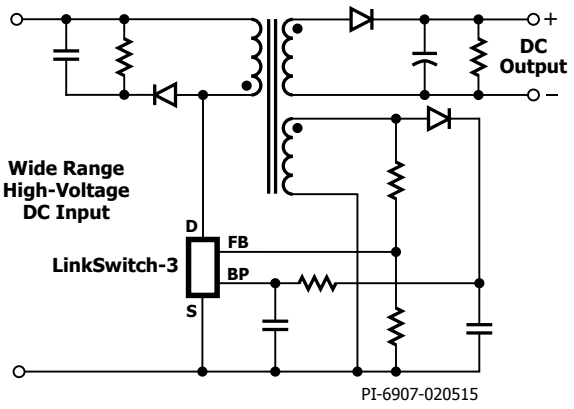


Figure 1. Typical Application – Not a Simplified Circuit.

Output Power Table[1,2,3,4]

Product[5]	90-264 VAC	
	D (SO-8C) Package	
	Adapter	Open Frame
LNK6404D / LNK6424D	3.5 W	4.1 W
LNK6405D / LNK6415D / LNK6425D	4.5 W	5.1 W
LNK6406D / LNK6416D / LNK6426D / LNK6436D / LNK6446D	5.5 W	6.1 W
LNK6407D / LNK6417D / LNK6427D	7.5 W	7.5 W
Product[5]	**E (eSIP-7C) and K (eSOP-12B) Packages**	
	Adapter	**Open Frame**
LNK6407K / LNK6417K / LNK6427K	8.5 W	9 W
LNK6408K / LNK6418K / LNK6428K / LNK6448K	10 W	10 W
LNK6408E / LNK6418E / LNK6428E / LNK6448E	10 W	10 W

Table 1. Output Power Table.

Notes:
1. Assumes minimum input DC voltage >90 VDC, K_p ≥1 (Recommend K_p ≥1.15 for accurate CC regulation), η >78%, D_{MAX} <55%.
2. Output power capability is reduced if a lower input voltage is used.
3. Minimum continuous power with adequate heat sink measured at 50 °C ambient with device junction below 110 °C.
4. Assumes bias winding is used to supply BYPASS pin.
5. Package: D: SO-8C, E: eSIP-7C, K: eSOP-12B.

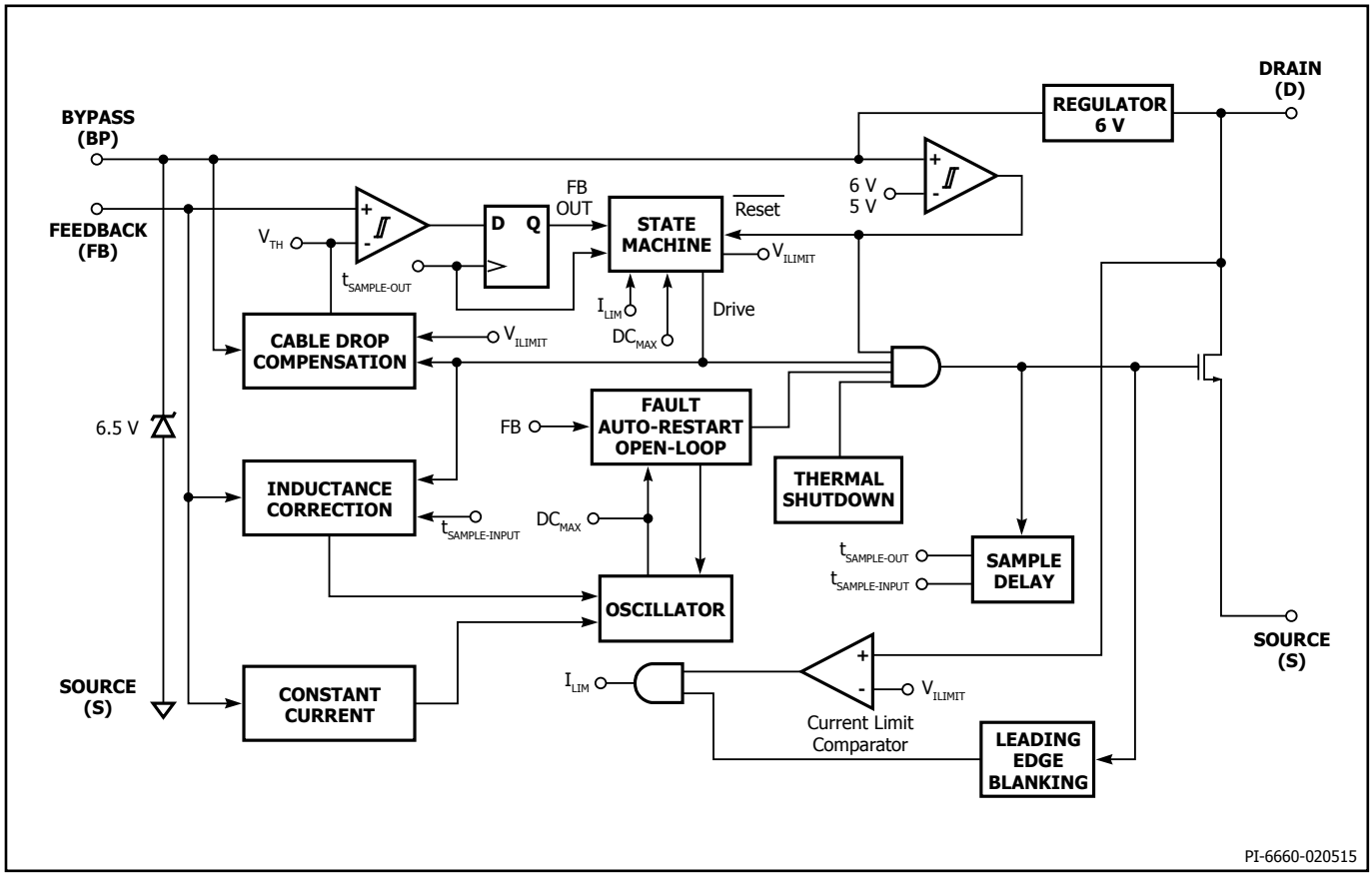


Figure 2 Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
This pin is the power MOSFET drain connection. It provides internal operating current for both start-up and steady-state operation.

BYPASS (BP) Pin:
This pin is the connection point for an external 1 μF bypass capacitor for the internally generated 6 V supply.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. This pin senses the AC voltage on the bias winding. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the bias winding. The internal inductance correction circuit uses the forward voltage on the bias winding to sense the bulk capacitor voltage.

SOURCE (S) Pin:
This pin is internally connected to the output MOSFET source for high-voltage power and control circuit common returns.

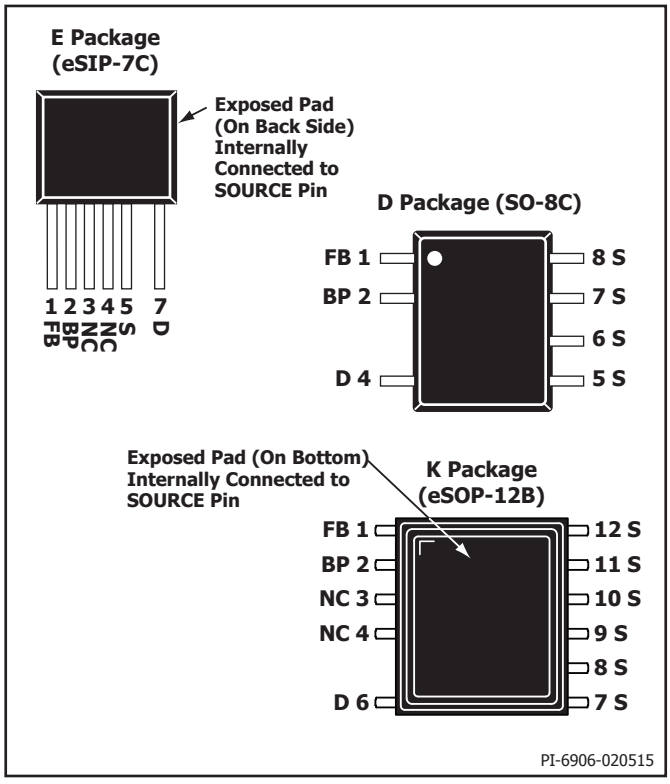


Figure 3. Pin Configuration.

LinkSwitch-3 Functional Description

The LinkSwitch-3 combines a high-voltage power MOSFET switch with a power supply controller in one device. It uses an ON/OFF control to regulate the output voltage. In addition, the switching frequency is modulated to regulate the output current to provide a constant current characteristic. The LinkSwitch-3 controller consists of an oscillator, feedback (sense and logic) circuit, 6 V regulator, over-temperature protection, frequency jittering, current limit circuit, leading-edge blanking, inductance correction circuitry, frequency control for constant current regulation and ON/OFF state machine for CV control.

Inductance Correction Circuitry
If the primary magnetizing inductance is either too high or low the converter will automatically compensate for this by adjusting the oscillator frequency. Since this controller is designed to operate in discontinuous-conduction mode the output power is directly proportional to the set primary inductance and its tolerance can be completely compensated with adjustments to the switching frequency.

Constant Current (CC) Operation
As the output voltage and therefore the flyback voltage across the bias winding ramps up, the FEEDBACK pin voltage increases. The switching frequency is adjusted as the FEEDBACK pin voltage increases to provide a constant output current regulation. The constant current circuit and the inductance correction circuit are designed to operate concurrently in the CC region.

Constant Voltage (CV) Operation
As the FEEDBACK pin approaches 2 V from the constant current regulation mode, the power supply transitions into CV operation. The switching frequency at this point is at its maximum value, corresponding to the peak power point of the CV/CC characteristic. The controller regulates the FEEDBACK pin voltage to remain at FEEDBACK pin threshold (V_{FBTH}) using an ON/OFF state-machine. The FEEDBACK pin voltage is sampled 2.5 μs after the turn-off of the high-voltage switch.

At light loads the current limit is also reduced to decrease the transformer flux density and the FEEDBACK pin sampling is done earlier.

Output Cable Compensation
This compensation provides a constant output voltage at the end of the cable over the entire load range in CV mode. As the converter load increases from no-load to the peak power point (transition point between CV and CC) the voltage drop introduced across the output cable is compensated by increasing the FEEDBACK pin reference voltage. The controller determines the output load and therefore the correct degree of compensation based on the output of the state machine. The amount of cable drop compensation is determined by the third digit in the device part number.

Auto-Restart and Open-Loop Protection
In the event of a fault condition such as an output short or an open-loop condition the LinkSwitch-3 enters into an appropriate protection mode as described below.

In the event the FEEDBACK pin voltage during the flyback period falls below 0.7 V before the FEEDBACK pin sampling delay (~2.5 μs) for a duration in excess of ~300 ms (auto-restart on-time (t_{AR-ON}) the converter enters into auto-restart, wherein the power MOSFET is disabled for 1500 ms. The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed.

In addition to the conditions for auto-restart described above, if the sensed FEEDBACK pin current during the forward period of the conduction cycle (switch "on" time) falls below 120 μA, the converter annunciates this as an open-loop condition (top resistor in potential divider is open or missing) and reduces the auto-restart time from 300 ms to approximately 6 clock cycles (90 μs), whilst keeping the disable period of 2 seconds.

Over-Temperature Protection
The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 60 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 60 °C, at which point the MOSFET is re-enabled.

Current Limit
The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction. The LinkSwitch-3 also contains a "di/dt" correction feature to minimize CC variation across the input line range.

6 V Regulator
The 6 V regulator charges the bypass capacitor connected to the BYPASS pin to 6 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the device runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows the LinkSwitch-3 to operate continuously from the current drawn from the DRAIN pin however for the best no-load input power, the BYPASS pin should be supplied current of I_{S1} from the bias winding at no-load conditions. A bypass capacitor value of 1 μF is sufficient for both high frequency decoupling and energy storage.

Applications Example

Circuit Description

This circuit shown in Figure 4 is configured as a primary-side regulated flyback power supply utilizing the LNK6448K. With an average efficiency of 78% and <30 mW no-load input power this design easily exceeds the most stringent current energy efficiency requirements.

Input Filter

AC input power is rectified by bridge BR1. The rectified DC is filtered by the bulk storage capacitors C1 and C2. Inductors L2 and L3, together with C1 and C2 form a pi (π) filter, which attenuates conducted differential-mode EMI noise. This configuration along with Power Integrations transformer E-Shield™ technology allows this design to meet EMI standard EN55022 class B with good margin without requiring a Y capacitor, even with the output connected to safety earth ground. A ferrite bead for L3 is sufficient especially when the output of the supply is floating. Fuse F1 provides protection against catastrophic failure. NTC (Negative Thermal Coefficient) thermistor RT1 is used to limit the rush current to below the peak specification of BR1 during start-up especially at high-line input voltage. High-line results in the highest current into C1 and C2. F1 and RT1 can be replaced by a single fusible resistor. If the reduction in efficiency is acceptable, a bridge with a higher I_{FSM} rating may also allow removal of RT1. If a fusible resistor is selected, use a flameproof type. It should be suitably rated (typically a wire wound type) to withstand the instantaneous dissipation while the input capacitors charge when first connected to the AC line.

LNK6448K Primary

The LNK6448K device (U1) incorporates the power switching device, oscillator, CC/CV control engine, start-up, and protection functions. The integrated 725 V MOSFET provides a large drain voltage margin in universal input AC applications, increasing reliability and also reducing the output diode voltage stress by allowing a greater transformer turns ratio. The device is completely self-powered from the BYPASS pin and decoupling capacitor C7. For the LNK64xx devices, there are 4 options for different amount of cable drop compensation determined by the third digit in the device part number. Table 2 shows the amount of compensation for each device. The LNK644x devices do not provide cable drop compensation.

The optional bias supply formed by D3 and C8 provides the operating current for U1 via resistor R8. This reduces the no-load consumption from ~200 mW to <30 mW and also increases light load efficiency.

The rectified and filtered input voltage is applied to one side of the primary winding of T1. The other side of the transformer's primary winding is driven by the integrated MOSFET in U1. The leakage inductance drain voltage spike is limited by an RCD-R clamp consisting of D2, R3, R11, and C6.

Output Rectification

The secondary of the transformer is rectified by D1, a 10 A, 45 V Schottky barrier type for higher efficiency, and filtered by C3, L1 and C4. If lower efficiency is acceptable then this can be replaced with a 5 A PN junction diode for lower cost. In this application C3 and C4 are sized to meet the required output voltage ripple specification with a ferrite bead L1, which eliminates the high switching noise on the output. A pre-load resistor R2 is used to meet the regulation specification. If the battery self-discharge is required, the pre-load resistor can be replaced with a series resistor and Zener network.

Output Regulation

The LNK64xx family of devices regulates the output using ON/OFF control in the constant voltage (CV) regulation region of the output characteristic and frequency control for constant current (CC) regulation. The feedback resistors (R6 and R7) were selected using standard 1% resistor values to center both the nominal output voltage and constant current regulation thresholds.

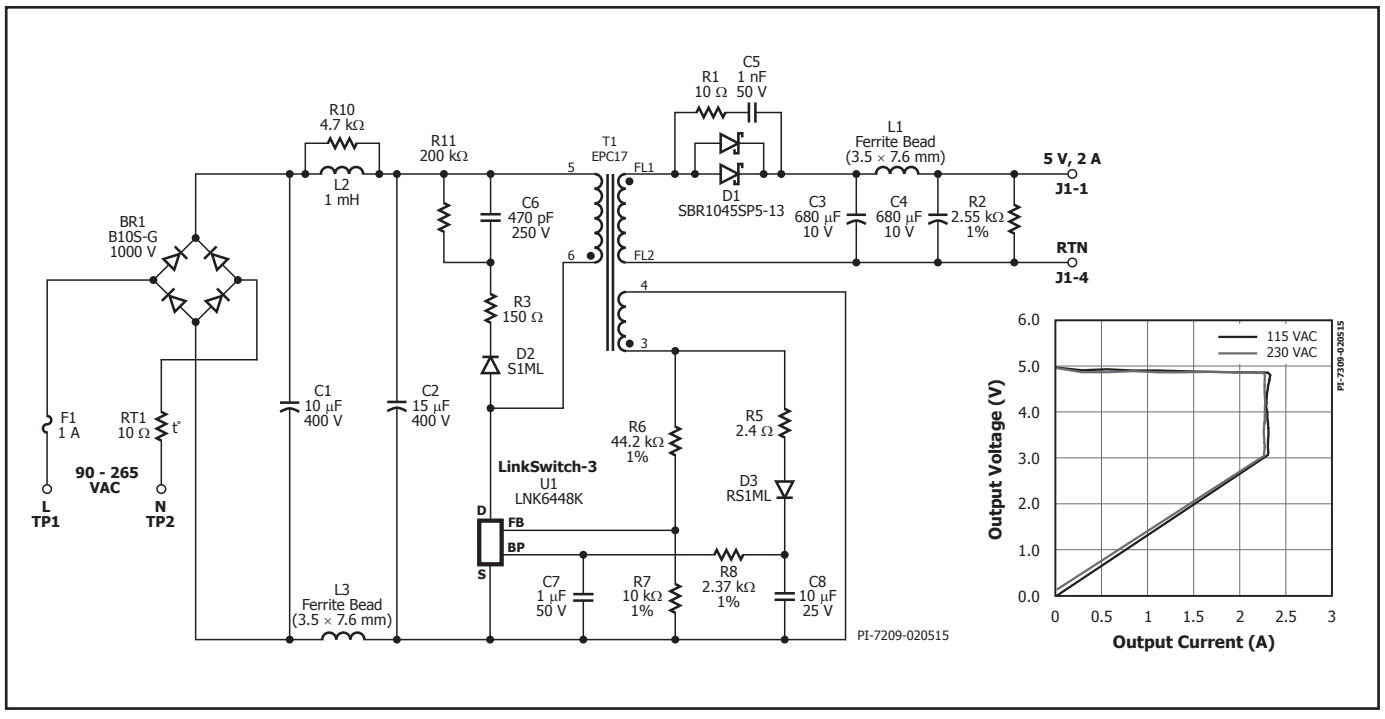


Figure 4. Energy Efficient USB Charger Power Supply (78% Average Efficiency, <30 mW No-load Input Power).

Key Application Considerations

Output Power Table

The data sheet maximum output power table (Table 1) repre- sents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. Assumes minimum input DC voltage >90 VDC, K_p ≥1 (Recommend K_p ≥1.15 for accurate CC regulation), η >78%, D_{MAX} <55%.
2. Output power capability is reduced if a lower input voltage is used.
3. Minimum continuous power with adequate heat sink measured at 50 °C ambient with device junction below 110 °C.
4. Assumes bias winding is used to supply BYPASS pin.

Output Tolerance
LinkSwitch-3 provides an overall output tolerance (including line, component variation and temperature) of ±5% for the output voltage in CV operation and ±10% for the output current during CC operation over a junction temperature range of 0 °C to 110 °C.

BYPASS Pin Capacitor Selection
A 1 μF BYPASS pin capacitor is recommended. The capacitor voltage rating should be greater than 7 V. The capacitor's dielectric material is not important but tolerance of capacitor should be ≤ ±50%. The capacitor must be physically located adjacent to the LinkSwitch-3 BYPASS pin.

Cable Drop Compensation
The amount of output cable compensation is determined by the third digit in the device part number. Table 2 shows the amount of compensation for each LinkSwitch-3 device.

The output voltage that is entered into PIXIs design spreadsheet is the voltage at the end of the output cable when the power supply is delivering maximum power. The output voltage at the terminals of the supply is the value measured at the end of the cable multiplied by the output voltage change factor.

LinkSwitch-3 Output Cable Voltage Drop Compensation

Device	Output Voltage Change Factor (±1%)
LNK640x	1.02
LNK641x	1.04
LNK642x	1.06
LNK643x	1.08
LNK644x	1.01

Table 2. Cable Compensation Change Factor vs. Device.

LinkSwitch-3 Layout Considerations

Circuit Board Layout
LinkSwitch-3 is a highly integrated power supply solution that integrates on a single die, both, the controller and the high- voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply. See Figure 5 for a recommended circuit board layout for LinkSwitch-3.

When designing a printed circuit board for the LinkSwitch-3 based power supply, it is important to follow the following guidelines:

Single Point Grounding
Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-3 SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.

Bypass Capacitor
The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.

Feedback Resistors
Place the feedback resistors directly at the FEEDBACK pin of the LinkSwitch-3 device. This minimizes noise coupling.

Thermal Considerations
The copper area connected to the SOURCE pins provides the LinkSwitch-3 heat sink. A good estimate is that the LinkSwitch-3 will dissipate 10% of the output power. Provide enough copper area to keep the SOURCE pin temperature below 110 °C is recommended to provide margin for part to part $R_{DS(ON)}$ variation.

Secondary Loop Area
To minimize leakage inductance and EMI the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

Electrostatic Discharge Spark Gap
A spark gap is created between the output and the AC input. The spark gap directs ESD energy from the secondary back to the AC input. The trace from the AC input to the spark gap electrode should be spaced away from other traces to prevent unwanted arcing occurring and possible circuit damage.

Drain Clamp Optimization
LinkSwitch-3 senses the feedback winding on the primary-side to regulate the output. The voltage that appears on the feedback winding is a reflection of the secondary winding voltage while the internal MOSFET is off. Therefore any leakage inductance induced ringing can affect output regulation. Optimizing the drain clamp to

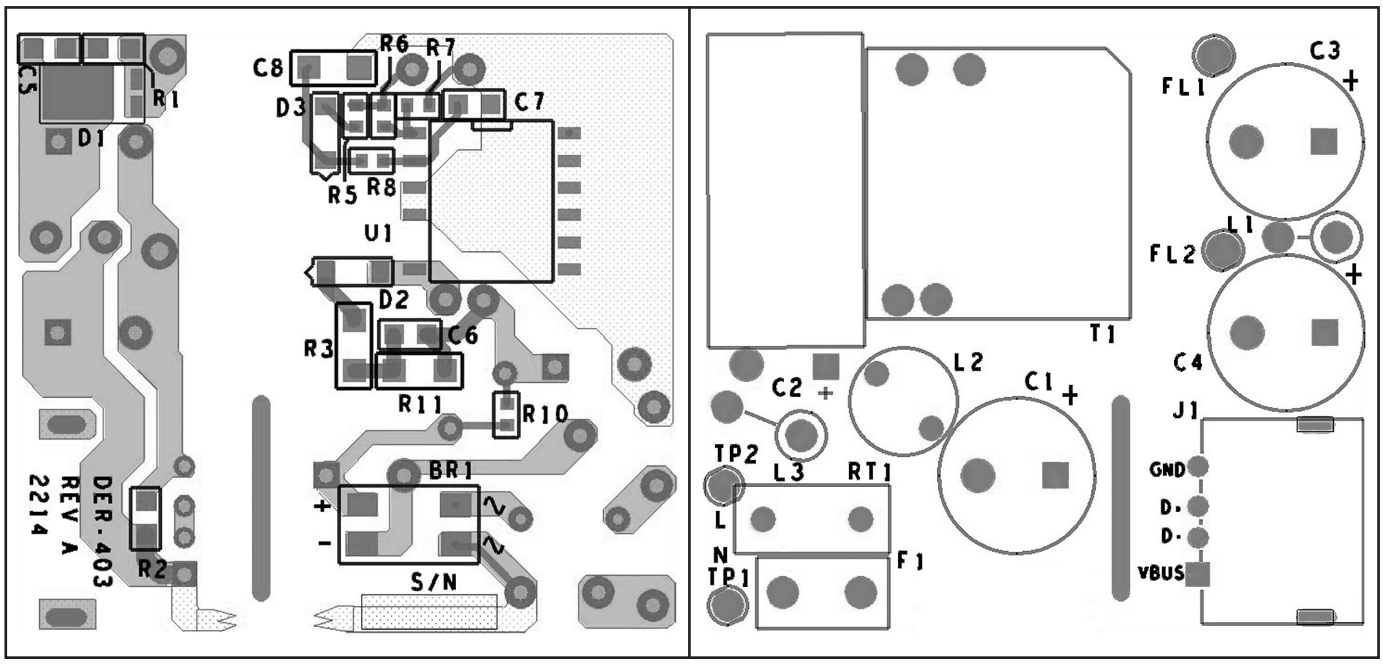


Figure 5. PCB (Bottom Layer on Left) (Top Layer on Right) Layout Example Showing 10 W Design using K Package.

minimize the high frequency ringing will give the best regulation. Figure 6 shows the desired drain voltage waveform compared to Figure 7 with a large undershoot due to the leakage inductance induced ring. This will reduce the output voltage regulation performance. To reduce this adjust the value of the resistor in series with the clamp diode.

Addition of a Bias Circuit for Higher Light Load Efficiency and Lower No-load Input Power Consumption

The addition of a bias circuit can decrease the no-load input power from ~200 mW down to less than 30 mW at 230 VAC input. Light load efficiency also increases which may avoid the need to use a Schottky barrier vs. PN junction output diode while still meeting average efficiency requirements.

The power supply schematic shown in Figure 4 has only one winding for both feedback and bias circuit. Diode D3, C8, R5 and R8 form the bias circuit. The feedback winding voltage is designed at 11 V, this provides a high enough voltage to supply the BYPASS pin even during low switching frequency operation at no-load.

A 10 μF capacitance value is recommended for C8 to hold up the bias voltage at the low switching frequencies that occur at light to no-load. The capacitor type is not critical but the voltage rating should be above the maximum value of V_{BIAS}. The recommended current into the BYPASS pin is equal to IC supply current (0.6 mA to 0.7 mA) at the minimum bias winding voltage. The BYPASS pin current should not exceed 10 mA at the maximum bias winding voltage. The value of R8 is calculated according to $(V_{BIAS} – V_{BP})/I_{S2}$, where V_{BIAS} (10 V typ.) is the voltage across C8, I_{S2} (0.6 mA to 0.7 mA typ.) is the IC supply current and V_{BP} (6.2 V typ.) is the BYPASS pin voltage. The parameters I_{S2} and V_{BP} are provided in the parameter table of the LinkSwitch-3 data sheet. Diode D3 can be any low cost diode such as FR102, 1N4148 or BAV19/20/21.

Quick Design Checklist

As with any power supply design, all LinkSwitch-3 designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions.

The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak VDS does not exceed 680 V at the highest input voltage and maximum output power.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch-3 has a leading edge blanking time of 170 ns to prevent premature termination of the ON-cycle.
3. Thermal check – At maximum output power, both minimum and maximum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for LinkSwitch-3, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-3, as specified in the data sheet.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.power.com

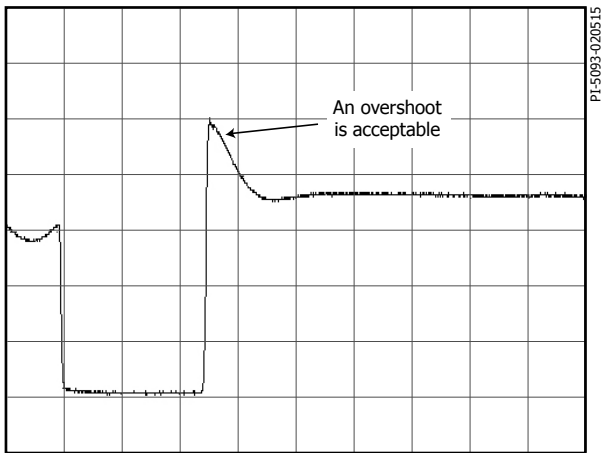


Figure 6. Desired Drain Voltage Waveform with Minimal Leakage Ringing Undershoot.

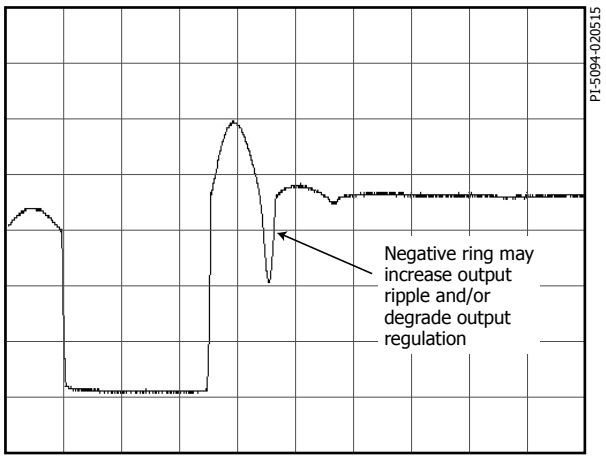


Figure 7. Undesirable Drain Voltage Waveform with Large Leakage Ring Undershoot.

Absolute Maximum Ratings[1,5]

DRAIN Voltage .....-0.3 V to 725 V
DRAIN Pin Peak Current: LNK64x4 ..... 400 (600) mA[4]
LNK64x5.....504 (750) mA[4]
LNK64x6 .....654 (980) mA[4]
LNK64x7..... 670 (1003) mA[4]
LNK64x8..... 718 (1076) mA[4]
Peak Negative Pulsed Drain Current..... -100 mA[2]
FEEDBACK Pin Voltage .....-0.3 to 9 V[6]
FEEDBACK Pin Current .....100 mA
BYPASS Pin Voltage ..... -0.3 to 9 V
BYPASS Pin Current .....10 mA
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[7]..... -40 to 150 °C
Lead Temperature .....260 °C[3]

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. Duration not to exceed 2 µs.
3. 1/16 in. from case for 5 seconds.
4. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
5. Maximum ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum ratings for extended periods of time may affect product reliability.
6. -1 V for current pulse ≤5 mA out of the pin and a duration of ≤500 ns.
7. Normally limited by internal circuitry.

Thermal Resistance

Thermal Resistance: D Package:
(θ_{JA}) .....100 °C/W[2], 80 °C/W[3]
(θ_{JC})[1] .....30 °C/W
E Package
(θ_{JA})..... 105 °C/W[4]
(θ_{JC}).....2 °C/W[5]
K Package
(θ_{JA}) .....45 °C/W[6], 38 °C/W[7]
(θ_{JC}).....2 °C/W[5]

Notes:
1. Measured on pin 8 (SOURCE) close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
3. Soldered to 1 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.
4. Free standing with no heat sink.
5. Measured at the back surface of tab.
6. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 0.36 sq. in. (232 mm²), 2 oz. (610 g/m²) copper clad.
7. Soldered (including exposed pad for K package) to typical application PCB with a heat sinking area of 1 sq. in. (645 mm²), 2 oz. (610 g/m²) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Programmable Maximum Frequency	f_{OSC}	T_J = 25 °C $t_{ON} \times I_{FB}$ = 1.4 mA-µs See Notes A, F	$V_{FB} = V_{FBth}$			85	kHz
Minimum Operation Frequency	$f_{OSC(MIN)}$	T_J = 25 °C $V_{FB} = V_{FBth}$	LNK64x4-64x6		350		Hz
			LNK64x7		760		
			LNK64x8		560		
Frequency Ratio (Constant Current)	$f_{RATIO(CC)}$	T_J = 25 °C Between V_{FB} = 1.3 V and V_{FB} = 1.9 V		1.42	1.47	1.53	
Frequency Ratio (Inductance Correction)	$f_{RATIO(IC)}$	Between $t_{ON} \times I_{FB}$ = 1.4 mA and $t_{ON} \times I_{FB}$ = 2 mA-µs		1.16	1.21	1.26	
Frequency Jitter		Peak-to-Peak Jitter Compared to Average Frequency, T_J = 25 °C			±7		%
Maximum Duty Cycle	DC_{MAX}	See Notes D, E			55		%
FEEDBACK Pin Voltage	V_{FBth}	T_J = 25 °C C_{BP} = 1 µF	LNK6404/6405/6406/6446	1.915	1.940	1.965	V
			LNK6415/6416	1.955	1.980	2.005	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions (cont.)							
FEEDBACK Pin Voltage	V_{FBth}	T_J = 25 °C C_{BP} = 1 µF	LNK6424/6425/ 6426	1.995	2.020	2.045	V
			6436	2.035	2.060	2.085	
			LNK6407, LNK6408, LNK6448	1.915	1.940	1.965	
			LNK6417, LNK6418	1.955	1.980	2.005	
			LNK6427, LNK6428	1.995	2.020	2.045	
FEEDBACK Pin Voltage at Turn-Off Threshold	$V_{FB(AR)}$			1.14	1.22	1.30	V
Minimum Switch ON-Time	$t_{ON(MIN)}$	See Note E			700		ns
FEEDBACK Pin Sampling Delay	t_{FB}	See Note G		2.55	2.75	2.95	µs
DRAIN Supply Current	I_{S1}	FB Voltage > V_{FBth} (MOSFET Not Switching			300	380	µA
	I_{S2}	Feedback Voltage = V_{FBth} -0.1 V, Switch ON-Time = t_{ON} (MOSFET Switching at f_{OSC})	LNK64x4		480	540	µA
			LNK64x5		500	560	
			LNK64x6		550	620	
			LNK64x7		600	680	
			LNK64x8		700	780	
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V	LNK64x4	-5.2	-4.4	-2.7	mA
			LNK64x5	-6.8	-5.8	-3.3	
			LNK64x6	-7.5	-6.1	-3.5	
			LNK64x7	-7.5	-6.1	-3.5	
			LNK64x8	-7.5	-6.1	-3.5	
	I_{CH2}	V_{BP} = 4 V	LNK64x4	-5	-2.8	-1.5	
			LNK64x5	-6.4	-4.0	-1.8	
			LNK64x6	-7	-4.2	-2	
			LNK64x7	-7	-4.2	-2.0	
			LNK64x8	-7	-4.2	-2.0	
BYPASS Pin Voltage	V_{BP}			5.65	5.90	6.25	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.70	0.95	1.20	V
BYPASS Pin Shunt Voltage	V_{SHUNT}			6.2	6.4	6.8	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Current Limit	I_{LIMIT}	di/dt = 60 mA/µs V_{BP} = 5.9 V T_J = 25 °C	LNK64x4	232	250	268	mA
		di/dt = 75 mA/µs V_{BP} = 5.9 V T_J = 25 °C	LNK64x5	290	315	340	
		di/dt = 95 mA/µs V_{BP} = 5.9 V T_J = 25 °C	LNK64x6	359	390	421	
		di/dt = 105 mA/µs V_{BP} = 5.9 V T_J = 25 °C	LNK64x7	390	420	449	
		di/dt = 120 mA/µs V_{BP} = 5.9 V T_J = 25 °C	LNK64x8	446	480	513	
Minimum Current Limit Scale Factor	$I_{LIMIT(MIN)}$			0.27	0.32	0.38	
Normalized Output Current	I_O	T_J = 25 °C		0.975	1.000	1.025	
Leading Edge Blanking Time	t_{LED}	T_J = 25 °C Set Note D		125	170		ns
Thermal Shutdown Temperature	t_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	t_{SDH}				60		°C
Output							
ON-State Resistance	$R_{DS(ON)}$	LNK64x4 I_D = 96 mA	T_J = 25 °C		19.7	23.7	Ω
			T_J = 100 °C		30.0	36.0	
		LNK64x5 I_D = 105 mA	T_J = 25 °C		13.2	15.8	
			T_J = 100 °C		19.8	23.8	
		LNK64x6 I_D = 105 mA	T_J = 25 °C		7.7	9.3	
			T_J = 100 °C		11.5	13.8	
		LNK64x7 I_D = 96 mA	T_J = 25 °C		4.8	5.8	
			T_J = 100 °C		7.2	8.5	
		LNK64x8 I_D = 105 mA	T_J = 25 °C		3.1	3.8	
			T_J = 100 °C		4.6	5.5	
OFF-State Leakage	I_{DSS1}	V_{DS} = 560 V T_J = 125 °C See Note C				50	µA
	I_{DSS2}	V_{DS} = 375 V T_J = 50 °C			15		

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Output (cont.)						
Breakdown Voltage	BV_{DSS}	T_J = 25 °C	725			V
DRAIN Supply Voltage			50			V
Auto-Restart ON-Time	t_{AR-ON}	See Notes A, E		300		ms
Auto-Restart OFF-Time	t_{AR-OFF}			1.5		s
Open-Loop FEEDBACK Pin Current Threshold	I_{OL}	See Note E		-90		µA
Open-Loop ON-Time		See Note E		90		µs

NOTES:

A. Auto-restart ON-time is a function of switching frequency programmed by $t_{ON} \times I_{FB}$ and minimum frequency in CC mode.

B. The current limit threshold is compensated to cancel the effect of current limit delay. As a result the output current stays constant across the input line range.

C. I_{DSS1} is the worst-case OFF-state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst-case application conditions (rectified 265 VAC) for no-load consumption calculations.

D. When the duty cycle exceeds DC_{MAX} the LinkSwitch-3 operates in on-time extension mode.

E. This parameter is derived from characterization.

F. The switching frequency is programmable between 60 kHz to 85 kHz.

G. At light load t_{FB} is reduced at 1.8 µs typical.

Typical Performance Characteristics

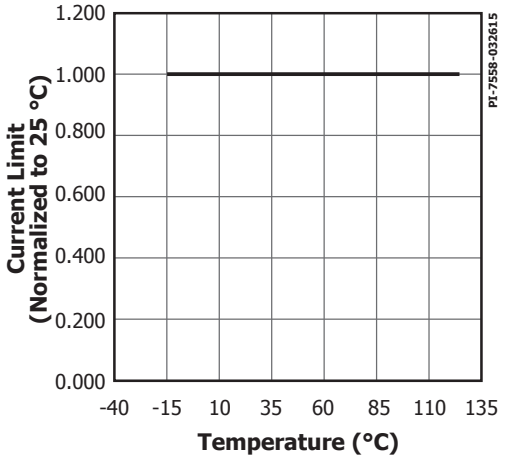


Figure 8. Current Limit vs. Temperature.

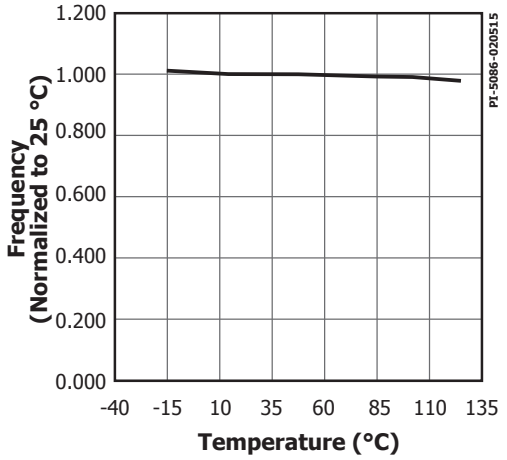


Figure 9. Output Frequency vs. Temperature.

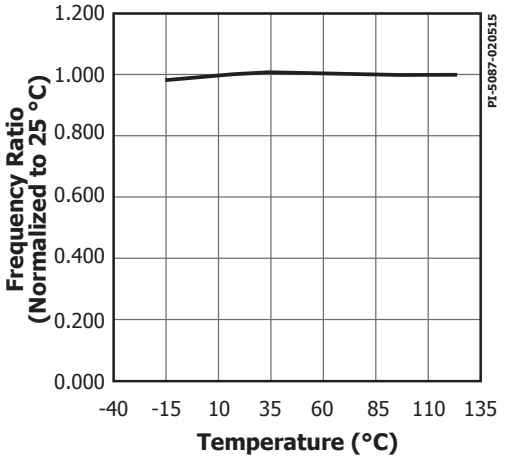


Figure 10. Frequency Ratio vs. Temperature (Constant Current).

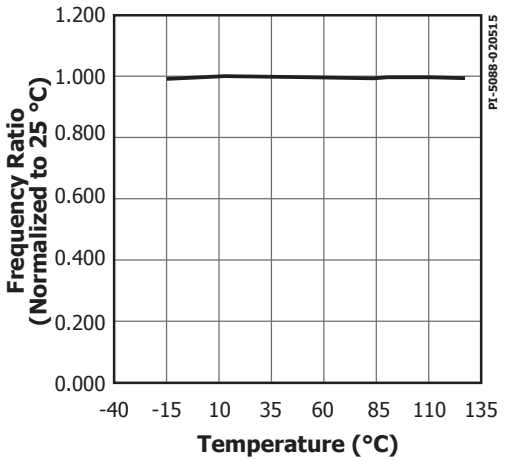


Figure 11. Frequency Ratio vs. Temperature (Inductor Current).

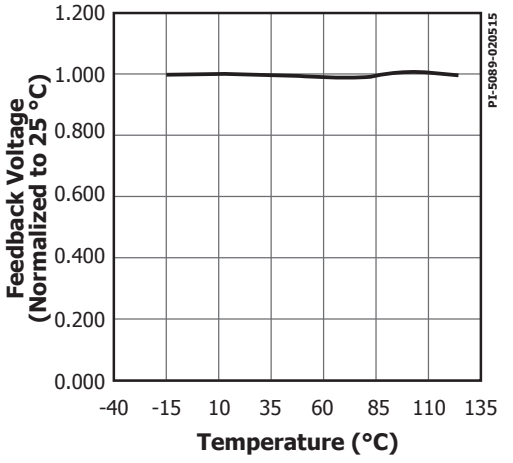


Figure 12. Feedback Voltage vs. Temperature.

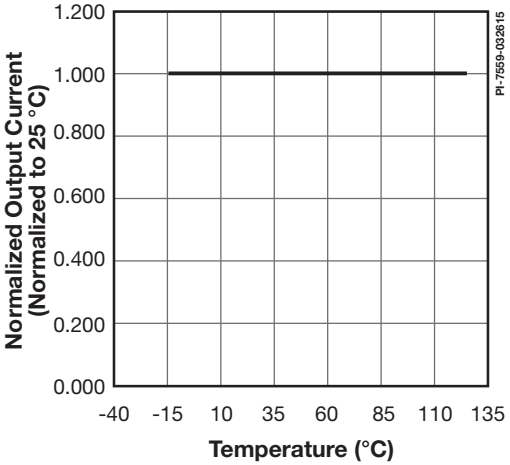


Figure 13. Normalized Output Current vs. Temperature.

Typical Performance Characteristics (cont.)

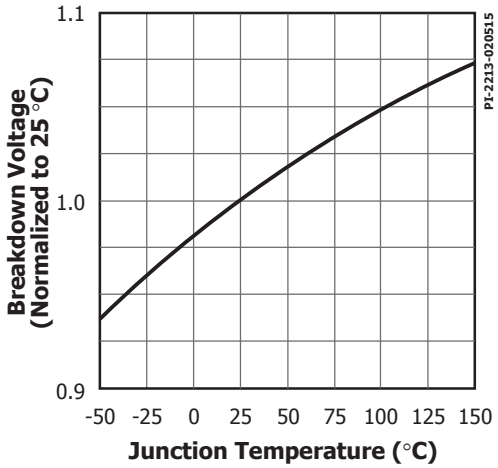


Figure 14. Breakdown vs. Temperature.

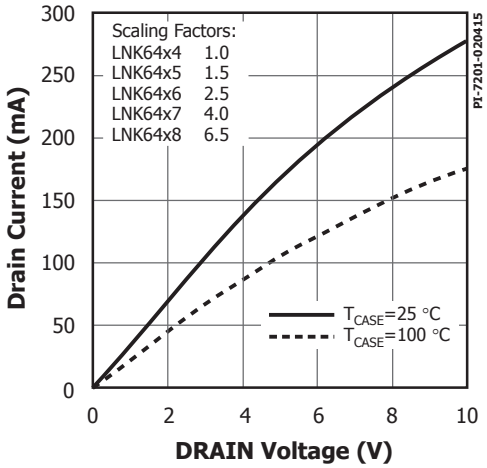


Figure 15. Output Characteristic.

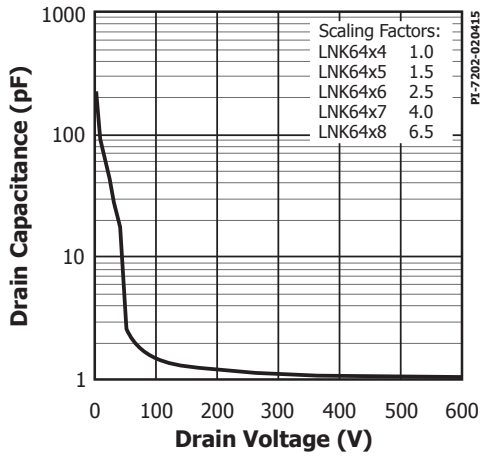


Figure 16. C_{OSS} vs. Drain Voltage.

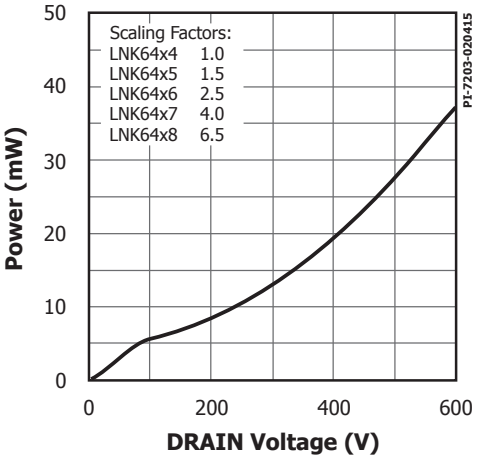
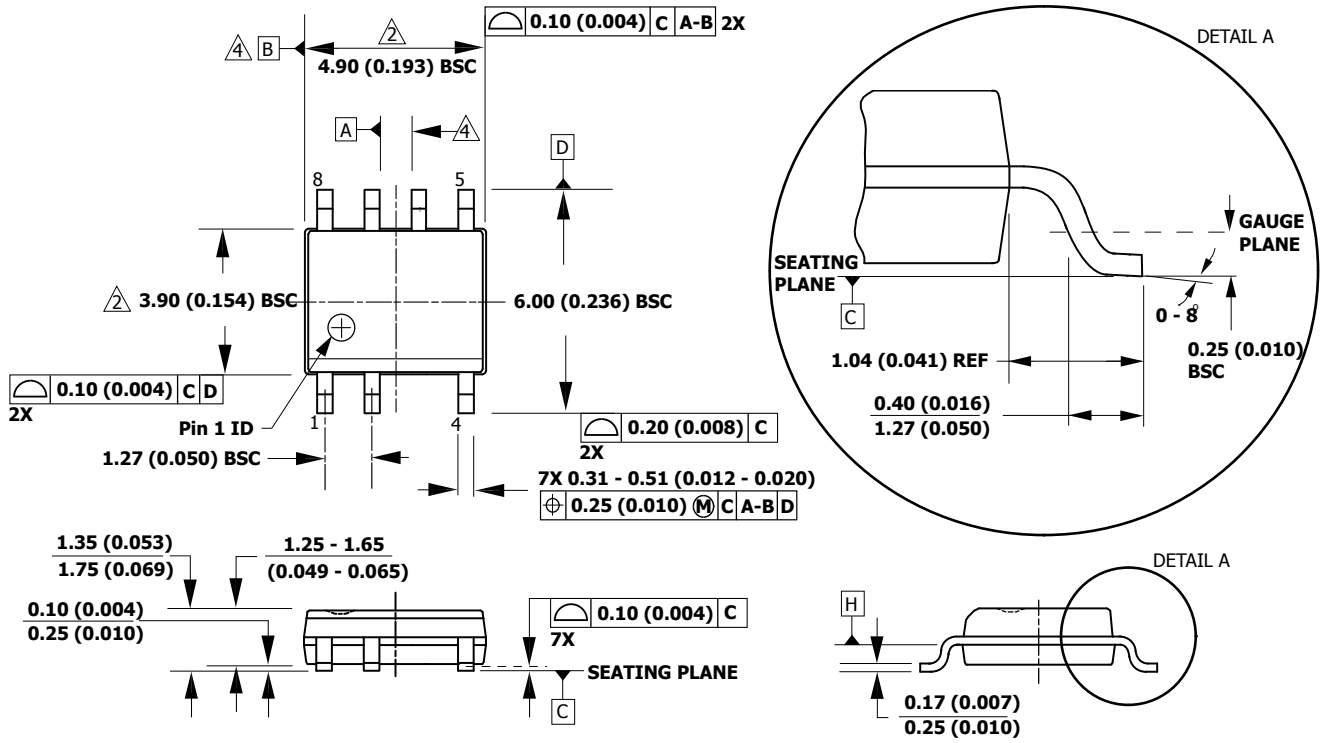


Figure 17. Drain Capacitance Power.

SO-8C (D Package)



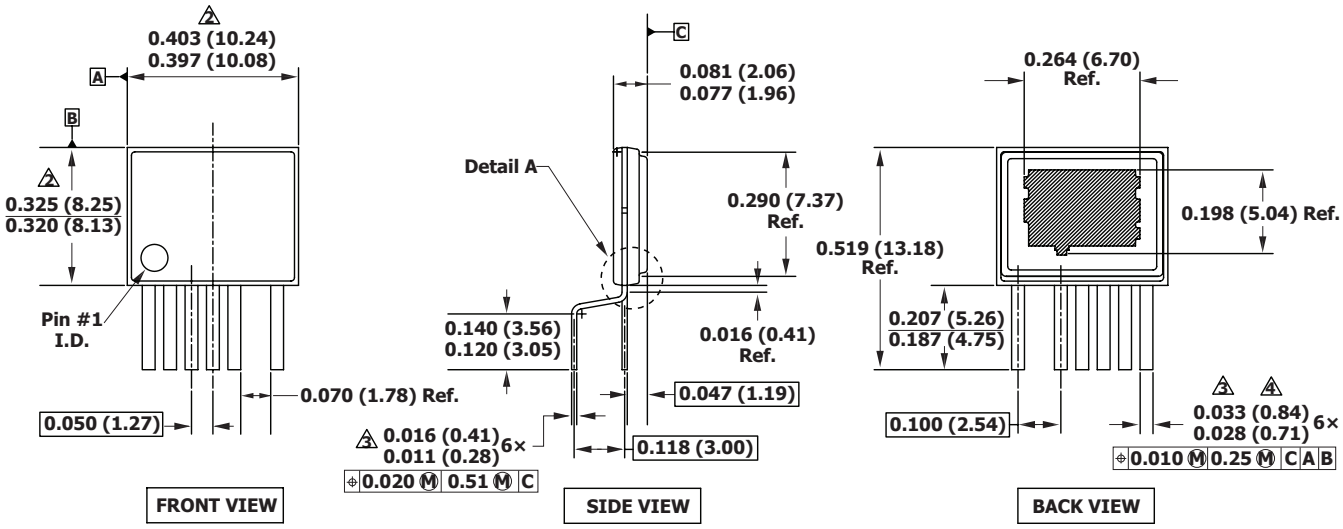
Notes:

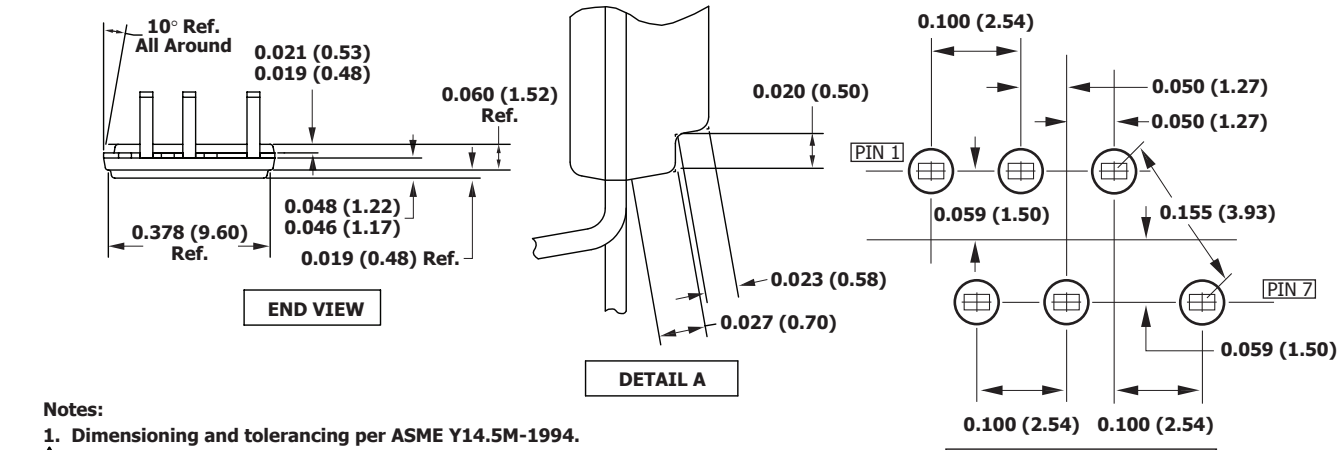
1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-012315

eSIP-7C (E Package)



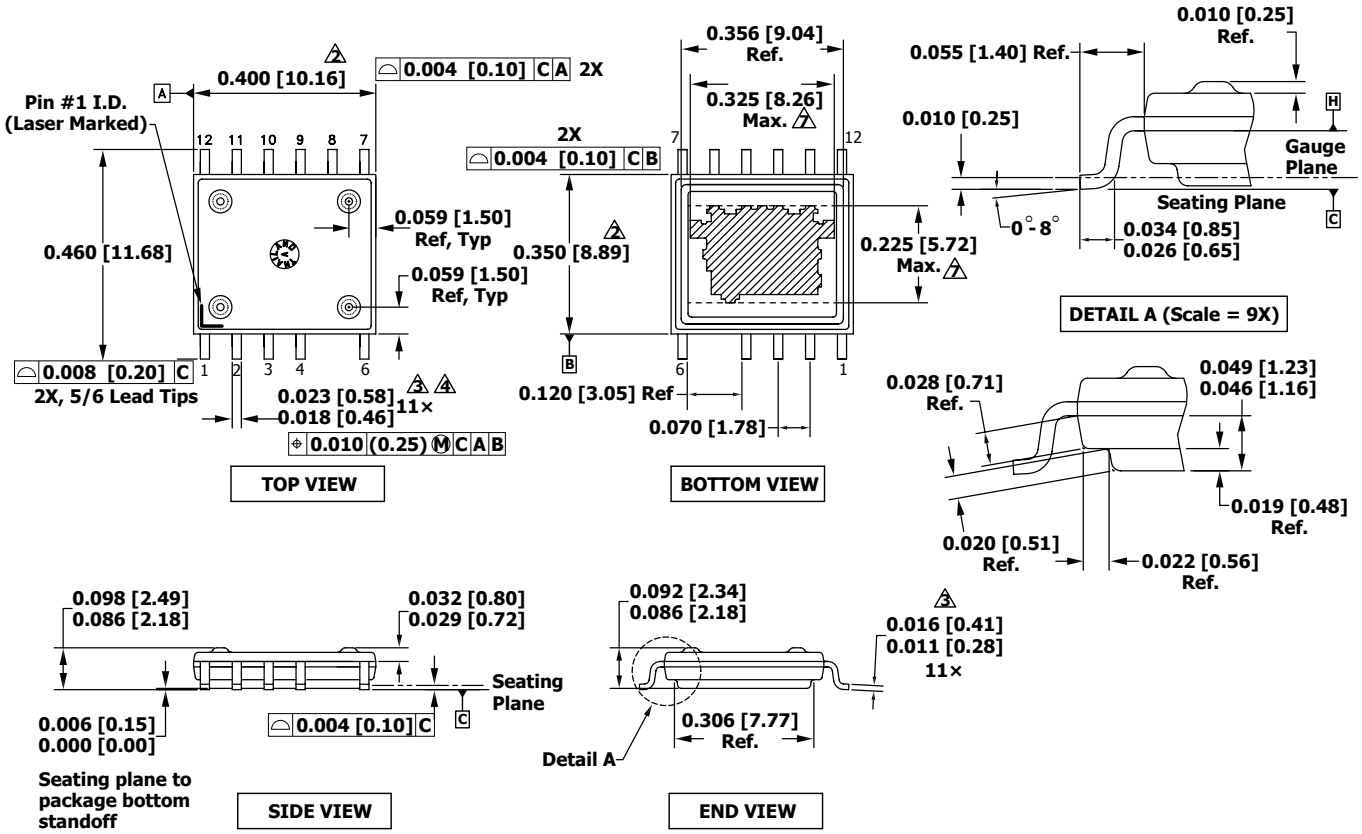


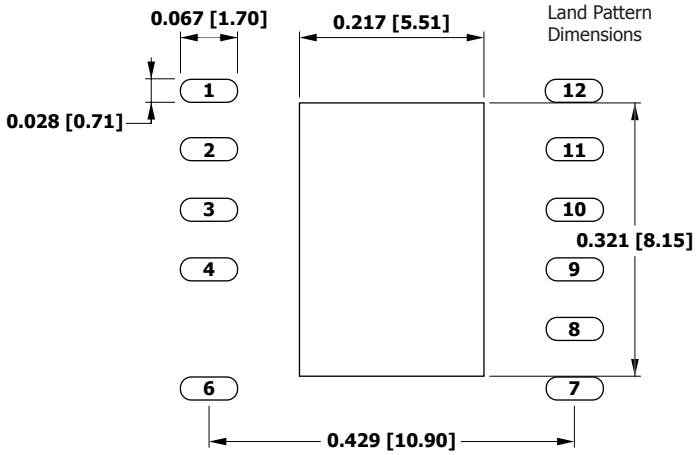
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).

PI-4917-020515

eSOP-12B (K Package)



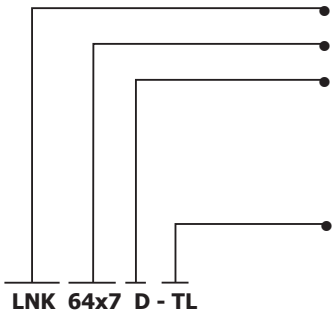


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined at Datum H.
7. Exposed pad is nominally located at the centerline of Datums A and B. "Max" dimensions noted include both size and positional tolerances.

PI-5748a-020515

Part Ordering Information



- **LinkSwitch Product Family**
- **3 Series Number**
- **Package Identifier**

D	SO-8C
E	eSIP-7C
K	eSOP-12B

- **Tape & Reel and Other Options**

Blank	Standard Configuration
TL	Tape & Reel, 2.5 k pcs for D package, 1 k pcs for K package.

Revision	Notes	Date
A	Code A.	10/16/13
A	Specified Max BYPASS Pin Current.	03/13/14
A	Code L. Updated Table 1 and Table 2.	06/11/14
B	Added LNK64x4, 64x5 and 64x6 parts. Updated $f_{RATIO(CC)}$, $I_{LIMIT(MIN)}$, t_{FB}, $V_{FB(AR)}$, $f_{OSC(MIN)}$, t_{AR-OFF} and I_{OL}. Updated ms values in Auto-Restart section on page 3. Removed $f_{OSC(AR)}$ and updated t_{AR-ON}.	03/31/15
C	Added Note G on page 11.	03/16

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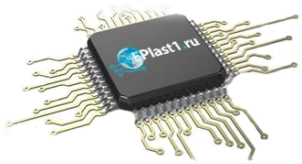

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