Introduction

This Application Note is intended to provide practical guidance in the selection of PIN Diodes for switch control circuit functions. Switches, Digital and Analog Attenuators, and Limiters each have unique functions that require proper device selection. The design difficulty lies within the parametric translation from Diode Specifications, to the circuit designers' Microwave Specifications. Diode parametric language such as Vb, Vf, Ct, Rs, τ_L, θ, must convert into Insertion Loss, VSWR, Isolation, P1dB, Input IP3, RF Operating Power, RF Power Dissipation, and D.C. Power Consumption Specification Terminology.

In addition to actual diode parameters, package parasitics play a significant role in determining switch circuit performance. Package capacitance, package inductance, package electrical resistance, and package thermal impedance are extremely important considerations to determine the effective frequency bandwidth and maximum incident power for reliable switch operation.

The manufacturing methodology dictates the type of diode selection. Surface mount assembly will mandate the usage of either plastic, HMIC SURMOUNT, or MELF & HiPAX ceramic devices. Chip and Wire (Hybrid) manufacturing will determine the usage of Cermachips, Flip Chips, or Beam Lead Devices. Schematics for the most common switch designs: Series-Exclusive, Shunt-Exclusive, and Series-Shunt are outlined below for consideration.

The Decision Making Process for PIN Diode Selection for Microwave Switch Design

The following procedure outlines and Effective Process for PIN Diode Selection for Switch Design.

1. Determine the Preferred Type of Manufacturing for the PIN Diode in the Switch Design: Surface Mount or Chip and Wire (Hybrid) Manufacturing.

2. Determine the Frequency of Operation and RF Power Handling of the Switch Design.

3. Use Table 1, "Relative Switch Performance and Design Evaluation Matrix" to determine the Type of Switch Design that Best Satisfies the Particular Switch Specifications and Requirements.

4. Use Table 2, "Relative PIN Diode Performance Evaluation Matrix" to Determine the Type of PIN Diode that Best Satisfies the Switch Design Selected from Table 1.

5. Use Table 3, "PIN Diode P/N Series Matrix" to Determine the PIN Diode P/N Series that Best Satisfies the Type of PIN Diode Selected from Table 2.

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Table 1: Relative Switch Performance and Design Evaluation Matrix

	Switch Design Configuration		
Parameter	**Series Diodes Exclusive**	**Shunt Diodes Exclusive**	**Series-Shunt Diodes**
Insertion Loss	Worst	Moderate	Best
VSWR	Moderate	Worst	Best
Isolation	Worst	Moderate	Best
P1dB	Moderate	Moderate	Moderate
Input IP3	Moderate	Moderate	Moderate
RF Incident Power	Worst	Best	Moderate
RF Power Dissipation	Worst	Best	Moderate
Switching Speed	Worst	Best	Moderate
D.C. Power Consumption	Best (Single +5 V)	Moderate (+5 V, -5 V)	Worst (+5 V, -5 V)
PIN Diode Driver Design Simplicity	Best (+5 V Only)	Moderate (+5 V, -5 V)	Moderate (+5 V, -5 V)
RF Design Simplicity	Best	Worst	Moderate
Cost	Best	Moderate	Moderate
Overall Evaluation	34 Points	38 Points	40 Points

Notes:

1. Evaluation based upon following grading : Best = 5 Points, Moderate = 3 Points, Worst = 1 Point. The higher the score, the better the overall relative design advantage.
2. Where there is No significant relative advantage, a “ Moderate ” weighting can be used.

Assumptions for SP2T Design:

1. Design is a Reflective SP2T.
2. (2) Diodes are used per RF port.
3. Frequency Bandwidth is 3.0 : 1 maximum.

Conclusions:

The Series-Shunt Design is the Best in terms of Overall Switch Performance and value. Since each Design has a specific advantage, the decision for a Switch Design Selection is determined by the Specific Design Priorities for the requirement.

Table 2: Relative PIN Diode Performance Evaluation Matrix

	Surface Mount Assembly			Chip & Wire Hybrid Assembly		
Key Parameter	**Plastic**	**MELF or Hi-Pax**	**SURMOUNT**	**Cerma Chip**	**Flip Chip**	**Beam Lead**
1 MHz < F < 1 GHz		Best Selection				
100 MHz < F < 4 GHz	Best Selection					
4 GHz < F < 20 GHz			Best Selection			
20 GHz < F < 60 GHz					Best Selection	Best Selection
100 MHz < F < 20 GHz				Best Selection		
Pinc < 0.1 W						Best Selection
0.1 W < Pinc < 1 W	Best Selection				Best Selection	
1 W < Pinc < 20 W			Best Selection			
20 W < Pinc < 200 W		Best Selection		Best Selection		
Relative Cost Index	Lowest	Moderate/Highest	Moderate/Highest	Lowest	Moderate	Highest

Conclusions:

1. **Plastic Devices** are best suited where **Cost** is a decision driver, the Operating Frequency < 4 GHz, and the RF C.W. Incident Power < 1 W (+ 30 dBm).
2. **MELF or HIPAX Ceramic Devices** are best utilized where **Highest Average Powe**r (> 20 W C.W.) is the Primary Design Goal and the Operating Frequency < 1 GHz.
3. **SURMOUNT Devices** are probably the **Best Overall Compromise** in Device Selection. They can Operate (In Various bands) from 10 MHz – 20 GHz and Perform well with RF Incident Power < 20 W C.W (+ 43 dBm).
4. **Cermachip Devices** provide the **Best Overall Performance** for Operating Frequeny (100 MHz – 20 GHz) , and RF Incident Power < 200 W C.W (+ 53 dBm).
5. **Flip Chip Devices** are best suited for **mmwave Frequencies** < 60 GHz, where the RF Incident C.W. < 1W (+ 30 dBm) and Conductive Epoxy or Soldering is Required.
6. **Beam Lead Devices** are best suited for **mmwave Frequencies** < 60 GHz, where the RF Incident C.W. < 0.1W (+ 20 dBm) and Thermo Compression Bonding is Required.

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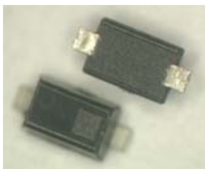
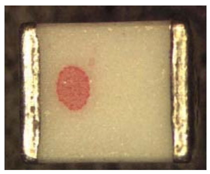
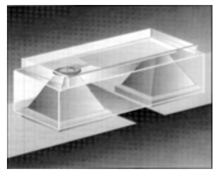
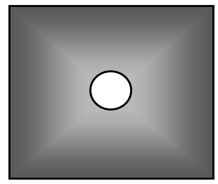
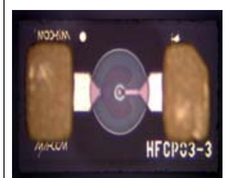
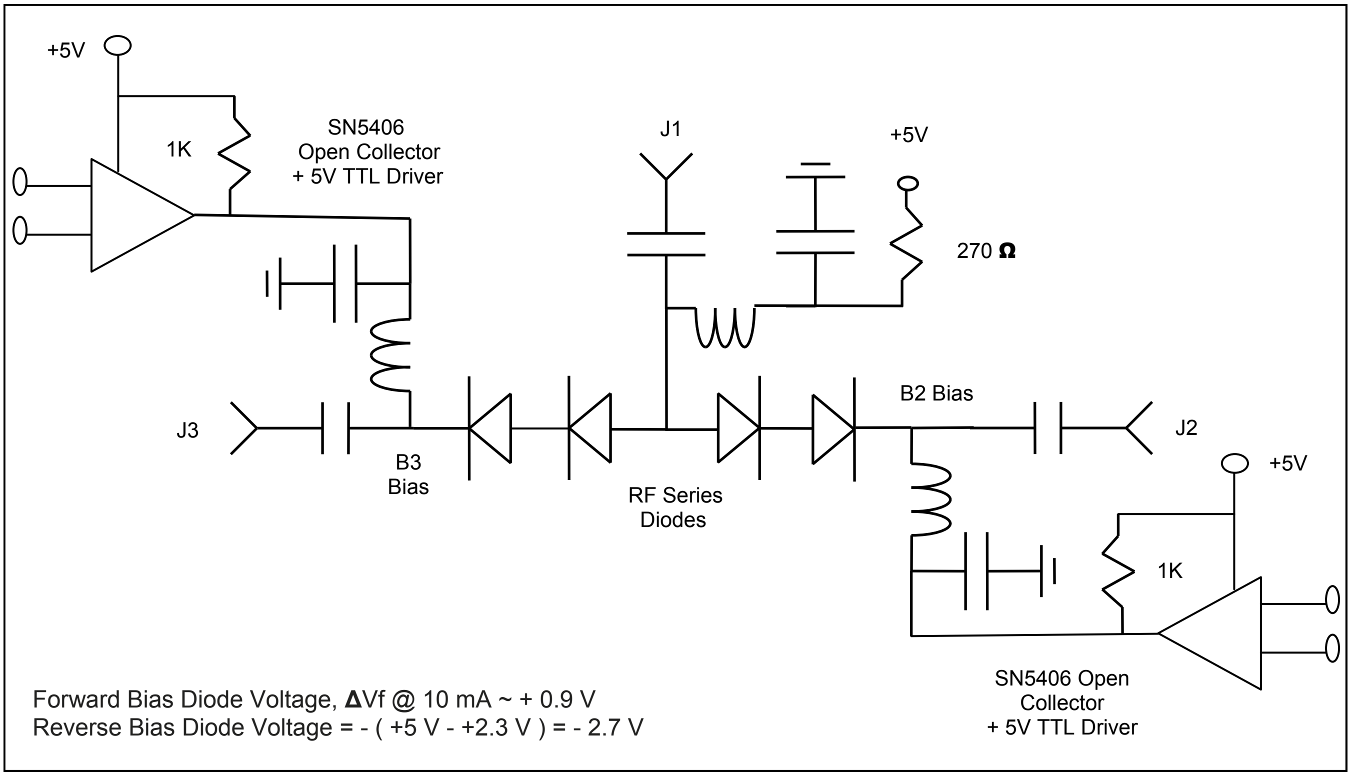
Table 3: PIN Diode Part Number Series Matrix

Plastic PIN Diodes	MELF & HiPax PIN Diodes	SURMOUNT PIN Diodes	Cermachip PIN Diodes	Flip Chip PIN Diodes	Beam Lead PIN Diodes
					
Part Numbers: MA4P275 Series MA4P282 Series MA4P789 Series MA4P274 Series	Part Numbers: MA4P1250 MA4P1450 MA4P4000 Series MA4P4300 Series MA4P7000 Series MA4P7100 Series MA4PH23X Series	Part Numbers: MA4SPS Series MADP-042XXX Series	Part Numbers: MA4P102 MA4P202, 203 MA4P303 MA4P404 MA4P504 MA4P505 MA4P604 MA4P606 MA4PK2000, 3000	Part Numbers: MA4FPC Series MA4AGFCP Series MA4AGSBP Series	Part Numbers: MA4PBL Series MA4AGBLP Series

Notes:

1. The following M/A-COM PIN Diode Drivers Operating with +5 V & -5 V D.C. Power Supplies are Practical with Many PIN Diode Switch Designs: DR65 Series, MADRMA0001 and MADRMA0002 Series.
2. M/A-COM Website Homepage Hyperlink Address: http://www.macom.com

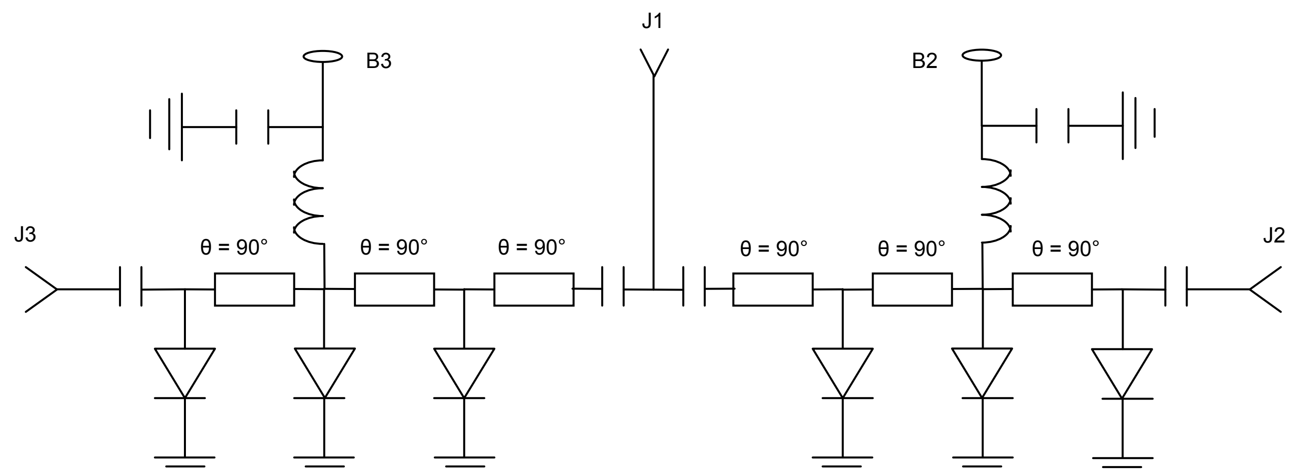
Schematic 1: SP2T Series Exclusive PIN Diode Switch, 40 dB Isolation with +5 V Supply



Schematic 1: D.C. Bias to RF Truth Table

RF State	B2 Bias	B3 Bias
Low Loss J1-J2 & Isolation J1-J3	+0.5 V @ 10 mA	+5 V @ 0 mA
Low Loss J1-J3 & Isolation J1-J2	+5 V @ 0 mA	+0.5 V @ 10 mA

Schematic 2: SP2T All Shunt, 60 dB Isolation Design with 90° Transformer using Distributed Transmission Line

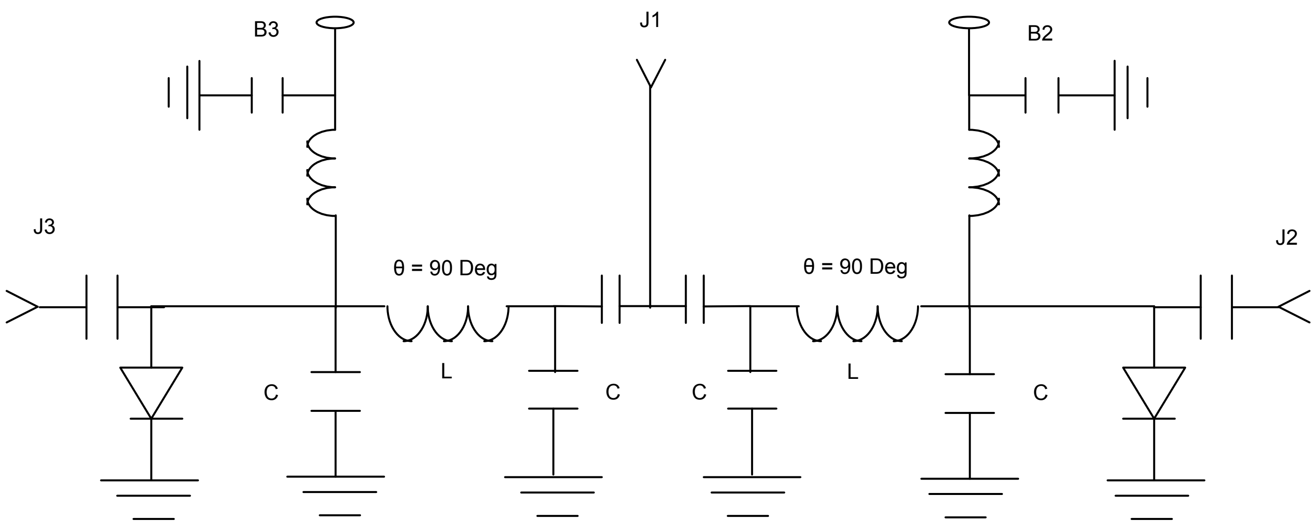


$\theta = 90° = \beta * L = (2\pi / \lambda) * L$, $L = \lambda/4 = [\, 11.807 / (\varepsilon_{eff}^{1/2} * F_o * 4)\,]$ inches.
$F_o = (F_{min} * F_{max})^{1/2}$ is in GHz, εeff is Effective Dielectric Constant of Transmission Line Medium and Air.

Schematic 2: D.C. Bias to RF Truth Table

RF State	B2 Bias	B3 Bias
Low Loss J1-J2 & Isolation J1-J3	-V @ 0 mA	+1 V @ (+20 mA per Diode)
Low Loss J1-J3 & Isolation J1-J2	+1 V @ (+20 mA per Diode)	-V @ 0 mA

Schematic 3: SP2T All Shunt, 30 dB Isolation Design using π, C-L-C Lumped Element 90° Transformer



$$L = Zo / (2\pi * Fo)$$

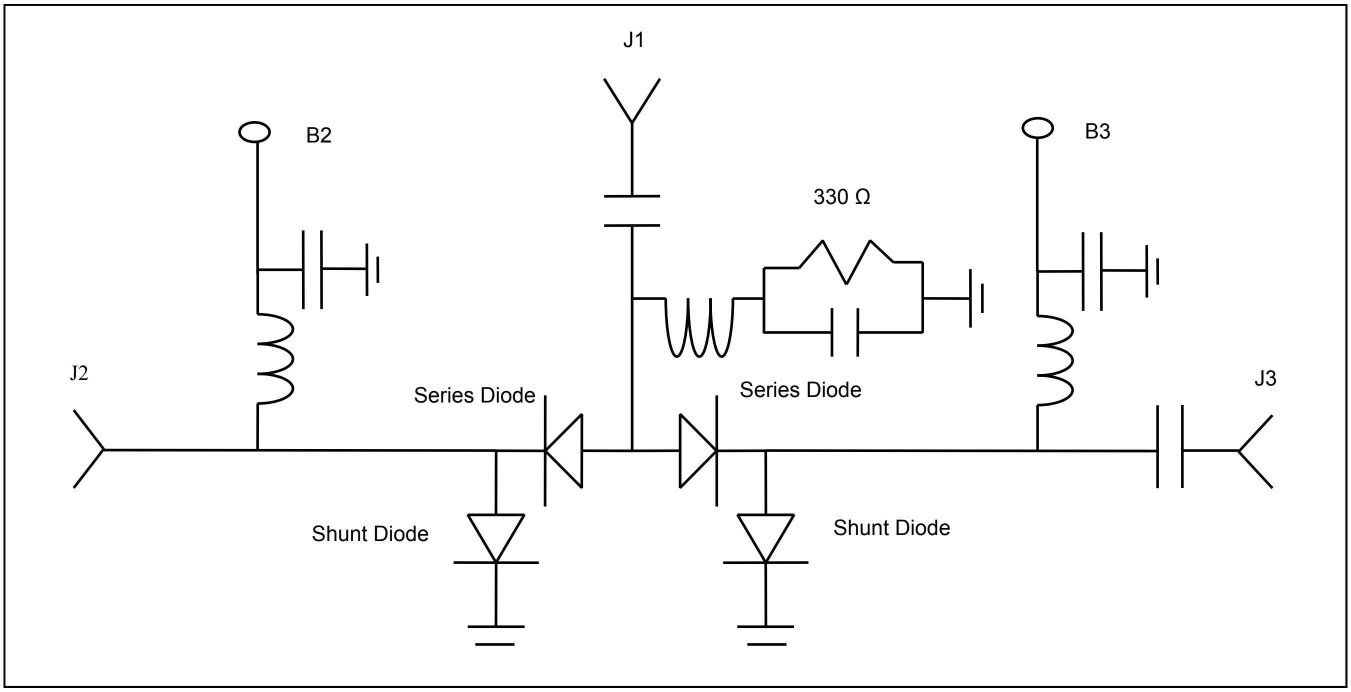
$$C = 1 / (2\pi * Fo * Zo)$$

$$Fo = (Fmin * Fmax)^{1/2}$$

Schematic 3: D.C. Bias to RF Truth Table

RF State	B2 Bias	B3 Bias
Low Loss J1-J2 & Isolation J1-J3	-V @ 0 mA	+1 V @ +20 mA
Low Loss J1-J3 & Isolation J1-J2	+1 V @ +20 mA	-V @ 0 mA

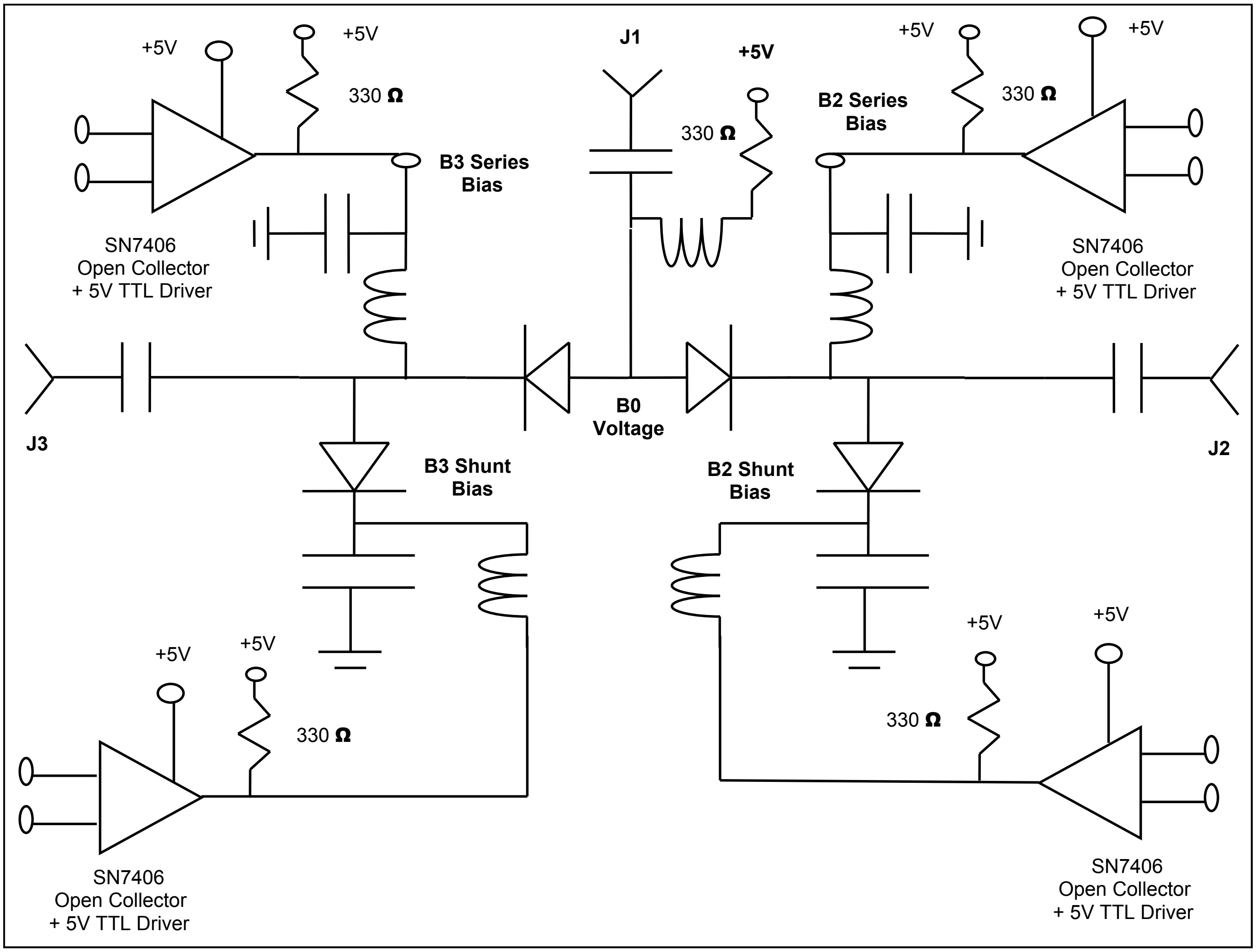
Schematic 4: SP2T Series-Shunt, 40 dB Isolation Design with Positive & Negative Bias Current



Schematic 4: D.C. Bias to RF Truth Table

RF State	B2 Bias	B3 Bias
Low Loss J1-J2 & Isolation J1-J3	-4 V @ 10 mA	+1 V @ +10 mA
Low Loss J1-J3 & Isolation J1-J2	+1 V @ +10 mA	-4 V @ -10 mA

Schematic 5: SP2T Series-Shunt, 40 dB Isolation Design with +5 V Supply



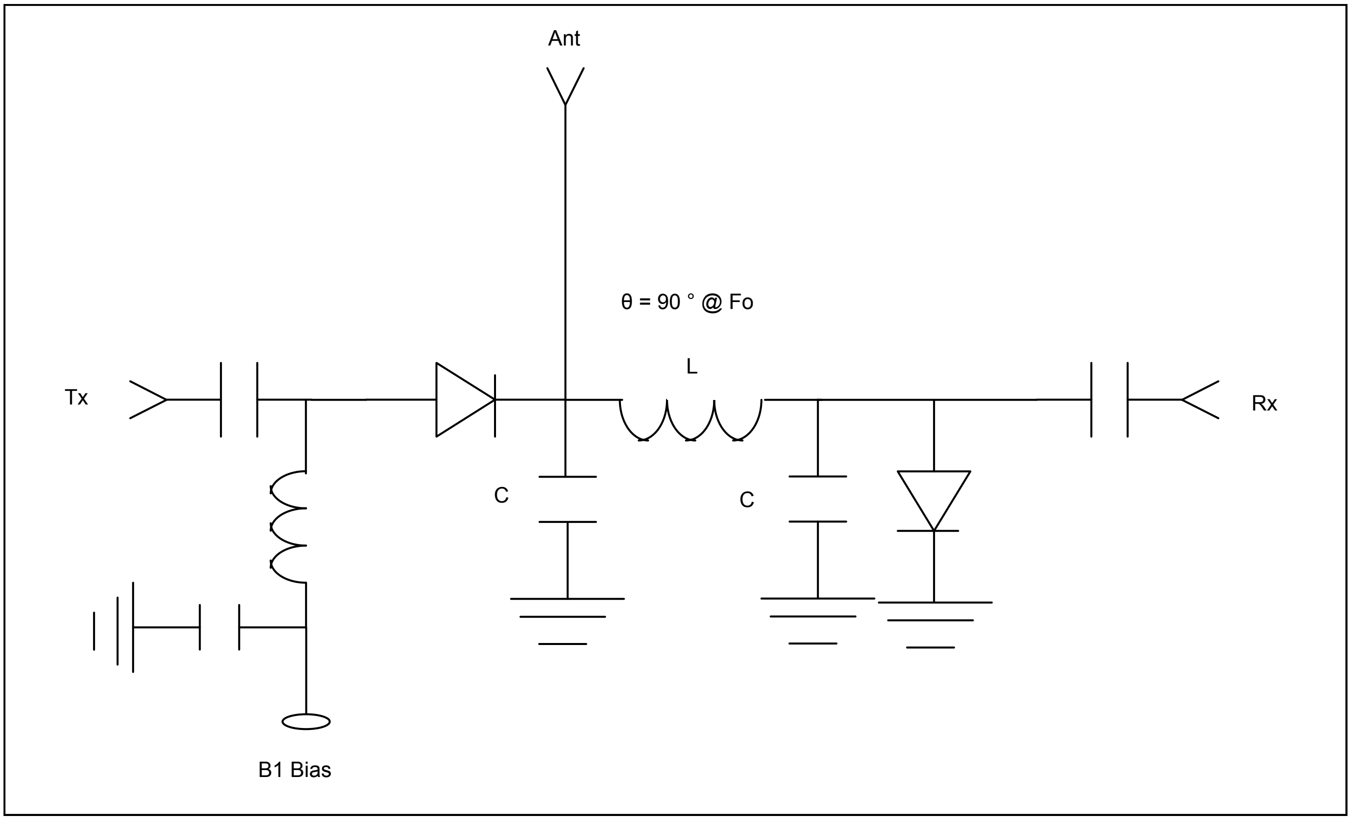
Schematic 5: D.C. Bias to RF Truth Table

RF State	B2 Series Bias	B2 Shunt Bias	B3 Series Bias	B3 Shunt Bias	B0 Voltage
J1-J2 Low Loss & J1-J3 Isolation	+0.5 V @ 11 mA	+5 V @ 0 mA	+1.4 V @ +11 mA (To J3 Shunt Diode)	+0.5 V @ +11 mA	+1.4 V
J1-J3 Low Loss & J1-J2 Isolation	+1.4 V @ +11 mA (To J2 Shunt Diode)	+0.5 V @ +11 mA	+0.5 V @ +10 mA	+5 V @ 0 mA	+1.4 V

Notes:

1. Forward Bias Diode ΔVf @ 10 mA ~ +0.9 V
2. Reverse Bias Series Diode = (+1.4 V - +1.4 V) = 0 V
3. Reverse Bias Shunt Diode = (+0.5 V - +5.0 V) = -4.5 V

Schematic 6: TR Switch Schematic with 25 dB Isolation Design with +3 V Supply



Schematic 6: TR Switch D.C. Bias to RF Truth Table

RF State	B1 Bias
Low Loss Tx - Ant & Isolation Rx - Tx	+2 V @ +10 mA
Low Loss Ant - Rx & Isolation Tx - Rx	0 V @ 0 mA

For Lumped Electrical Transmission Line Length, θ, between Junction and Rx Shunt Diode :

L = Zo/ (2π Fo) , C = 1/ (2π Fo Zo) , Where Fo is the Resonant Frequency = $(F_1 * F_2)^{½}$ & F_1 & F_2 are Band Edge Frequencies.

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