TEXAS INSTRUMENTS

CSD15380F3

SLPS579 – MAY 2016

CSD15380F3 20-V N-Channel FemtoFET™ MOSFET

1 Features

- Ultra-Low C_{iss} and C_{oss}
- Ultra-Low Q_g and Q_{gd}
- Ultra-Small Footprint
  - 0.73 mm × 0.64 mm
- Ultra-Low Profile
  - 0.35-mm Max Height
- Integrated ESD Protection Diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and Halogen Free
- RoHS Compliant

2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

3 Description

This 20-V, 990-mΩ, N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. Ultra-low capacitance improves switching speeds. When used in data line applications, the low capacitance minimizes noise coupling. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	20		V
Q_g	Gate Charge Total (4.5 V)	0.216		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.027		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5 V	2220	mΩ
		V_{GS} = 4.5 V	1170	mΩ
		V_{GS} = 8 V	990	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

Ordering Information(1)

Device	Qty	Media	Package	Ship
CSD15380F3	3000	7-Inch Reel	Femto 0.73-mm × 0.64-mm Land Grid Array (LGA)	Tape and Reel
CSD15380F3T	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

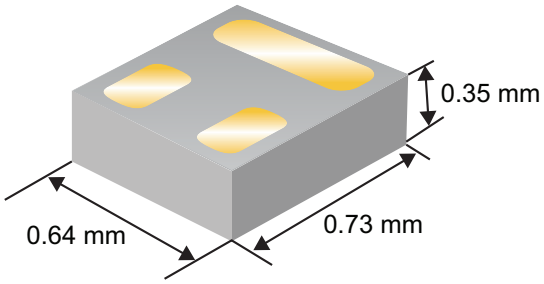
Absolute Maximum Ratings

T_A = 25°C (unless otherwise stated)		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	10	V
I_D	Continuous Drain Current(1)	0.5	A
I_{DM}	Pulsed Drain Current(2)	1.6	A
P_D	Power Dissipation(1)	500	mW
$V_{(ESD)}$	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature	–55 to 150	°C

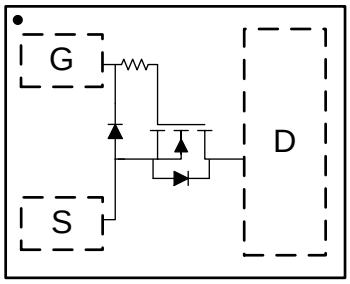
(1) Typical $R_{\theta JA}$ = 255°C/W on 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.

Typical Part Dimensions



Top View



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4 Revision History

DATE	REVISION	NOTES
May 2016	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	20			V
I_{DSS}	Drain-to-Source leakage current	V_{GS} = 0 V, V_{DS} = 16 V			50	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 10 V			25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 2.5 µA	0.85	1.10	1.35	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 0.1 A		2220	4000	mΩ
		V_{GS} = 4.5 V, I_{DS} = 0.1 A		1170	1460	mΩ
		V_{GS} = 8 V, I_{DS} = 0.1 A		990	1190	mΩ
g_{fs}	Transconductance	V_{DS} = 2 V, I_{DS} = 0.1 A		0.64		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 10 V, f = 1 MHz		8.1	10.5	pF
C_{oss}	Output capacitance			5.9	7.7	pF
C_{rss}	Reverse transfer capacitance			0.13	0.17	pF
R_G	Series gate resistance			9.6		Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 10 V, I_{DS} = 0.1 A		0.216	0.281	nC
Q_{gd}	Gate charge gate-to-drain			0.027		nC
Q_{gs}	Gate charge gate-to-source			0.077		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.048		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{DS} = 0.1 A, R_G = 0 Ω		3		ns
t_r	Rise time			1		ns
$t_{d(off)}$	Turn off delay time			7		ns
t_f	Fall time			7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 0.1 A, V_{GS} = 0 V		0.85	1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	90	°C/W
	Junction-to-ambient thermal resistance(2)	255	°C/W

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

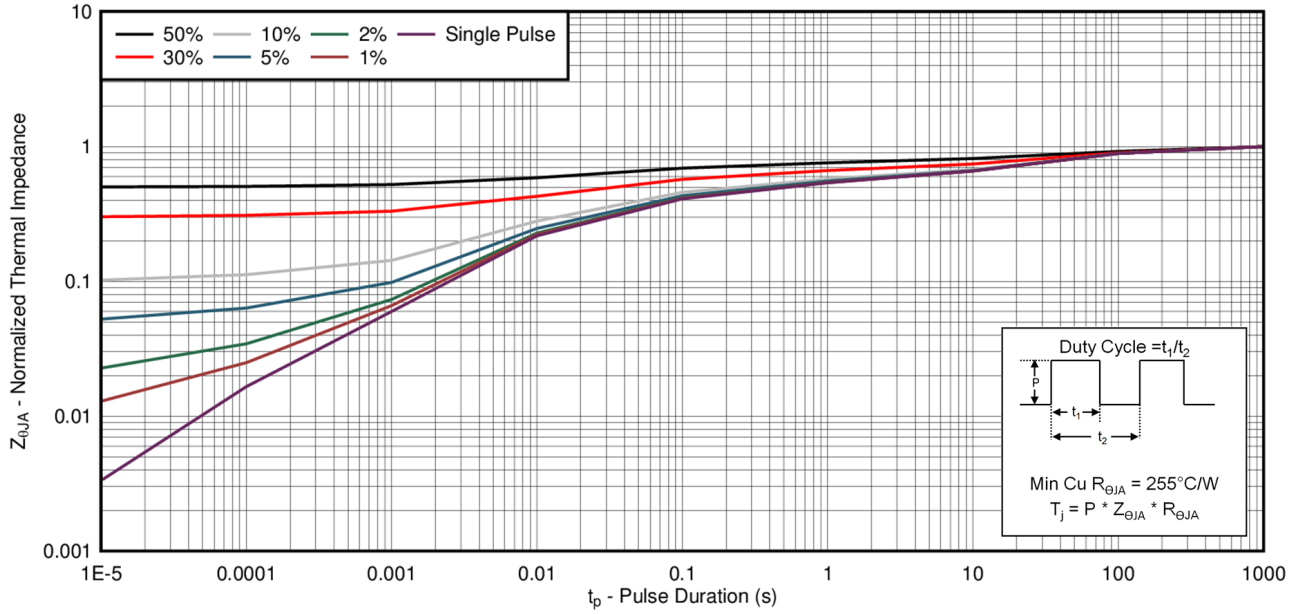

Figure 1. Transient Thermal Impedance

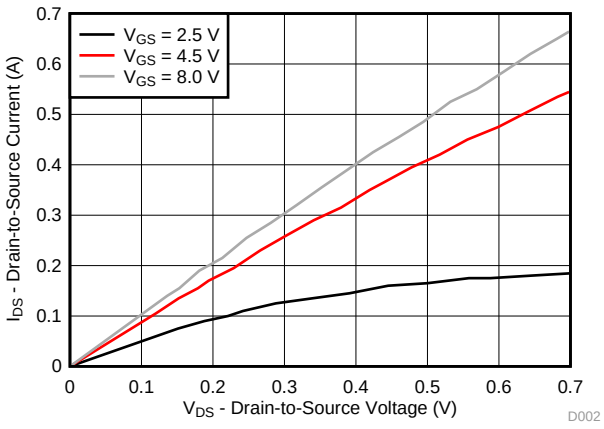

Figure 2. Saturation Characteristics

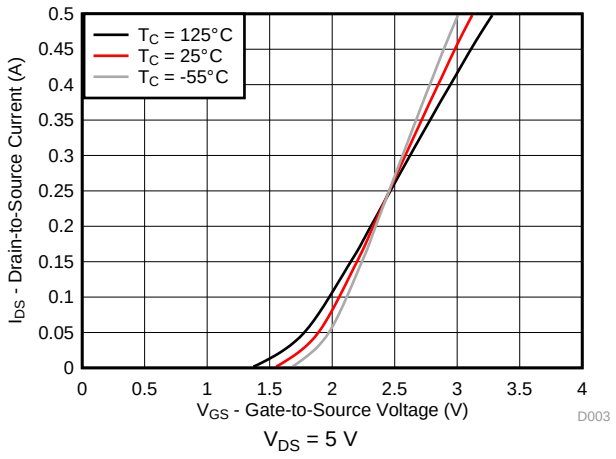

Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

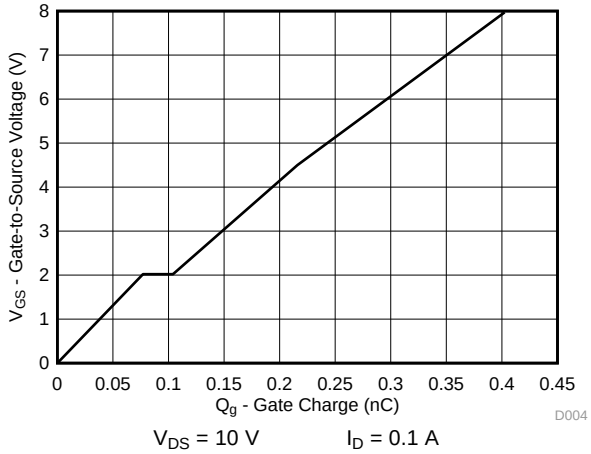

Figure 4. Gate Charge

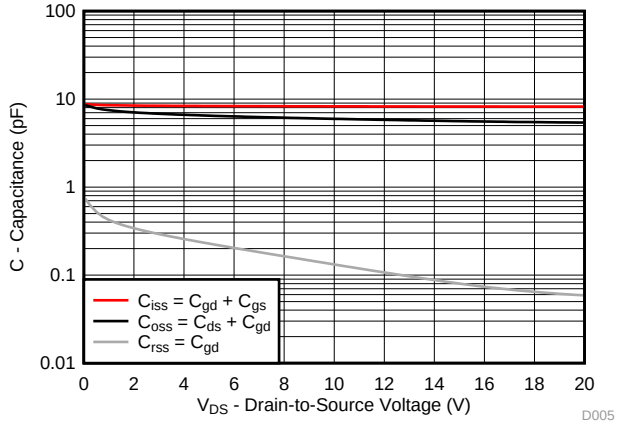

Figure 5. Capacitance

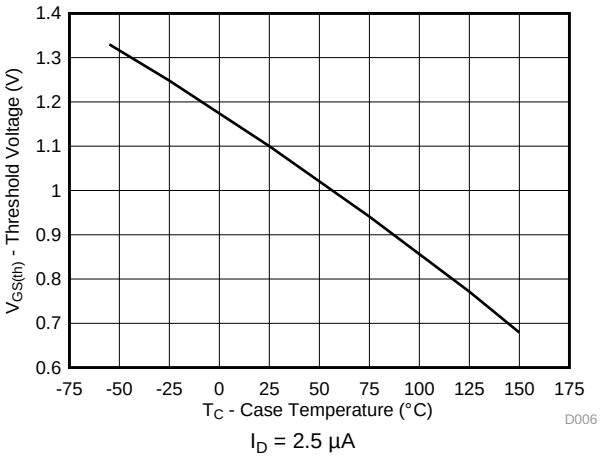

Figure 6. Threshold Voltage vs Temperature

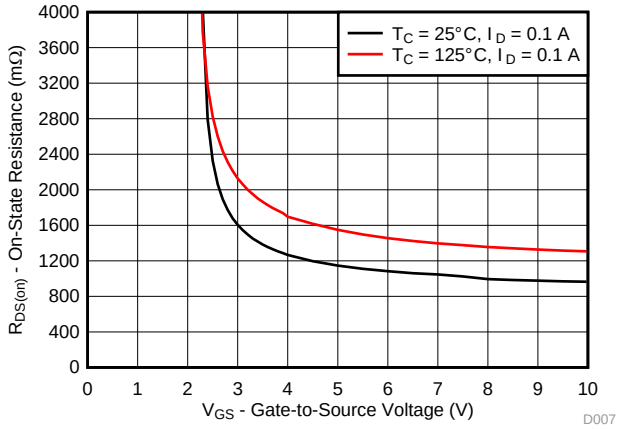

Figure 7. On-State Resistance vs Gate-to-Source Voltage

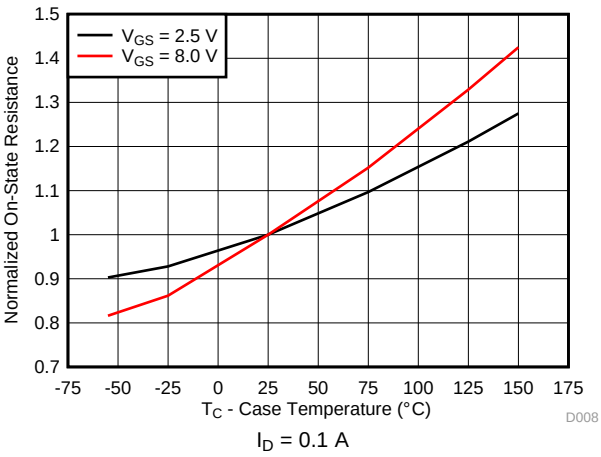

Figure 8. Normalized On-State Resistance vs Temperature

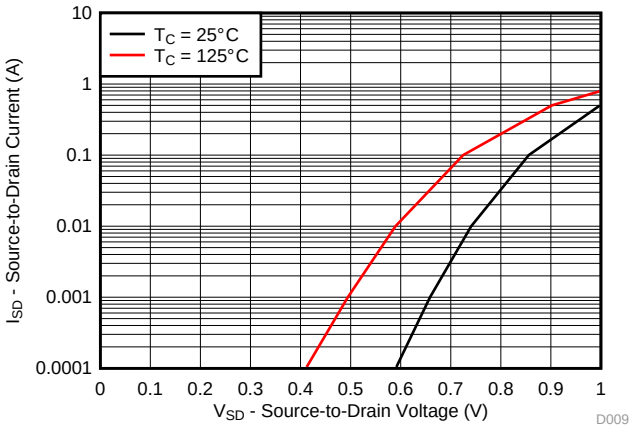

Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

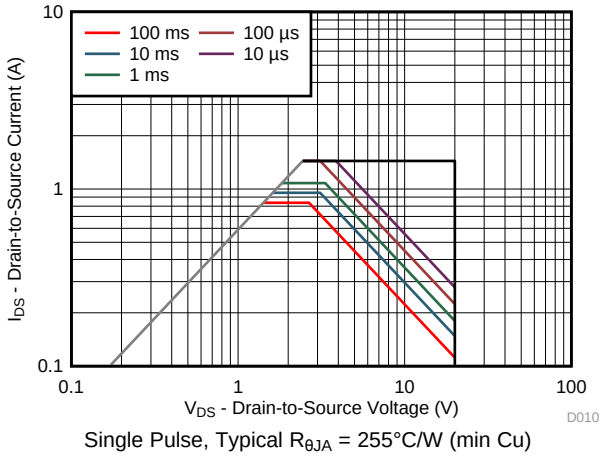

Figure 10. Maximum Safe Operating Area

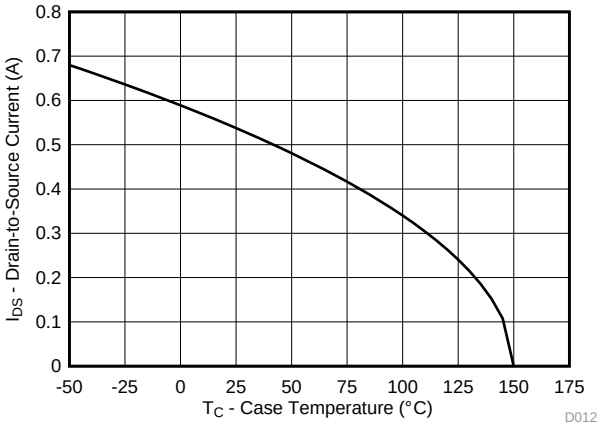

Figure 11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

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6.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

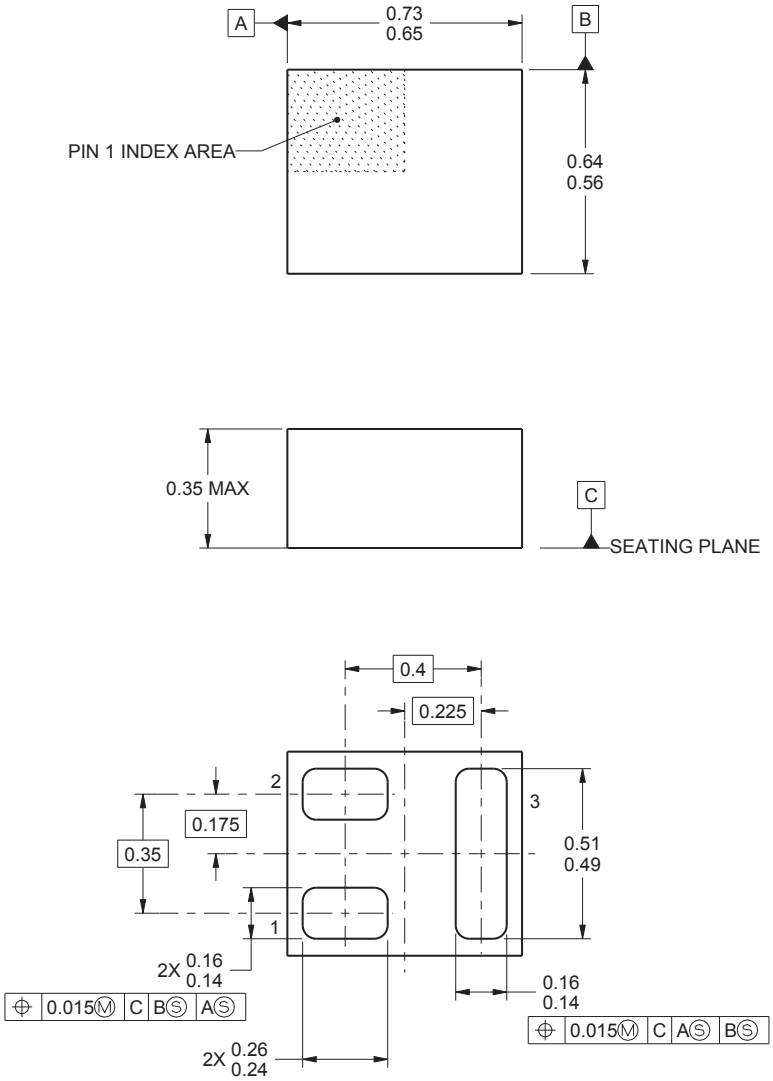
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



(1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).

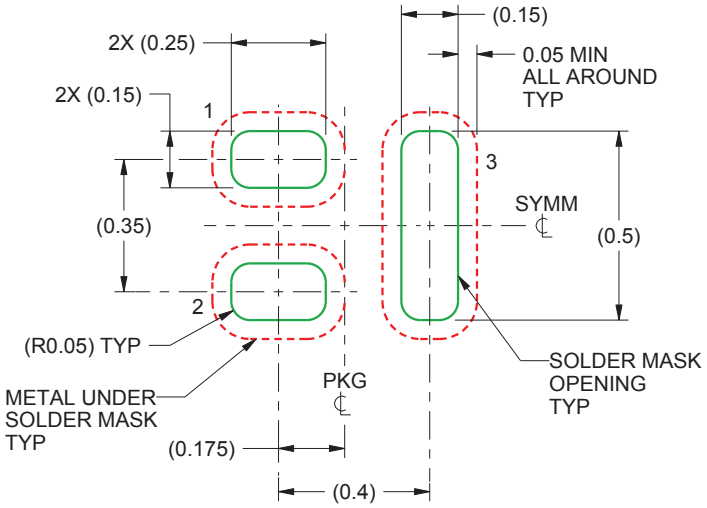
(2) This drawing is subject to change without notice.

(3) This package is a PB-free solder land design.

Pin Configuration

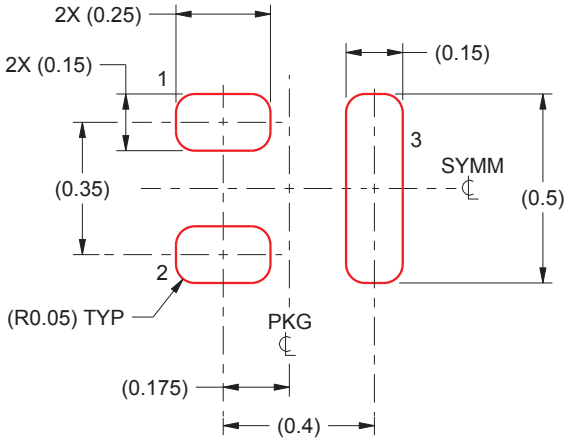
Position	Designation
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD15380F3	ACTIVE	PICOSTAR	YJM	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	6	Samples
CSD15380F3T	ACTIVE	PICOSTAR	YJM	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

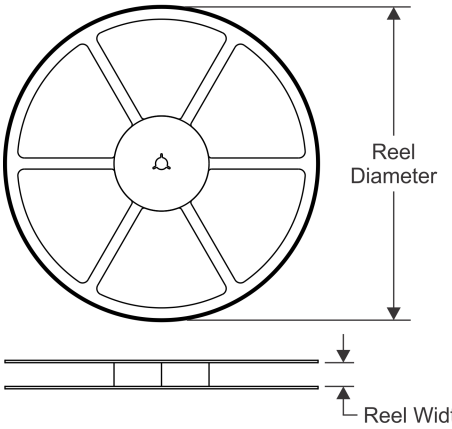
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

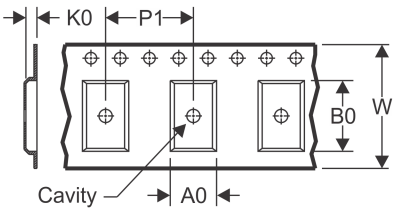
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

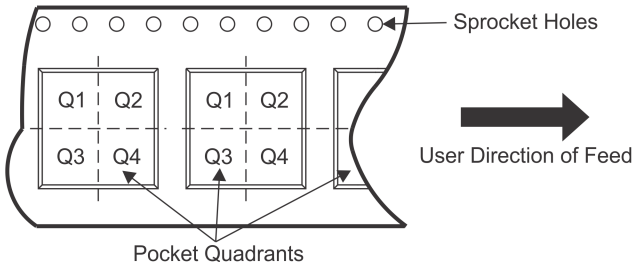


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

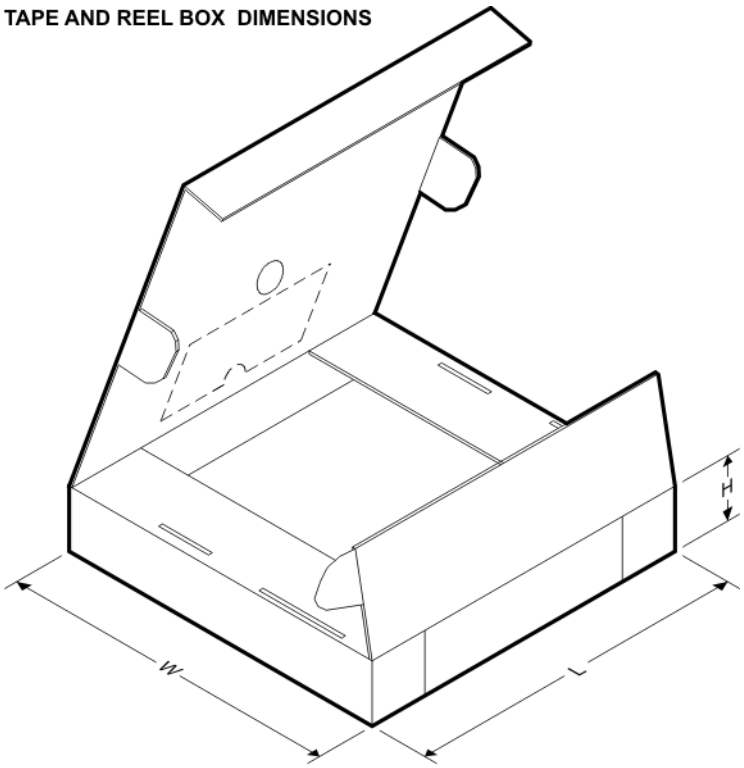
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD15380F3	PICOSTAR	YJM	3	3000	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD15380F3	PICOSTAR	YJM	3	3000	180.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2
CSD15380F3T	PICOSTAR	YJM	3	250	178.0	8.4	0.7	0.79	0.44	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD15380F3	PICOSTAR	YJM	3	3000	220.0	220.0	35.0
CSD15380F3	PICOSTAR	YJM	3	3000	182.0	182.0	20.0
CSD15380F3T	PICOSTAR	YJM	3	250	220.0	220.0	35.0

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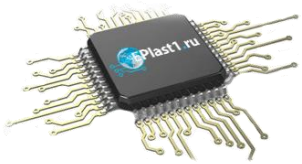
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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