



THCV242

SerDes receiver with bi-directional transceiver

1. General Description

THCV242 is designed to support 1080p60 2Mpixel uncompressed video data over 15m 100ohm differential STP or single-end 50ohm Coaxial cable with 4 in-line connectors between camera and processor by V-by-One® HS.

THCV242 supports a MIPI CSI-2. Each CSI-2 data lane can transmit up to 1.2Gbps/lane. Virtual channel is supported. MIPI 2nd port output supports data copy and distribution.

One high-speed V-by-One® HS lane can transmit up to 1080p60fps. The maximum serial data rate is 4Gbps/lane. 2nd input lane supports HDR large amount of data or camera switch experience.

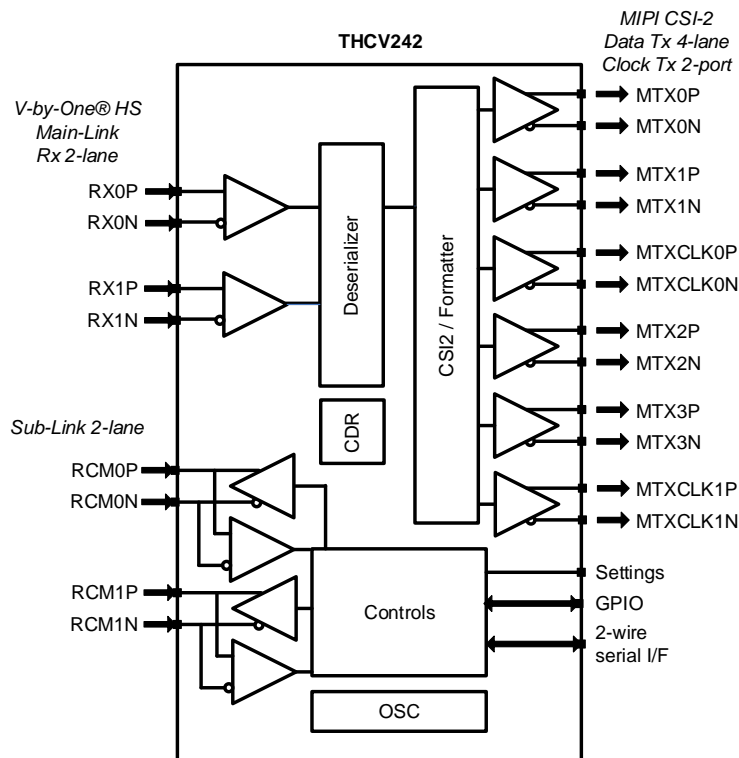
THCV242 is capable to control and monitor remote camera module from MPU via GPIO or 1Mbps 2-wire serial interface.

Several fault and error detection function including CRC provides hardware functional safety design.

2. Features

- MIPI CSI-2 with 1,2 or 4-lane output
- MIPI D-PHY supports 80Mbps~1.2Gbps
- MIPI Virtual channel supported
- Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, User-defined generic 8-bit
- V-by-One® HS 400Mbps~4Gbps x2lane
- V-by-One® HS standard version1.5
- Video stream switch and copy/distribution
- Frame sync remote supply scheme for multiple camera stream synchronization
- Wide range IO voltage from 1.7V to 3.6V
- 2-wire serial interface 1Mbps bridge function
- Remote GPIO/UART control and monitoring
- Error detection including CRC and notification
- QFN64 9x9mm 0.5mm pitch Exp-pad package

3. Block Diagram



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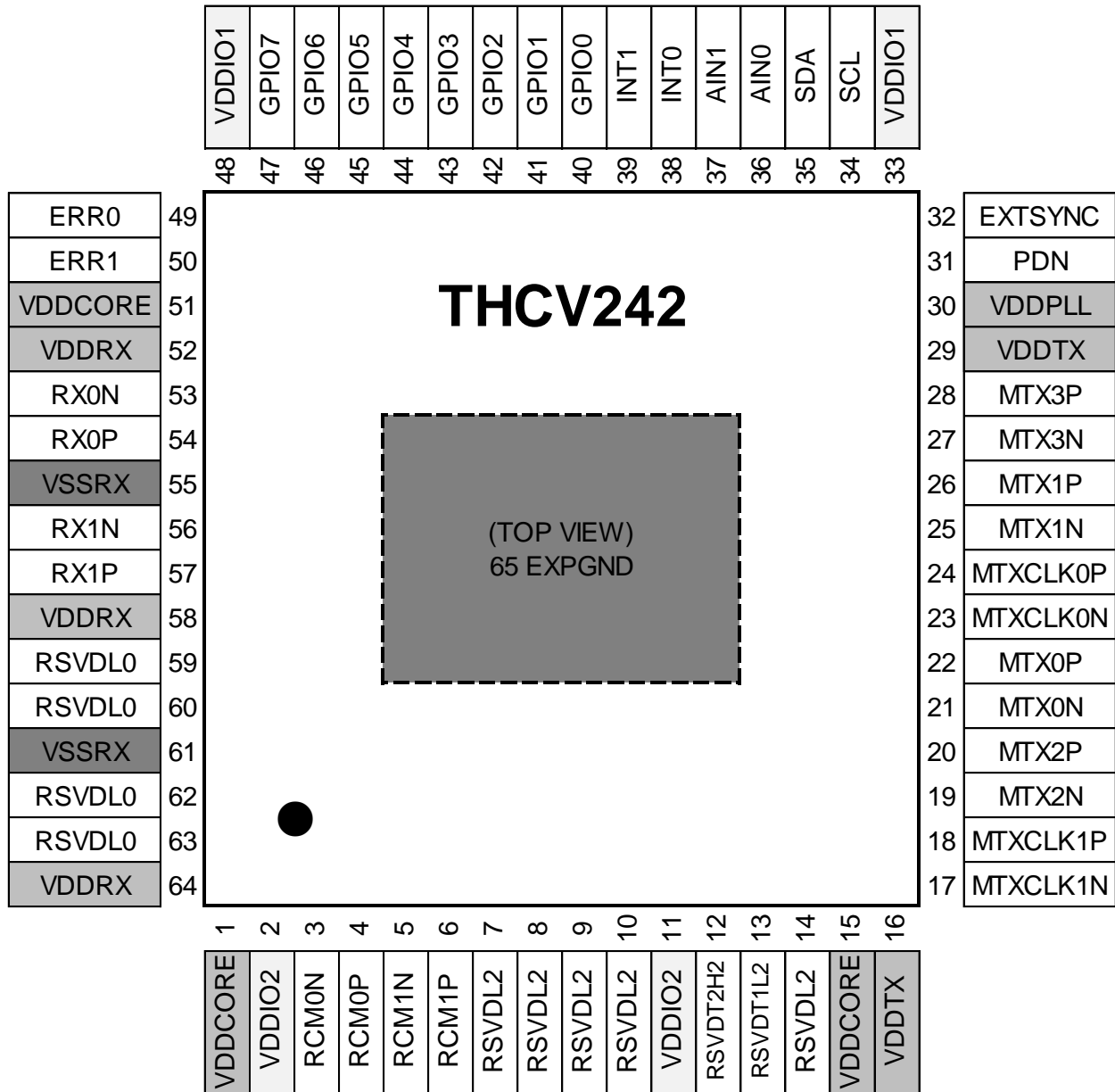
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4. Pin Configuration



5. Pin Description

| Pin Name | Pin # | type* | Description |
|------------|-----------------|-------|--|
| RX0P/N | 54, 53 | CI | V-by-One® HS Input lane0 |
| RX1P/N | 57, 56 | CI | V-by-One® HS Input lane1 |
| RCM0P/N | 4, 3 | CB | CML Bi-directional Input/Output (Sub-Link). |
| RCM1P/N | 6, 5 | CB | CML Bi-directional Input/Output (Sub-Link). |
| MTX0P/N | 22, 21 | MO | MIPI differential data outputs lane0 |
| MTX1P/N | 26, 25 | MO | MIPI differential data outputs lane1 |
| MTX2P/N | 20, 19 | MO | MIPI differential data outputs lane2 |
| MTX3P/N | 28, 27 | MO | MIPI differential data outputs lane3 |
| MTXCLK0P/N | 24, 23 | MO | MIPI differential clock outputs lane0 |
| MTXCLK1P/N | 18, 17 | MO | MIPI differential clock outputs lane1 |
| RSVDT1L2 | 13 | I2 | Reserved Pin, Must be tied to ground for normal operation. |
| RSVDT2H2 | 12 | I2 | Reserved pin. Must be tied to VDDIO2 for normal operation. |
| PDN | 31 | I1 | Power Down (User Power On Reset control must be required.) 0: Power Down Mode 1: Normal Operation |
| AIN1 | 37 | I1 | Device Address Setting for 2-wire Serial Interface [AIN1:AIN0]=00: ID=7'h0B [AIN1:AIN0]=01: ID=7'h34 |
| AIN0 | 36 | I1 | [AIN1:AIN0]=10: ID=7'h77 [AIN1:AIN0]=11: ID=7'h65 |
| SCL | 34 | B | 2-wire Serial Interface clock line |
| SDA | 35 | B | 2-wire Serial Interface data line |
| GPIO0 | 40 | B | General Purpose Input/Output |
| GPIO1 | 41 | B | General Purpose Input/Output |
| GPIO2 | 42 | B | General Purpose Input/Output |
| GPIO3 | 43 | B | General Purpose Input/Output |
| GPIO4 | 44 | B | General Purpose Input/Output |
| GPIO5 | 45 | B | General Purpose Input/Output |
| GPIO6 | 46 | B | General Purpose Input/Output |
| GPIO7 | 47 | B | General Purpose Input/Output |
| INT0 | 38 | O | Interrupt signal output. It must be connected with a pull-up resistor. |
| INT1 | 39 | O | 0 : Interrupt occurred 1 : Steady state |
| ERR0 | 49 | O | Internal Error / status signal monitoring output |
| ERR1 | 50 | O | Internal Error / status signal monitoring output |
| EXTSYNC | 32 | B | External Sync input/output for multiple camera synchronization |
| RSVDL0 | 59, 60, 62, 63 | I0 | Reserved Pins, Must be tied to ground for normal operation. |
| RSVDL2 | 7, 8, 9, 10, 14 | I2 | Reserved Pins, Must be tied to ground for normal operation. |
| VDDIO1 | 33, 48 | P | Power Supply for CMOS I/O |
| VDDIO2 | 2,11 | P | Power Supply for Sub-Link I/O |
| VDDCORE | 1,15,51 | P | Power Supply for Digital Circuit |
| VDDRFX | 52,58,64 | P | Power Supply for Analog Circuit |
| VSSRX | 55,61 | G | GND for Analog Circuit |
| VDDTX | 16,29 | P | Power Supply for Analog Circuit |
| VDDPLL | 30 | P | Power Supply for Analog Circuit |
| EXPAND | 65 | G | Exposed GND Pad |

*type symbol ; MO=MIPI Output, CI=CML Input, CB=CML Bi-directional input/output

I0=1.2V CMOS Input, I1=1.8~3.3V VDDIO1 domain CMOS Input, I2=1.8~3.3V VDDIO2 domain CMOS Input

O=1.8~3.3V VDDIO1 domain CMOS Output, B=1.8~3.3V VDDIO1 domain CMOS Bi-directional input/output

P=Power, G=Ground

6. Functional Description

6.1. Functional Overview

THCV242 can receive CML video signal transmitted over 15m length and encode it to MIPI CSI-2 format. With High Speed CML SerDes, high reliability and robustness encoding scheme and CDR (Clock and Data Recovery) architecture, the THCV242 enables to receive RAW/YUV/RGB/JPEG/Generic8bit data through Main-Link by single 100ohm differential pair or 50ohm Coax cable with minimal external components. In addition, THCV242 has Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link through the other 1-pair of CML-Line. The THCV242 system is able to watch remote devices and to control them via 2-wire serial interface or GPIOs. They also can report interrupt events caused by change of remote device statuses and internal statuses such as CRC error.

6.2. V-by-One® HS

6.2.1. V-by-One® HS input setting

Setting of V-by-One® HS input format can be configurable by 2-wire access to internal register.

Table 1. V-by-One® HS input format setting

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|-----------------|-------|-----|------|--|
| 0x10 10 | [7:6] | R_MLNK_NHSEL0 | 2 | R/W | 2'h2 | V-by-One® Main-Link Mode Select (for LINK0) 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard mode 11 : Reserved |
| 0x10 10 | [5:4] | R_MLNK_COLO | 2 | R/W | 2'h1 | V-by-One® Main-Link Byte Mode Select (for LINK0) 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved |
| 0x10 12 | [4] | R_RGB565_ON_L0 | 1 | R/W | 1'b0 | Main-Link Input Data Format Setting2 (This register could use only when R_VX1_LANE_FMT0=0x1) 0: RGB888 1: RGB565 |
| 0x10 12 | [3:0] | R_VX1_LANE_FMT0 | 4 | R/W | 4'h0 | Main-Link Input Data Format Setting 0: MPRF 1: RGBxxx 2,3,4,5,6: YUV422 (NormalYU1,NormalYU2,NormalYU3, DemuxYU1, DemuxYU2) 7,8,9: RAW8 (NormalR081,NormalR082, DemuxR081) 10,11,12: RAW10 (NormalR101, DemuxR101, DemuxR102) 13,14,15: RAW12 (NormalR121, DemuxR121, DemuxR122) |
| 0x10 14 | [7:6] | R_VRZ_NHSEL1 | 2 | R/W | 2'h2 | V-by-One® Main-Link Mode Select (for LINK1) 00 : Reserved 01 : Reserved 10 : V-by-One® HS standard mode 11 : Reserved |
| 0x10 14 | [5:4] | R_VRZ_COL1 | 2 | R/W | 2'h1 | V-by-One® Main-Link Byte Mode Select (for LINK1) 00 : Reserved 01 : 8bit (3Byte mode) 10 : 10bit (4Byte mode) 11 : Reserved |

6.2.2. MPRF (Main-Link PRivate Format)

MPRF format encoding preserves original data packet input to V-by-One® HS transmitter and output the data packet from THCV242. The counterpart transmitter must have installed MPRF format decoder like THCV241 because MPRF is not standard format.

Input V-by-One® HS Byte Mode is 4Byte Mode.

Video formats: RAW8/10/12/14/16/20, YUV422/420, RGB888/666/565, JPEG, and User-defined generic 8-bit are all supported with MPRF.

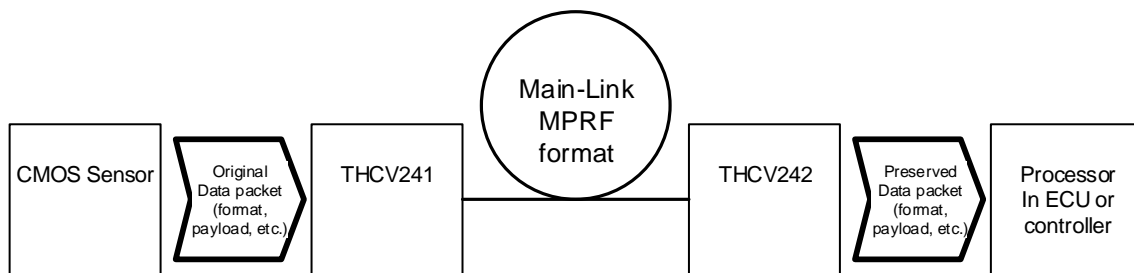


Figure 1. MPRF (Main-Link PRivate Format)

6.2.3. V-by-One® HS standard format

THCV242 input format capabilities as receiver are shown as follows. D[31:0] indicates V-by-One® HS standard version1.5 UnPacker packet definition. Data can be transmitted normally only when both transmitter and receiver are set to the same available format. Some of the THCV242 format may not be supported by particular counterpart transmitter because THCV242 prepares multiple formats that suit to multiple transmitter devices alternatives.

Table 2. V-by-One® HS input data mapping format 1/4

| Format Name Vx1HS std. Packer Packet ref. | RGB888 | YUV422 | | | | |
|--|--------|--------------|--------------|--------------|-----------------|-----------------|
| | | Normal Mode1 | Normal Mode2 | Normal Mode3 | Demux Mode1 | Demux Mode2 |
| V-by-One®HS_D[31] | 0 | 0 | 0 | 0 | Y[7](1st pixel) | Cb[7] |
| V-by-One®HS_D[30] | 0 | 0 | 0 | 0 | Y[6](1st pixel) | Cb[6] |
| V-by-One®HS_D[29] | 0 | 0 | 0 | 0 | Y[5](1st pixel) | Cb[5] |
| V-by-One®HS_D[28] | 0 | 0 | 0 | 0 | Y[4](1st pixel) | Cb[4] |
| V-by-One®HS_D[27] | 0 | 0 | 0 | 0 | Y[3](1st pixel) | Cb[3] |
| V-by-One®HS_D[26] | 0 | 0 | 0 | 0 | Y[2](1st pixel) | Cb[2] |
| V-by-One®HS_D[25] | 0 | 0 | 0 | 0 | Y[1](1st pixel) | Cb[1] |
| V-by-One®HS_D[24] | 0 | 0 | 0 | 0 | Y[0](1st pixel) | Cb[0] |
| V-by-One®HS_D[23] | B[7] | 0 | Cb[7]/Cr[7] | Y[7] | Cb[7] | Y[7](1st pixel) |
| V-by-One®HS_D[22] | B[6] | 0 | Cb[6]/Cr[6] | Y[6] | Cb[6] | Y[6](1st pixel) |
| V-by-One®HS_D[21] | B[5] | 0 | Cb[5]/Cr[5] | Y[5] | Cb[5] | Y[5](1st pixel) |
| V-by-One®HS_D[20] | B[4] | 0 | Cb[4]/Cr[4] | Y[4] | Cb[4] | Y[4](1st pixel) |
| V-by-One®HS_D[19] | B[3] | 0 | Cb[3]/Cr[3] | Y[3] | Cb[3] | Y[3](1st pixel) |
| V-by-One®HS_D[18] | B[2] | 0 | Cb[2]/Cr[2] | Y[2] | Cb[2] | Y[2](1st pixel) |
| V-by-One®HS_D[17] | B[1] | 0 | Cb[1]/Cr[1] | Y[1] | Cb[1] | Y[1](1st pixel) |
| V-by-One®HS_D[16] | B[0] | 0 | Cb[0]/Cr[0] | Y[0] | Cb[0] | Y[0](1st pixel) |
| V-by-One®HS_D[15] | G[7] | Y[7] | 0 | 0 | Y[7](2nd pixel) | Cr[7] |
| V-by-One®HS_D[14] | G[6] | Y[6] | 0 | 0 | Y[6](2nd pixel) | Cr[6] |
| V-by-One®HS_D[13] | G[5] | Y[5] | 0 | 0 | Y[5](2nd pixel) | Cr[5] |
| V-by-One®HS_D[12] | G[4] | Y[4] | 0 | 0 | Y[4](2nd pixel) | Cr[4] |
| V-by-One®HS_D[11] | G[3] | Y[3] | 0 | 0 | Y[3](2nd pixel) | Cr[3] |
| V-by-One®HS_D[10] | G[2] | Y[2] | 0 | 0 | Y[2](2nd pixel) | Cr[2] |
| V-by-One®HS_D[9] | G[1] | Y[1] | 0 | 0 | Y[1](2nd pixel) | Cr[1] |
| V-by-One®HS_D[8] | G[0] | Y[0] | 0 | 0 | Y[0](2nd pixel) | Cr[0] |
| V-by-One®HS_D[7] | R[7] | Cb[7]/Cr[7] | Y[7] | Cb[7]/Cr[7] | Cr[7] | Y[7](2nd pixel) |
| V-by-One®HS_D[6] | R[6] | Cb[6]/Cr[6] | Y[6] | Cb[6]/Cr[6] | Cr[6] | Y[6](2nd pixel) |
| V-by-One®HS_D[5] | R[5] | Cb[5]/Cr[5] | Y[5] | Cb[5]/Cr[5] | Cr[5] | Y[5](2nd pixel) |
| V-by-One®HS_D[4] | R[4] | Cb[4]/Cr[4] | Y[4] | Cb[4]/Cr[4] | Cr[4] | Y[4](2nd pixel) |
| V-by-One®HS_D[3] | R[3] | Cb[3]/Cr[3] | Y[3] | Cb[3]/Cr[3] | Cr[3] | Y[3](2nd pixel) |
| V-by-One®HS_D[2] | R[2] | Cb[2]/Cr[2] | Y[2] | Cb[2]/Cr[2] | Cr[2] | Y[2](2nd pixel) |
| V-by-One®HS_D[1] | R[1] | Cb[1]/Cr[1] | Y[1] | Cb[1]/Cr[1] | Cr[1] | Y[1](2nd pixel) |
| V-by-One®HS_D[0] | R[0] | Cb[0]/Cr[0] | Y[0] | Cb[0]/Cr[0] | Cr[0] | Y[0](2nd pixel) |

Table 3. V-by-One® HS input data mapping format 2/4

| Format Name Vx1HS std. Packer Packet ref. | RAW8 | | |
|--|--------------------|--------------------|--------------------|
| | Normal Mode1 | Normal Mode2 | Demux Mode1 |
| V-by-One®HS_D[31] | 0 | 0 | RAW[7] (2nd pixel) |
| V-by-One®HS_D[30] | 0 | 0 | RAW[6] (2nd pixel) |
| V-by-One®HS_D[29] | 0 | 0 | RAW[5] (2nd pixel) |
| V-by-One®HS_D[28] | 0 | 0 | RAW[4] (2nd pixel) |
| V-by-One®HS_D[27] | 0 | 0 | RAW[3] (2nd pixel) |
| V-by-One®HS_D[26] | 0 | 0 | RAW[2] (2nd pixel) |
| V-by-One®HS_D[25] | 0 | 0 | RAW[1] (2nd pixel) |
| V-by-One®HS_D[24] | 0 | 0 | RAW[0] (2nd pixel) |
| V-by-One®HS_D[23] | 0 | RAW[7] (1st pixel) | RAW[7] (1st pixel) |
| V-by-One®HS_D[22] | 0 | RAW[6] (1st pixel) | RAW[6] (1st pixel) |
| V-by-One®HS_D[21] | 0 | RAW[5] (1st pixel) | RAW[5] (1st pixel) |
| V-by-One®HS_D[20] | 0 | RAW[4] (1st pixel) | RAW[4] (1st pixel) |
| V-by-One®HS_D[19] | 0 | RAW[3] (1st pixel) | RAW[3] (1st pixel) |
| V-by-One®HS_D[18] | 0 | RAW[2] (1st pixel) | RAW[2] (1st pixel) |
| V-by-One®HS_D[17] | 0 | RAW[1] (1st pixel) | RAW[1] (1st pixel) |
| V-by-One®HS_D[16] | 0 | RAW[0] (1st pixel) | RAW[0] (1st pixel) |
| V-by-One®HS_D[15] | RAW[7] (2nd pixel) | 0 | RAW[7] (4th pixel) |
| V-by-One®HS_D[14] | RAW[6] (2nd pixel) | 0 | RAW[6] (4th pixel) |
| V-by-One®HS_D[13] | RAW[5] (2nd pixel) | 0 | RAW[5] (4th pixel) |
| V-by-One®HS_D[12] | RAW[4] (2nd pixel) | 0 | RAW[4] (4th pixel) |
| V-by-One®HS_D[11] | RAW[3] (2nd pixel) | 0 | RAW[3] (4th pixel) |
| V-by-One®HS_D[10] | RAW[2] (2nd pixel) | 0 | RAW[2] (4th pixel) |
| V-by-One®HS_D[9] | RAW[1] (2nd pixel) | 0 | RAW[1] (4th pixel) |
| V-by-One®HS_D[8] | RAW[0] (2nd pixel) | 0 | RAW[0] (4th pixel) |
| V-by-One®HS_D[7] | RAW[7] (1st pixel) | RAW[7] (2nd pixel) | RAW[7] (3rd pixel) |
| V-by-One®HS_D[6] | RAW[6] (1st pixel) | RAW[6] (2nd pixel) | RAW[6] (3rd pixel) |
| V-by-One®HS_D[5] | RAW[5] (1st pixel) | RAW[5] (2nd pixel) | RAW[5] (3rd pixel) |
| V-by-One®HS_D[4] | RAW[4] (1st pixel) | RAW[4] (2nd pixel) | RAW[4] (3rd pixel) |
| V-by-One®HS_D[3] | RAW[3] (1st pixel) | RAW[3] (2nd pixel) | RAW[3] (3rd pixel) |
| V-by-One®HS_D[2] | RAW[2] (1st pixel) | RAW[2] (2nd pixel) | RAW[2] (3rd pixel) |
| V-by-One®HS_D[1] | RAW[1] (1st pixel) | RAW[1] (2nd pixel) | RAW[1] (3rd pixel) |
| V-by-One®HS_D[0] | RAW[0] (1st pixel) | RAW[0] (2nd pixel) | RAW[0] (3rd pixel) |

Table 4. V-by-One® HS input data mapping format 3/4

| Format Name Vx1HS std. Packer Packet ref. | RAW10 | | |
|--|--------|-------------------|-------------------|
| | Normal | Demux Mode1 | Demux Mode2 |
| V-by-One®HS_D[31] | 0 | 0 | 0 |
| V-by-One®HS_D[30] | 0 | 0 | 0 |
| V-by-One®HS_D[29] | 0 | 0 | 0 |
| V-by-One®HS_D[28] | 0 | 0 | 0 |
| V-by-One®HS_D[27] | 0 | 0 | 0 |
| V-by-One®HS_D[26] | 0 | 0 | 0 |
| V-by-One®HS_D[25] | 0 | RAW[1](1st pixel) | 0 |
| V-by-One®HS_D[24] | 0 | RAW[0](1st pixel) | 0 |
| V-by-One®HS_D[23] | 0 | RAW[9](1st pixel) | 0 |
| V-by-One®HS_D[22] | 0 | RAW[8](1st pixel) | 0 |
| V-by-One®HS_D[21] | 0 | RAW[7](1st pixel) | RAW[1](1st pixel) |
| V-by-One®HS_D[20] | 0 | RAW[6](1st pixel) | RAW[0](1st pixel) |
| V-by-One®HS_D[19] | 0 | RAW[5](1st pixel) | RAW[9](1st pixel) |
| V-by-One®HS_D[18] | 0 | RAW[4](1st pixel) | RAW[8](1st pixel) |
| V-by-One®HS_D[17] | 0 | RAW[3](1st pixel) | RAW[7](1st pixel) |
| V-by-One®HS_D[16] | 0 | RAW[2](1st pixel) | RAW[6](1st pixel) |
| V-by-One®HS_D[15] | 0 | 0 | RAW[5](1st pixel) |
| V-by-One®HS_D[14] | 0 | 0 | RAW[4](1st pixel) |
| V-by-One®HS_D[13] | 0 | 0 | RAW[3](1st pixel) |
| V-by-One®HS_D[12] | 0 | 0 | RAW[2](1st pixel) |
| V-by-One®HS_D[11] | 0 | 0 | 0 |
| V-by-One®HS_D[10] | 0 | 0 | 0 |
| V-by-One®HS_D[9] | RAW[1] | RAW[1](2nd pixel) | RAW[1](2nd pixel) |
| V-by-One®HS_D[8] | RAW[0] | RAW[0](2nd pixel) | RAW[0](2nd pixel) |
| V-by-One®HS_D[7] | RAW[9] | RAW[9](2nd pixel) | RAW[9](2nd pixel) |
| V-by-One®HS_D[6] | RAW[8] | RAW[8](2nd pixel) | RAW[8](2nd pixel) |
| V-by-One®HS_D[5] | RAW[7] | RAW[7](2nd pixel) | RAW[7](2nd pixel) |
| V-by-One®HS_D[4] | RAW[6] | RAW[6](2nd pixel) | RAW[6](2nd pixel) |
| V-by-One®HS_D[3] | RAW[5] | RAW[5](2nd pixel) | RAW[5](2nd pixel) |
| V-by-One®HS_D[2] | RAW[4] | RAW[4](2nd pixel) | RAW[4](2nd pixel) |
| V-by-One®HS_D[1] | RAW[3] | RAW[3](2nd pixel) | RAW[3](2nd pixel) |
| V-by-One®HS_D[0] | RAW[2] | RAW[2](2nd pixel) | RAW[2](2nd pixel) |

Table 5. V-by-One® HS input data mapping format 4/4

| Format Name Vx1HS std. Packer Packet ref. | RAW12 | | |
|--|---------|--------------------|--------------------|
| | Normal | Demux Mode1 | Demux Mode2 |
| V-by-One®HS_D[31] | 0 | 0 | 0 |
| V-by-One®HS_D[30] | 0 | 0 | 0 |
| V-by-One®HS_D[29] | 0 | 0 | 0 |
| V-by-One®HS_D[28] | 0 | 0 | 0 |
| V-by-One®HS_D[27] | 0 | RAW[3](1st pixel) | 0 |
| V-by-One®HS_D[26] | 0 | RAW[2](1st pixel) | 0 |
| V-by-One®HS_D[25] | 0 | RAW[1](1st pixel) | 0 |
| V-by-One®HS_D[24] | 0 | RAW[0](1st pixel) | 0 |
| V-by-One®HS_D[23] | 0 | RAW[11](1st pixel) | RAW[3](1st pixel) |
| V-by-One®HS_D[22] | 0 | RAW[10](1st pixel) | RAW[2](1st pixel) |
| V-by-One®HS_D[21] | 0 | RAW[9](1st pixel) | RAW[1](1st pixel) |
| V-by-One®HS_D[20] | 0 | RAW[8](1st pixel) | RAW[0](1st pixel) |
| V-by-One®HS_D[19] | 0 | RAW[7](1st pixel) | RAW[11](1st pixel) |
| V-by-One®HS_D[18] | 0 | RAW[6](1st pixel) | RAW[10](1st pixel) |
| V-by-One®HS_D[17] | 0 | RAW[5](1st pixel) | RAW[9](1st pixel) |
| V-by-One®HS_D[16] | 0 | RAW[4](1st pixel) | RAW[8](1st pixel) |
| V-by-One®HS_D[15] | 0 | 0 | RAW[7](1st pixel) |
| V-by-One®HS_D[14] | 0 | 0 | RAW[6](1st pixel) |
| V-by-One®HS_D[13] | 0 | 0 | RAW[5](1st pixel) |
| V-by-One®HS_D[12] | 0 | 0 | RAW[4](1st pixel) |
| V-by-One®HS_D[11] | RAW[3] | RAW[3](2nd pixel) | RAW[3](2nd pixel) |
| V-by-One®HS_D[10] | RAW[2] | RAW[2](2nd pixel) | RAW[2](2nd pixel) |
| V-by-One®HS_D[9] | RAW[1] | RAW[1](2nd pixel) | RAW[1](2nd pixel) |
| V-by-One®HS_D[8] | RAW[0] | RAW[0](2nd pixel) | RAW[0](2nd pixel) |
| V-by-One®HS_D[7] | RAW[11] | RAW[11](2nd pixel) | RAW[11](2nd pixel) |
| V-by-One®HS_D[6] | RAW[10] | RAW[10](2nd pixel) | RAW[10](2nd pixel) |
| V-by-One®HS_D[5] | RAW[9] | RAW[9](2nd pixel) | RAW[9](2nd pixel) |
| V-by-One®HS_D[4] | RAW[8] | RAW[8](2nd pixel) | RAW[8](2nd pixel) |
| V-by-One®HS_D[3] | RAW[7] | RAW[7](2nd pixel) | RAW[7](2nd pixel) |
| V-by-One®HS_D[2] | RAW[6] | RAW[6](2nd pixel) | RAW[6](2nd pixel) |
| V-by-One®HS_D[1] | RAW[5] | RAW[5](2nd pixel) | RAW[5](2nd pixel) |
| V-by-One®HS_D[0] | RAW[4] | RAW[4](2nd pixel) | RAW[4](2nd pixel) |

6.2.4. Link Status (HTPDN/LOCKN)

Hot-Plug Function

HTPDN indicates Main-Link connect condition between Transmitter and Receiver. HTPDN of Transmitter side is high when Receiver is not active or not connected. Then Transmitter can enter into power down mode. HTPDN is set to Low by the Receiver when Receiver is active and connects to the Transmitter, and then Transmitter must start up and transmit CDR training pattern for link training. HTPDN is open drain output at the receiver side. Transmitter side needs Pull-up resistor.

There is an application option to omit HTPDN connection between Transmitter and Receiver. In this case, HTPDN at Transmitter side should always be at Low.

Lock Detect Function

LOCKN indicates whether CDR PLL of Main-Link is in lock status or not. LOCKN at Transmitter input is set to High by pull-up resistor when Receiver is not active or in CDR PLL training. LOCKN is set to Low by Receiver when CDR lock is completed. After that the CDR training mode finishes and then Transmitter shifts to the normal mode. LOCKN of Receiver is open drain. Transmitter side needs pull-up resistor.

When an application omits HTPDN, LOCKN signal should only be considered with HTPDN pulled low by Receiver.

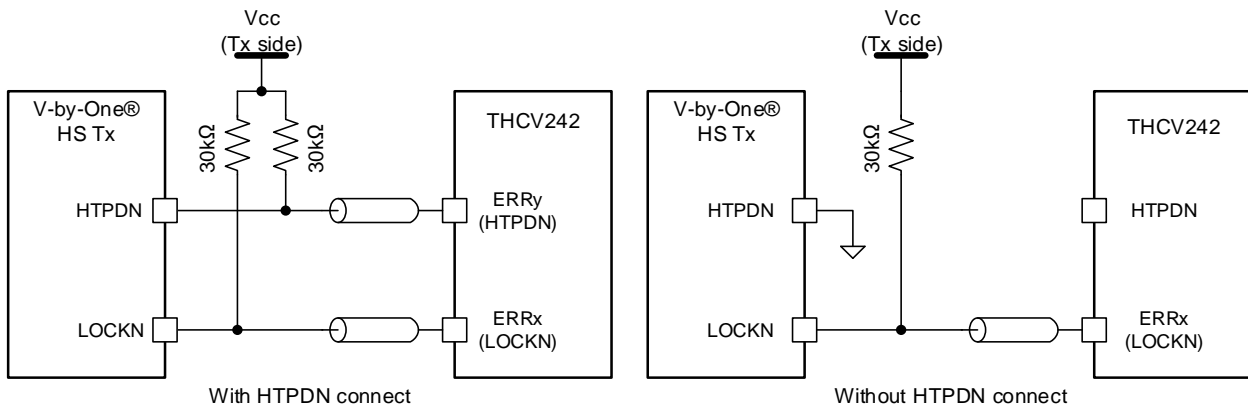


Figure 2. Physical wire connection for wired Hot-plug and Lock detect scheme

It will need same GND potential reference between transmitter and receiver device to connect HTPDN and LOCKN pins directly like above. HTPDN and LOCKN can also be transmitted via Sub-Link without physical wire connection. Assignment can be configurable by 2-wire access to internal register.

Table 6. HTPDN/LOCKN register

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|-----------------|-------|-----|--|---------|
| 0x0019 | [7:4] | ReservedL | 4 | RW | Must be set 0 | 4'd0 |
| | [3:2] | R_LOCKN_LN1_SEL | 2 | RW | Sub-Link Lane1 LOCKN/HTPDN scheme of releted Main-Link select 0:LOCKN1 1:LOCKN0 LOCKN1 2:Reserved 3:1'b0 (Forced LOCKN/HTPDN=Low) *LOCKN1=LOCKN signal of V-by-One(R) HS Lane1=RX1P/RX1N *HTPDN of the same lane as above set LOCKN lane is used | 2'd0 |
| | [1:0] | R_LOCKN_LN0_SEL | 2 | RW | Sub-Link Lane0 LOCKN/HTPDN scheme of releted Main-Link select 0:LOCKN0 1:LOCKN0 LOCKN1 2:Reserved 3:1'b0 (Forced LOCKN/HTPDN=Low) *LOCKN0=LOCKN signal of V-by-One(R) HS Lane0=RX0P/RX0N *HTPDN of the same lane as above set LOCKN lane is used | 2'd0 |

6.3. Local, Remote and Remote Slave Register Programming

6.3.1. 2-wire serial I/F slave Device ID

To use basic functions, initialization, GPIO (General Purpose Input/Output), fault/error detection, and interrupt function, 2-wire serial I/F enables to access registers. AIN<1:0> pin determines 2-wire slave Device ID setting.

Table 7. 2-wire serial I/F Device ID select by AIN pin

| | | | |
|------|----|----|--|
| AIN1 | 37 | 11 | Device Address Setting for 2-wire Serial Interface [AIN1:AIN0]=00: ID=7'h0B [AIN1:AIN0]=01: ID=7'h34 [AIN1:AIN0]=10: ID=7'h77 [AIN1:AIN0]=11: ID=7'h65 |
| AIN0 | 36 | 11 | |

As an additional method, 2-wire slave Device ID setting can be changed from default value by register setting.

Table 8. 2-wire serial I/F Device ID select by register setting

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|---------------|-------|-----|---|---------|
| 0x0030 | [7:0] | R_2WIRE_SADR | 8 | RW | 2WIRE slave device address setting [7]2WIRE slave device address control 0: 2WIRE slv device addr. is set by AIN<1:0> pin 1: 2WIRE slv device addr. is set by following register [6:0] [6:0]2WIRE slave device address value for register control | 8'd0 |

6.3.2. 2-wire serial Read/Write access to local Register

HOST MPU can directly access THCV242 local register by 2-wire serial I/F.

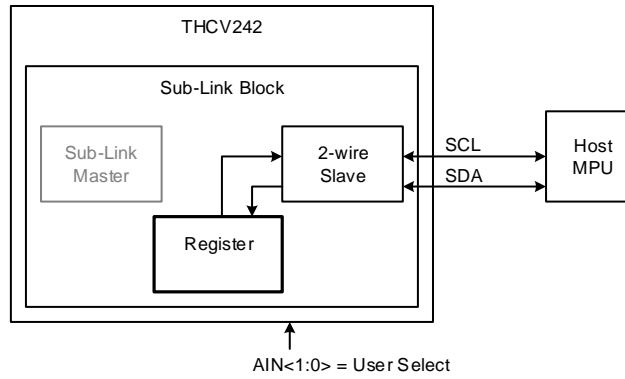


Figure 3. Host to THCV242 local register access configuration

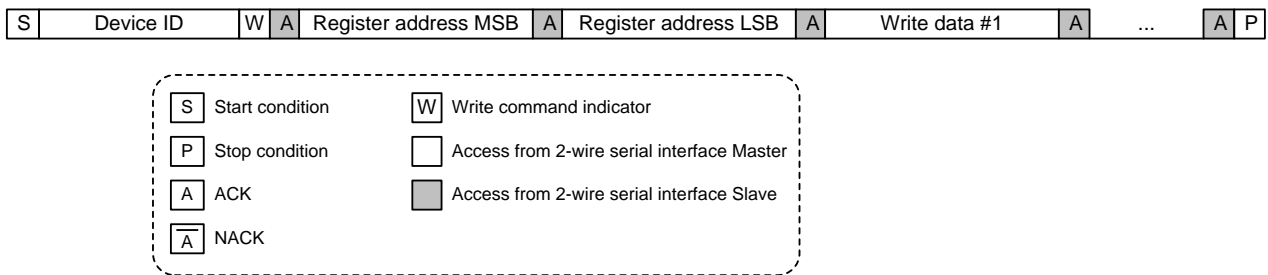


Figure 4. 2-wire serial I/F write to THCV242 local register protocol

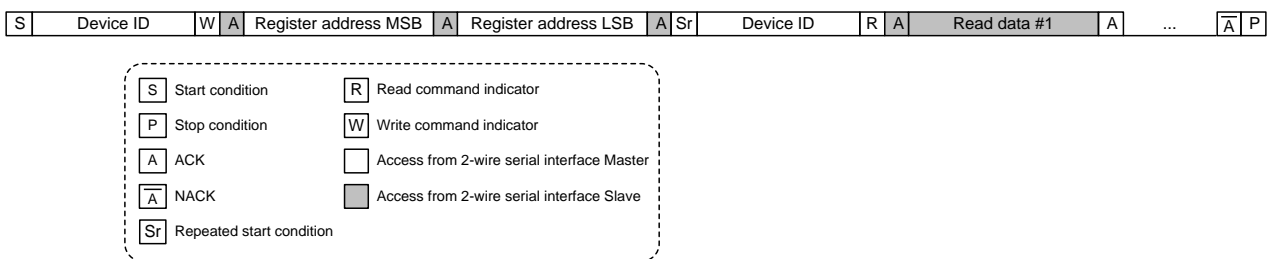


Figure 5. 2-wire serial I/F read to THCV242 local register protocol

6.3.3. 2-wire serial I/F Watch Dog Timer

2-wire Watch Dog Timer (WDT) is installed to monitor status.

Table 9. 2-wire WDT setting

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|-------------------|-------|-----|---|---------|
| 0x003B | [7:5] | reserved | 3 | - | - | - |
| | [4] | R_2WIRE_WD_EN | 1 | RW | 2WIRE WDT Enable 0:Disable 1:Enable | 1'b1 |
| | [3:1] | reserved | 3 | - | - | - |
| | [0] | R_2WIRE_WD_OFFSET | 1 | RW | 2WIRE_WDT_OffsetTime 1:11'd2047 0:11'd1023 | 1'd1 |
| 0x003C | [7:0] | R_2WIRE_WD_TIM | 8 | RW | 2WIRE WDT_time=64x{(R_2WIRE_WD_TIM<7:0>+1)}x{2WIRE_WDT_OffsetTime}xtOSC | 8'd255 |

6.3.4. Sub-Link setting

THCV242 has Sub-Link which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for Main-Link. THCV242 is Sub-Link Master and connectable to Sub-Link Slave device such as THCV241.

Sub-Link Polling interval is controllable from about 20us to 800us, that may have relationships on fault/error detection, interrupt, or other UART / GPIO transfer time designed on application. SSR (Sub-Link Status Read) interval determines recovery quickness from 2-wire serial remote communication completion. SSR interval effects only on Sub-Link Master “2-wire Set&Trigger mode1” (R_SLINK_MODE setting).

Table 10. Sub-Link Master protocol basic setting

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|-----------------------|-------|-----|---|---------|
| 0x0004 | [7:3] | reserved | 5 | - | - | - |
| | [2:0] | R_SLINK_MODE | 3 | RW | Sub-Link basic protocol setting as Sub-Link Master 1: 2-wire Set&Trigger (Normal) mode1 3: 2-wire Pass Through mode1 0,2,4,5,6,7: Reserved | 3'd1 |
| 0x0010 | [7:4] | R_SLINK_EN | 4 | RW | Sub-Link Enable [7] Reserved [6] Reserved [5] 0: Lane1 Disable, 1: Lane1 Enable [4] 0: Lane0 Disable, 1: Lane0 Enable | 4'd0 |
| | [3:0] | R_SLINK_POL_EN | 4 | RW | Sub-Link Polling Enable [3] Reserved [2] Reserved [1] 0: Lane1 Disable, 1: Lane1 Enable [0] 0: Lane0 Disable, 1: Lane0 Enable | 4'hF |
| 0x0011 | [7:4] | R_SLINK_SSR_EN | 4 | RW | Sub-Link SSR Enable [7] Reserved [6] Reserved [5] 0: Lane1 Disable, 1: Lane1 Enable [4] 0: Lane0 Disable, 1: Lane0 Enable | 4'hF |
| | [3:0] | R_SLINK_WD_EN | 4 | RW | Sub-Link WDT Enable [3] Reserved [2] Reserved [1] 0: Lane1 Disable, 1: Lane1 Enable [0] 0: Lane0 Disable, 1: Lane0 Enable | 4'hF |
| 0x001A | [7:5] | reserved | 3 | - | - | - |
| | [4] | R_SLINK_POL_OFFSET_EN | 1 | RW | Sub-Link Polling Offset Enable 0: Disable 1: Enable, Polling time phase of each lanes are shifted as below lane1 offset from lane0: Sub-Link Poling interval x 1/4 | 1'b0 |
| | [3:2] | reserved | 2 | - | - | - |
| 0x001B | [1:0] | R_SLINK_POL_TIM_UP | 2 | RW | Sub-Link Polling interval setting (min. 0x018, about 20us) | 2'd0 |
| | [7:0] | R_SLINK_POL_TIM_DN | 8 | RW | Sub-Link Polling interval time=64x(256xR_SLINK_POL_TIM_UP<1:0>+R_SLINK_POL_TIM_DN<7:0>+1)xTOSC *No Polling when R_SLINK_POL_TIM_UP=0 and R_SLINK_POL_TIM_DN=0 | 8'd124 |
| 0x001C | [7:2] | reserved | 6 | - | - | - |
| | [1:0] | R_SLINK_SSR_TIM_UP | 2 | RW | Sub-Link SSR interval setting | 2'd0 |
| 0x001D | [7:0] | R_SLINK_SSR_TIM_DN | 8 | RW | Sub-Link SSR interval time=64x(256xR_SLINK_SSR_TIM_UP<1:0>+R_SLINK_SSR_TIM_DN<7:0>+1)xTOSC *No SSR when R_SLINK_SSR_TIM_UP=0 and R_SLINK_SSR_TIM_DN=0 | 8'd249 |

To use GPIO (General Purpose Input/Output) pin, fault/error detection and interrupt function, “2-wire Set&Trigger mode1”, “2-wire Pass Through mode1” enables remote register access. THCV242, Sub-Link Master device has 2-wire serial slave block and can connect to HOST MPU. On the other hand, the counterpart Sub-Link Slave device has 2-wire serial master block and can connect to remote side 2-wire serial slave devices.

HOST MPU can access register of Sub-Link Master device, Sub-Link Slave device and remote side 2-wire serial slave devices.

6.3.5. Sub-Link 2-wire Read/Write access to remote Register

6.3.5.1. Sub-Link 2-wire Set and Trigger mode

HOST MPU can access to Sub-Link Slave's register via THCV242 as Sub-Link Master only by THCV242 internal local register control and monitoring on 2-wire Set&Trigger mode1.

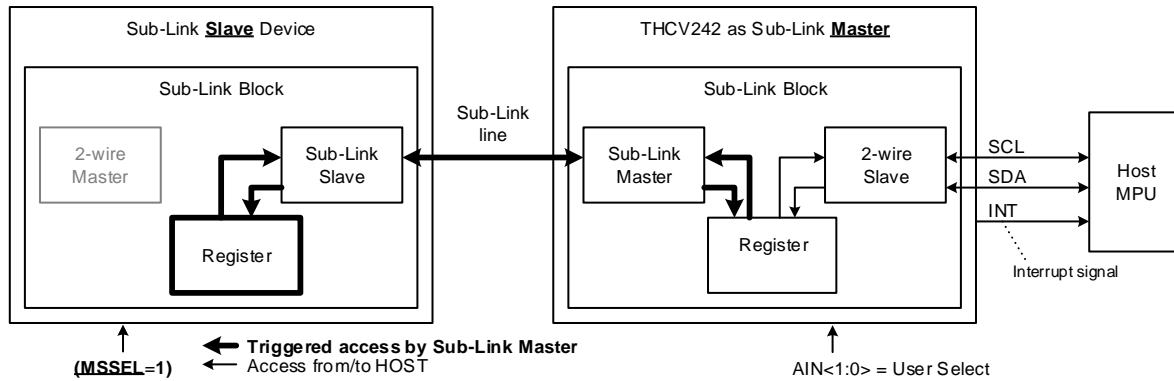


Figure 6. Host MPU to Sub-Link Slave Register via THCV242 access configuration

HOST MPU can access to remote side 2-wire serial slave register via THCV242 as Sub-Link Master only by THCV242 internal local register control and monitoring on 2-wire Set&Trigger mode1.

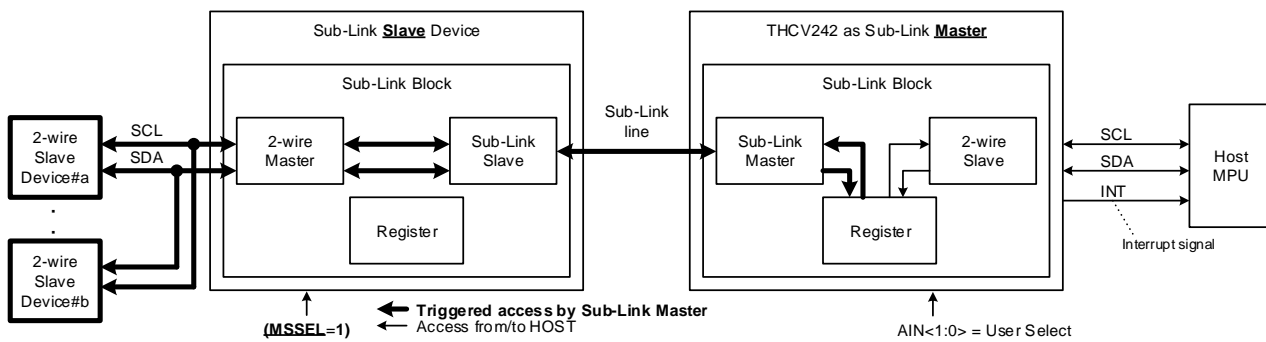


Figure 7. Host MPU to remote 2-wire slave devices via THCV242 access configuration

In principle, when Sub-Link bridges 2-wire serial interface communication from Sub-Link Master to Sub-Link Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and Sub-Link Slave internal bus access or remote side 2-wire serial access.

R_2WIRE_CLKSEN (Sub-Link Master side register, 0x0042 bit0) selects whether 2-wire serial slave of Sub-Link Master perform clock stretching.

When R_2WIRE_CLKSEN = 1, Sub-Link Master device waits HOST MPU until Sub-Link Slave register access or remote side 2-wire serial slave register access complete by clock stretching.

When R_2WIRE_CLKSEN = 0, Sub-Link Master device informs HOST MPU that Sub-Link Slave register access or remote side 2-wire serial register access has completed by interruption (detectable on INT pin) without clock stretching.

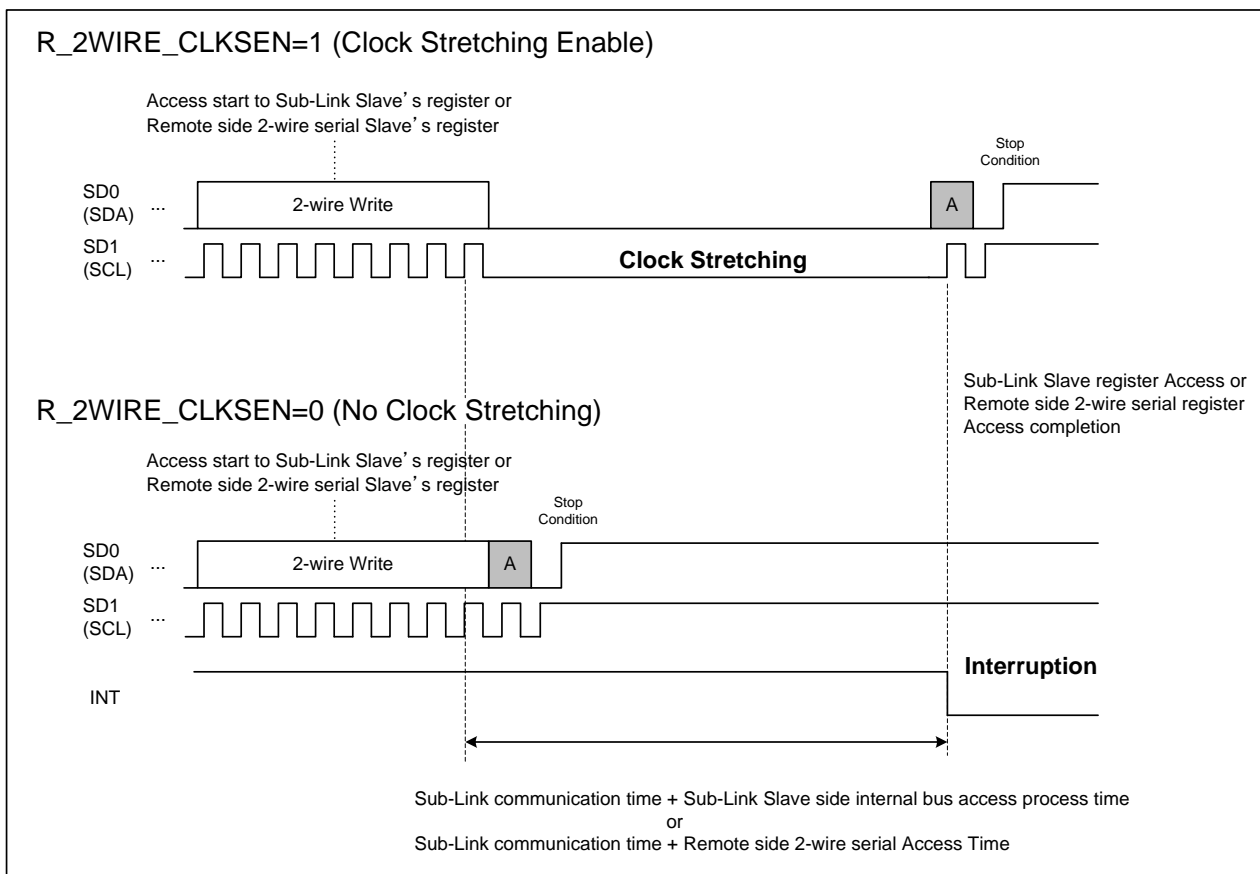


Figure 8. Sub-Link Master 2-wire slave clock stretching operation

Table 11. 2-wire serial I/F Set& Trigger mode remote access control and monitoring local registers

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|---------------------|-------|-----|---|---------|
| 0x00D0 | [7:0] | R_2WIRE_DATA0 | 8 | RW | 2-wire serial I/F remote write/read data #0 | 8'd0 |
| 0x00D1 | [7:0] | R_2WIRE_DATA1 | 8 | RW | 2-wire serial I/F remote write/read data #1 | 8'd0 |
| 0x00D2 | [7:0] | R_2WIRE_DATA2 | 8 | RW | 2-wire serial I/F remote write/read data #2 | 8'd0 |
| 0x00D3 | [7:0] | R_2WIRE_DATA3 | 8 | RW | 2-wire serial I/F remote write/read data #3 | 8'd0 |
| 0x00D4 | [7:0] | R_2WIRE_DATA4 | 8 | RW | 2-wire serial I/F remote write/read data #4 | 8'd0 |
| 0x00D5 | [7:0] | R_2WIRE_DATA5 | 8 | RW | 2-wire serial I/F remote write/read data #5 | 8'd0 |
| 0x00D6 | [7:0] | R_2WIRE_DATA6 | 8 | RW | 2-wire serial I/F remote write/read data #6 | 8'd0 |
| 0x00D7 | [7:0] | R_2WIRE_DATA7 | 8 | RW | 2-wire serial I/F remote write/read data #7 | 8'd0 |
| 0x00D8 | [7:0] | R_2WIRE_DATA8 | 8 | RW | 2-wire serial I/F remote write/read data #8 | 8'd0 |
| 0x00D9 | [7:0] | R_2WIRE_DATA9 | 8 | RW | 2-wire serial I/F remote write/read data #9 | 8'd0 |
| 0x00DA | [7:0] | R_2WIRE_DATA10 | 8 | RW | 2-wire serial I/F remote write/read data #10 | 8'd0 |
| 0x00DB | [7:0] | R_2WIRE_DATA11 | 8 | RW | 2-wire serial I/F remote write/read data #11 | 8'd0 |
| 0x00DC | [7:0] | R_2WIRE_DATA12 | 8 | RW | 2-wire serial I/F remote write/read data #12 | 8'd0 |
| 0x00DD | [7:0] | R_2WIRE_DATA13 | 8 | RW | 2-wire serial I/F remote write/read data #13 | 8'd0 |
| 0x00DE | [7:0] | R_2WIRE_DATA14 | 8 | RW | 2-wire serial I/F remote write/read data #14 | 8'd0 |
| 0x00DF | [7:0] | R_2WIRE_DATA15 | 8 | RW | 2-wire serial I/F remote write/read data #15 | 8'd0 |
| 0x00E0 | [7:1] | R_2WIRE_DEVADR | 7 | RW | 2-wire serial I/F remote access target device address. if target=self addr.; access to Sub-Link Slave inside register, else; access to remote side 2-wire serial Slave devices externally connected to Sub-Link slave | 7'h00 |
| | [0] | R_2WIRE_WR | 1 | RW | 2-wire serial I/F remote access write or read select 0:Write 1:Read | 1'b0 |
| 0x00E1 | [7] | reserved | 1 | - | - | - |
| | [6:4] | R_2WIRE_WADR_BYTE | 3 | RW | 2-wire serial I/F remote device's Sub Address (Word Address, register address) Byte width select. address Byte width=R_2WIRE_WADR_BYTE<2:0>+1 0 : 1Byte= 8bit Sub addr.(register addr.) 1 : 2Byte=16bit Sub addr.(register addr.) 4 : 5Byte=40bit Sub addr.(register addr.), etc. | 3'd0 |
| | [3:0] | R_2WIRE_DATA_BYTE | 4 | RW | 2-wire serial I/F remote access data Byte number Byte Number = R_2WIRE_DATA_BYTE + 1 (e.g. 0x2 for 3byte burst) [write rule] R_2WIRE_WADR_BYTE+R_2WIRE_DATA_BYTE < 'd16 [read rule] R_2WIRE_DATA_BYTE<'d16 | 4'd0 |
| 0x00E2 | [7:1] | reserved | 7 | - | - | - |
| | [0] | R_2WIRE_CLKSEN | 1 | RW | 2-wire serial I/F local response clock stretching Enable 0: Sub-Link Master (2-wire slave) No clock stretching 1: Sub-Link Master (2-wire slave) clock stretching Enable *2-wire Pass Through mode forces clock stretching Enable | 1'b0 |
| 0x00E3 | [7:2] | reserved | 6 | - | - | - |
| | [1:0] | R_2WIRE_RD_LANE_SEL | 2 | RW | Sub-Link transaction read lane select 0: Lane0 Sub-Link read 1: Lane1 Sub-Link read 2,3: Reserved | 2'd0 |
| 0x00E4 | [7:2] | reserved | 4 | - | - | - |
| | [1:0] | R_2WIRE_WR_LANE_SEL | 4 | RW | Sub-Link transaction write lane select [1] 0: Lane1 Disable, 1: Lane1 Enable [0] 0: Lane0 Disable, 1: Lane0 Enable *Only active when R_SLINK_MODE=4'd0 or 4'd1 | 4'hF |
| 0x00E5 | [7:1] | reserved | 7 | - | - | - |
| | [0] | R_2WIRE_START | 1 | W | 2-wire serial I/F remote access start trigger | - |

6.3.5.2. Sub-Link 2-wire Pass Through mode

Sub-Link Master 2-wire Pass Through mode1 can bridge original local 2-wire commands to remote side basically with no logical change.

2-wire Pass Through mode1 uses 2-wire slave clock stretching scheme at local Sub-Link Master side. Host MCU 2-wire master must be no problem with clock stretching wait from 2-wire slave.

Sub-Link Slave side processing protocol “Divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are sent separately on remote side. Burst write/read access target Sub-Address (Word-Address) is interpreted so that subsequent Sub-Address (Word-Address) from 2nd group is automatically and properly incremented. As shown below, remote side 2-wire accesses are independent each other by determined Byte, which are defined in R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE at R_2WIREPT1_PASS_MODE[1]=1.

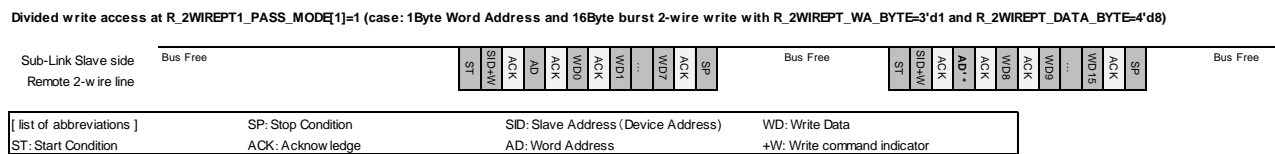


Figure 9. 2-wire Pass Through mode1 Sub-Link Slave command Divided scheme

On address processing protocol “Assigned address & rename”, THCV242 2-wire slave respond only to 2-wire device address defined in R_2WIREPT1_PASS_ADRxy1 (x=Lane0 or Lane1, y=0/1/2/3) for remote Pass Through operation. Otherwise, 2-wire commands are ignored except THCV242 itself address. The device address can be renamed before remote send. The counterpart Sub-Link Slave internal register access is available with R_2WIREPT1_PASS_ADRINx (x=Lane0 or Lane1) setting.

On address processing protocol “All Through”, THCV242 2-wire slave respond basically all 2-wire device address for remote Pass Through operation except THCV242 itself address. Additionally, Defined addresses in R_2WIREPT2_NOPASS_ADRxz (x=Lane0 or Lane1, z=0/1/2/3/4/5/6/7) can be ignored by THCV242.

Table 12. 2-wire serial I/F Pass Through mode remote access setting 1/2

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|-------------------------|-------|-----|---|---------|
| 0x0031 | [7:2] | reserved | 6 | - | - | - |
| | [1:0] | R_2WIREPT_MODE | 2 | RW | 2WIRE Pass Through mode setting [1]Pass Through processing protocol on Sub-Link Slave 0:Reserved 1:Divided write & Divided read** (available with 2-wire Pass Through mode1) **:Transaction address and data Byte number is set as R_2WIREPT_WA_BYTE and R_2WIREPT_DATA_BYTE. [0]Pass Through 2WIRE device address processing 0:Address rename (rule as R_2WIREPT1_PASS_ADRxy0/1. x is Lane0or1, y=<3:0>) 1:All Through (exception definition of address to ignore as R_2WIREPT2_NOPASS_ADRxz. x is Lane0or1, z=<7:0>) | 2'd0 |
| 0x0032 | [7] | reserved | 1 | - | - | - |
| | [6:4] | R_2WIREPT_WA_BYTE | 3 | RW | 2WIRE Pass Through Divided write/read Sub-Address (Word Address) Byte number setting, being active only at R_2WIREPT1_PASS_MODE[1]=1 Byte Number = R_2WIREPT_WA_BYTE + 1 (e.g. 0x1 for 2Byte Sub-Address) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < 14 is required. | 3'd0 |
| | [3:0] | R_2WIREPT_DATA_BYTE | 4 | RW | 2WIRE Pass Through Divided write/read data Byte number per one transaction setting, being active only at R_2WIREPT1_PASS_MODE[1]=1 Byte Number = R_2WIREPT_DATA_BYTE + 1 (e.g. 0x2 for 3Byte per transaction) *R_2WIREPT_WA_BYTE + R_2WIREPT_DATA_BYTE < 14 is required. | 4'd0 |
| 0x0040 | [7:0] | R_2WIREPT1_PASS_ADR000 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane0 #0, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0041 | [7:0] | R_2WIREPT1_PASS_ADR001 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane0 #0, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0042 | [7:0] | R_2WIREPT1_PASS_ADR010 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane0 #1, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0043 | [7:0] | R_2WIREPT1_PASS_ADR011 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane0 #1, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0044 | [7:0] | R_2WIREPT1_PASS_ADR020 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane0 #2, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0045 | [7:0] | R_2WIREPT1_PASS_ADR021 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane0 #2, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0046 | [7:0] | R_2WIREPT1_PASS_ADR030 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane0 #3, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0047 | [7:0] | R_2WIREPT1_PASS_ADR031 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane0 #3, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0048 | [7:0] | R_2WIREPT2_NOPASS_ADR00 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #0, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x0049 | [7:0] | R_2WIREPT2_NOPASS_ADR01 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #1, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004A | [7:0] | R_2WIREPT2_NOPASS_ADR02 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #2, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004B | [7:0] | R_2WIREPT2_NOPASS_ADR03 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #3, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004C | [7:0] | R_2WIREPT2_NOPASS_ADR04 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #4, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004D | [7:0] | R_2WIREPT2_NOPASS_ADR05 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #5, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004E | [7:0] | R_2WIREPT2_NOPASS_ADR06 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #6, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x004F | [7:0] | R_2WIREPT2_NOPASS_ADR07 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane0 #7, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x0050 | [7:0] | R_2WIREPT1_PASS_ADRIN0 | 8 | RW | 2WIRE Pass Through counterpart Sub-Link Slave internal access dedicated address for Lane0, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |

Table 13. 2-wire serial I/F Pass Through mode remote access setting 2/2

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|-------------------------|-------|-----|--|---------|
| 0x0060 | [7:0] | R_2WIREPT1_PASS_ADR100 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane1 #0, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0061 | [7:0] | R_2WIREPT1_PASS_ADR101 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane1 #0, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0062 | [7:0] | R_2WIREPT1_PASS_ADR110 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane1 #1, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0063 | [7:0] | R_2WIREPT1_PASS_ADR111 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane1 #1, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0064 | [7:0] | R_2WIREPT1_PASS_ADR120 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane1 #2, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0065 | [7:0] | R_2WIREPT1_PASS_ADR121 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane1 #2, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0066 | [7:0] | R_2WIREPT1_PASS_ADR130 | 8 | RW | 2WIRE Pass Through received "before rename" address for Lane1 #3, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0067 | [7:0] | R_2WIREPT1_PASS_ADR131 | 8 | RW | 2WIRE Pass Through "after renamed" address to send for Lane1 #3, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |
| 0x0068 | [7:0] | R_2WIREPT2_NOPASS_ADR10 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #0, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x0069 | [7:0] | R_2WIREPT2_NOPASS_ADR11 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #1, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006A | [7:0] | R_2WIREPT2_NOPASS_ADR12 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #2, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006B | [7:0] | R_2WIREPT2_NOPASS_ADR13 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #3, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006C | [7:0] | R_2WIREPT2_NOPASS_ADR14 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #4, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006D | [7:0] | R_2WIREPT2_NOPASS_ADR15 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #5, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006E | [7:0] | R_2WIREPT2_NOPASS_ADR16 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #6, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x006F | [7:0] | R_2WIREPT2_NOPASS_ADR17 | 8 | RW | 2WIRE Pass Through ignore address /otherwise All Through for Lane1 #7, being active only at R_2WIREPT_MODE[0]=1. | 8'd0 |
| 0x0070 | [7:0] | R_2WIREPT1_PASS_ADRIN1 | 8 | RW | 2WIRE Pass Through counterpart Sub-Link Slave internal access dedicated address for Lane1, being active only at R_2WIREPT_MODE[0]=0. | 8'd0 |

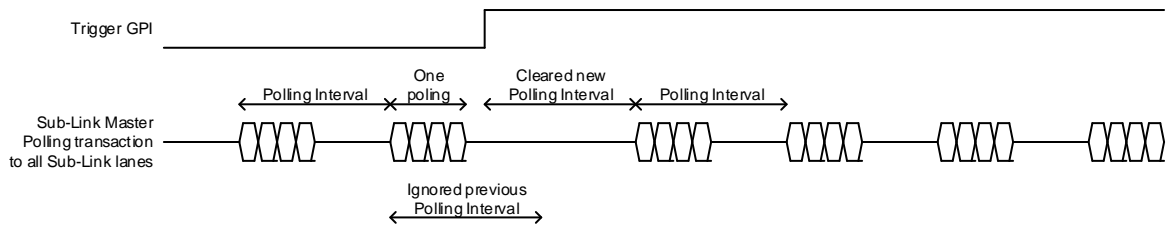
6.3.6. Sub-Link transaction time accuracy Improvement

Sub-Link Polling timing can be controllable by GPI input. All Sub-Link lane transaction timing can be arranged.

Table 14. Sub-Link transaction time accuracy control

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|------------------|-------|-----|---|---------|
| 0x0016 | [7:6] | reserved | 2 | - | - | - |
| | [5:4] | R_POL_TIM_CLR_EN | 2 | RW | Polling Timer Clear/Mask Enable 0:Disable 1:Polling Timer Clear by GPI mode Enable 2:Polling Timer Mask by GPI mode Enable 3:Disable | 2'd0 |
| | [3] | reserved | 1 | - | - | - |
| | [2:0] | R_GPI_TRG_SEL | 3 | RW | Polling Timer Clear/Mask GPI select 0:GPI0, 1:GPI1, 2:GPI2, 3:GPI3, 4:GPI4, 5:GPI5, 6:GPI6, 7:GPI7 *Only 0and1 are available at 2-wire mode1 (R_SLINK_MODE[1:0]=2'd1) | 3'd0 |

Polling Timer Clear



Polling Timer Mask

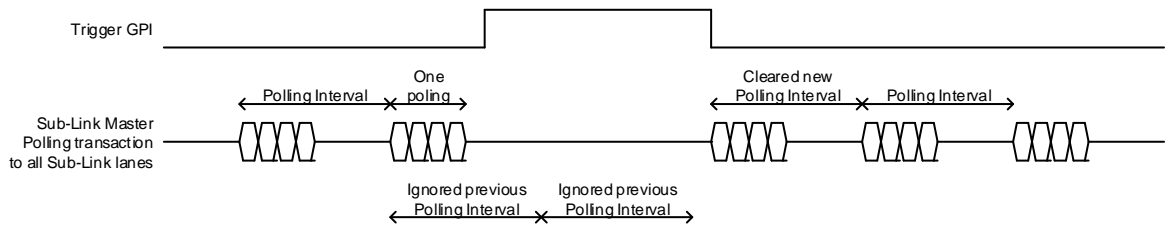


Figure 10. Sub-Link transaction time accuracy control

6.4. GPIO setting

Setting of GPIO can be configurable by 2-wire access to internal register.

Table 15. GPIO setting 1/2

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|---------------|-------|-----|------|--|
| 0x10 01 | [7:4] | R_GPIO7_MODE | 4 | R/W | 4'h0 | GPIO7 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 01 | [3:0] | R_GPIO6_MODE | 4 | R/W | 4'h0 | GPIO6 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 02 | [7:4] | R_GPIO5_MODE | 4 | R/W | 4'h0 | GPIO5 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 02 | [3:0] | R_GPIO4_MODE | 4 | R/W | 4'h0 | GPIO4 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 03 | [7:4] | R_GPIO3_MODE | 4 | R/W | 4'h0 | GPIO3 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 03 | [3:0] | R_GPIO2_MODE | 4 | R/W | 4'h0 | GPIO2 I/O Mode 0:Disable 1:Programmable GPO (Output Low) 2:Programmable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |

Table 16. GPIO setting 2/2

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|---------------|-------|-----|------|---|
| 0x10 04 | [7:4] | R_GPIO1_MODE | 4 | R/W | 4'h0 | GPIO1 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |
| 0x10 04 | [3:0] | R_GPIO0_MODE | 4 | R/W | 4'h0 | GPIO0 I/O Mode 0:Disable 1:Programable GPO (Output Low) 2:Programable GPO (Output High) 3:Through GPI Mode 4:Through GPO Mode 5:Second 2WIRE Mode (SCL) 6:Second 2WIRE Mode (SDA) 7-F:Reserved |

6.4.1. Register GPIO

GPIO output control are available with register.

6.4.2. Through GPIO

Local GPIO input is continuously reflected to remote GPIO output via Sub-Link polling. Bridging data are sampled every Sub-Link polling, whose basic interval is controlled by register R_SLINK_POL_TIM_UP/DN. Remote 2-wire access may become long transaction and could lengthen Through GPIO polling reflection interval.

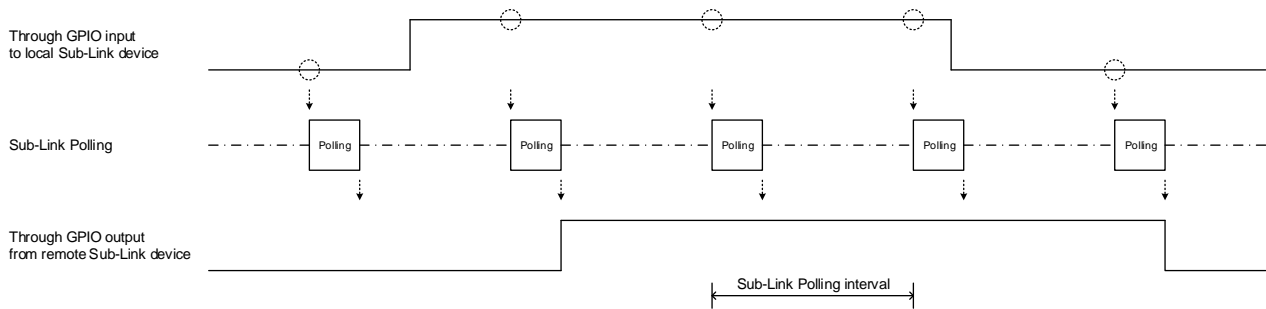


Figure 11. Through GPIO bridge sampling

As default setting with THCV231 as Sub-Link Slave communication (THCV242 as Sub-Link Master), GPIO1 Sub-Link Polling bridges input to THCV231-GPIO4 Through Mode and GPIO0 Sub-Link Polling bridges input to THCV231-GPIO3 Through Mode respectively.

As default setting with THCV241 as Sub-Link Slave communication (THCV242 as Sub-Link Master), GPIO0/1 are dedicated to GPI to Sub-Link Lane0. GPIO2/3 are dedicated to GPI to Sub-Link Lane1. GPIO2/3 are also dedicated to GPO from selected Sub-Link Lane.

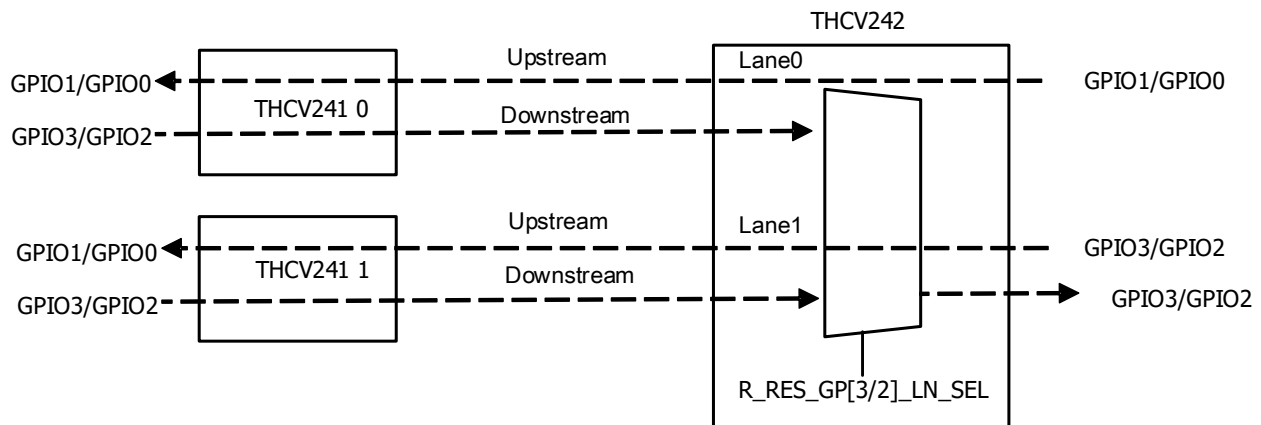


Figure 12. Through GPIO via Sub-Link transaction assignment with THCV241

Remote UART bridge is supported with Sub-Link Through GPIO input/output. Remote UART Tx and Rx bridge baud rate is supposed to be designed against Sub-Link Polling interval to accommodate deterministic jitter caused by intermittent Sub-Link communication timing.



6.4.3. GPIO as secondary 2-wire port

GPIO port can be secondary 2-wire port, which can accommodate dual 2-wire access from two processors.

6.5. MIPI

6.5.1. Deserializer and CSI-2 Formatter

6.5.1.1. PLL setting

PLL setting is required. PLL setting set R_PLL_SETTING[47:0] is related with Main-Link data-rate.

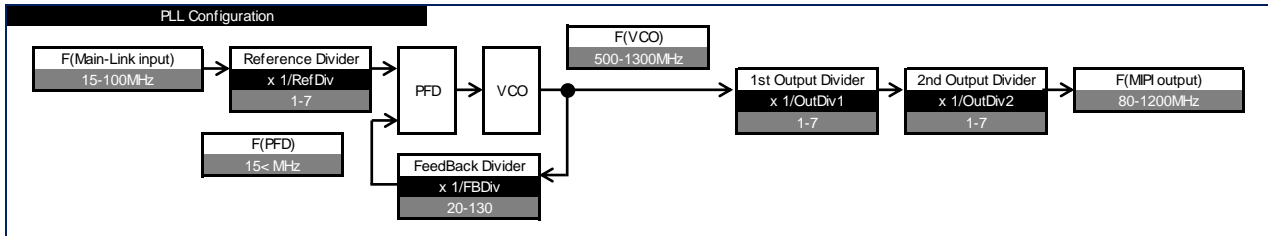


Figure 1 Reference clock supply basic method

PLL_SETTING[47:0] must be selected proper to meet below constraints.

Table 1 PLL constraints

| symbol | discription | min | typ | max | unit |
|---------|---|-----|-----|-------|------|
| F(IN) | PLL input pixel clock frequency | 10 | - | 133.3 | MHz |
| RefDiv | Reference Divider value | 1 | - | 7 | - |
| FBDiv | FeedBack Divider value | 20 | - | 130 | - |
| OutDiv1 | 1st Output Divider value (OutDiv1 must be >= OutDiv2) | 1 | - | 7 | - |
| OutDiv2 | 2nd Output Divider value (OutDiv1 must be >= OutDiv2) | 1 | - | 7 | - |
| F(PFD) | PFD frequency | 10 | - | | MHz |
| F(VCO) | VCO frequency | 500 | - | 1300 | MHz |
| F(OUT) | PLL output pixel clock frequency | 80 | - | 1200 | MHz |

Pixel clock frequency made by PLL is calculated as below.

$$[\text{PCLK.input}] = \text{Pixel clock recovered on V-by-One® HS per lane} = [\text{F(Main-Link input)}] = \text{F(IN)}$$

$$[\text{F(Main-Link input)}] = \text{Main-Link data-rate per lane} / (\text{Byte mode} \times 8 \times 10/8)$$

$$\begin{aligned} \text{MIPI data-rate per lane (Mbps)} &= [\text{F(MIPI output)}] \text{ (MHz)} \\ &= \text{MIPI High Speed mode data-rate per lane} \end{aligned}$$

$$\text{F(VCO)} = \frac{[\text{F(Main-Link input)}] \times [\text{FBDiv}]}{[\text{RefDiv}]}$$

$$[\text{PCLK.output}] = [\text{F(MIPI output)}] = \frac{[\text{F(Main-Link input)}] \times [\text{FBDiv}]}{[\text{RefDiv}] \times [\text{OutDiv1}] \times [\text{OutDiv2}]} = \text{F(OUT)}$$

$$\frac{[\text{F(MIPI output)}]}{[\text{F(Main-Link input)}]} = \frac{[\text{FBDiv}]}{[\text{RefDiv}] \times [\text{OutDiv1}] \times [\text{OutDiv2}]}$$

$$\text{MIPI High Speed mode DDR output clock per lane} = [\text{F(MIPI output)}] / 2 \text{ (MHz)}$$

Table 2 PLL setting

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|----------------------|-------|-----|------|--|
| 0x10 21 | [7:0] | R_PLL_SETTING[47:40] | 8 | R/W | 8'h0 | PLL setting value, Feedback Divider value (integer part) |
| 0x10 22 | [7:3] | R_PLL_SETTING[39:35] | 5 | - | 5'h0 | PLL setting value (Must be set 0) |
| 0x10 22 | [2:0] | R_PLL_SETTING[34:32] | 3 | R/W | 3'h0 | PLL setting value, Reference Divider value |
| 0x10 23 | [7] | R_PLL_SETTING[31] | 1 | - | 1'h0 | PLL setting value (Must be set 0) |
| 0x10 23 | [6:4] | R_PLL_SETTING[30:28] | 3 | R/W | 3'h0 | PLL setting value, OutDiv1 (OutDiv1 must be >= OutDiv2) |
| 0x10 23 | [3] | R_PLL_SETTING[27] | 1 | - | 1'h0 | PLL setting value (Must be set 0) |
| 0x10 23 | [2:0] | R_PLL_SETTING[26:24] | 3 | R/W | 3'h0 | PLL setting value, OutDiv2 (OutDiv1 must be >= OutDiv2) |
| 0x10 24 | [7:0] | R_PLL_SETTING[23:16] | 8 | R/W | 8'h0 | PLL setting value, Feedback Divider value (decimal part MSB) |
| 0x10 25 | [7:0] | R_PLL_SETTING[15:8] | 8 | R/W | 8'h0 | PLL setting value, Feedback Divider value (decimal part) |
| 0x10 26 | [7:0] | R_PLL_SETTING[7:0] | 8 | R/W | 8'h0 | PLL setting value, Feedback Divider value (decimal part LSB) |

PLL setting must fulfill below frequency ratio rule.

Table 3 PLL frequency ratio rule

| Format | $\frac{[F(\text{MPI output})]}{[F(\text{Main-Link input})]}$ frequency ratio |
|---------------|--|
| MPRF | $\frac{1 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RGB888 | $\frac{3/4 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| YUV422 Normal | $\frac{2/4 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| YUV422 Demux | $\frac{1 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW8 Normal | $\frac{2/4 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW8 Demux | $\frac{1 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW10 Normal | $\frac{10/32 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW10 Demux | $\frac{20/32 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW12 Normal | $\frac{12/32 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |
| RAW12 Demux | $\frac{24/32 * [\text{Main-Link input lane#}] * 4 * 8}{[\text{MPI output lane#}]}$ |

Below Table is Look Up Table example for typical cases.

Table 4 PLL setting Look Up Table example

| Index | condition | Main-Link input | MPI output | Distribution | F(MLINK in) | F(VCO) | F(MPI out) | PLL[47:40] | PLL[39:32] | PLL[31:24] | PLL[23:16] | PLL[15:8] | PLL[7:0] |
|-------|-------------------|------------------------------|-------------------|--------------|-------------|--------|------------|------------|------------|------------|------------|-----------|----------|
| 1 | 720p30fps RAW | 742.5Mbps 1lane MPRF | 594Mbps x1lane | off | 18.5625 | 1188 | 594 | 0x40 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 3 | 720p30fps YUV422 | 750Mbps 1lane MPRF | 600Mbps x1lane | off | 18.75 | 1200 | 600 | 0x40 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 4 | 720p60fps RAW | 1.114Gbps 1lane MPRF | 445.5Mbps x2lane | off | 27.84375 | 891 | 445.5 | 0x20 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 5 | 1080p30fps RAW | 1.114Gbps 1lane MPRF | 445.5Mbps x2lane | off | 27.84375 | 891 | 445.5 | 0x20 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 6 | 720p60fps YUV422 | 1.485Gbps 1lane MPRF | 594Mbps x2lane | off | 37.125 | 1188 | 594 | 0x20 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 7 | 1080p30fps YUV422 | 1.485Gbps 1lane MPRF | 594Mbps x2lane | off | 37.125 | 1188 | 594 | 0x20 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 8 | 720p60fps YUV422 | 1.485Gbps 1lane MPRF | 594Mbps x2lane x2 | on | 37.125 | 1188 | 594 | 0x20 | 0x01 | 0x21 | 0x00 | 0x00 | 0x00 |
| 9 | 720p120fps RAW | 2.2275Gbps 1lane MPRF | 891Mbps x2lane | off | 55.6875 | 891 | 891 | 0x20 | 0x02 | 0x11 | 0x00 | 0x00 | 0x00 |
| 10 | 1080p60fps RAW | 2.2275Gbps 1lane MPRF | 891Mbps x2lane | off | 55.6875 | 891 | 891 | 0x20 | 0x02 | 0x11 | 0x00 | 0x00 | 0x00 |
| 11 | 720p120fps YUV422 | 2.97Gbps 1lane MPRF | 594Mbps x4lane | off | 74.25 | 1188 | 594 | 0x20 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |
| 12 | 1080p60fps YUV422 | 2.97Gbps 1lane MPRF | 594Mbps x4lane | off | 74.25 | 1188 | 594 | 0x20 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |
| 13 | 1080p120fps RAW | 2.2275Gbps 2lane MPRF | 891Mbps x4lane | off | 55.6875 | 891 | 891 | 0x20 | 0x02 | 0x11 | 0x00 | 0x00 | 0x00 |
| 15 | 720p30fps RAW | 990Mbps 1lane RAW12 Demux | 594Mbps x1lane | off | 24.75 | 594 | 594 | 0x18 | 0x01 | 0x11 | 0x00 | 0x00 | 0x00 |
| 17 | 720p30fps YUV422 | 1.6Gbps 1lane YUV422 Normal | 640Mbps x1lane | off | 40 | 640 | 640 | 0x20 | 0x02 | 0x11 | 0x00 | 0x00 | 0x00 |
| 18 | 720p60fps RAW | 1.485Gbps 1lane RAW12 Demux | 445.5Mbps x2lane | off | 37.125 | 891 | 445.5 | 0x30 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |
| 19 | 1080p30fps RAW | 1.485Gbps 1lane RAW12 Demux | 445.5Mbps x2lane | off | 37.125 | 891 | 445.5 | 0x30 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |
| 20 | 720p60fps YUV422 | 2.97Gbps 1lane YUV422 Normal | 594Mbps x2lane | off | 74.25 | 1188 | 594 | 0x20 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |
| 21 | 1080p30fps YUV422 | 2.97Gbps 1lane YUV422 Normal | 594Mbps x2lane | off | 74.25 | 1188 | 594 | 0x20 | 0x02 | 0x21 | 0x00 | 0x00 | 0x00 |

6.5.1.2. Video stream switch and copy/distribution

Setting of data stream handling can be configurable by 2-wire access to internal register.

Table 17. Data stream handling setting

| Address | bit | Register Name | R/W | Initial | Description |
|---------|-------|---------------|-----|-----------|--|
| 0x1501 | [7:5] | - | - | 3'b000 | Reserved |
| | [4:0] | R_MODE_NO | R/W | 5'b0000_0 | Main-Link input data stream handling mode number 5'd0,1,2,3,8,10,11 are available. Others: reserved |

Table 18. Data stream handling mode

| Handling R_MODE_NO | Input Camera | Distribution | Output port | Output sw ap | Input | | Output | |
|-----------------------|-----------------|--------------|-------------|--------------|-------------|-------------|--------|--------|
| | | | | | Main-Link_0 | Main-Link_1 | MIPL_0 | MIPL_1 |
| 5'd0 | 1 | Disable | 1 | - | Cam A | - | Cam A | - |
| 5'd1 | 1 | Enable | 2 | - | Cam A | - | Cam A | Cam A |
| 5'd2 | 1 | Disable | 1 | - | - | Cam B | Cam B | - |
| 5'd3 | 1 | Enable | 2 | - | - | Cam B | Cam B | Cam B |
| 5'd8 | 1(2port) | Disable | 1 | - | Cam A | Cam A | Cam A | - |
| 5'd10 | 2 | - | 2 | Disable | Cam A | Cam B | Cam A | Cam B |
| 5'd11 | 2 | - | 2 | Enable | Cam A | Cam B | Cam B | Cam A |

6.5.2. Header/Packet/Sync Pre-processing

Setting of Header, Packet and Sync pre-processing can be configurable by 2-wire access to internal register. Settings of Header, Packet and Sync pre-processing exist for each Main-Link input lanes respectively.

Table 19. Header/Packet/Sync pre-processing setting for Main-Link Lane0 example

| Address | bit | Register Name | R/W | Initial | Description |
|---------|-------|--------------------|-----|---------|--|
| 0x1100 | [7:1] | - | - | 7'h00 | Reserved |
| | [0] | R_VX1_PH_EN0 | R/W | 1'b0 | Main-Link Lane0 Input MIPI Packet Header intake 1'b0: Packet Header from Main-Link Lane0 not used 1'b1: Packet Header from Main-Link Lane0 input |
| 0x1101 | [7:1] | - | - | 7'h00 | Reserved |
| | [0] | R_VX1_CRC_EN0 | R/W | 1'b0 | Main-Link Lane0 Input CRC intake 1'b0: CRC from Main-Link Lane0 not used 1'b1: CRC from Main-Link Lane0 input |
| 0x1102 | [7:1] | - | - | 7'h00 | Reserved |
| | [0] | R_VX1_SP_EN0 | R/W | 1'b0 | Main-Link Lane0 Input MIPI Short Packet intake 1'b0: Short Packet from Main-Link Lane0 not used 1'b1: Short Packet from Main-Link Lane0 input |
| 0x1103 | [7:1] | - | - | 7'h00 | Reserved |
| | [0] | R_VX1_VVALID_MODE0 | R/W | 1'b0 | Main-Link Lane0 to MIPI VVALID generation mode 1'b0: mode1 (available with THCV241) 1'b1: mode2 (FS/FE generation from VSYNC) |
| 0x1104 | [7:1] | - | - | 7'h00 | Reserved |
| | [0] | R_VX1_VSYNC_POL0 | R/W | 1'b0 | Main-Link Lane0 VSYNC intake polarity 1'b0: Low active / VSYNC=Low pulse 1'b1: High active / VSYNC=High pulse |
| 0x1105 | [7:0] | R_VX1_WC_LOW0 | R/W | 8'h00 | Main-Link Lane0 to MIPI Word Count (LSB 8bit) manual setting (Only active when R_VX1_PH_EN=0) |
| 0x1106 | [7:0] | R_VX1_WC_UP0 | R/W | 8'h00 | Main-Link Lane0 to MIPI Word Count (MSB 8bit) manual setting (Only active when R_VX1_PH_EN=0) |
| 0x1107 | [7:0] | R_VX1_DATAID0 | R/W | 8'h00 | Main-Link Lane0 to MIPI Data ID manual setting (Only active when R_VX1_PH_EN=0) |

6.5.3. MIPI output setting

Setting of MIPI output can be configurable by 2-wire access to internal register.

Table 20. MIPI output setting 1/2

| Address | bit | Register Name | R/W | Initial | Description |
|---------|-------|----------------|-----|--------------|---|
| 0x1600 | [7:5] | - | - | 3'b000 | Reserved |
| | [4:0] | R_ANALOG | R/W | 5'h00 | [4] MIPI Power Down 0: Power Down 1: Normal operation [3] MIPI Soft Reset 0: Reset 1: Normal operation [2] ReservedL: Must be set 0 [1] ReservedH: Must be set 1 [0] ReservedL: Must be set 0 |
| 0x1602 | [7:0] | R_TX_LANE_SELO | R/W | 8'b1110_0100 | MIPI Tx Lane assignment select (SWAP) [7:6]Lane3, [5:4]Lane2, [3:2]Lane1, [1:0]Lane0 2'b00:1st Byte output 2'b01:2nd Byte output 2'b10:3rd Byte output 2'b11:4th Byte output *On 2port output configuration, 3rd and 4th Byte are 2nd PORT1 *On 2port 1lane output configuration, 1st and 3rd Byte are used |
| 0x1603 | [7:1] | - | - | 7'h00 | Reserved |
| | [1:0] | R_TX_LANE_SEL1 | R/W | 2'b00 | MIPI 2port output 2nd PORT1 select (Select 3rd Byte assigned 2nd PORT1 TX lane) |
| 0x1605 | [7] | - | - | 1'b0 | Reserved |
| | [6:0] | R_LANE_EN | R/W | 7'b0101_011 | [6:5] MIPI Data lane Enable [6] Data PORT1 / 0:OFF, 1:ON [5] Data PORT0 / 0:OFF, 1:ON [4:3] MIPI CLK lane Enable [4] CLK lane1 / 0:OFF, 1:ON [3] CLK lane0 / 0:OFF, 1:ON [2:0] MIPI Configuration 3'b000:1PORT1LANE 3'b001:1PORT2LANE 3'b010:Reserved 3'b011:1PORT4LANE 3'b100:2PORT1LANE 3'b101:2PORT2LANE 3'b110:Reserved 3'b111:Reserved |

Table 21. MIPI output setting 2/2

| Address | bit | Register Name | R/W | Initial | Description |
|---------|-------|-------------------|-----|-------------|--|
| 0x1606 | [7] | - | - | 1'b0 | Reserved |
| | [6:0] | R_MODE_SET | R/W | 7'b100_0000 | [6] ReservedH: Must be set 1 [5:4] ReservedL: Must be set 0 [3:2] HBLANK CLK OFF [3] HBLANK CLK OFF PORT1 0:OFF (HS clock off and go into LP at HBlank) 1:ON (HS clock continuously on at HBlank) [2] HBLANK CLK OFF PORT0 0:OFF (HS clock off and go into LP at HBlank) 1:ON (HS clock continuously on at HBlank) [1:0] CLK_NOT_STOP [1] CLK_NOT_STOP PORT1 0:OFF (HS clock off at VBlank) 1:ON (HS clock permanently on) [0] CLK_NOT_STOP PORT0 0:OFF (HS clock off at VBlank) 1:ON (HS clock permanently on) "7'b100_1100" is typical usage |
| 0x1609 | [7:0] | R_TX_CLK_PREPARE0 | R/W | 8'd4 | CLK lane PrePare period setting PORT0 |
| 0x160a | [7:0] | R_TX_CLK_ZERO0 | R/W | 8'h1d | CLK lane ZERO period setting PORT0 |
| 0x160b | [7:0] | R_TX_CLK_TRAILO | R/W | 8'h07 | CLK lane TRAIL period setting PORT0 |
| 0x160c | [7:0] | R_TX_CLK_PRE0 | R/W | 8'h02 | CLK lane PRE period setting PORT0 |
| 0x160d | [7:0] | R_TX_CLK_POST0 | R/W | 8'h0c | CLK lane POST period setting PORT0 |
| 0x160e | [7:0] | R_TX_THS_EXIT0 | R/W | 8'h0b | Data lane EXIT period setting PORT0 |
| 0x160f | [7:0] | R_TX_TLPX0 | R/W | 8'h05 | Data lane TLPX period setting PORT0 |
| 0x1610 | [7:0] | R_TX_THS_PREPARE0 | R/W | 8'h04 | Data lane Prepare period setting PORT0 |
| 0x1611 | [7:0] | R_TX_THS_ZERO0 | R/W | 8'h10 | Data lane ZERO period setting PORT0 |
| 0x1612 | [7:0] | R_TX_THS_TRAILO | R/W | 8'h07 | Data lane TRAIL period setting PORT0 |
| 0x1614 | [7:0] | R_TX_CLK_PREPARE1 | R/W | 8'h04 | CLK lane PrePare period setting PORT1 |
| 0x1615 | [7:0] | R_TX_CLK_ZERO1 | R/W | 8'h1d | CLK lane ZERO period setting PORT1 |
| 0x1616 | [7:0] | R_TX_CLK_TRAIL1 | R/W | 8'h07 | CLK lane TRAIL period setting PORT1 |
| 0x1617 | [7:0] | R_TX_CLK_PRE1 | R/W | 8'h02 | CLK lane PRE period setting PORT1 |
| 0x1618 | [7:0] | R_TX_CLK_POST1 | R/W | 8'h0c | CLK lane POST period setting PORT1 |
| 0x1619 | [7:0] | R_TX_THS_EXIT1 | R/W | 8'h0b | Data lane EXIT period setting PORT1 |
| 0x161a | [7:0] | R_TX_TLPX1 | R/W | 8'h05 | Data lane TLPX period setting PORT1 |
| 0x161b | [7:0] | R_TX_THS_PREPARE1 | R/W | 8'h04 | Data lane Prepare period setting PORT1 |
| 0x161c | [7:0] | R_TX_THS_ZERO1 | R/W | 8'h10 | Data lane ZERO period setting PORT1 |
| 0x161d | [7:0] | R_TX_THS_TRAIL1 | R/W | 8'h07 | Data lane TRAIL period setting PORT1 |
| 0x161f | [7:4] | - | - | 2'b00 | Reserved |
| | [3:0] | R_REQ_SEL | R/W | 4'h0 | MIPI Tx Lane PORT assignment [3]Lane3, [2]Lane2, [1]Lane1, [0]Lane0 0:PORT0 1:PORT1 |

MTX0P/N and MTX2P/N can be assigned to be MIPI 2nd port (port1).

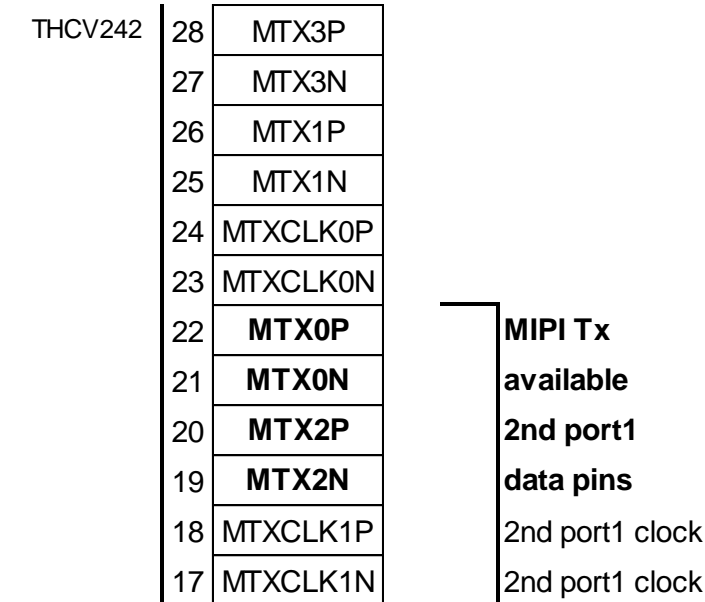


Figure 13. MIPI 2nd port available pins

Setting of MIPI 2port output examples are shown below.

Table 22. MIPI 2port output setting example

| R_TX_LANE_SEL0 | | | | R_TX_LANE_SEL1 | | | | R_LANE_EN | | | R_REQ_SEL | | | | MIPI Physical pin order output assignment | | | | | | |
|----------------|-------|-------|-------|----------------|----|----|-----|-------------|------------|--------|-----------|-------|-------|----------------|---|-------------|----------------|----------------|----------------|-------------|-------|
| lane3 | lane2 | lane1 | lane0 | port1 select | | | | port enable | clk enable | config | lane3 | lane2 | lane1 | lane0 | lane3 | lane1 | lane0 | lane2 | lane0 | lane2 | lane0 |
| [7:6] | [5:4] | [3:2] | [1:0] | [1:0] | | | | [6:5] | [4:3] | [2:0] | [3] | [2] | [1] | [0] | lane3 | lane1 | lane0 | lane2 | lane0 | lane2 | lane0 |
| 01 | 11 | 00 | 10 | 00 | 11 | 11 | 101 | 0 | 1 | 0 | 1 | 0 | 1 | MTX3PN | MTX1PN | MTXCLK0PN | MTX0PN | lane2 | lane0 | MTXCLK1PN | |
| 01 | 11 | 00 | 10 | 00 | 11 | 11 | 101 | 0 | 1 | 0 | 1 | 0 | 1 | port0 2nd Byte | port0 1st Byte | port0 clock | port1 1st Byte | port1 2nd Byte | port1 1st Byte | port1 clock | |
| 00 | 11 | 01 | 10 | 00 | 11 | 11 | 101 | 0 | 1 | 0 | 1 | 0 | 1 | port0 1st Byte | port0 2nd Byte | port0 clock | port1 1st Byte | port1 2nd Byte | port1 1st Byte | port1 clock | |
| 01 | 11 | 00 | 10 | 00 | 11 | 11 | 100 | 0 | 1 | 0 | 1 | 0 | 1 | No output | port0 1st Byte | port0 clock | port1 1st Byte | No output | port1 1st Byte | port1 clock | |
| 01 | 10 | 00 | 11 | 10 | 11 | 11 | 100 | 0 | 1 | 0 | 1 | 0 | 1 | No output | port0 1st Byte | port0 clock | No output | port1 1st Byte | port1 1st Byte | port1 clock | |
| 00 | 11 | 01 | 10 | 00 | 11 | 11 | 100 | 0 | 1 | 0 | 1 | 0 | 1 | port0 1st Byte | No output | port0 clock | port1 1st Byte | No output | port1 1st Byte | port1 clock | |

6.5.4. MIPI CSI-2 Virtual Channel

MIPI Virtual Channel (VC) is supported. When MIPI PH(Packet Header) is intake from V-by-One® HS input, MIPI Virtual Channel information in PH is also bridged from V-by-One® HS at the same time. Virtual Channel information can be intake from Main-Link input and properly applied on MIPI Packet Header by selectable register setting.

6.5.5. Multiple camera synchronization Frame Vsync supply

Frame VSYNC can be supplied from THCV242 to Sub-Link Slave GPO.

EXTSYNC input or internally generated VSYNC become supply source. Settings are configurable by 2-wire access to internal register. When internal VSYNC is selected, generated VSYNC is not only sent to remote Sub-Link Slave but also output from EXTSYNC pin.

Internal VSYNC uses two clock source, internal oscillator clock and video pixel clock from Main-Link input. At the beginning of internal VSYNC generation operation, oscillator clock is used to supply VSYNC. After Main-Link video source is received stable, internal VSYNC generation source is switched to video pixel clock from selected Main-Link input. When Main-Link video pixel clock input is lost, internal VSYNC generator again uses internal oscillator clock until Main-Link video pixel clock input is regained.

Table 23. Multiple camera synchronization Frame Vsync supply setting 1/2

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|----------------|-------|-----|------|---|
| 0x10 07 | [7:4] | reserved | 4 | - | - | - |
| 0x10 07 | [3:0] | R_EXTSYNC_MODE | 4 | R/W | 4'h0 | EXTSYNC I/O Mode 0:Disable 1:Normal Mode (Controlled by Sub-Link Register) 2-F: Reserved |

Table 24. Multiple camera synchronization Frame Vsync supply setting 2/2

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|------------------|-------|-----|---|---------|
| 0x0020 | [7:5] | reserved | 3 | - | - | - |
| | [4] | R_VS_PHASE_EN | 1 | RW | Internal VSYNC supply Phase Shift Enable (R_VS_MODE=2'd2) 0:Disable 1:Enable, Sub-Link phase of each lanes are shifted as below lane1 offset from lane0: R_VS_PHASE_WIDTH | 1'b0 |
| | [3:2] | reserved | 2 | - | - | - |
| | [1:0] | R_VS_MODE | 2 | RW | multiple camera synchronization Frame VSYNC supply mode setting 0: Disable 1: External VSYNC from EXTSYNC to remote camera supply 2: Internal VSYNC to remote camera supply and EXTSYNC pin output supply 3: Disable | 2'd0 |
| 0x0021 | [7:5] | reserved | 3 | - | - | - |
| | [4] | ReservedL | 1 | RW | Must be set 0 | 1'b0 |
| | [3:1] | reserved | 3 | - | - | - |
| | [0] | R_VS_POL | 1 | RW | Internal VSYNC supply polarity (R_VS_MODE=2'd2) 0: Active Low negative polarity at Vertical blanking pulse 1: Active High positive polarity at Vertical blanking pulse | 1'b0 |
| 0x0022 | [7] | reserved | 1 | - | - | - |
| | [6:4] | R_VS_GPI_SEL | 3 | RW | Frame VSYNC supply mode Sub-Link GPI assignment bit on applied Sub-Link port 0:GPI0, 1:GPI1, 2:GPI2, 3:GPI3, 4:GPI4, 5:GPI5, 6:GPI6, 7:GPI7 *only GPI0 or GPI1 are available for 2-wire Set&Trigger mode1 and 2-wire Pass Through mode1 | 3'd0 |
| | [3:2] | ReservedL | 2 | RW | Must be set 0 | 2'd0 |
| | [1:0] | R_VS_LANE_SEL | 2 | RW | Frame VSYNC supply target Sub-Link port [0]:Sub-Link port0; 0:no supply, 1:Frame VSYNC supply [1]:Sub-Link port1; 0:no supply, 1:Frame VSYNC supply | 2'd0 |
| 0x0023 | [7:4] | reserved | 4 | - | - | - |
| | [3:0] | R_VSOOSC_LINE_UP | 4 | RW | Internal VSYNC clock number / line by oscillator setting | 4'd0 |
| 0x0024 | [7:0] | R_VSOOSC_LINE_DN | 8 | RW | Internal VSYNC clock number / line by oscillator = (256xR_VSOOSC_LINE_UP<3:0> +R_VSOOSC_LINE_DN<7:0>+1)xOSC *Clock / line is 1 when R_VSOOSC_LINE_UP=0 and R_VSOOSC_LINE_DN=0 | 8'd15 |
| 0x0025 | [7:0] | R_VSOOSC_WIDTH | 8 | RW | Internal VSYNC pulse width line number by oscillator setting Line Number = R_VSOOSC_WIDTH + 1 (e.g. 0x0 for 1line) | 8'd4 |
| 0x0026 | [7:4] | reserved | 4 | - | - | - |
| | [3:0] | R_VSOOSC_TIM_UP | 4 | RW | Internal VSYNC pulse interval line number by oscillator setting | 4'd0 |
| 0x0027 | [7:0] | R_VSOOSC_TIM_DN | 8 | RW | Internal VSYNC pulse interval line number by oscillator = (256xR_VSOOSC_TIM_UP<3:0> +R_VSOOSC_TIM_DN<7:0>+1)xOSC *Interval line is 2 when R_VSOOSC_TIM_UP=0 and R_VSOOSC_TIM_DN=0 | 8'd15 |
| 0x0028 | [7:2] | reserved | 6 | - | - | - |
| | [1:0] | R_VS_PCLK_SEL | 2 | RW | Internal VSYNC generation base pixel clock domain select 0: CLK_I from Main-Link Lane0 1: CLK_I from Main-Link Lane1 2: Reserved 3: Reserved | 2'd0 |
| 0x0029 | [7:4] | reserved | 4 | - | - | - |
| | [3:0] | R_VSP_LINE_UP | 4 | RW | Internal VSYNC clock number / line by base pixel clock setting | 4'd0 |
| 0x002A | [7:0] | R_VSP_LINE_DN | 8 | RW | Internal VSYNC clock number / line by base pixel clock = (256xR_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)xCLK_I *Clock / line is 1 when R_VSP_LINE_UP=0 and R_VSP_LINE_DN=0 *For setting or reset of this register, R_VS_MODE is supposed to be Disable | 8'd15 |
| 0x002B | [7:0] | R_VSP_WIDTH | 8 | RW | Internal VSYNC pulse width line number by base pixel clock setting Line Number = R_VSP_WIDTH + 1 (e.g. 0x0 for 1line) *For setting or reset of this register, R_VS_MODE is supposed to be Disable | 8'd4 |
| 0x002C | [7:4] | reserved | 4 | - | - | - |
| | [3:0] | R_VSP_TIM_UP | 4 | RW | Internal VSYNC pulse interval line number setting | 4'd0 |
| 0x002D | [7:0] | R_VSP_TIM_DN | 8 | RW | Internal VSYNC pulse interval line number = (256xR_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) Internal VSYNC pulse interval frame period by base pixel clock = (256xR_VSP_TIM_UP<3:0> +R_VSP_TIM_DN<7:0>+1) x (256xR_VSP_LINE_UP<3:0> +R_VSP_LINE_DN<7:0>+1)xCLK_I *Interval line is 2 when R_VSP_TIM_UP=0 and R_VSP_TIM_DN=0 *For setting or reset of this register, R_VS_MODE is supposed to be Disable | 8'd15 |
| 0x002E | [7:0] | R_VS_PHASE_WIDTH | 8 | RW | VSYNC Phase shift difference = 16xR_VS_PHASE_WIDTH<7:0>xCLK_I *Phase shift difference is 16xCLK_I as exception when R_VS_PHASE_WIDTH=0 *For setting or reset of this register, R_VS_PHASE_EN is supposed to be Disable | 8'd1 |
| 0x002F | [7:0] | reserved | 8 | - | - | - |

6.6. Status monitoring, Interrupt and Error Detection

6.6.1. Internal Error / status signal monitoring pin output

Internal error or status signal can be monitored as external ERR0/ERR1 pin output by register setting.

Table 25. Internal Error / status signal monitoring ERR0/ERR1 pin output setting

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|---------------|-------|-----|------|---|
| 0x10 05 | [7:4] | R_ERR1_MODE | 4 | R/W | 4'h0 | ERRR1 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3-F:Reserved |
| 0x10 05 | [3:0] | R_ERR0_MODE | 4 | R/W | 4'h0 | ERRR0 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3-F:Reserved |
| 0x10 0C | [7:0] | R_ERR1_SEL | 8 | R/W | 8'h0 | ERR1 Pin Signal Select |
| 0x10 0D | [7:0] | R_ERR0_SEL | 8 | R/W | 8'h0 | ERR0 Pin Signal Select |

Table 26. IC Internal selectable Error / status signal 1/3

| R_ERR1/0_SEL[7:0] | Error signal | Description |
|-------------------|-----------------------|--|
| 0x00 | 0 Fixed | |
| 0x01 | 1 Fixed | |
| 0x02 | Vx1_LOCKN_ALL | OR operated of all operating lanes |
| 0x03 | Vx1_HTPDN_ALL | OR operated of all operating lanes |
| 0x04 | Vx1_FBETOUT_LATCH_ALL | OR operated of all operating lanes |
| 0x05 | Vx1_FBETOUT_REAL_ALL | OR operated of all operating lanes |
| 0x06 | Vx1_PERR_ALL | OR operated of all operating lanes, protocol error |
| 0x07 | MLINK_CRCERR_ALL | OR operated of all operating lanes |
| 0x08 | Vx1_CLOCKSTP_ALL | clock stop detector of all lanes |
| 0x09 | MLINK_VDSK_OK_ALL | Vsync synchronization OK flag of all lanes |
| 0x0A | MLINK_VDSK_NG_ALL | Vsync synchronization NG flag of all lanes |
| 0x0B | MLINK_DSHNDLRERR_ALL | Data Stream Handler Error of all lanes |
| 0x0C | Reserved | |
| 0x0D | SLINK_PERR_ALL | OR operated of all operating lanes, protocol error |
| 0x0E | SLINK_TMOUT_ALL | OR operated of all operating lanes, time out error |
| 0x0F | SLINK_FBETOUT | OR operated of all operating lanes |
| 0x10 | Vx1_LOCKN0 | lane0 |
| 0x11 | Vx1_LOCKN1 | lane1 |
| 0x12 | Reserved | |
| 0x13 | Reserved | |
| 0x14 | Vx1_HTPDN0 | lane0 |
| 0x15 | Vx1_HTPDN1 | lane1 |
| 0x16 | Reserved | |
| 0x17 | Reserved | |
| 0x18 | Vx1_BETOUT_LATCH0 | lane0 |
| 0x19 | Vx1_BETOUT_LATCH1 | lane1 |
| 0x1A | Reserved | |
| 0x1B | Reserved | |
| 0x1C | Vx1_BETOUT_REAL0 | lane0 |
| 0x1D | Vx1_BETOUT_REAL1 | lane1 |
| 0x1E | Reserved | |
| 0x1F | Reserved | |

Table 27. IC Internal selectable Error / status signal 2/3

| R_ERR1/0_SEL[7:0] | Error signal | Description |
|-------------------|---------------|-----------------------|
| 0x20 | Vx1_PERR0 | lane0, protocol error |
| 0x21 | Vx1_PERR1 | lane1, protocol error |
| 0x22 | Reserved | |
| 0x23 | Reserved | |
| 0x24 | MLINK_CRCERR0 | lane0 |
| 0x25 | MLINK_CRCERR1 | lane1 |
| 0x26 | Reserved | |
| 0x27 | Reserved | |
| 0x28 | MLINK_VSYNC0 | lane0 |
| 0x29 | MLINK_VSYNC1 | lane1 |
| 0x2A | Reserved | |
| 0x2B | Reserved | |
| 0x2C | MLINK_HSYNC0 | lane0 |
| 0x2D | MLINK_HSYNC1 | lane1 |
| 0x2E | Reserved | |
| 0x2F | Reserved | |
| 0x30 | MLINK_DE0 | lane0 |
| 0x31 | MLINK_DE1 | lane1 |
| 0x32 | Reserved | |
| 0x33 | Reserved | |
| 0x34 | MLINK_CLK0 | lane0 |
| 0x35 | MLINK_CLK1 | lane1 |
| 0x36 | Reserved | |
| 0x37 | Reserved | |
| 0x38 | MIPI_BYTECLK | |
| 0x39 | OSCCLK | |
| 0x3A | Reserved | |
| 0x3B | Reserved | |
| 0x3C | Reserved | |
| 0x3D | Reserved | |
| 0x3E | Reserved | |
| 0x3F | Reserved | |

Table 28. IC Internal selectable Error / status signal 3/3

| R_ERR1/0_SEL[7:0] | Error signal | Description |
|-------------------|----------------|--------------------------------------|
| 0x40 | MLINK_FS0 | lane0, Frame Start |
| 0x41 | MLINK_FS1 | lane1, Frame Start |
| 0x42 | Reserved | |
| 0x43 | Reserved | |
| 0x44 | MLINK_FE0 | lane0, Frame End |
| 0x45 | MLINK_FE1 | lane1, Frame End |
| 0x46 | Reserved | |
| 0x47 | Reserved | |
| 0x48 | MLINK_VDSK_NG0 | lane0, Vsync synchronization NG flag |
| 0x49 | MLINK_VDSK_NG1 | lane1, Vsync synchronization NG flag |
| 0x4A | Reserved | |
| 0x4B | Reserved | |
| 0x4C | TOP_CKSUM_ERR | register checksum error |
| 0x4D | Reserved | |
| 0x4E | Reserved | |
| 0x4F | Reserved | |
| 0x50 | Reserved | |
| 0x51 | Reserved | |
| 0x52 | Reserved | |
| 0x53 | Reserved | |
| 0x54 | SLINK_PERR0 | lane0, protocol error |
| 0x55 | SLINK_PERR1 | lane1, protocol error |
| 0x56 | Reserved | |
| 0x57 | Reserved | |
| 0x58 | SLINK_TMOUT0 | lane0, time out error |
| 0x59 | SLINK_TMOUT1 | lane1, time out error |
| 0x5A | Reserved | |
| 0x5B | Reserved | |

6.6.2. Internal Error / status signal monitoring register

Internal error or status signal can be monitored as register read value.

Error count register can be cleared by particular register write “1” access.

Table 29. Internal Error / status signal monitoring register 1/2

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|------------------------|-------|-----|--|---------|
| 0x00F1 | [7:1] | reserved | 7 | - | - | - |
| | [0] | R_SLINK_FBETERR_CLR | 1 | W | Sub-Link FieldBET error count clear 1: Clear | - |
| 0x00F2 | [7:0] | R_SLINK_FBETERR_NUM_UP | 8 | R | Sub-Link FieldBET error count parameter | - |
| 0x00F3 | [7:0] | R_SLINK_FBETERR_NUM_DN | 8 | R | Sub-Link FieldBET error count =256×R_SLINK_FBETERR_NUM_UP<7:0> +R_SLINK_FBETERR_NUM_DN<7:0> | - |

Table 30. Internal Error / status signal monitoring register 2/2

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|-------------------------|-------|-----|------|--|
| 0x17 4F | [7:4] | R_MLINK_CRC_ERRCLR | 4 | W | - | Main-Link CRC Error Counter Clear 1:Clear |
| | [3:0] | R_MLINK_BET_ERRCLR | 4 | W | - | Main-Link BET Error Counter Clear 1:Clear |
| 0x17 50 | [7:0] | MLINK0_CRC_ERRNUM[15:8] | 8 | R | - | Main-Link(Lane0) CRC Error Number (Upper Byte) |
| 0x17 51 | [7:0] | MLINK0_CRC_ERRNUM[7:0] | 8 | R | - | Main-Link(Lane0) CRC Error Number (Lower Byte) |
| 0x17 52 | [7:0] | MLINK1_CRC_ERRNUM[15:8] | 8 | R | - | Main-Link(Lane1) CRC Error Number (Upper Byte) |
| 0x17 53 | [7:0] | MLINK1_CRC_ERRNUM[7:0] | 8 | R | - | Main-Link(Lane1) CRC Error Number (Lower Byte) |
| 0x17 58 | [7:0] | MLINK0_BET_ERRNUM[15:8] | 8 | R | - | Main-Link(Lane0) BET Error Number (Upper Byte) |
| 0x17 59 | [7:0] | MLINK0_BET_ERRNUM[7:0] | 8 | R | - | Main-Link(Lane0) BET Error Number (Lower Byte) |
| 0x17 5A | [7:0] | MLINK1_BET_ERRNUM[15:8] | 8 | R | - | Main-Link(Lane1) BET Error Number (Upper Byte) |
| 0x17 5B | [7:0] | MLINK1_BET_ERRNUM[7:0] | 8 | R | - | Main-Link(Lane1) BET Error Number (Lower Byte) |

6.6.3. Interrupt monitoring

Interrupt (INT1/0) detects occurrence of internal error or status signal and then, latch the detected state.

Interrupt factor can be cleared by particular register* write “1” access. (*They are indicated as “R_INTC_*”)

Interrupt factor can be masked to “0” fixed by particular register appropriate write access.

INT interrupt function is supposed to be cleared before start monitoring any desired status because INT status may change at power on condition and THCV242 internal boot up procedure.

Table 31. Interrupt monitoring

| Register | Address | bit | Description | |
|---------------|-------------------|--|--|----------------------------------|
| R_INTR_MLRX | 0x1710/ 0x1718 | 7 | Reserved | |
| | | 6 | Reserved | |
| | | 5 | MAINLINKRX protocol error for Lane1 | |
| | | 4 | MAINLINKRX protocol error for Lane0 | |
| | | 3 | Reserved | |
| | | 2 | Reserved | |
| | | 1 | MAINLINKRX LOCKN=L to H detection for Lane1 | |
| | | 0 | MAINLINKRX LOCKN=L to H detection for Lane0 | |
| | | R_INTR_MODE | 0x1711/ 0x1719 | 7 |
| R_INTR_DSHDLR | 6 | All MAINLINKRX LOCKN=H detection | | |
| | 5 | Data Stream Handler Distribution error | | |
| R_INTR_FMT | 4 | Data Stream Handler error | | |
| | 3 | Reserved | | |
| | 2 | Reserved | | |
| | 1 | MAINLINKRX CRC error for Lane1 | | |
| R_INTR_CSI | 0x1712/ 0x171A | 1 | | MIPI CSI-2 ULPS END signal PORT1 |
| | | 0 | | MIPI CSI-2 ULPS END signal PORT0 |
| | 0x1713/ 0x171B | 6 | MIPI CSI-2 general error | |
| | | 5 | MIPI CSI-2 EOT error for CLK Lane1 | |
| | | 4 | MIPI CSI-2 EOT error for CLK Lane0 | |
| | | 3 | MIPI CSI-2 SOT error for Data Lane3 | |
| | | 2 | MIPI CSI-2 SOT error for Data Lane2 | |
| | | 1 | MIPI CSI-2 SOT error for Data Lane1 | |
| | | 0 | MIPI CSI-2 SOT error for Data Lane0 | |
| R_INTR_BDC2Q | 0x1714/ 0x171C | 1 | Internal Register AutoCheckSum error flag | |
| | | 0 | All Interrption Clear to remote Sub-Link slave complete flag | |
| | 0x1715/ 0x171D | 7 | Reserved | |
| | | 6 | Reserved | |
| | | 5 | Sub-Link Slave side 2-wire access complete flag for Lane1 | |
| | | 4 | Sub-Link Slave side 2-wire access complete flag for Lane0 | |
| | | 3 | Reserved | |
| | | 2 | Reserved | |
| | 0x1716/ 0x171E | 1 | Sub-Link Slave side interrupt detection flag for Lane1 | |
| | | 0 | Sub-Link Slave side interrupt detection flag for Lane0 | |
| | | 7 | Reserved | |
| | | 6 | Reserved | |
| | | 5 | Sub-Link protocol error for Lane1 | |
| | | 4 | Sub-Link protocol error for Lane0 | |
| | | 3 | Reserved | |
| 2 | Reserved | | | |
| 1 | Reserved | | | |
| 0 | Reserved | | | |

As a register, interrupt detected state is “1” and cleared state is “0”. When multiple interrupt sources are activated, the OR operated result is indicated as IC external INT1/0 pin output.

As an external INT1/0 pin output, open drain output interrupt detected state is “Low” and cleared state is “Hi-Z”, while INT1/0 pin CMOS push-pull output interrupt detected state is “Low” and cleared state is “High”.

Table 32. INT1/0 pin output control

| Adr | bit | Register Name | width | R/W | init | Description |
|---------|-------|---------------|-------|-----|------|--|
| 0x10 06 | [7:4] | R_INT1_MODE | 4 | R/W | 4'h0 | INT1 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3-F:Reserved |
| 0x10 06 | [3:0] | R_INT0_MODE | 4 | R/W | 4'h0 | INT0 I/O Mode 0:Disable 1:OpenDrain Output Mode 2:Push/Pull Output Mode 3-F:Reserved |

INT1/0 interrupt function is supposed to be cleared before start monitoring any desired status because INT1/0 status may have been changed before monitoring activation.

6.6.4. Register Auto Checksum diagnosis

Register values checksum is continuously calculated as R_CKSUM_RVAL.

Table 33. Register Auto Checksum diagnosis control and monitoring

| Addr(h) | bit | Register Name | width | R/W | Description | Default |
|---------|-------|---------------|-------|-----|---|---------|
| 0x0008 | [7:1] | reserved | 7 | - | - | - |
| | [0] | R_CKSUM_EN | 1 | RW | Internal Register AutoCheckSum Enable 0:Disable 1:Enable | 1'b0 |
| 0x0009 | [7:0] | R_CKSUM_TIM | 8 | RW | Internal Register AutoCheckSum check interval =1024x64x(R_CKSUM_TIM<7:0>+1) x tOSC | 8'd19 |
| 0x000A | [7:0] | R_CKSUM_VAL | 8 | RW | Internal Register AutoCheckSum expected target value | 8'd0 |
| 0x000B | [7:0] | R_CKSUM_RVAL | 8 | R | Internal Register AutoCheckSum read value | - |

6.7. Power On Sequence

Power On Sequence must be controlled appropriate.

For Power On Reset, PDN input must be low at the moment when VDDCORE (VDD12) reach operating condition voltage. As a note, PDN pin itself does not belongs to VDDCORE (VDD12) but to VDDIO1 (VDDH). PDN Power On Reset control is mandatory.

MIPI, PLL and V-by-One® HS block are reset state at power on default and require Reset Release.

V-by-One® HS Soft Reset / PLL Soft Reset => MIPI Soft Reset is proper. See below detail.

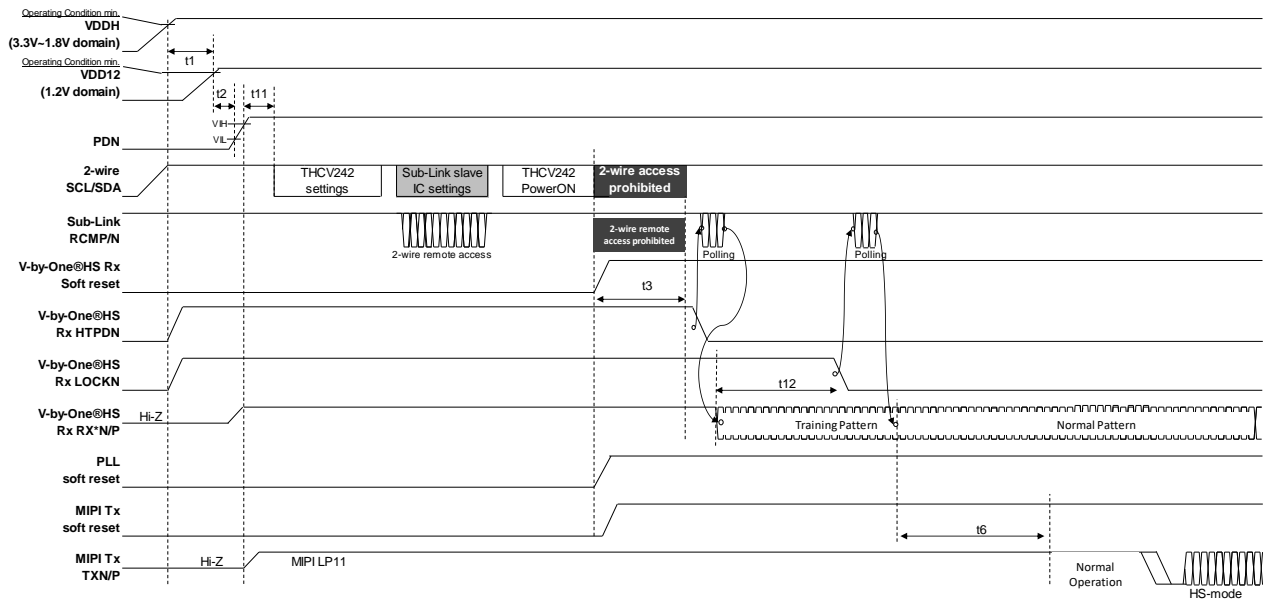


Figure 14. Power On Sequence procedure

Table 34. Power On Sequence specification

| symbol | discription | min | typ | max | unit |
|--------|--|------|-----|------------|------|
| t1 | Required wait from VDD33 assert to VDD12 assert | 0 | - | - | us |
| t2 | Required wait from Power On to PDN High control | 1000 | - | - | us |
| t11 | Required wait from PDN High to Register Access | 300 | - | - | us |
| t3 | Time of V-by-One@HS Rx soft reset High to HTPDN Low | - | - | 10 | us |
| t12 | Time of Training Pattern Input to LOCKN Low | - | - | 980 | us |
| t6 | Time of V-by-One@HS Normal operation input to MIPI normal operation output | - | - | 50+ 1frame | us |

The first MIPI output from Power On waits vertical blanking period and starts output; therefore, MIPI normal operation may be hold for maximum 1frame, which depends on used video format.

6.8. Lock / Re-Lock Sequence

Lock and re-lock sequence are as follows. V-by-One® HS automatically shifts into lock status from initial status or unlock status caused by external noise under appropriate parameter set condition.

THCV242 LOCK Sequence

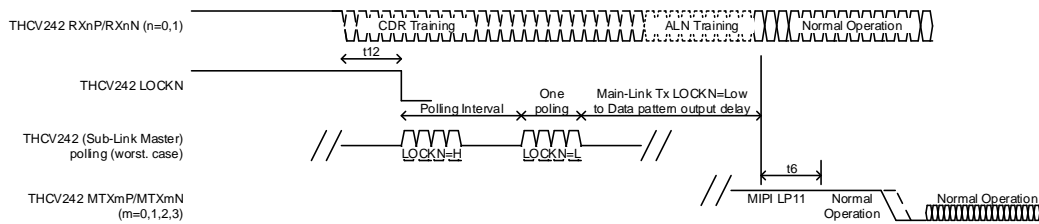


Figure 15. Lock Sequence

THCV242 Re-LOCK Sequence

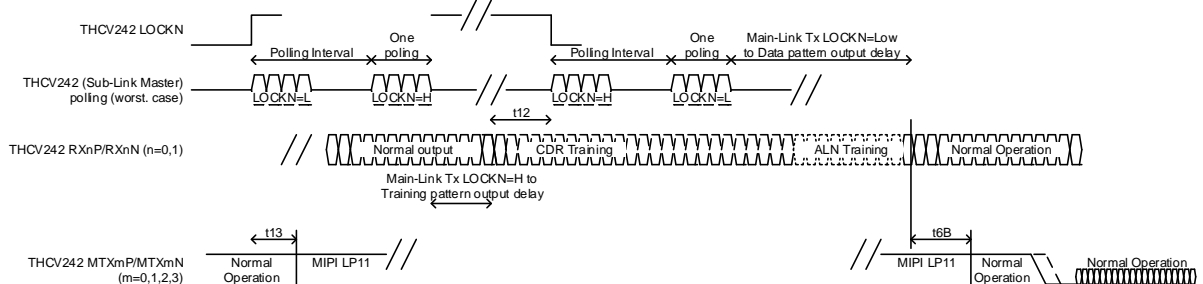


Figure 16. Re-Lock Sequence

Table 35. Lock / Re-Lock Sequence specification

| symbol | discription | min | typ | max | unit |
|--------|--|-----|-----|-----|------|
| t13 | Time of LOCKN=H to MIPI Stand-by LP11 output | - | - | 98 | us |
| t6B | Time of V-by-One®HS Normal operation re-input to MIPI normal operation re-output | - | - | 50 | us |

7. Absolute Maximum Ratings

Table 36. Absolute Maximum Ratings*

| Parameter | min. | typ. | max. | Unit |
|--|------|------|---------------|----------|
| Supply Voltage (VDDIO1,VDDIO2) | -0.3 | - | 4 | V |
| Supply Voltage (VDDCORE,VDDR,X,VDDTX,VDDPLL) | - | - | 1.6 | V |
| LVC MOS Input Voltage (1.2V domain) | -0.3 | - | VDDR,X+0.3 *2 | V |
| LVC MOS Input Voltage (VDDIO1 domain) | -0.3 | - | VDDIO1+0.3 *1 | V |
| LVC MOS Output Voltage | -0.3 | - | VDDIO1+0.3 *1 | V |
| LVC MOS Bi-directional buffer Input Voltage | -0.3 | - | VDDIO1+0.3 *1 | V |
| LVC MOS Bi-directional buffer Output Voltage | -0.3 | - | VDDIO1+0.3 *1 | V |
| LVC MOS Input Voltage (VDDIO2 domain) | -0.3 | - | VDDIO2+0.3 *1 | V |
| CML Receiver Voltage | -0.3 | - | VDDR,X+0.3 *2 | V |
| MIPI Transmitter Voltage | -0.3 | - | VDDTX+0.3 *2 | V |
| CML Bi-directional buffer Input Voltage | -0.3 | - | VDDIO2+0.3 *1 | V |
| CML Bi-directional buffer Output Voltage | -0.3 | - | VDDIO2+0.3 *1 | V |
| Output Current | -30 | - | 30 | mA |
| Storage Temperature | -55 | - | 125 | degC |
| Junction Temperature | - | - | 125 | degC |
| Reflow Peak Temperature/time | - | - | 26 | degC/sec |
| Maximum Power Dissipation @ +25°C | - | - | 3.9 | W |

*1 Max. must be below 4V at the same time

*2 Max. must be below 1.6V at the same time

* “Absolute Maximum Ratings” are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of “Recommended Operating Condition” specify conditions for device operation.

8. Recommended Operating Conditions

Table 37. Recommended Operating Conditions

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|--|------------|-----|-----|-----|------|
| VDDH | Supply Voltage (VDDIO1, VDDIO2) | 3.3V Drive | 3.0 | 3.3 | 3.6 | V |
| | | 2.5V Drive | 2.0 | 2.5 | 3.0 | V |
| | | 1.8V Drive | 1.7 | 1.8 | 2.0 | V |
| VDD12 | Supply Voltage 1.2V (VDDCORE, VDDR,X, VDDTX, VDDPLL) | - | 1.1 | - | 1.3 | V |
| Ta | Operating Ambient Temperature | - | -40 | - | 105 | degC |

9. Consumption Current

Table 38. Consumption Current at Power Down

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|---------------------------|-------------------|-----|-----|-----|------|
| ICCS33 | Power Down Supply Current | PDN=0, VDDH=3.6V | - | 0.1 | - | mA |
| ICCS12 | | PDN=0, VDD12=1.3V | - | 8 | - | mA |

Table 39. Consumption Current of VDDH

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|------------|---------------|-----------------------|-----|-----|-----|------|
| ICCVH_33_1 | VDDIO1/2=3.3V | Sub-Link 1lane active | - | 16 | 20 | mA |
| ICCVH_33_2 | | Sub-Link 2lane active | - | 32 | 38 | mA |
| ICCVH_18_1 | VDDIO1/2=1.8V | Sub-Link 1lane active | - | 14 | 17 | mA |
| ICCVH_18_2 | | Sub-Link 2lane active | - | 27 | 32 | mA |

Table 40. Consumption Current of VDD12

| Symbol | port.in# | port.out# | video format | input | output | min. | typ. | max. | Unit | |
|------------|-------------------|-----------|----------------------|-----------------------------|-------------------------|------------------|------|------|------|----|
| lccw12_01 | 1 | 1 | quasi-1080p low fps | 400Mbps x1lane | 320Mbps x1lane | - | 49 | 111 | mA | |
| lccw12_02 | | | | | 80Mbps x4lane | - | 49 | 109 | mA | |
| lccw12_157 | 2 | | quasi-1080p high fps | 4Gbps x2lane selected | 800Mbps x4lane | - | 177 | 251 | mA | |
| lccw12_03 | 1 | 1 | 720p30fps RAW | 742.5Mbps x1lane | 594Mbps x1lane | - | 60 | 123 | mA | |
| lccw12_04 | | | 720p30fps YUV422 | 1Gbps x1lane | 600Mbps x1lane | - | 64 | 126 | mA | |
| lccw12_05 | | | 720p60fps RAW | 1.11375Gbps x1lane | 445.5Mbps x2lane | - | 65 | 128 | mA | |
| lccw12_06 | | | 1080p30fps RAW | | | | | | | |
| lccw12_07 | | | 720p60fps YUV422 | 1.485Gbps x1lane | 594Mbps x2lane | - | 75 | 139 | mA | |
| lccw12_08 | | | 1080p30fps YUV422 | | | | | | | |
| lccw12_09 | | 2 | | 594Mbps x2lane x2port Dist. | - | 89 | 158 | mA | | |
| lccw12_10 | | 1 | 1 | 720p120fps RAW | 2.2275Gbps x1lane | 891Mbps x2lane | - | 93 | 160 | mA |
| lccw12_11 | | | | 1080p60fps RAW | | 445.5Mbps x4lane | - | 85 | 150 | mA |
| lccw12_12 | | | 720p120fps YUV422 | 2.97Gbps x1lane | 594Mbps x4lane | - | 98 | 165 | mA | |
| lccw12_13 | 1080p60fps YUV422 | | 1188Mbps x2lane | | - | 113 | 184 | mA | | |
| lccw12_14 | 2 | 2 | 1080p120fps RAW | 2.2275Gbps x2lane | 891Mbps x4lane | - | 149 | 238 | mA | |
| lccw12_15 | | | 1080p120fps YUV422 | 3Gbps x2lane | 1200Mbps x4lane | - | 184 | 276 | mA | |
| lccw12_153 | 2 | 2 | 720p30fps RAW | 742.5Mbps x1lane x2port | 594Mbps x1lane x2port | - | 89 | 148 | mA | |
| lccw12_B12 | | | 720p30fps YUV422 | 750Mbps x1lane x2port | 600Mbps x1lane x2port | - | 90 | 148 | mA | |
| lccw12_B13 | | | 720p60fps RAW | 1.11375Gbps x1lane x2port | 445.5Mbps x2lane x2port | - | 102 | 165 | mA | |
| lccw12_31 | | | 1080p30fps RAW | | | | | | | |
| lccw12_33 | | | 720p60fps YUV422 | 1.485Gbps x1lane x2port | 594Mbps x2lane x2port | - | 120 | 186 | mA | |
| lccw12_34 | | | 1080p30fps YUV422 | | | | | | | |
| lccw12_35 | | | 720p120fps RAW | 2.2275Gbps x1lane x2port | 891Mbps x2lane x2port | - | 151 | 219 | mA | |
| lccw12_36 | | | 1080p60fps RAW | | | | | | | |
| lccw12_37 | | | 720p120fps YUV422 | 2.97Gbps x1lane x2port | 1188Mbps x2lane x2port | - | 184 | 258 | mA | |
| lccw12_38 | | | 1080p60fps YUV422 | | | | | | | |
| lccw12_39 | | | | | | | | | | |
| lccw12_402 | | | | | | | | | | |
| lccw12_412 | | | | | | | | | | |

10. DC Specifications

10.1. CMOS DC Specifications

Table 41. CMOS DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-----------------|-----------------------------------|--------------------------|-------------------------|-----|------------------------|------|
| I _{IH} | LVC MOS Input Leak Current High | - | - | - | 10 | uA |
| I _{IL} | LVC MOS Input Leak Current Low | - | - | - | 10 | uA |
| V _{IH} | LVC MOS High Level Input Voltage | V _{DDIOx} =3.3V | 2 | - | V _{DDIO} | V |
| | | V _{DDIOx} =2.5V | 0.70*V _{DDIO} | - | V _{DDIO} | V |
| | | V _{DDIOx} =1.8V | 0.65*V _{DDIO} | - | V _{DDIO} | V |
| V _{IL} | LVC MOS Low Level Input Voltage | V _{DDIOx} =3.3V | 0 | - | 0.8 | V |
| | | V _{DDIOx} =2.5V | 0 | - | 0.30*V _{DDIO} | V |
| | | V _{DDIOx} =1.8V | 0 | - | 0.35*V _{DDIO} | V |
| V _{OH} | LVC MOS High Level Output Voltage | V _{DDIOx} =3.3V | V _{DDIO} -0.6 | - | V _{DDIO} | V |
| | | V _{DDIOx} =2.5V | V _{DDIO} -0.5 | - | V _{DDIO} | V |
| | | V _{DDIOx} =1.8V | V _{DDIO} -0.45 | - | V _{DDIO} | V |
| V _{OL} | LVC MOS Low Level Output Voltage | - | 0 | - | 0.45 | V |

10.2. CML Receiver DC Specifications

Table 42. CML Receiver DC Specifications

| Symbol | Parameter | Condition | min. | typ. | max. | Unit |
|-------------------|---------------------------------------|--|------|------|------|------|
| V _{RTH} | CML Differential Input High Threshold | - | - | - | 50 | mV |
| V _{RTL} | CML Differential Input Low Threshold | - | -50 | - | - | mV |
| I _{RIH} | CML Input Leak Current High | P _{DN} =L, R _{XP/N} =1.2V | - | - | ±15 | uA |
| I _{RIL} | CML Input Leak Current Low | P _{DN} =L, R _{XP/N} =GND | - | - | ±15 | uA |
| I _{RRIH} | CML Input Current High | R _{XP/N} =1.2V | - | - | 1.6 | mA |
| I _{RRIL} | CML Input Current Low | R _{XP/N} =GND | -4.6 | - | - | mA |
| R _{RIN} | CML Differential Input Resistance | - | 80 | 100 | 120 | ohm |

10.3. MIPI Transmitter DC Specifications

Table 43. MIPI Transmitter DC Specifications

| Symbol | Parameter | Condition | min. | typ. | max. | Unit |
|---------------|-------------------------------------|---------------|-------|------|------|---------|
| Γ_{IL} | Input Leak Current Low | PDN=0 | -10 | - | 10 | μ A |
| Γ_{IH} | Input Leak Current High | PDN=0 | -10 | - | 10 | μ A |
| VTCMTX | HS-mode statics Common-mode Voltage | ZID=80~125ohm | 160 | 200 | 240 | mV |
| VTOD | HS-mode Differential Voltage | ZID=100ohm | 150 | 200 | 260 | mV |
| VTOHHS | HS-mode High Level Output Voltage | ZID=100ohm | - | - | 350 | mV |
| VTOHLP | LP-mode High Level Output Voltage | - | 1.1 | - | 1.3 | V |
| VTOLLP | LP-mode Low Level Output Voltage | - | -0.05 | - | 0.05 | V |
| ZTOLP | LP-mode Output Impedance | - | 120 | - | - | ohm |

10.4. CML Bi-directional Buffer DC Specifications

Table 44. CML Bi-directional Buffer DC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|--|--|------|---------|-----|------|
| VBTH | CML Bi-Directional Buffer Differential Input High Threshold | R_BDCZ_HYS=0 | - | - | 50 | mV |
| | | R_BDCZ_HYS=1 | - | - | 150 | mV |
| VBTL | CML Bi-Directional Buffer Differential Input Low Threshold | R_BDCZ_HYS=0 | -50 | - | - | mV |
| | | R_BDCZ_HYS=1 | -150 | - | - | mV |
| VBIC | CML Bi-Directional Buffer Input Terminated Common Voltage | R_BDCZ_TERM_** [1:0]= 2'b00 R_BDCZ_DRIVE_** DRIVE[1:0]= 2'b00 | - | VDD-300 | - | mV |
| IBIH | CML Bi-Directional Buffer Output Leak Current High | TCMP/N=VDD | -10 | - | 10 | uA |
| IBIL | CML Bi-Directional Buffer Output Leak Current Low | TCMP/N=0V | -10 | - | 10 | uA |
| VBOD | CML Bi-Directional Buffer Differential Output Voltage | R_BDCZ_TERM_** [1:0]=2'b10 R_BDCZ_DRIVE_** [1:0]=2'b10 Diff. 100ohm terminated | 200 | 300 | 400 | mV |
| VBOC | CML Bi-Directional Buffer Common Output Voltage | R_BDCZ_TERM_** [1:0]=2'b00 R_BDCZ_DRIVE_** [1:0]=2'b00 | - | VDD-300 | - | mV |
| IBOZ | CML Bi-Directional Buffer TRI-STATE Current | PDN1=0 | -10 | - | 10 | uA |
| RTERM | CML Bi-Directional Buffer Termination Registance | R_BDCZ_TERM_TX/ RX [1:0]=2'b10 | - | 50 | - | ohm |
| | | R_BDCZ_TERM_TX/ RX [1:0]=2'b01 | - | 100 | - | ohm |
| | | R_BDCZ_TERM_TX/ RX [1:0]=2'b00 | - | 200 | - | ohm |
| IDRIVE | CML Bi-Directional Buffer Drive Current | R_BDCZ_DRIVE_TX/ RX [1:0]=2'b10 | - | 12 | - | mA |
| | | R_BDCZ_DRIVE_TX/ RX [1:0]=2'b01 | - | 6 | - | mA |
| | | R_BDCZ_DRIVE_TX/ RX [1:0]=2'b00 | - | 3 | - | mA |

11. AC Specifications

11.1. General AC Specifications

Table 45. General AC Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|--------------|---|---------|-------|---------|------|
| tDL | Data Latency | MainLink 1Gbps Data stream handling mode1 | Typ.-98 | 16000 | Typ.+98 | ns |

11.2. CML Receiver AC Specifications

Table 46. CML Receiver AC Specifications

| Symbol | Parameter | Condition | min. | typ. | max. | Unit |
|--------|---------------|-----------|------|------|------|------|
| tRBIT | Unit Interval | - | 250 | - | 2500 | ps |
| | | | 0.4 | - | 4 | Gbps |

11.3. MIPI Transmitter AC Specifications

Table 47. MIPI Transmitter AC Specifications

| Symbol | Parameter | Conditions | min. | typ. | max. | Unit |
|--------|------------------|------------|-------|------|------|------|
| tTBIT | Tx Unit Interval | - | 0.833 | - | 12.5 | ns |
| | | | 80 | - | 1200 | Mbps |

11.4. CML B-directional Buffer AC Specifications

Table 48. CML B-directional Buffer AC Specifications

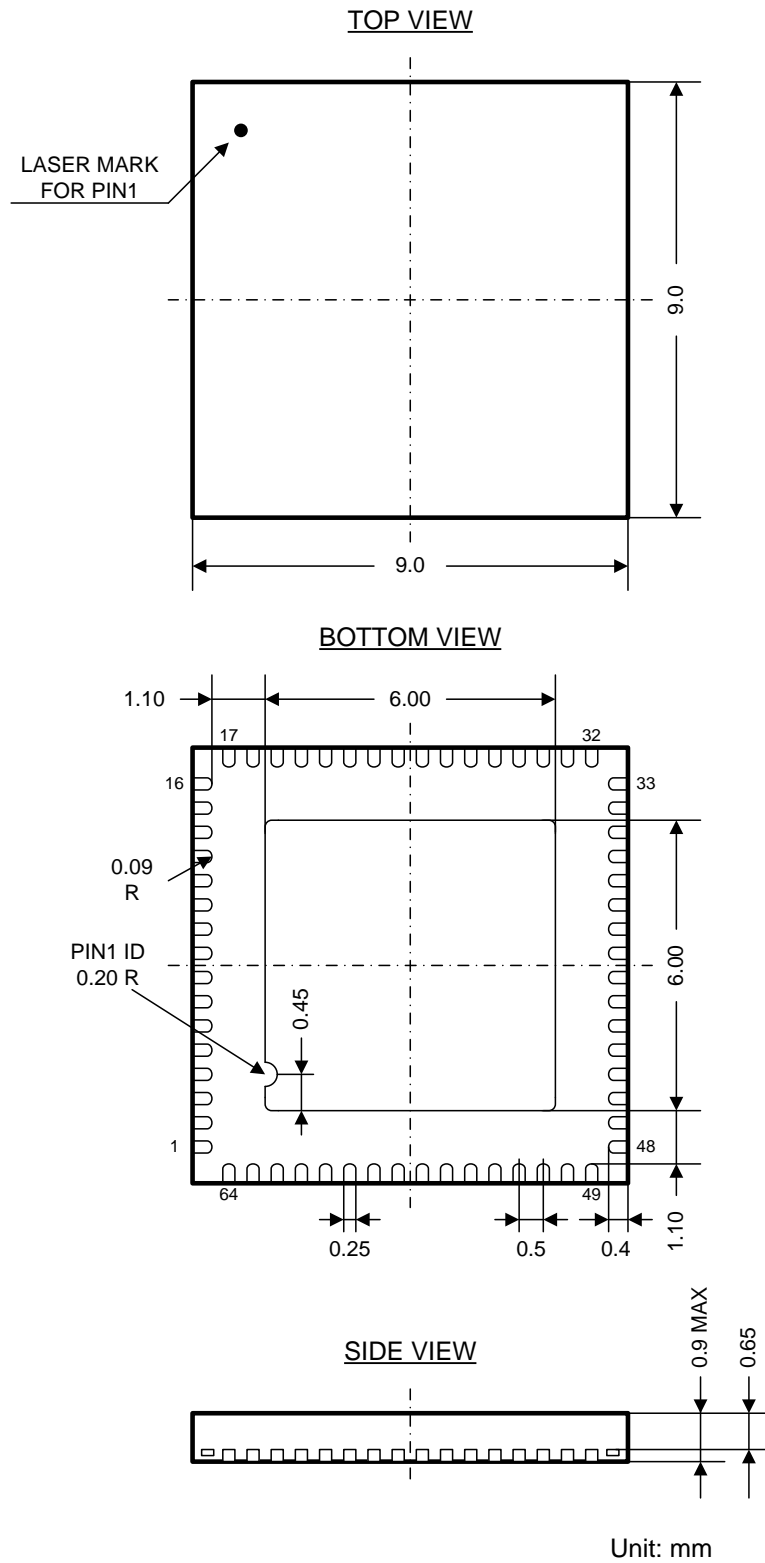
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|---|-----------|-------|-------|-------|------|
| tBUI | Bi-Directional CML Buffer Unit Interval | - | 128.7 | 137.5 | 172.7 | ns |

11.5. 2-wire serial Slave AC Specifications

Table 49. 2-wire serial Slave AC Specifications (Sub-Link Master)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--------|------------------------------------|-----------|------|------|------|------|
| tOSC | Cycle of internal oscillator clock | - | 11.7 | 12.5 | 15.7 | ns |
| fSCL | SCL clock frequency | - | - | - | 1000 | kHz |

12. Package





13. Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.
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 - 5.1 Application of this product is intended for and limited to the following applications: audio-video device, office automation device, communication device, consumer electronics, smartphone, feature phone, and amusement machine device. This product must not be used for applications that require extremely high-reliability/safety such as aerospace device, traffic device, transportation device, nuclear power control device, combustion chamber device, medical device related to critical care, or any kind of safety device.
 - 5.2 This product is not intended to be used as an automotive part, unless the product is specified as a product conforming to the demands and specifications of IATF16949 ("the Specified Product") in this data sheet. THine accepts no liability whatsoever for any product other than the Specified Product for it not conforming to the aforementioned demands and specifications.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.
9. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act.
10. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

Contact:

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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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