

Description

The 8T49N287 has two independent, fractional-feedback PLLs that can be used as jitter attenuators and frequency translators. It is equipped with six integer and two fractional output dividers, allowing the generation of up to 8 different output frequencies, ranging from 8kHz to 1GHz. Four of these frequencies are completely independent of each other and the inputs. The other four are related frequencies. The eight outputs may select among LVPECL, LVDS, HCSL, or LVCMOS output levels.

This makes it ideal to be used in any frequency translation application, including 1G, 10G, 40G and 100G Synchronous Ethernet, OTN, and SONET/SDH, including ITU-T G.709 (2009) FEC rates. The device may also behave as a frequency synthesizer.

The 8T49N287 accepts up to two differential or single-ended input clocks and a crystal input. Each of the two internal PLLs can lock to different input clocks which may be of independent frequencies. Each PLL can use the other input for redundant backup of the primary clock, but in this case, both input clocks must be related in frequency.

The device supports hitless reference switching between input clocks. The device monitors all input clocks for Loss of Signal (LOS), and generates an alarm when an input clock failure is detected. Automatic and manual hitless reference switching options are supported. LOS behavior can be set to support gapped or un-gapped clocks.

The 8T49N287 supports holdover for each PLL. The holdover has an initial accuracy of ± 50 ppB from the point where the loss of all applicable input reference(s) has been detected. It maintains a historical average operating point for each PLL that may be returned to in holdover at a limited phase slope.

The device places no constraints on input to output frequency conversion, supporting all FEC rates, including the new revision of ITU-T Recommendation G.709 (2009), most with 0ppm conversion error.

Each PLL has a register-selectable loop bandwidth from 1.4Hz to 360Hz.

Each output supports individual phase delay settings to allow output-output alignment.

The device supports Output Enable inputs and Lock, Holdover and LOS status outputs.

The device is programmable through an I²C interface. It also supports I²C master capability to allow the register configuration to be read from an external EEPROM.

Typical Applications

- OTN or SONET / SDH equipment Line cards (up to OC-192, and supporting FEC ratios)
- OTN de-mapping (Gapped Clock and DCO mode)
- Gigabit and Terabit IP switches / routers including support of Synchronous Ethernet
- SyncE (G.8262) applications
- Wireless base station baseband
- Data communications
- 100G Ethernet

Features

- Supports SDH/SONET and Synchronous Ethernet clocks including all FEC rate conversions
- <0.3ps RMS Typical jitter (including spurs), 12kHz to 20MHz
- Operating modes: locked to input signal, holdover and free-run
- Initial holdover accuracy of ± 50 ppb
- Accepts up to two LVPECL, LVDS, LVHSTL, HCSL, or LVCMOS input clocks
 - Accepts frequencies ranging from 8kHz up to 875MHz
 - Auto and manual input clock selection with hitless switching
 - Clock input monitoring, including support for gapped clocks
- Phase-Slope Limiting and Fully Hitless Switching options to control output phase transients
- Operates from a 10MHz to 40MHz fundamental-mode crystal
- Generates 8 LVPECL / LVDS / HCSL or 16 LVCMOS output clocks
 - Output frequencies ranging from 8kHz up to 1.0GHz (diff)
 - Output frequencies ranging from 8kHz to 250MHz (LVCMOS)
- Four General Purpose I/O pins with optional support for status & control:
 - Four Output Enable control inputs may be mapped to any of the eight outputs
 - Lock, Holdover and Loss-of-Signal status outputs
- Open-drain Interrupt pin
- Nine programmable loop bandwidth settings for each PLL from 1.4Hz to 360Hz
 - Optional Fast Lock function
- Programmable output phase delays in steps as small as 16ps
- Register programmable through I²C or via external I²C EEPROM
- Bypass clock paths for system tests
- Power supply modes
 - $V_{CC} / V_{CCA} / V_{CCO}$
 - 3.3V / 3.3V / 3.3V
 - 3.3V / 3.3V / 2.5V
 - 3.3V / 3.3V / 1.8V (LVCMOS)
 - 2.5V / 2.5V / 3.3V
 - 2.5V / 2.5V / 2.5V
 - 2.5V / 2.5V / 1.8V (LVCMOS)
- -40°C to 85°C ambient operating temperature
- Package: 56QFN, lead-free (RoHS 6)

8T49N287 Block Diagram

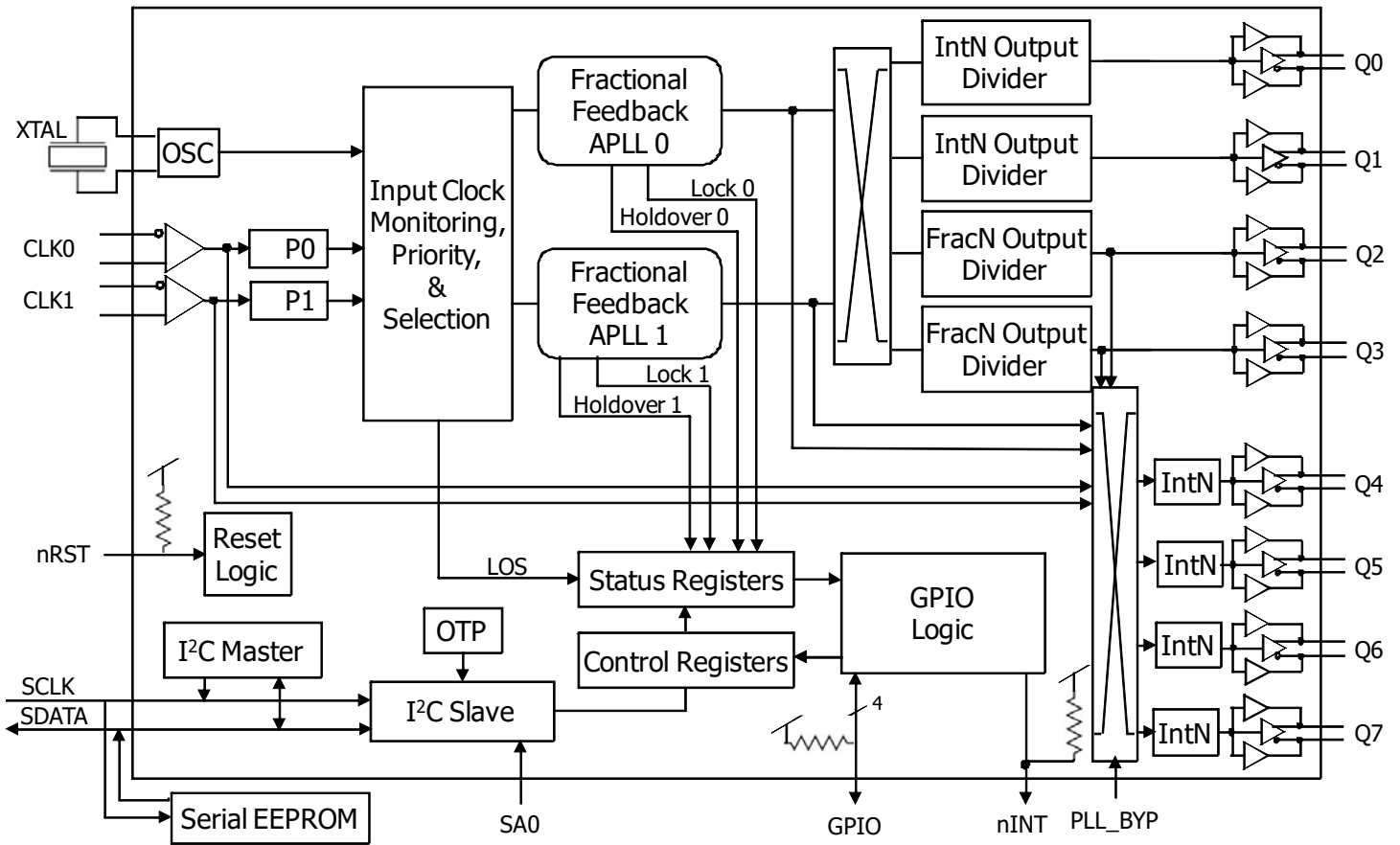
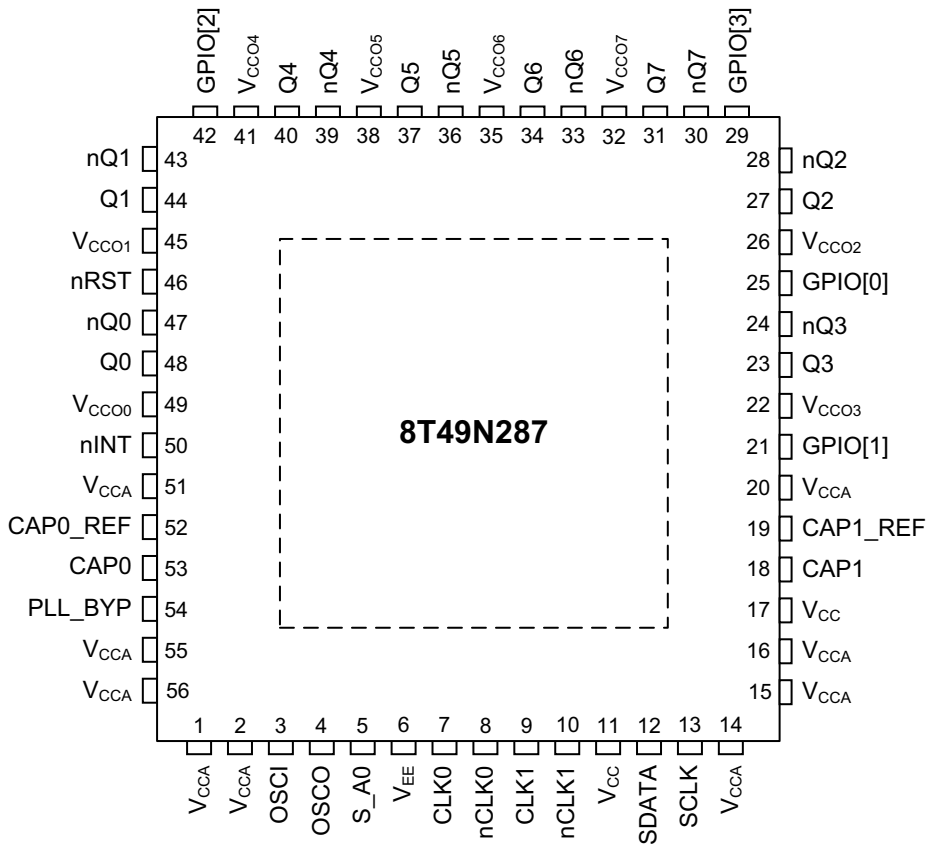


Figure 1. 8T49N287 Functional Block Diagram

Pin Assignment



56-pin, 8mm x 8mm VFQFN Package

Figure 2. Pinout Drawing

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|----------------|------------|-------|------------------------|---|
| 3 | OSCI | I | | Crystal Input. Accepts a 10MHz-40MHz reference from a clock oscillator or a 12pF fundamental mode, parallel-resonant crystal. |
| 4 | OSCO | O | | Crystal Output. This pin should be connected to a crystal. If an oscillator is connected to OSCI, then this pin must be left unconnected. |
| 5 | S_A0 | I | Pulldown | I ² C lower address bit A0. |
| 12 | SDATA | I/O | Pullup | I ² C interface bi-directional Data. |
| 13 | SCLK | I/O | Pullup | I ² C interface bi-directional Clock. |
| 7 | CLK0 | I | Pulldown | Non-inverting differential clock input. |
| 8 | nCLK0 | I | Pullup / Pulldown | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.) |
| 9 | CLK1 | I | Pulldown | Non-inverting differential clock input. |
| 10 | nCLK1 | I | Pullup / Pulldown | Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pullup and pulldown resistors.) |
| 48, 47 | Q0, nQ0 | O | Universal | Output Clock 0. Please refer to the Output Drivers section for more details. |
| 44, 43 | Q1, nQ1 | O | Universal | Output Clock 1. Please refer to the Output Drivers section for more details. |
| 27, 28 | Q2, nQ2 | O | Universal | Output Clock 2. Please refer to the Output Drivers section for more details. |
| 23, 24 | Q3, nQ3 | O | Universal | Output Clock 3. Please refer to the Output Drivers section for more details. |
| 40, 39 | Q4, nQ4 | O | Universal | Output Clock 4. Please refer to the Output Drivers section for more details. |
| 37, 36 | Q5, nQ5 | O | Universal | Output Clock 5. Please refer to the Output Drivers section for more details. |
| 34, 33 | Q6, nQ6 | O | Universal | Output Clock 6. Please refer to the Output Drivers section for more details. |
| 31, 30 | Q7, nQ7 | O | Universal | Output Clock 7. Please refer to the Output Drivers section for more details. |
| 46 | nRST | I | Pullup | Master Reset input. LVTTTL / LVCMOS interface levels: 0 = All registers and state machines are reset to their default values 1 = Device runs normally |
| 50 | nINT | O | Open-drain with pullup | Interrupt output. |
| 29, 42, 21, 25 | GPIO[3:0] | I/O | Pullup | General-purpose input-outputs. LVTTTL / LVCMOS Input levels Open-drain output. Pulled-up with 5.1k Ω resistor to V_{CC} . |
| 54 | PLL_BYP | I | Pulldown | Bypass Selection. Allow input references to bypass both PLLs. LVTTTL / LVCMOS interface levels. |
| 6, ePad | V_{EE} | Power | | Negative supply voltage. All V_{EE} pins and EPAD must be connected before any positive supply voltage is applied. |
| 11 | V_{CC} | Power | | Core and digital functions supply voltage. |
| 17 | V_{CC} | Power | | Core and digital functions supply voltage. |
| 2 | V_{CCA} | Power | | Analog functions supply voltage for core analog functions. |
| 14, 15, 16, 20 | V_{CCA} | Power | | Analog functions supply voltage for analog functions associated with PLL1. |
| 1, 51, 55, 56 | V_{CCA} | Power | | Analog functions supply voltage for analog functions associated with PLL0. |
| 49 | V_{CCO0} | Power | | High-speed output supply voltage for output pair Q0, nQ0. |
| 45 | V_{CCO1} | Power | | High-speed output supply voltage for output pair Q1, nQ1. |
| 26 | V_{CCO2} | Power | | High-speed output supply voltage for output pair Q2, nQ2. |
| 22 | V_{CCO3} | Power | | High-speed output supply voltage for output pair Q3, nQ3. |

| Number | Name | Type | Description |
|----------|-------------------|--------|---|
| 41 | V _{CCO4} | Power | High-speed output supply voltage for output pair Q4, nQ4. |
| 38 | V _{CCO5} | Power | High-speed output supply voltage for output pair Q5, nQ5. |
| 35 | V _{CCO6} | Power | High-speed output supply voltage for output pair Q6, nQ6. |
| 32 | V _{CCO7} | Power | High-speed output supply voltage for output pair Q7, nQ7. |
| 53 52 | CAP0, CAP0_REF | Analog | PLL0 External Capacitance. |
| 18 19 | CAP1, CAP1_REF | Analog | PLL1 External Capacitance. |

NOTE: Pullup and Pulldown refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

Table 2. Pin Characteristics, V_{CC} = V_{CCOX} = 3.3V±5% or 2.5V±5%

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|---|--------------------------------------|--------------------------------------|---------|---------|-------|
| C _{IN} | Input Capacitance; NOTE 1 | | | 3.5 | | pF |
| R _{PULLUP} | Internal Pullup Resistor | nRST, SDATA, SCLK | | 51 | | kΩ |
| | | nINT | | 50 | | kΩ |
| | | GPIO[3:0] | | 5.1 | | kΩ |
| R _{PULLDOWN} | Internal Pulldown Resistor | | | 51 | | kΩ |
| C _{PD} | Power Dissipation Capacitance (per output pair) | LVC MOS; Q[0:1], Q[4:7] | V _{CCOX} = 3.465V | 14.5 | | pF |
| | | LVC MOS Q[2:3] | V _{CCOX} = 3.465V | 18.5 | | pF |
| | | LVC MOS; Q[0:1], Q[4:7] | V _{CCOX} = 2.625V | 13 | | pF |
| | | LVC MOS; Q[2:3] | V _{CCOX} = 2.625V | 17.5 | | pF |
| | | LVC MOS; Q[0:1], Q[4:7] | V _{CCOX} = 1.89V | 12.5 | | pF |
| | | LVC MOS; Q[2:3] | V _{CCOX} = 1.89V | 17 | | pF |
| | | LVDS, HCSL or LVPECL; Q[0:1], Q[4:7] | V _{CCOX} = 3.465V or 2.625V | 2 | | pF |
| | | LVDS, HCSL or LVPECL; Q[2:3] | V _{CCOX} = 3.465V or 2.625V | 4.5 | | pF |
| R _{OUT} | Output Impedance | GPIO [3:0] | Output HIGH | 5.1 | | kΩ |
| | | | Output LOW | 25 | | Ω |
| | | LVC MOS; Q[0:7], nQ[0:7] | | 20 | | Ω |

NOTE: V_{CCOX} denotes: V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4}, V_{CCO5}, V_{CCO6}, V_{CCO7}.

NOTE 1: This specification does not apply to OSCI and OSCO pins.

Principles of Operation

The 8T49N287 has two PLLs that can each independently be locked to any of the input clocks and generate a wide range of synchronized output clocks.

It incorporates two completely independent PLLs. These could be used for example in the transmit and receive path of Synchronous Ethernet equipment. Either of the input clocks can be selected as the reference for either PLL. From the output of the two PLLs a wide range of output frequencies can be simultaneously generated.

The 8T49N287 accepts up to two differential input clocks ranging from 8kHz up to 875MHz. It generates up to eight output clocks ranging from 8kHz up to 1.0GHz.

Each PLL path within the 8T49N287 supports three states: Lock, Holdover and Free-run. Lock & holdover status may be monitored on register bits and pins. Each PLL also supports automatic and manual hitless reference switching. In the locked state, the PLL locks to a valid clock input and its output clocks have a frequency accuracy equal to the frequency accuracy of the input clock. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. Each of the PLL paths within the 8T49N287 has an initial holdover frequency offset of ± 50 ppb. In the Free-run state, the PLL outputs a clock with the same frequency accuracy as the external crystal.

Upon power up, each PLL will enter Free-run state, in this state it generates output clocks with the same frequency accuracy as the external crystal. The 8T49N287 continuously monitors each input for activity (signal transitions).

In automatic reference switching, when an input clock has been validated the PLL will transition to the locked state. If the selected input clock fails and there are no other valid input clocks, the PLL will quickly detect that and go into holdover. In the Holdover state, the PLL will output a clock which is based on the selected holdover behavior. If the selected input clock fails and another input clock is available then the 8T49N287 will hitlessly switch to that input clock. The reference switch can be either revertive or non-revertive.

The device supports conversion of any input frequency to four different, independent output frequencies on the Q[0:3] outputs. Additionally, a further four output frequencies may be generated that are integer-related to the four independent frequencies. These additional four frequencies are on the Q[4:7] outputs.

The 8T49N287 has a programmable loop bandwidth from 1.4Hz to 360Hz.

The device monitors all input clocks and generates an alarm when an input clock failure is detected.

The device supports programmable individual output phase adjustments in order to allow control of input to output phase adjustments and output to output phase alignment.

The device is programmable through an I²C and may also autonomously read its register settings from an internal One-Time Programmable (OTP) memory or an external serial I²C EEPROM.

Crystal Input

The crystal input on the 8T49N287 is capable of being driven by a parallel-resonant, fundamental mode crystal with a frequency range of 10MHz - 40MHz.

The oscillator input also supports being driven by a single-ended crystal oscillator or reference clock.

The initial holdover frequency offset is set by the device, but the long term drift depends on the quality of the crystal or oscillator attached to this port.

Bypass Path

For system test purposes, each of PLL0 and PLL1 may be bypassed. When PLL_BYP is asserted the CLK0 input reference will be presented directly on the Q4 output. The CLK1 input reference will be presented directly on the Q5 output.

Additionally, CLK0 or CLK1 may be used as a clock source for the output dividers of Q[4:7]. This may only be done for input frequencies of 250MHz or less.

Input Clock Selection

The 8T49N287 accepts up to two input clocks with frequencies ranging from 8kHz up to 875MHz. Each input can accept LVPECL, LVDS, LVHSTL, HCSL or LVCMOS inputs using 1.8V, 2.5V or 3.3V logic levels. To use LVCMOS inputs, refer to the Application Note, [Wiring the Differential Input to Accept Single-Ended Levels](#) for biasing instructions.

The device has independent input clock selection control for each PLL. In Manual mode, only one of these inputs may be chosen per PLL and if that input fails that PLL will enter holdover.

Manual mode may be operated by directly selecting the desired input reference in the REFSEL register field. It may also operate via pin-selection of the desired input clock by selecting that mode in the REFSEL register field. In that case, GPIOs must be used as Clock Select inputs (CSELn). CSEL0 = 0 will select the CLK0 input and CSEL0 = 1 will select the CLK1 input for PLL0. CSEL1 will perform the same function for PLL1.

In addition, the crystal frequency may be passed directly to the output dividers for Q[4:7] for use as a reference.

Inputs do not support transmission of spread-spectrum clocking sources. Since this family is intended for high-performance applications, it will assume input reference sources to have stabilities of ± 100 ppm or better, except where gapped clock inputs are used.

If the PLL is working in automatic mode, then each of the input reference sources is assigned a priority of 1-2. At power-up or if the currently selected input reference fails, the PLL will switch to the highest priority input reference that is valid at that time (see Input Clock Monitor section for details).

Automatic mode has two sub-options: revertive or non-revertive. In revertive mode, the PLL will switch to a reference with a higher priority setting whenever one becomes valid. In non-revertive mode the PLL remains with the currently selected source as long as it remains valid.

The clock input selection is based on the input clock priority set by the Clock Input Priority control registers. It is recommended that all input references for a PLL be given different priority settings in the Clock Input Priority control registers for that PLL.

Input Clock Monitor

Each clock input is monitored for Loss of Signal (LOS). If no activity has been detected on the clock input within a user-selectable time period then the clock input is considered to be failed and an internal Loss-of-Signal status flag is set, which may cause an input switchover depending on other settings. The user-selectable time period has sufficient range to allow a gapped clock missing many consecutive edges to be considered a valid input.

User-selection of the clock monitor time-period is based on a counter driven by a monitor clock. The monitor clock is fixed at the frequency of PLL0's VCO divided by 8. With a VCO range of 3GHz - 4GHz, the monitor clock has a frequency range of 375MHz to 500MHz.

The monitor logic for each input reference will count the number of monitor clock edges indicated in the appropriate Monitor Control register. If an edge is received on the input reference being monitored, then the count resets and begins again. If the target edge count is reached before an input reference edge is received, then an internal soft alarm is raised and the count re-starts. During the soft alarm period, the PLL(s) tracking this input will not be adjusted. If an input reference edge is received before the count expires for the second time, then the soft alarm status is cleared and the PLL(s) will resume adjustments. If the count expires again without any input reference edge being received, then a Loss-of-Signal alarm is declared.

It is expected that for normal (non-gapped) clock operation, users will set the monitor clock count for each input reference to be slightly longer than the nominal period of that input reference. A margin of 2-3 monitor clock periods should give a reasonably quick reaction time and yet prevent false alarms.

For gapped clock operation, the user will set the monitor clock count to a few monitor clock periods longer than the longest expected clock gap period. The monitor count registers support 17-bit count values, which will support at least a gap length of two clock periods for any supported input reference frequency, with longer gaps being supported for faster input reference frequencies. Since gapped clocks usually occur on input reference frequencies above 100MHz, gap lengths of thousands of periods can be supported.

Using this configuration for a gapped clock, the PLL will continue to adjust while the normally expected gap is present, but will freeze once the expected gap length has been exceeded and alarm after twice the normal gap length has passed.

Once a LOS on any of the input clocks is detected, the appropriate internal LOS alarm will be asserted and it will remain asserted until that input clock returns and will be validated by the receipt of 8 rising clock edges on that input reference. If another error condition on the same input clock is detected during the validation time then the alarm remains asserted and the validation time starts over.

Each LOS flag may also be reflected on one of the GPIO[3:0] outputs. Changes in status of any reference can also generate an interrupt if not masked.

Holdover

8T49N287 supports a small initial holdover frequency offset for each PLL path in non-gapped clock mode. When the input clock monitor is set to support gapped clock operation, this initial holdover frequency offset is indeterminate since the desired behavior with gapped clocks is for the PLL to continue to adjust itself even if clock edges are missing. In gapped clock mode, the PLL will not enter holdover until the input is missing for two LOS monitor periods.

The holdover performance characteristics of a clock are referred as its accuracy and stability, and are characterized in terms of the fractional frequency offset. The 8T49N287 can only control the initial frequency accuracy. Longer-term accuracy and stability are determined by the accuracy and stability of the external oscillator.

When a PLL loses all valid input references, it will enter the holdover state. In non-gapped clock mode, the PLL will initially maintain its most recent frequency offset setting and then transition at a rate dictated by its selected phase-slope limit setting to a frequency offset setting that is based on historical settings.

This behavior is intended to compensate for any frequency drift that may have occurred on the input reference before it was detected to be lost.

The historical holdover value will have three options:

- Return to center of tuning range within the VCO band.
- Instantaneous mode - the holdover frequency will use the DPLL current frequency 100msec before it entered holdover. The accuracy is shown in the [AC Electrical Characteristics, Table 11A](#).
- Fast average mode - an internal IIR (Infinite Impulse Response) filter is employed to get the frequency offset. The IIR filter gives a 3 dB attenuation point corresponding to a nominal period of 20 minutes. The accuracy is shown in the [AC Electrical Characteristics, Table 11A](#).

When entering holdover, each PLL will set a separate internal HOLD alarm internally. This alarm may be read from internal status register, appear on the appropriate GPIO pin and/or assert the nINT output.

While a PLL is in holdover, its frequency offset is now relative to the crystal input and so the output clocks derived from that PLL will be tracing their accuracy to the local oscillator or crystal. At some point in time, depending on the stability & accuracy of that source, the clock(s) derived from that PLL will have drifted outside of the limits of the holdover state and the system will be considered to be in a free-run state. Since this borderline is defined outside the PLL and dictated by the accuracy and stability of the external local crystal or oscillator, the 8T49N287 cannot know or influence when that transition occurs. As a result, the 8T49N287 will remain in the holdover state internally.

Input to Output Clock Frequency

The 8T49N287 is designed to accept any frequency in its input range and generate eight different output frequencies that are independent from each other and from the input frequencies. The internal architecture of the device ensures that most such translations will result in the exact output frequency specified. Where exact frequency translation is not possible, the frequency translation error will be minimized. Please contact IDT for configuration software or other assistance in determining if a desired configuration will be supported exactly.

Synthesizer Mode Operation

The device may also act as a frequency synthesizer with either or both PLL's generating their operating frequency from just the crystal input. By setting the SYN_MODEn register bit and setting the STATEn[1:0] field to Freerun, no input clock references are required to generate the desired output frequencies.

Loop Filter and Bandwidth

When operating in Synthesizer Mode as described above, the 8T49N287 has a fixed loop bandwidth of approximately 200kHz. When operating in all other modes, the following information applies:

The 8T49N287 uses no external components to support a range of loop bandwidths: 1.40625Hz, 2.8125Hz, 5.625Hz, 11.25Hz, 22.5Hz, 45Hz, 90Hz, 180Hz or 360Hz. Each PLL shall support separate loop filter settings.

The device supports two different loop bandwidth settings for each PLL: acquisition and locked. These loop bandwidths are selected from the list of options described above. If enabled, the acquisition bandwidth is used while lock is being acquired to allow the PLL to “fast-lock”. Once locked the PLL will use the locked bandwidth setting. If the acquisition bandwidth setting is not used, the PLL will use the locked bandwidth setting at all times.

Output Dividers and Mapping to PLLs

The 8T49N287 will support eight output dividers that may be mapped to either PLL. Six of the output dividers will have IntN capability only (see [Table 3](#)) and the other two will support FracN division.

Integer Output Divider Programming (Q[0:1], Q[4:7] only)

Each integer output divider block consists of two divider stages in a series to achieve the desired total output divider ratio. The first stage divider may be set to divide by 4, 5 or 6. The second stage of the divider may be bypassed (i.e. divide-by-1) or programmed to any even divider ratio from 2 to 131,070. The total divide ratios, settings and possible output frequencies are shown in [Table 3](#).

In addition, the first divider stage for the Q[4:7] outputs supports a bypass (i.e. divide-by-1) operation for some clock sources.

Table 3. Q[0:1], Q[4:7] Output Divide Ratios

| 1st-Stage Divide | 2nd-Stage Divide | Total Divide | Minimum F _{OUT} MHz | Maximum F _{OUT} MHz |
|------------------|------------------|--------------|------------------------------|------------------------------|
| 4 | 1 | 4 | 750 | 1000 |
| 5 | 1 | 5 | 600 | 800 |
| 6 | 1 | 6 | 500 | 666.7 |
| 4 | 2 | 8 | 375 | 500 |
| 5 | 2 | 10 | 300 | 400 |
| 6 | 2 | 12 | 250 | 333.3 |
| 4 | 4 | 16 | 187.5 | 250 |
| 5 | 4 | 20 | 150 | 200 |
| 6 | 4 | 24 | 125 | 166.7 |
| ... | | | | |
| 4 | 131,070 | 524,280 | 0.0057 | 0.0076 |
| 5 | 131,070 | 655,350 | 0.0046 | 0.0061 |
| 6 | 131,070 | 786,420 | 0.0038 | 0.0051 |

NOTE: Above frequency ranges for Q[4:7] apply when driven directly from PLL0 or PLL1.

Fractional Output Divider Programming (Q[2:3] only)

For the FracN output dividers Q[2:3], the output divide ratio is given by:

$$\text{Output Divide Ratio} = (N.F) \times 2$$

$$N = \text{Integer Part: } 4, 5, \dots, (2^{18}-1)$$

$$F = \text{Fractional Part: } [0, 1, 2, \dots, (2^{28}-1)] / (2^{28})$$

For integer operation of these outputs dividers, N = 3 is also supported.

Output Divider Frequency Sources

Output dividers associated with the Q[0:3] outputs can take their input frequencies from either PLL0 or PLL1.

Output dividers associated with the Q[4:7] outputs can take their input frequencies from PLL0, PLL1, Q2 or Q3 output dividers, CLK0 or CLK1 input frequencies or the crystal frequency.

Output Banks

Outputs of the 8T49N287 are divided into three banks for purposes of output skew measurement:

- Q0, nQ0, Q1, nQ1
- Q4, nQ4, Q5, nQ5
- Q6, nQ6, Q7, nQ7

Output Phase Control on Switchover

When the 8T49N287 switches between input references, enters or leaves the holdover state for either PLL, there are two options on how the output phase can be controlled in these events: phase-slope limiting or fully hitless switching (sometimes called phase build-out) may be selected. The SWMODEn bit selects which behavior is to be followed for PLLn.

If fully hitless switching is selected, then the output phase will remain unchanged under any of these conditions. Note that fully hitless switching is not supported when external loopback is being used. Fully hitless switching should not be used unless all input references are in the same clock domain. Note that use of this mode may prevent an output frequency and phase from being able to trace its alignment back to a primary reference source.

If phase-slope limiting is selected, then the output phase will adjust from its previous value until it is tracking the new condition at a rate dictated by the SLEWn[1:0] bits. Phase-slope limiting should be used if all input references are not in the same clock domain or users wish to retain traceability to a primary reference source.

Input-Output Delay Control

When using the 8T49N287 in external loopback or in a situation where input-output delay needs to be known and controlled, it is necessary to examine the exact signal path through the device. Due to the flexibility of the device, there are a large number of potential signal paths from input to output through it that depend on the desired configuration. Each of those potential paths may include or exclude logic blocks from the path and change the absolute value of the delay (Static Phase Offset or SPO) through the device. Considering the range of SPO values to cover all those potential paths would not be useful in achieving the target delays for any specific user configuration. Please contact IDT for the specific SPO value associated with a desired input-output path. Note that events such as switchovers, entering or leaving holdover or re-configuring the signal path can result in one-time changes to the SPO due to that path re-configuration. The [AC Electrical Characteristics](#), ([Table 11A](#)) indicates the maximum variation in SPO that could be expected for a particular path through the device.

Output Phase Alignment

The device has a programmable output to output phase alignment for each of the eight output dividers. After power-up and the PLLs have achieved lock, the device will be in a state where the outputs are synchronized with a deterministic offset relative to each other. After synchronization, the output alignment will depend on the particular configuration of each output according to the following rules. The step size is defined as the period of the clock to that divider:

- 1) Only outputs derived from the same source will be aligned with each other. 'Source' means the reference selected to drive the output divider as controlled by the CLK_SELn bit for each output.
- 2) For integer dividers (Q[0:1], Q[4:7]) when both divider stages are active, edges are aligned. This case is used as a baseline to compare the other cases here.

3) For integer dividers where the 1st-stage divider is bypassed (only Q[4:7] support this), coarse delay adjustments can't be performed. The output phase will be one step earlier than in Case 2.

4) Fractional output dividers (Q2 or Q3) do not guarantee any specific phase on power-up or after a synchronization event.

5) Integer dividers using Q2 or Q3 as a source (Q[4:7] support this option) will be aligned to their source divider's output (Q2 or Q3). Note that the output skews described above are not included in any of the phase adjustments described here.

Once the device is in operation, the outputs associated with each PLL may have their phase adjustments re-synced in one of two ways:

- 1) If the PLL becomes unlocked, the coarse phase adjustments will be reset and the fine phase adjustments will be re-loaded once it becomes locked again.
- 2) Toggling of a register bit for either PLL (PLLn_SYN bits in register 00A8h) may also be used to force a re-sync / re-load for outputs associated with that PLL.

The user may apply adjustments that are proportional to the period of the clock source each output divider is operating from. For example, if the divider associated with Output Q3 is running off PLL0, which has a VCO frequency of 4GHz, then the appropriate period would be 250ps. The output phase may be adjusted in these steps across the full period of the output.

- **Coarse Adjustment:** all Output Dividers may have their phase adjusted in steps of the source clock period. For example a 4GHz VCO gives a step size of 250ps. The user may request an adjustment of phase of up to 31 steps using a single register write. The phase will be adjusted by lengthening the period of the output by 250ps at a time. This process will be repeated every four output clock periods until the full requested adjustment has been achieved. A busy signal will remain asserted in the phase delay register until the requested adjustment is complete. Then a further adjustment may be setup and triggered by toggling the trigger bit.
- **Fine Adjustment:** For the Fractional Output Dividers associated with the Q2 and Q3 outputs, the phase of those outputs may be further adjusted with a granularity of 1/16th of the VCO period. For example a 4GHz VCO frequency gives a granularity of 16ps. This is performed by directly writing the required offset (from the nominal rising edge position) in units of 1/16th of the output period into a register. Then the appropriate PLLn_SYN bit must be toggled to load the new value. Note that toggling this bit will clear all Coarse Delays for all outputs associated with that PLL, so Fine Delays should be set first, before Coarse Delays. The output will then jump directly to that new offset value. For this reason, this adjustment should be made as the input is initially programmed or in High-Impedance.

Each output has the capability of being inverted (180° phase shift).

Jitter and Wander Tolerance

The 8T49N287 can be used as a line card device and therefore is expected to tolerate the jitter and wander output of a timing card PLL (e.g. 82P33714).

Output Drivers

The Q0 to Q7 clock outputs are provided with register-controlled output drivers. By selecting the output drive type in the appropriate register, any of these outputs can support LVCMOS, LVPECL, HCSL or LVDS logic levels.

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCO}) and thus each can have different output voltage levels. Output voltage levels of 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.8V V_{CCO} .

Each output may be enabled or disabled by register bits and/or GPIO pins configured as Output Enables. The outputs will be enabled if the register bit and the associated OE pin are both asserted (high). When disabled an output will be in a high impedance state.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, phase alignment, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q and nQ outputs can be selected to be phase-aligned with each other or inverted relative to one another. Phase-aligned outputs will have increased simultaneous switching currents which can negatively affect phase noise performance and power consumption. It is recommended that use of this selection be kept to a minimum.

Power-Saving Modes

To allow the device to consume the least power possible for a given application, the following functions are included under register control:

- PLL1 may be shut down.
- Any unused output, including all output divider and phase adjustment logic, can be individually powered-off.
- Clock gating on logic that is not being used.

Status / Control Signals and Interrupts

General-Purpose I/Os & Interrupts

The 8T49N287 provides 4 General Purpose Input / Output (GPIO) pins for miscellaneous status & control functions. Each GPIO may be configured as an input or an output. Each GPIO may be directly controlled from register bits or be used as a predefined function as shown in [Table 4](#). Note that the default state prior to configuration being loaded from internal OTP or external EEPROM will be to set each GPIO to function as an Output Enable.

Table 4. GPIO Configuration

| GPIO Pin | Configured as Input | | | | Configured as Output | | |
|----------|-------------------------|---------------|--------------|-----------------|----------------------|---------|-----------------|
| | Fixed Function | | | General Purpose | Fixed Function | | General Purpose |
| | Output Enable (default) | Output Enable | Clock Select | | | | |
| 3 | OE[3] | OE[7] | CSEL1 | GPI[3] | - | - | GPO[3] |
| 2 | OE[2] | OE[6] | CSEL0 | GPI[2] | LOS[0] | LOS[1] | GPO[2] |
| 1 | OE[1] | OE[5] | - | GPI[1] | HOLD[0] | HOLD[1] | GPO[1] |
| 0 | OE[0] | OE[4] | - | GPI[0] | LOL[0] | LOL[1] | GPO[0] |

If used in the Fixed Function mode of operation, the GPIO bits will reflect the real-time status of their respective status bits as shown in [Table 4](#). Note that the LOL signal represents the lock status of the PLL. It does not account for the process of synchronization of the output dividers associated with that PLL. The output dividers programmed to operate from that PLL will automatically go through a re-synchronization process when the PLL locks or re-locks, or if the user triggers a re-sync manually via register bit PLLn_SYN. This synchronization process may result in a period of instability on the affected outputs for a duration of up to 350ns after the re-lock (LOL de-asserts) or the PLLn_SYN bit is de-asserted.

Interrupt Functionality

Interrupt functionality includes an interrupt status flag for each of PLL Loss-of-Lock Status (LOL[1:0]), PLL Holdover Status (HOLD[1:0]) and Input Reference Status (LOS[1:0]) that is set whenever there is an alarm on any of those signals. The Status Flag will remain set until the alarm has been cleared and a '1' has been written to the Status Flag's register location or if a reset occurs. Each Status Flag will also have an Interrupt Enable bit that will determine if that Status Flag is allowed to cause the Interrupt Status to be affected (enabled) or not (disabled). All Interrupt Enable bits will be in the disabled state after reset. The Device Interrupt Status flag and nINT output pin are asserted if any of the enabled Interrupt Status flags are set.

Device Hardware Configuration

The 8T49N287 supports an internal One-Time Programmable (OTP) memory that can be pre-programmed at the factory with 1 complete device configuration. If the device is set to read a configuration from an external, serial EEPROM, then the values read will overwrite the OTP-defined values.

This configuration can be over-written using the serial interface once reset is complete. Any configuration written via the programming interface needs to be re-written after any power cycle or reset. Please contact IDT if a specific factory-programmed configuration is desired.

Device Start-up and Reset Behavior

The 8T49N287 has an internal power-up reset (POR) circuit and a Master Reset input pin nRST. If either is asserted, the device will be in the Reset State.

For highly programmable devices, it is common practice to reset the device immediately after the initial power-on sequence. IDT recommends connecting the nRST input pin to a programmable logic source for optimal functionality. It is recommended that a minimum pulse width of 10ns be used to drive the nRST input pin.

While in the reset state (nRST input asserted or POR active), the device will operate as follows:

- All registers will return to & be held in their default states as indicated in the applicable register description.
- All internal state machines will be in their reset conditions.
- The serial interface will not respond to read or write cycles.
- The GPIO signals will be configured as General-Purpose inputs.
- All clock outputs will be disabled.
- All interrupt status and Interrupt Enable bits will be cleared, negating the nINT signal.

Upon the later of the internal POR circuit expiring or the nRST input negating, the device will exit reset and begin self-configuration.

The device will load an initial block of its internal registers using the configuration stored in the internal One-Time Programmable (OTP) memory. Once this step is complete, the 8T49N287 will check the register settings to see if it should load the remainder of its configuration from an external I²C EEPROM at a defined address or continue loading from OTP. See the section on I²C Boot Initialization for details on how this is performed.

Once the full configuration has been loaded, the device will respond to accesses on the serial port and will attempt to lock both PLLs to the selected sources and begin operation. Once the PLLs are locked, all the outputs derived from a given PLL will be synchronized and output phase adjustments can then be applied if desired.

Serial Control Port Description

Serial Control Port Configuration Description

The device has a serial control port capable of responding as a slave in an I²C compatible configuration, to allow access any of the internal registers for device programming or examination of internal status. All registers are configured to have default values. See the specifics for each register for details.

The device has the additional capability of becoming a master on the I²C bus only for the purpose of reading its initial register configurations from a serial EEPROM on the I²C bus. Writing of the configuration to the serial EEPROM must be performed by another device on the same I²C bus or pre-programmed into the device prior to assembly.

I²C Mode Operation

The I²C interface is designed to fully support v2.1 of the I²C Specification for Normal and Fast mode operation. The device acts as a slave device on the I²C bus at 100kHz or 400kHz using the address defined in the Status Interface Control register (0006h), as modified by the S_A0 input pin setting. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

For full electrical I²C compliance, it is recommended to use external pull-up resistors for SDATA and SCLK. The internal pull-up resistors have a size of 51kΩ typical.

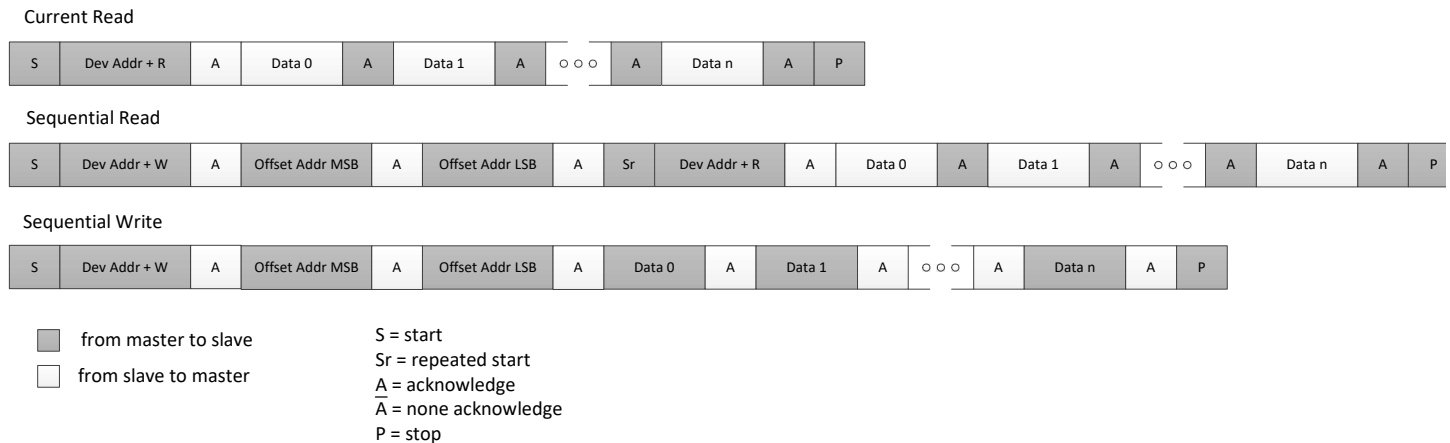


Figure 3. I²C Slave Read and Write Cycle Sequencing

I²C Master Mode

When operating in I²C mode, the 8T49N287 has the capability to become a bus master on the I²C bus for the purposes of reading its configuration from an external I²C EEPROM. Only a block read cycle will be supported.

As an I²C bus master, the 8T49N287 will support the following functions:

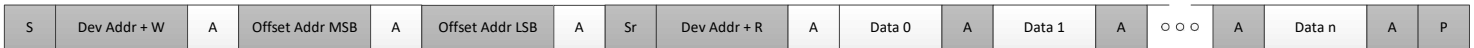
- 7-bit addressing mode
- Base address register for EEPROM
- Validation of the read block via CCITT-8 CRC check against value stored in last byte (E0h) of EEPROM
- Support for 100kHz and 400kHz operation with speed negotiation. If bit d0 is set at Byte address 05h in the EEPROM, this will shift from 100kHz operation to 400kHz operation.
- Support for 1 or 2-byte addressing mode
- Master arbitration with programmable number of retries

- Fixed-period cycle response timer to prevent permanently hanging the I²C bus.
- Read will abort with an alarm (BOOTFAIL) if any of the following conditions occur: Slave NACK, Arbitration Fail, Collision during Address Phase, CRC failure, Slave Response time-out
- The 8T49N287 will not support the following functions:
 - I²C General Call
 - Slave clock stretching
 - I²C Start Byte protocol
 - EEPROM Chaining
 - CBUS compatibility
- Responding to its own slave address when acting as a master
- Writing to external I²C devices including the external EEPROM used for booting

Sequential Read (1-byte offset address)



Sequential Read (2-byte offset address)



- from master to slave
- from slave to master

S = start
 Sr = repeated start
 A = acknowledge
 \bar{A} = none acknowledge
 P = stop

Figure 4. I²C Master Read Cycle Sequencing

I²C Boot-up Initialization Mode

If enabled (via the BOOT_EEP bit in the Startup register), once the nRST input has been de-asserted (high) and its internal power-up reset sequence has completed, the device will contend for ownership of the I²C bus to read its initial register settings from a memory location on the I²C bus. The address of that memory location is kept in non-volatile memory in the Startup register. During the boot-up process, the device will not respond to serial control port accesses. Once the initialization process is complete, the contents of any of the device's registers can be altered. It is the responsibility of the user to make any desired adjustments in initial values directly in the serial bus memory.

If a NACK is received to any of the read cycles performed by the device during the initialization process, or if the CRC does not match the one stored in address E0h of the EEPROM the process will be aborted and any uninitialized registers will remain with their default values. The BOOTFAIL bit (021Eh) in the Global Interrupt Status register will also be set in this event.

If the BOOTFAIL bit is set, then both LOL[n] indicators will be set.

Contents of the EEPROM should be as shown in [Table 5](#).

Table 5. External Serial EEPROM Contents

| EEPROM Offset (Hex) | Contents | | | | | | | | |
|------------------------|--|--|----|----|----|----|----|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 00 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 01 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 02 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 03 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 04 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 05 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Serial EEPROM Speed Select 0 = 100kHz 1 = 400kHz | |
| 06 | 1 | 8T49N287 Device I ² C Address [6:2] | | | | | | 0 | 1 |
| 07 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 08 - DF | Desired contents of Device Registers 08h - DFh | | | | | | | | |
| E0 | Serial EEPROM CRC | | | | | | | | |
| E1 - FF | Unused | | | | | | | | |

Register Descriptions

Table 6A. Register Blocks

| Register Ranges Offset (Hex) | Register Block Description |
|------------------------------|---|
| 0000 - 0001 | Startup Control Registers |
| 0002 - 0005 | Device ID Control Registers |
| 0006 - 0007 | Serial Interface Control Registers |
| 0008 - 003A | Digital PLL0 Control Registers |
| 003B - 006D | Digital PLL1 Control Registers |
| 006E - 0076 | GPIO Control Registers |
| 0077 - 00AB | Output Clock Control Registers |
| 00AC - 00AF | Analog PLL0 Control Registers |
| 00B0 - 00B3 | Analog PLL1 Control Registers |
| 00B4 - 00B8 | Power-Down Control Registers |
| 00B9 - 00C6 | Input Monitor Control Registers |
| 00C7 | Interrupt Enable Register |
| 00C8 - 00CB | Digital Phase Detector Control Registers |
| 00CC - 01FF | Reserved ¹ |
| 0200 - 0203 | Interrupt Status Registers |
| 0204 | Output Phase Adjustment Status Register |
| 0205 - 020E | Digital PLL0 Status Registers |
| 020F - 0218 | Digital PLL1 Status Registers |
| 0219 | General-Purpose Input Status Register |
| 021A - 021F | Global Interrupt and Boot Status Register |
| 0220 - 03FF | Reserved ¹ |

NOTE 1: Reserved. Always write 0 to this bit location. Read values are not defined.

Table 6B. Startup Control Register Bit Field Locations and Descriptions

| Startup Control Register Block Field Locations | | | | | | | | | |
|--|--------------|---------------|----|----|----|------|-----------|-----------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0000 | EEP_RTY[4:0] | | | | | Rsvd | nBOOT_OTP | nBOOT_EEP | |
| 0001 | EEP_A15 | EEP_ADDR[6:0] | | | | | | | |

| Startup Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| EEP_RTY[4:0] | R/W | 00001b | Select number of times arbitration for the I ² C bus to read the serial EEPROM will be retried before being aborted. Note that this number does not include the original try. |
| nBOOT_OTP | R/W | NOTE 1 | Internal One-Time Programmable (OTP) memory usage on power-up: 0 = Load power-up configuration from OTP 1 = Only load 1st eight bytes from OTP |
| nBOOT_EEP | R/W | NOTE 1 | External EEPROM usage on power-up: 0 = Load power-up configuration from external serial EEPROM (overwrites OTP values) 1 = Don't use external EEPROM |
| EEP_A15 | R/W | NOTE 1 | Serial EEPROM supports 15-bit addressing mode (multiple pages). |
| EEP_ADDR[6:0] | R/W | NOTE 1 | I ² C base address for serial EEPROM. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* for more details.

Table 6C. Device ID Control Register Bit Field Locations and Descriptions

| Device ID Control Register Block Field Locations | | | | | | | | | |
|--|-----------------|----|----|----|------------------|----|----|----|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0002 | REV_ID[3:0] | | | | DEV_ID[15:12] | | | | |
| 0003 | DEV_ID[11:4] | | | | | | | | |
| 0004 | DEV_ID[3:0] | | | | DASH_CODE [10:7] | | | | |
| 0005 | DASH_CODE [6:0] | | | | | | | 1 | |

| Device ID Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| REV_ID[3:0] | R/W | 0000b | Device revision. |
| DEV_ID[15:0] | R/W | 605h | Device ID code. |
| DASH CODE [10:0] | R/W | NOTE 1 | Device Dash Code: Decimal value assigned by IDT to identify the configuration loaded at the factory. May be over-written by users at any time. Refer to <i>FemtoClock NG Universal Frequency Translator Ordering Product Information guide</i> to identify major configuration parameters associated with this Dash Code value. |

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Refer to the *FemtoClock NG Universal Frequency Translator Ordering Product Information guide* or custom datasheet addendum for more details.

Table 6D. Serial Interface Control Register Bit Field Locations and Descriptions

| Serial Interface Control Block Field Locations | | | | | | | | | |
|--|------|-------------|----|----|----|----|-----------|-----------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0006 | Rsvd | UFTADD[6:2] | | | | | UFTADD[1] | UFTADD[0] | |
| 0007 | Rsvd | | | | | | | 1 | |

| Serial Interface Control Register Block Field Descriptions | | | |
|--|------------|------------------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| UFTADD[6:2] | R/W | NOTE 1 | Configurable portion of I ² C Base Address (bits 6:2) for this device. |
| UFTADD[1] | R/O | 0b | I ² C Base Address bit 1. This bit is fixed at 0. |
| UFTADD[0] | R/O | 0b | I ² C base address bit 0. This address bit reflects the status of the S_A0 external input pin. See Table 1 , Pin Description. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

NOTE 1: These values are specific to the device configuration and can be customized when ordering. Generic dash codes -900 through -908, -998 and -999 are available and programmed with the default I²C address of 1111100b. Please refer to the FemtoClock NG Universal Frequency Translator Ordering Product Information guide for more details.

Table 6E. Digital PLL0 Input Control Register Bit Field Locations and Descriptions

| Digital PLL0 Input Control Register Block Field Locations | | | | | | | | |
|---|--------------|----|-----------|---------------|-------------|------|-------------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0008 | REFSEL0[2:0] | | | FBSEL0[1:0] | | | RVRT0 | SWMODE0 |
| 0009 | 11 | | 10 | | PRI0_1[1:0] | | PRI0_0[1:0] | |
| 000A | 1 | 1 | REFDIS0_1 | REFDIS0_0 | Rsvd | Rsvd | STATE0[1:0] | |
| 000B | Rsvd | | | PRE0_0[20:16] | | | | |
| 000C | PRE0_0[15:8] | | | | | | | |
| 000D | PRE0_0[7:0] | | | | | | | |
| 000E | Rsvd | | | PRE0_1[20:16] | | | | |
| 000F | PRE0_1[15:8] | | | | | | | |
| 0010 | PRE0_1[7:0] | | | | | | | |
| 0011 | Rsvd | | | Rsvd | | | | |
| 0012 | Rsvd | | | | | | | |
| 0013 | Rsvd | | | | | | | |
| 0014 | Rsvd | | | Rsvd | | | | |
| 0015 | Rsvd | | | | | | | |
| 0016 | Rsvd | | | | | | | |

| Digital PLL0 Input Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| REFSEL0[2:0] | R/W | 000b | Input reference selection for Digital PLL0: 000 = Automatic selection 001 = Manual selection by GPIO inputs 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = Do not use 111 = Do not use |
| FBSEL0[2:0] | R/W | 000b | Feedback mode selection for Digital PLL0: 000 through 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = do not use 111 = do not use |
| RVRT0 | R/W | 1b | Automatic switching mode for Digital PLL0: 0 = non-revertive switching 1 = revertive switching |
| SWMODE0 | R/W | 1b | Controls how Digital PLL0 adjusts output phase when switching between input references: 0 = Absorb any phase differences between old and new input references at the PLL output. Recommended for use when both input references are in the same clock domain. 1 = Limit the maximum rate of phase change at the PLL output when adjusting to a new input reference's phase/frequency using phase-slope limiting as set in the SLEWn bits. Recommended for use when the input references are not in the same clock domain. |
| PRI0_0[1:0] | R/W | 00b | Switchover priority for Input Reference 0 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = do not use 11 = do not use |

Digital PLL0 Input Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| PRI0_1[1:0] | R/W | 01b | Switchover priority for Input Reference 1 when used by Digital PLL0: 00 = 1st priority 01 = 2nd priority 10 = do not use 11 = do not use |
| REFDIS0_0 | R/W | 0b | Input Reference 0 Switching Selection Disable for Digital PLL0: 0 = Input Reference 0 is included in the switchover sequence for Digital PLL0 1 = Input Reference 0 is not included in the switchover sequence for Digital PLL0 |
| REFDIS0_1 | R/W | 0b | Input Reference 1 Switching Selection Disable for Digital PLL0: 0 = Input Reference 1 is included in the switchover sequence for Digital PLL0 1 = Input Reference 1 is not included in the switchover sequence for Digital PLL0 |
| STATE0[1:0] | R/W | 00b | Digital PLL0 State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode for PLL0 10 = Force NORMAL state 11 = Force HOLDOVER state |
| PRE0_0[20:0] | R/W | 000000h | Pre-divider ratio for Input Reference 0 when used by Digital PLL0. |
| PRE0_1[20:0] | R/W | 000000h | Pre-divider ratio for Input Reference 1 when used by Digital PLL0. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6F. Digital PLL0 Feedback Control Register Bit Field Locations and Descriptions

| Digital PLL0 Feedback Control Register Block Field Locations | | | | | | | | |
|--|----------------|----------------|---------------|-----------------|----------------|---------------|-------------|----|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0017 | M1_0_0[23:16] | | | | | | | |
| 0018 | M1_0_0[15:8] | | | | | | | |
| 0019 | M1_0_0[7:0] | | | | | | | |
| 001A | M1_0_1[23:16] | | | | | | | |
| 001B | M1_0_1[15:8] | | | | | | | |
| 001C | M1_0_1[7:0] | | | | | | | |
| 001D | Rsvd | | | | | | | |
| 001E | Rsvd | | | | | | | |
| 001F | Rsvd | | | | | | | |
| 0020 | Rsvd | | | | | | | |
| 0021 | Rsvd | | | | | | | |
| 0022 | Rsvd | | | | | | | |
| 0023 | LCKBW0[3:0] | | | ACQBW0[3:0] | | | | |
| 0024 | LCKDAMP0[2:0] | | ACQDAMP0[2:0] | | | PLLGAIN0[1:0] | | |
| 0025 | Rsvd | | Rsvd | Rsvd | | | Rsvd | |
| 0026 | Rsvd | | | | | | | |
| 0027 | Rsvd | | | | | | | |
| 0028 | Rsvd | | | | | | Rsvd | |
| 0029 | Rsvd | | | | | | | |
| 002A | Rsvd | | | | | | | |
| 002B | FFh | | | | | | | |
| 002C | FFh | | | | | | | |
| 002D | FFh | | | | | | | |
| 002E | FFh | | | | | | | |
| 002F | SLEW0[1:0] | Rsvd | HOLD0[1:0] | | Rsvd | HOLDAVG0 | FASTLCK0 | |
| 0030 | LOCK0[7:0] | | | | | | | |
| 0031 | Rsvd | | | | | | DSM_INT0[8] | |
| 0032 | DSM_INT0[7:0] | | | | | | | |
| 0033 | Rsvd | | | DSMFRAC0[20:16] | | | | |
| 0034 | DSMFRAC0[15:8] | | | | | | | |
| 0035 | DSMFRAC0[7:0] | | | | | | | |
| 0036 | Rsvd | | | | | | | |
| 0037 | 01h | | | | | | | |
| 0038 | Rsvd | | | | | | | |
| 0039 | Rsvd | | | | | | | |
| 003A | DSM_ORD0[1:0] | DCXOGAIN0[1:0] | | Rsvd | DITHGAIN0[2:0] | | | |

| Digital PLL0 Feedback Configuration Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| M1_0_0[23:0] | R/W | 070000h | M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL0. |
| M1_0_1[23:0] | R/W | 070000h | M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL0. |
| LCKBW0[3:0] | R/W | 0111b | Digital PLL Loop Bandwidth while locked: 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved |
| ACQBW0[3:0] | R/W | 0111b | Digital PLL0 Loop Bandwidth while in acquisition (not-locked): 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved |
| LCKDAMP0[2:0] | R/W | 011b | Damping factor for Digital PLL0 while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved |
| ACQDAMP0[2:0] | R/W | 011b | Damping factor for Digital PLL0 while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved |
| PLLGAIN0[1:0] | R/W | 01b | Digital Loop Filter Gain Settings for Digital PLL0: 00 = 0.5 01 = 1 10 = 1.5 11 = 2 |

| Digital PLL0 Feedback Configuration Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| SLEW0[1:0] | R/W | 00b | Phase-slope control for Digital PLL0: 00 = no limit - controlled by loop bandwidth of Digital PLL0 (NOTE 1) 01 = 83 μ sec/sec 10 = 13 μ sec/sec 11 = Reserved |
| HOLD0[1:0] | R/W | 00b | Holdover Averaging mode selection for Digital PLL0: 00 = Instantaneous mode - uses historical value 100ms prior to entering holdover 01 = Fast Average Mode 10 = Reserved 11 = Set VCO control voltage to $V_{CC}/2$ |
| HOLDAVG0 | R/W | 0b | Holdover Averaging Enable for Digital PLL0: 0 = Holdover averaging disabled 1 = Holdover averaging enabled as defined in HOLD0[1:0] |
| FASTLCK0 | R/W | 0b | Enables Fast Lock operation for Digital PLL0: 0 = Normal locking using LCKBW0 & LCKDAMP0 fields in all cases 1 = Fast Lock mode using ACQBW0 & ACQDAMP0 when not phase locked and LCKBW0 & LCKDAMP0 once phase locked |
| LOCK0[7:0] | R/W | 3Fh | Lock window size for Digital PLL0. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0. |
| DSM_INT0[8:0] | R/W | 02Dh | Integer portion of the Delta-Sigma Modulator value. Do not set higher than FFh. This implies that for crystal frequencies lower than 16MHz, the doubler circuit must be enabled. |
| DSMFRAC0[20:0] | R/W | 000000h | Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{21} to determine the actual fraction. |
| DSM_ORD0[1:0] | R/W | 11b | Delta-Sigma Modulator Order for Digital PLL0: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation |
| DCXOGAIN0[1:0] | R/W | 01b | Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL0: 00 = 0.5 01 = 1 10 = 2 11 = 4 |
| DITHGAIN0[2:0] | R/W | 000b | Dither Gain setting for Digital PLL0: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

NOTE 1: Settings other than "00" may result in a significant increase in initial lock time.

Table 6G. Digital PLL1 Input Control Register Bit Field Locations and Descriptions

| Digital PLL1 Input Control Register Block Field Locations | | | | | | | | |
|---|--------------|----|-----------|---------------|-------------|------|-------------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 003B | REFSEL1[2:0] | | | FBSEL1[1:0] | | | RVRT1 | SWMODE1 |
| 003C | 11 | | 10 | | PRI1_1[1:0] | | PRI1_0[1:0] | |
| 003D | 1 | 1 | REFDIS1_1 | REFDIS1_0 | Rsvd | Rsvd | STATE1[1:0] | |
| 003E | Rsvd | | | PRE1_0[20:16] | | | | |
| 003F | PRE1_0[15:8] | | | | | | | |
| 0040 | PRE1_0[7:0] | | | | | | | |
| 0041 | Rsvd | | | PRE1_1[20:16] | | | | |
| 0042 | PRE1_1[15:8] | | | | | | | |
| 0043 | PRE1_1[7:0] | | | | | | | |
| 0044 | Rsvd | | | Rsvd | | | | |
| 0045 | Rsvd | | | | | | | |
| 0046 | Rsvd | | | | | | | |
| 0047 | Rsvd | | | Rsvd | | | | |
| 0048 | Rsvd | | | | | | | |
| 0049 | Rsvd | | | | | | | |

| Digital PLL1 Input Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| REFSEL1[2:0] | R/W | 000b | Input reference selection for Digital PLL1: 000 = Automatic selection 001 = Manual selection by GPIO inputs 010 through 011 = Reserved 100 = Force selection of Input Reference 0 101 = Force selection of Input Reference 1 110 = do not use 111 = do not use |
| FBSEL1[2:0] | R/W | 000b | Feedback mode selection for Digital PLL1: 000 through 011 = internal feedback divider 100 = external feedback from Input Reference 0 101 = external feedback from Input Reference 1 110 = do not use 111 = do not use |
| RVRT1 | R/W | 1b | Automatic switching mode for Digital PLL1: 0 = non-revertive switching 1 = revertive switching |
| SWMODE1 | R/W | 1b | Controls how Digital PLL1 adjusts output phase when switching between input references: 0 = Absorb any phase differences between old and new input references at the PLL output. Recommended for use when both input references are in the same clock domain. 1 = Limit the maximum rate of phase change at the PLL output when adjusting to a new input reference's phase/frequency using phase-slope limiting as set in the SLEWn bits. Recommended for use when the input references are not in the same clock domain. |
| PRI1_0[1:0] | R/W | 00b | Switchover priority for Input Reference 0 when used by Digital PLL1: 00 = 1st priority 01 = 2nd priority 10 = do not use 11 = do not use |

Digital PLL1 Input Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| PRI1_1[1:0] | R/W | 01b | Switchover priority for Input Reference 1 when used by Digital PLL1: 00 = 1st priority 01 = 2nd priority 10 = do not use 11 = do not use |
| REFDIS1_0 | R/W | 0b | Input Reference 0 Switching Selection Disable for Digital PLL1: 0 = Input Reference 0 is included in the switchover sequence for Digital PLL1 1 = Input Reference 0 is not included in the switchover sequence for Digital PLL1 |
| REFDIS1_1 | R/W | 0b | Input Reference 1 Switching Selection Disable for Digital PLL1: 0 = Input Reference 1 is included in the switchover sequence for Digital PLL1 1 = Input Reference 1 is not included in the switchover sequence for Digital PLL1 |
| STATE1[1:0] | R/W | 00b | Digital PLL1 State Machine Control: 00 = Run automatically 01 = Force FREERUN state - set this if in Synthesizer Mode for PLL1 10 = Force NORMAL state 11 = Force HOLDOVER state |
| PRE1_0[20:0] | R/W | 000000h | Pre-divider ratio for Input Reference 0 when used by Digital PLL1. |
| PRE1_1[20:0] | R/W | 000000h | Pre-divider ratio for Input Reference 1 when used by Digital PLL1. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6H. Digital PLL1 Feedback Control Register Bit Field Locations and Descriptions

| Digital PLL1 Feedback Control Register Block Field Locations | | | | | | | | |
|--|----------------|----|----------------|-----------------|-------------|----------------|---------------|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 004A | M1_1_0[23:16] | | | | | | | |
| 004B | M1_1_0[15:8] | | | | | | | |
| 004C | M1_1_0[7:0] | | | | | | | |
| 004D | M1_1_1[23:16] | | | | | | | |
| 004E | M1_1_1[15:8] | | | | | | | |
| 004F | M1_1_1[7:0] | | | | | | | |
| 0050 | Rsvd | | | | | | | |
| 0051 | Rsvd | | | | | | | |
| 0052 | Rsvd | | | | | | | |
| 0053 | Rsvd | | | | | | | |
| 0054 | Rsvd | | | | | | | |
| 0055 | Rsvd | | | | | | | |
| 0056 | LCKBW1[3:0] | | | | ACQBW1[3:0] | | | |
| 0057 | LCKDAMP1[2:0] | | | ACQDAMP1[2:0] | | | PLLGAIN1[1:0] | |
| 0058 | Rsvd | | | Rsvd | Rsvd | | | Rsvd |
| 0059 | Rsvd | | | | | | | |
| 005A | Rsvd | | | | | | | |
| 005B | Rsvd | | | | | | Rsvd | |
| 005C | Rsvd | | | | | | | |
| 005D | Rsvd | | | | | | | |
| 005E | FFh | | | | | | | |
| 005F | FFh | | | | | | | |
| 0060 | FFh | | | | | | | |
| 0061 | FFh | | | | | | | |
| 0062 | SLEW1[1:0] | | Rsvd | HOLD1[1:0] | | Rsvd | HOLDAVG1 | FASTLCK1 |
| 0063 | LOCK1[7:0] | | | | | | | |
| 0064 | Rsvd | | | | | | DSM_INT1[8] | |
| 0065 | DSM_INT1[7:0] | | | | | | | |
| 0066 | Rsvd | | | DSMFRAC1[20:16] | | | | |
| 0067 | DSMFRAC1[15:8] | | | | | | | |
| 0068 | DSMFRAC1[7:0] | | | | | | | |
| 0069 | Rsvd | | | | | | | |
| 006A | 01h | | | | | | | |
| 006B | Rsvd | | | | | | | |
| 006C | Rsvd | | | | | | | |
| 006D | DSM_ORD1[1:0] | | DCXOGAIN1[1:0] | | Rsvd | DITHGAIN1[2:0] | | |

| Digital PLL1 Feedback Configuration Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| M1_1_0[23:0] | R/W | 070000h | M1 Feedback divider ratio for Input Reference 0 when used by Digital PLL1. |
| M1_1_1[23:0] | R/W | 070000h | M1 Feedback divider ratio for Input Reference 1 when used by Digital PLL1. |
| LCKBW1[3:0] | R/W | 0111b | Digital PLL1 Loop Bandwidth while locked: 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved |
| ACQBW1[3:0] | R/W | 0111b | Digital PLL1 Loop Bandwidth while in acquisition (not-locked): 0000 = Reserved 0001 = Reserved 0010 = Reserved 0011 = 1.40625Hz 0100 = 2.8125Hz 0101 = 5.625Hz 0110 = 11.25Hz 0111 = 22.5Hz 1000 = 45Hz 1001 = 90Hz 1010 = 180Hz 1011 = 360Hz 1100 through 1111 = Reserved |
| LCKDAMP1[2:0] | R/W | 011b | Damping factor for Digital PLL1 while locked: 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved |
| ACQDAMP1[2:0] | R/W | 011b | Damping factor for Digital PLL1 while in acquisition (not locked): 000 = Reserved 001 = 1 010 = 2 011 = 5 100 = 10 101 = 20 110 = Reserved 111 = Reserved |
| PLLGAIN1[1:0] | R/W | 01b | Digital Loop Filter Gain Settings for Digital PLL1: 00 = 0.5 01 = 1 10 = 1.5 11 = 2 |

| Digital PLL1 Feedback Configuration Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| SLEW1[1:0] | R/W | 00b | Phase-slope control for Digital PLL1: 00 = no limit - controlled by loop bandwidth of Digital PLL0 (NOTE 1) 01 = 83 μ sec/sec 10 = 13 μ sec/sec 11 = Reserved |
| HOLD1[1:0] | R/W | 00b | Holdover Averaging mode selection for Digital PLL1: 00 = Instantaneous mode - uses historical value 100ms prior to entering holdover 01 = Fast Average Mode 10 = Reserved 11 = Set VCO control voltage to $V_{CC}/2$ |
| HOLDAVG1 | R/W | 0b | Holdover Averaging Enable for Digital PLL1: 0 = Holdover averaging disabled 1 = Holdover averaging enabled as defined in HOLD1[1:0] |
| FASTLCK1 | R/W | 0b | Enables Fast Lock operation for Digital PLL1: 0 = Normal locking using LCKBW1 & LCKDAMP1 fields in all cases 1 = Fast Lock mode using ACQBW1 & ACQDAMP1 when not phase locked and LCKBW1 & LCKDAMP1 once phase locked |
| LOCK1[7:0] | R/W | 3Fh | Lock window size for Digital PLL1. Unsigned 2's complement binary number in steps of 2.5ns, giving a total range of 640ns. Do not program to 0. |
| DSM_INT1[8:0] | R/W | 02Dh | Integer portion of the Delta-Sigma Modulator value. Do not set higher than FFh. This implies that for crystal frequencies lower than 16MHz, the doubler circuit must be enabled. |
| DSMFRAC1[20:0] | R/W | 000000h | Fractional portion of Delta-Sigma Modulator value. Divide this number by 2^{21} to determine the actual fraction. |
| DSM_ORD1[1:0] | R/W | 11b | Delta-Sigma Modulator Order for Digital PLL1: 00 = Delta-Sigma Modulator disabled 01 = 1st order modulation 10 = 2nd order modulation 11 = 3rd order modulation |
| DCXOGAIN1[1:0] | R/W | 01b | Multiplier applied to instantaneous frequency error before it is applied to the Digitally Controlled Oscillator in Digital PLL1: 00 = 0.5 01 = 1 10 = 2 11 = 4 |
| DITHGAIN1[2:0] | R/W | 000b | Dither Gain setting for Digital PLL1: 000 = no dither 001 = Least Significant Bit (LSB) only 010 = 2 LSBs 011 = 4 LSBs 100 = 8 LSBs 101 = 16 LSBs 110 = 32 LSBs 111 = 64 LSBs |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

NOTE 1: Settings other than "00" may result in a significant increase in initial lock time.

Table 6I. GPIO Control Register Bit Field Locations and Descriptions

The values observed on any GPIO pins that are used as general purpose inputs are visible in the GPI[3:0] register that is located at location 0219h near a number of other read-only registers.

| GPIO Control Register Block Field Locations | | | | | | | | |
|---|------|----|----|---------------|------------|------------|------------|----|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 006E | Rsvd | | | GPIO_DIR[3:0] | | | | |
| 006F | Rsvd | | | GPI3SEL[2] | GPI2SEL[2] | GPI1SEL[2] | GPI0SEL[2] | |
| 0070 | Rsvd | | | GPI3SEL[1] | GPI2SEL[1] | GPI1SEL[1] | GPI0SEL[1] | |
| 0071 | Rsvd | | | GPI3SEL[0] | GPI2SEL[0] | GPI1SEL[0] | GPI0SEL[0] | |
| 0072 | Rsvd | | | GPO3SEL[2] | GPO2SEL[2] | GPO1SEL[2] | GPO0SEL[2] | |
| 0073 | Rsvd | | | GPO3SEL[1] | GPO2SEL[1] | GPO1SEL[1] | GPO0SEL[1] | |
| 0074 | Rsvd | | | GPO3SEL[0] | GPO2SEL[0] | GPO1SEL[0] | GPO0SEL[0] | |
| 0075 | Rsvd | | | | | | | |
| 0076 | Rsvd | | | GPO[3:0] | | | | |

| GPIO Control Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| GPIO_DIR[3:0] | R/W | 00h | Direction control for General-Purpose I/O Pins GPIO[3:0]: 0 = input mode 1 = output mode |
| GPI0SEL[2:0] | R/W | 000b | Function of GPIO[0] pin when set to input mode by GPIO_DIR[0] register bit: 000 = General Purpose Input (value on GPIO[0] pin directly reflected in GPI[0] register bit) 001 = Output Enable control for output Q0 010 = Output Enable control for output Q4 011 = reserved 100 through 111 = reserved |
| GPI1SEL[2:0] | R/W | 000b | Function of GPIO[1] pin when set to input mode by GPIO_DIR[1] register bit: 000 = General Purpose Input (value on GPIO[1] pin directly reflected in GPI[1] register bit) 001 = Output Enable control for output Q1 010 = Output Enable control for output Q5 011 through 111 = reserved |
| GPI2SEL[2:0] | R/W | 000b | Function of GPIO[2] pin when set to input mode by GPIO_DIR[2] register bit: 000 = General Purpose Input (value on GPIO[2] pin directly reflected in GPI[2] register bit) 001 = Output Enable control for output Q2 010 = Output Enable control for output Q6 011 = reserved 100 = reserved 101 = CSEL0: Manual Clock Select Input for PLL0 110 through 111 = reserved |
| GPI3SEL[2:0] | R/W | 000b | Function of GPIO[3] pin when set to input mode by GPIO_DIR[3] register bit: 000 = General Purpose Input (value on GPIO[3] pin directly reflected in GPI[3] register bit) 001 = Output Enable control for output Q3 010 = Output Enable control for output Q7 011 = reserved 101 = CSEL1: Manual Clock Select Input for PLL1 100, 110, 111 = reserved |

GPIO Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| GPO0SEL[2:0] | R/W | 000b | Function of GPIO[0] pin when set to output mode by GPIO_DIR[0] register bit: 000 = General Purpose Output (value in GPO[0] register bit driven on GPIO[0] pin) 001 = Loss-of-Lock Status Flag for Digital PLL0 reflected on GPIO[0] pin 010 = Loss-of-Lock Status Flag for Digital PLL1 reflected on GPIO[0] pin 011 = reserved 100 = reserved 101 = reserved 110 through 111 = reserved |
| GPO1SEL[2:0] | R/W | 000b | Function of GPIO[1] pin when set to output mode by GPIO_DIR[1] register bit: 000 = General Purpose Output (value in GPO[1] register bit driven on GPIO[1] pin) 001 = Holdover Status Flag for Digital PLL0 reflected on GPIO[1] pin 010 = Holdover Status Flag for Digital PLL1 reflected on GPIO[1] pin 011 = reserved 100 = reserved 101 = reserved 110 = reserved 111 = reserved |
| GPO2SEL[2:0] | R/W | 000b | Function of GPIO[2] pin when set to output mode by GPIO_DIR[2] register bit: 000 = General Purpose Output (value in GPO[2] register bit driven on GPIO[2] pin) 001 = Loss-of-Signal Flag for Input Reference 0 reflected on GPIO[2] pin 010 = Loss-of-Signal Flag for Input Reference 1 reflected on GPIO[2] pin 011 = reserved 100 = reserved 101 through 111 = reserved |
| GPO3SEL[2:0] | R/W | 000b | Function of GPIO[3] pin when set to output mode by GPIO_DIR[3] register bit: 000 = General Purpose Output (value in GPO[3] register bit driven on GPIO[3] pin) 001 = Loss-of-Lock Status Flag for Digital PLL1 reflected on GPIO[3] pin 010 = Loss-of-Signal Status Flag for Input Reference 1 reflected on GPIO[3] pin 011 = reserved 100 = reserved 101 through 111 = reserved |
| GPO[3:0] | R/W | 00h | Output Values reflect on pin GPIO[3:0] when General-Purpose Output Mode selected. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6J. Output Driver Control Register Bit Field Locations and Descriptions

| Output Driver Control Register Block Field Locations | | | | | | | | |
|--|---------------|----|----|----------|---------------|----|----|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0077 | OUTEN[7:0] | | | | | | | |
| 0078 | POL_Q[7:0] | | | | | | | |
| 0079 | OUTMODE7[2:0] | | | SE_MODE7 | OUTMODE6[2:0] | | | SE_MODE6 |
| 007A | OUTMODE5[2:0] | | | SE_MODE5 | OUTMODE4[2:0] | | | SE_MODE4 |
| 007B | OUTMODE3[2:0] | | | SE_MODE3 | OUTMODE2[2:0] | | | SE_MODE2 |
| 007C | OUTMODE1[2:0] | | | SE_MODE1 | OUTMODE0[2:0] | | | SE_MODE0 |

| Output Driver Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| OUTEN[7:0] | R/W | 00h | Output Enable control for Clock Outputs Q[7:0], nQ[7:0]: 0 = Qn is in a high-impedance state 1 = Qn is enabled as indicated in appropriate OUTMODEn[2:0] register field |
| POL_Q[7:0] | R/W | 00h | Polarity of Clock Outputs Q[7:0], nQ[7:0]: 0 = normal polarity 1 = inverted polarity |
| OUTMODEm[2:0] | R/W | 001b | Output Driver Mode of Operation for Clock Output Pair Qm, nQm: 000 = High-impedance 001 = LVPECL 010 = LVDS 011 = LVCMOS 100 = HCSL 101 - 111 = reserved |
| SE_MODEm | R/W | 0b | Behavior of Output Pair Qm, nQm when LVCMOS operation is selected: (Must be 0 if LVDS, HCSL or LVPECL output style is selected) 0 = Qm and nQm are both the same frequency but inverted in phase 1 = Qm and nQm are both the same frequency and phase |

Table 6K. Output Divider Control Register Bit Field Locations and Descriptions

| Output Divider Control Register Block Field Locations | | | | | | | | |
|---|-----------------|----|----|----|-----------------|----|-------------|----|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 007D | Rsvd | | | | | | NS1_Q0[1:0] | |
| 007E | NS2_Q0[15:8] | | | | | | | |
| 007F | NS2_Q0[7:0] | | | | | | | |
| 0080 | Rsvd | | | | | | NS1_Q1[1:0] | |
| 0081 | NS2_Q1[15:8] | | | | | | | |
| 0082 | NS2_Q1[7:0] | | | | | | | |
| 0083 | Rsvd | | | | | | N_Q2[17:16] | |
| 0084 | N_Q2[15:8] | | | | | | | |
| 0085 | N_Q2[7:0] | | | | | | | |
| 0086 | Rsvd | | | | | | N_Q3[17:16] | |
| 0087 | N_Q3[15:8] | | | | | | | |
| 0088 | N_Q3[7:0] | | | | | | | |
| 0089 | Rsvd | | | | | | NS1_Q4[1:0] | |
| 008A | NS2_Q4[15:8] | | | | | | | |
| 008B | NS2_Q4[7:0] | | | | | | | |
| 008C | Rsvd | | | | | | NS1_Q5[1:0] | |
| 008D | NS2_Q5[15:8] | | | | | | | |
| 008E | NS2_Q5[7:0] | | | | | | | |
| 008F | Rsvd | | | | | | NS1_Q6[1:0] | |
| 0090 | NS2_Q6[15:8] | | | | | | | |
| 0091 | NS2_Q6[7:0] | | | | | | | |
| 0092 | Rsvd | | | | | | NS1_Q7[1:0] | |
| 0093 | NS2_Q7[15:8] | | | | | | | |
| 0094 | NS2_Q7[7:0] | | | | | | | |
| 0095 | Rsvd | | | | NFRAC_Q2[27:24] | | | |
| 0096 | NFRAC_Q2[23:16] | | | | | | | |
| 0097 | NFRAC_Q2[15:8] | | | | | | | |
| 0098 | NFRAC_Q2[7:0] | | | | | | | |
| 0099 | Rsvd | | | | NFRAC_Q3[27:24] | | | |
| 009A | NFRAC_Q3[23:16] | | | | | | | |
| 009B | NFRAC_Q3[15:8] | | | | | | | |
| 009C | NFRAC_Q3[7:0] | | | | | | | |

Output Divider Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|---------------------------------|------------|---------------|---|
| NS1_Qm[1:0] (m = 0, 1) | R/W | 10b | 1st Stage Output Divider Ratio for Output Clock Qm, nQm: (m = 0, 1): 00 = /5 01 = /6 10 = /4 11 = Output Qm, nQm not switching |
| NS1_Qm[1:0] (m = 4, 5, 6, 7) | R/W | 10b | 1st Stage Output Divider Ratio for Output Clock Qm, nQm (m = 4, 5, 6, 7): 00 = /5 01 = /6 10 = /4 11 = /1 (Do not use this selection if PLL0 or PLL1 are the source since the 2nd-stage divider has a limit of 1GHz.) |
| NS2_Qm[15:0] | R/W | 0002h | 2nd Stage Output Divider Ratio for Output Clock Qm, nQm (m = 0, 1, 4, 5, 6, 7): Actual divider ratio is 2x the value written here. A value of 0 in this register will bypass the second stage of the divider. |
| N_Qm[17:0] | R/W | 00008h | Integer Portion of Output Divider Ratio for Output Clock Qm, nQm (m = 2, 3): Values of 0, 1 or 2 cannot be written to this register. Actual divider ratio is 2x the value written here. |
| NFRAC_Qm[27:0] | R/W | 0000000h | Fractional Portion of Output Divider Ratio for Output Clock Qm, nQm (m = 2, 3): Actual fractional portion is 2x the value written here. Fraction = (NFRAC_Qm * 2) * 2 ⁻²⁸ |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6L. Output Clock Phase Adjustment Control Register Bit Field Locations and Descriptions

| Output Clock Phase Adjustment Control Register Block Field Locations | | | | | | | | |
|--|---------------|------|------|----|----|--------------|----|----|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 009D | CRSE_TRG[7:0] | | | | | | | |
| 009E | | Rsvd | | | | COARSE0[4:0] | | |
| 009F | | Rsvd | | | | COARSE1[4:0] | | |
| 00A0 | | Rsvd | | | | COARSE2[4:0] | | |
| 00A1 | | Rsvd | | | | COARSE3[4:0] | | |
| 00A2 | | Rsvd | | | | COARSE4[4:0] | | |
| 00A3 | | Rsvd | | | | COARSE5[4:0] | | |
| 00A4 | | Rsvd | | | | COARSE6[4:0] | | |
| 00A5 | | Rsvd | | | | COARSE7[4:0] | | |
| 00A6 | | | Rsvd | | | FINE2[3:0] | | |
| 00A7 | | | Rsvd | | | FINE3[3:0] | | |

| Output Clock Phase Adjustment Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| CRSE_TRG[7:0] | R/W | 00h | Trigger Coarse Phase Adjustment for output Qm, nQm by amount specified in COARSEm[4:0] register upon 0→1 transition of this Trigger register bit. Please ensure the PA_BUSYm status bit is 0 before triggering another adjustment cycle on that particular output. Trigger bit must be returned to 0 before another delay cycle can be triggered. |
| COARSEm[4:0] | R/W | 00000b | Number of periods to be inserted when Trigger happens. Relevant clock period is determined by the clock source selected for output Qm, nQm in its CLK_SELm register field. |
| FINEm[3:0] | R/W | 0000b | Number of 1/16ths of the relevant clock period to add to the phase of output Qm, nQm (m = 2,3). Relevant clock period is determined by the clock source selected for output Qm, nQm in its CLK_SELm register field. The PLLn_SYN bit for the PLL driving the output divider for the output in question must be toggled to make this value take effect. Note that toggling the PLLn_SYN bit will clear all Coarse delay values and so Fine delay should be set first. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6M. Output Clock Source Control Register Bit Field Locations and Descriptions

| Output Clock Source Control Register Block Field Locations | | | | | | | | |
|--|------|---------------|----------|----------|----------|---------------|----------|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00A8 | Rsvd | | PLL1_SYN | PLL0_SYN | CLK_SEL3 | CLK_SEL2 | CLK_SEL1 | CLK_SEL0 |
| 00A9 | Rsvd | CLK_SEL5[2:0] | | | Rsvd | CLK_SEL4[2:0] | | |
| 00AA | Rsvd | CLK_SEL7[2:0] | | | Rsvd | CLK_SEL6[2:0] | | |
| 00AB | 11 | | 11 | | Rsvd | | Rsvd | |

| Output Clock Source Control Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| PLL1_SYN | R/W | 0b | Output Synchronization Control for Outputs Derived from PLL1: Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0. |
| PLL0_SYN | R/W | 0b | Output Synchronization Control for Outputs Derived from PLL0: Setting this bit from 0→1 will cause the output divider(s) for the affected outputs to be held in reset. Setting this bit from 1→0 will release all the output divider(s) for the affected outputs to run from the same point in time with the coarse output phase adjustment reset to 0. |
| CLK_SEL0 | R/W | 0b | Clock Source Selection for output Q0, nQ0: 0 = PLL0 1 = PLL1 |
| CLK_SEL1 | R/W | 1b | Clock Source Selection for output Q1, nQ1: 0 = PLL0 1 = PLL1 |
| CLK_SEL2 | R/W | 0b | Clock Source Selection for output Q2, nQ2: 0 = PLL0 1 = PLL1 |
| CLK_SEL3 | R/W | 1b | Clock Source Selection for output Q3, nQ3: 0 = PLL0 1 = PLL1 |
| CLK_SEL4[2:0] | R/W | 000b | Clock Source Selection for output Q4, nQ4. Do not select Input Reference 0 or 1 if that input is faster than 250MHz. 000 = PLL0 001 = PLL1 010 = Output Q2, nQ2 011 = Output Q3, nQ3 100 = Input Reference 0 (CLK0) 101 = Input Reference 1 (CLK1) 110 = Reserved 111 = Crystal input |
| CLK_SEL5[2:0] | R/W | 010b | Clock Source Selection for output Q5, nQ5. Do not select Input Reference 0 or 1 if that input is faster than 250MHz. 000 = PLL0 001 = PLL1 010 = Output Q2, nQ2 011 = Output Q3, nQ3 100 = Input Reference 0 (CLK0) 101 = Input Reference 1 (CLK1) 110 = Reserved 111 = Crystal input |

Output Clock Source Control Register Block Field Descriptions

| Bit Field Name | Field Type | Default Value | Description |
|----------------|------------|---------------|---|
| CLK_SEL6[2:0] | R/W | 000b | Clock Source Selection for output Q6, nQ6. Do not select Input Reference 0 or 1 if that input is faster than 250MHz. 000 = PLL0 001 = PLL1 010 = Output Q2, nQ2 011 = Output Q3, nQ3 100 = Input Reference 0 (CLK0) 101 = Input Reference 1 (CLK1) 110 = Reserved 111 = Crystal input |
| CLK_SEL7[2:0] | R/W | 101b | Clock Source Selection for output Q7, nQ7. Do not select Input Reference 0 or 1 if that input is faster than 250MHz. 000 = PLL0 001 = PLL1 010 = Output Q2, nQ2 011 = Output Q3 nQ3 100 = Input Reference 0 (CLK0) 101 = Input Reference 1 (CLK1) 110 = Reserved 111 = Crystal input |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6N. Analog PLL0 Control Register Bit Field Locations and Descriptions

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

| Analog PLL0 Control Register Block Field Locations | | | | | | | | |
|--|--------------|----|----------|--------------|---------------|-----------|---------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00AC | CPSET_0[2:0] | | | RS_0[1:0] | | CP_0[1:0] | | WPOST_0 |
| 00AD | Rsvd | | | | SYN_MODE 0 | Rsvd | DLCNT_0 | DBITM_0 |
| 00AE | Rsvd | | VCOMAN_0 | DBIT1_0[4:0] | | | | |
| 00AF | Rsvd | | | DBIT2_0[4:0] | | | | |

| Analog PLL0 Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| CPSET_0[2:0] | R/W | 100b | Charge Pump Current Setting for Analog PLL0: 000 = 110µA 001 = 220µA 010 = 330µA 011 = 440µA 100 = 550µA 101 = 660µA 110 = 770µA 111 = 880µA |
| RS_0[1:0] | R/W | 01b | Internal Loop Filter Series Resistor Setting for Analog PLL0: 00 = 330Ω 01 = 640Ω 10 = 1.2kΩ 11 = 1.79kΩ |
| CP_0[1:0] | R/W | 01b | Internal Loop Filter Parallel Capacitor Setting for Analog PLL0: 00 = 40pF 01 = 80pF 10 = 140pF 11 = 200pF |
| WPOST_0 | R/W | 1b | Internal Loop Filter 2nd-Pole Setting for Analog PLL0: 0 = Rpost = 497Ω, Cpost = 40pF 1 = Rpost = 1.58kΩ, Cpost = 40pF |
| DLCNT_0 | R/W | 1b | Digital Lock Count Setting for Analog PLL0: Value should be set to 0 (1ppm accuracy) if external capacitor value is >95nF, otherwise set to 1. 0 = 1ppm accuracy 1 = 16ppm accuracy |
| DBITM_0 | R/W | 0b | Digital Lock Manual Override Setting for Analog PLL0: 0 = Automatic Mode 1 = Manual Mode |
| VCOMAN_0 | R/W | 1b | Manual Lock Mode VCO Selection Setting for Analog PLL0: 0 = VCO2 1 = VCO1 |
| DBIT1_0[4:0] | R/W | 01011b | Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL0. |

| Analog PLL0 Control Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| DBIT2_0[4:0] | R/W | 00000b | Manual Mode Digital Lock Control Setting for VCO2 in Analog PLL0. |
| SYN_MODE0 | R/W | 0b | Frequency Synthesizer Mode Control for PLL0: 0 = PLL0 jitter attenuates and translates one or more input references 1 = PLL0 synthesizes output frequencies using only the crystal as a reference Note that the STATE0[1:0] field in the Digital PLL0 Control Register must be set to Force Freerun state. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 60. Analog PLL1 Control Register Bit Field Locations and Descriptions

Please contact IDT through one of the methods listed on the last page of this datasheet for details on how to set these fields for a particular user configuration.

| Analog PLL1 Control Register Block Field Locations | | | | | | | | |
|--|--------------|----|----------|--------------|---------------|-----------|---------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00B0 | CPSET_1[2:0] | | | RS_1[1:0] | | CP_1[1:0] | | WPOST_1 |
| 00B1 | Rsvd | | | | SYN_MOD E1 | Rsvd | DLCNT_1 | DBITM_1 |
| 00B2 | Rsvd | | VCOMAN_1 | DBIT1_1[4:0] | | | | |
| 00B3 | Rsvd | | | DBIT2_1[4:0] | | | | |

| Analog PLL1 Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| CPSET_1[2:0] | R/W | 100b | Charge Pump Current Setting for Analog PLL1: 000 = 110 μ A 001 = 220 μ A 010 = 330 μ A 011 = 440 μ A 100 = 550 μ A 101 = 660 μ A 110 = 770 μ A 111 = 880 μ A |
| RS_1[1:0] | R/W | 01b | Internal Loop Filter Series Resistor Setting for Analog PLL1: 00 = 330 Ω 01 = 640 Ω 10 = 1.2k Ω 11 = 1.79k Ω |
| CP_1[1:0] | R/W | 01b | Internal Loop Filter Parallel Capacitor Setting for Analog PLL1: 00 = 40pF 01 = 80pF 10 = 140pF 11 = 200pF |
| WPOST_1 | R/W | 1b | Internal Loop Filter 2nd-Pole Setting for Analog PLL1: 0 = Rpost = 497 Ω , Cpost = 40pF 1 = Rpost = 1.58k Ω , Cpost = 40pF |
| DLCNT_1 | R/W | 1b | Digital Lock Count Setting for Analog PLL1: Value should be set to 0 (1ppm accuracy) if external capacitor value is >95nF, otherwise set to 1. 0 = 1ppm accuracy 1 = 16ppm accuracy |
| DBITM_1 | R/W | 0b | Digital Lock Manual Override Setting for Analog PLL1: 0 = Automatic Mode 1 = Manual Mode |

| Analog PLL1 Control Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| VCOMAN_1 | R/W | 1b | Manual Lock Mode VCO Selection Setting for Analog PLL1: 0 = VCO2 1 = VCO1 |
| DBIT1_1[4:0] | R/W | 01011b | Manual Mode Digital Lock Control Setting for VCO1 in Analog PLL1. |
| DBIT2_1[4:0] | R/W | 00000b | Manual Mode Digital Lock Control Setting for VCO2 in Analog PLL1. |
| SYN_MODE1 | R/W | 0b | Frequency Synthesizer Mode Control for PLL1: 0 = PLL1 jitter attenuates and translates one or more input references 1 = PLL1 synthesizes output frequencies using only the crystal as a reference Note that the STATE1[1:0] field in the Digital PLL1 Control Register must be set to Force Freerun state. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6P. Power Down Control Register Bit Field Locations and Descriptions

| Power Down Control Register Block Field Locations | | | | | | | | |
|---|--------|--------|--------|----------|-----------|-----------|----------|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00B4 | Rsvd | | | | | | | DBL_DIS |
| 00B5 | Rsvd | | | | 1 | 1 | CLK1_DIS | CLK0_DIS |
| 00B6 | Rsvd | | | PLL1_DIS | Rsvd | | | |
| 00B7 | Q7_DIS | Q6_DIS | Q5_DIS | Q4_DIS | Q3_DIS | Q2_DIS | Q1_DIS | Q0_DIS |
| 00B8 | Rsvd | | | | DPLL1_DIS | DPLL0_DIS | CALRST1 | CALRST0 |

| Power Down Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| DBL_DIS | R/W | 0b | Controls whether Crystal Input Frequency is Doubled before Being used in PLL0 or PLL1: 0 = 2x Actual Crystal Frequency Used 1 = Actual Crystal Frequency Used |
| CLKm_DIS | R/W | 0b | Disable Control for Input Reference m: 0 = Input Reference m is Enabled 1 = Input Reference m is Disabled |
| PLL1_DIS | R/W | 0b | Disable Control for Analog PLL1: 0 = PLL1 Enabled 1 = Analog PLL1 Disabled |
| Qm_DIS | R/W | 0b | Disable Control for Output Qm, nQm: 0 = Output Qm, nQm functions normally 1 = All logic associated with Output Qm, nQm is Disabled & Driver in High-Impedance state |
| DPLLm_DIS | R/W | 0b | Disable Control for Digital PLLm: 0 = Digital PLLm Enabled 1 = Digital PLLm Disabled |
| CALRSTm | R/W | 0b | Reset Calibration Logic for APLLm: 0 = Calibration Logic for APLLm Enabled 1 = Calibration Logic for APLLm Disabled |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6Q. Input Monitor Control Register Bit Field Locations and Descriptions

| Input Monitor Control Register Block Field Locations | | | | | | | | |
|--|-------------|----|----|----|----|----|----|-----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00B9 | Rsvd | | | | | | | LOS_0[16] |
| 00BA | LOS_0[15:8] | | | | | | | |
| 00BB | LOS_0[7:0] | | | | | | | |
| 00BC | Rsvd | | | | | | | LOS_1[16] |
| 00BD | LOS_1[15:8] | | | | | | | |
| 00BE | LOS_1[7:0] | | | | | | | |
| 00BF | Rsvd | | | | | | | Rsvd |
| 00C0 | Rsvd | | | | | | | |
| 00C1 | Rsvd | | | | | | | |
| 00C2 | Rsvd | | | | | | | Rsvd |
| 00C3 | Rsvd | | | | | | | |
| 00C4 | Rsvd | | | | | | | |
| 00C5 | Rsvd | | | | | | | |
| 00C6 | Rsvd | | | | | | | |

| Input Monitor Control Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| LOS_m[16:0] | R/W | 1FFFFh | Number of Input Monitoring clock periods before Input Reference m is considered to be missed (soft alarm). Minimum setting is 3. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6R. Interrupt Enable Control Register Bit Field Locations and Descriptions

| Interrupt Enable Control Register Block Field Locations | | | | | | | | |
|---|---------|---------|----------|----------|------|------|---------|---------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00C7 | LOL1_EN | LOL0_EN | HOLD1_EN | HOLD0_EN | Rsvd | Rsvd | LOS1_EN | LOS0_EN |

| Interrupt Enable Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| LOLm_EN | R/W | 0b | Interrupt Enable Control for Loss-of-Lock Interrupt Status Bit for PLLm: 0 = LOLm_INT register bit will not affect status of nINT output signal 1 = LOLm_INT register bit will affect status of nINT output signal |
| HOLDm_EN | R/W | 0b | Interrupt Enable Control for Holdover Interrupt Status Bit for PLLm: 0 = HOLDm_INT register bit will not affect status of nINT output signal 1 = HOLDm_INT register bit will affect status of nINT output signal |
| LOSm_EN | R/W | 0b | Interrupt Enable Control for Loss-of-Signal Interrupt Status Bit for Input Reference m: 0 = LOSm_INT register bit will not affect status of nINT output signal 1 = LOSm_INT register bit will affect status of nINT output signal |

Table 6S. Digital Phase Detector Control Register Bit Field Locations and Descriptions

| Digital Phase Detector Control Register Block Field Locations | | | | | | | | |
|---|------|----|----|------|----|------|------|------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00C8 | 27h | | | | | | | |
| 00C9 | Rsvd | | 1 | Rsvd | 1 | Rsvd | Rsvd | Rsvd |
| 00CA | 27h | | | | | | | |
| 00CB | Rsvd | | 1 | Rsvd | 1 | Rsvd | Rsvd | Rsvd |

| Digital Phase Detector Control Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6T. Interrupt Status Register Bit Field Locations and Descriptions

This register contains “sticky” bits for tracking the status of the various alarms. Whenever an alarm occurs, the appropriate Interrupt Status bit will be set. The Interrupt Status bit will remain asserted even after the original alarm goes away. The Interrupt Status bits remain asserted until explicitly cleared by a write of a ‘1’ to the bit over the serial port. This type of functionality is referred to as Read / Write-1-to-Clear (R/W1C).

| Interrupt Status Register Block Field Locations | | | | | | | | |
|---|----------|----------|-----------|-----------|------|------|----------|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0200 | LOL1_INT | LOLO_INT | HOLD1_INT | HOLD0_INT | Rsvd | Rsvd | LOS1_INT | LOS0_INT |
| 0201 | Rsvd | | | | | | | |
| 0202 | Rsvd | | | | | | | |
| 0203 | Rsvd | | | | | | | |

| Interrupt Status Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| LOLm_INT | R/W1C | 0b | Interrupt Status Bit for Loss-of-Lock on PLLm: 0 = No Loss-of-Lock alarm flag on PLLm has occurred since the last time this register bit was cleared 1 = At least one Loss-of-Lock alarm flag on PLLm has occurred since the last time this register bit was cleared |
| HOLDm_INT | R/W1C | 0b | Interrupt Status Bit for Holdover on PLLm: 0 = No Holdover alarm flag on PLLm has occurred since the last time this register bit was cleared 1 = At least one Holdover alarm flag on PLLm has occurred since the last time this register bit was cleared |
| LOSm_INT | R/W1C | 0b | Interrupt Status Bit for Loss-of-Signal on Input Reference m: 0 = No Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared 1 = At least one Loss-of-Signal alarm flag on Input Reference m has occurred since the last time this register bit was cleared |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6U. Output Phase Adjustment Status Register Bit Field Locations and Descriptions

| Output Phase Adjustment Status Register Block Field Locations | | | | | | | | |
|---|----------|----------|----------|----------|----------|----------|----------|----------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0204 | PA_BUSY7 | PA_BUSY6 | PA_BUSY5 | PA_BUSY4 | PA_BUSY3 | PA_BUSY2 | PA_BUSY1 | PA_BUSY0 |

| Output Phase Adjustment Status Register Block Field Descriptions | | | |
|--|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| PA_BUSYm | R/O | - | Phase Adjustment Event Status for output Qm, nQm: 0 = No phase adjustment is currently in progress on output Qm, nQm 1 = Phase adjustment still in progress on output Qm, nQm. Do not initiate any new phase adjustment at this time |

The following register is included for debug purposes only. It shows the actual digital PLL0 state directly. This means that the bits may change rapidly as the DPLL operates. The fields in this register do not represent a “snapshot” in time, so they may be inconsistent with one another if the DPLL is rapidly changing at the time of reading. Fast changes in the status of the PLL cannot be captured by polling these bits, in which case, IDT recommends using the Sticky Bits interrupts and GPIOs.

Table 6V. Digital PLL0 Status Register Bit Field Locations and Descriptions

| Digital PLL0 Status Register Block Field Locations | | | | | | | | | |
|--|------|------|----|---------|---------|----------------|--------------|------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0205 | | Rsvd | | EXTLOS0 | NO_REF0 | CURR_REF0[2:0] | | | |
| 0206 | | Rsvd | | PLL0LCK | Rsvd | Rsvd | SM_STS0[1:0] | | |
| 0207 | Rsvd | | | | | | | Rsvd | |
| 0208 | Rsvd | | | | | | | | |
| 0209 | Rsvd | | | | | | | | |
| 020A | Rsvd | | | | | | | Rsvd | |
| 020B | Rsvd | | | | | | | | |
| 020C | Rsvd | | | | | | | | |
| 020D | Rsvd | | | | | | | | |
| 020E | Rsvd | | | | | | | | |

| Digital PLL0 Status Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| EXTLOS0 | R/O | - | External Loopback signal lost for PLL0: 0 = PLL0 has a valid feedback reference signal 1 = PLL0 has lost the external feedback reference signal and is no longer locked |
| NO_REF0 | R/O | - | Valid Reference Status for Digital PLL0: 0 = At least one valid Input Reference is present 1 = No valid Input References present |
| CURR_REF0[2:0] | R/O | - | Currently Selected Reference Status for Digital PLL0: 000 - 011 = No reference currently selected 100 = Input Reference 0 (CLK0, nCLK0) selected 101 = Input Reference 1 (CLK1, nCLK1) selected 110 = Reserved 111 = Reserved |

| Digital PLL0 Status Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| PLL0LCK | R/O | - | Digital PLL0 phase error value is less than lock criteria. Not asserted if PLL0 in Synthesizer Mode. |
| SM_STS0[1:0] | R/O | - | Current State of Digital PLL0: 00 = Reserved 01 = Freerun 10 = Normal 11 = Holdover |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

The following register is included for debug purposes only. It shows the actual digital PLL1 state directly. This means that the bits may change rapidly as the DPLL operates. The fields in this register do not represent a “snapshot” in time, so they may be inconsistent with one another if the DPLL is rapidly changing at the time of reading. Fast changes in the status of the PLL cannot be captured by polling these bits, in which case, IDT recommends using the Sticky Bits interrupts and GPIOs.

Table 6W. Digital PLL1 Status Register Bit Field Locations and Descriptions

| Digital PLL1 Status Register Block Field Locations | | | | | | | | | |
|--|------|------|----|---------|---------|----------------|--------------|------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 020F | | Rsvd | | EXTLOS1 | NO_REF1 | CURR_REF1[2:0] | | | |
| 0210 | | Rsvd | | PLL1LCK | Rsvd | Rsvd | SM_STS1[1:0] | | |
| 0211 | Rsvd | | | | | | | Rsvd | |
| 0212 | Rsvd | | | | | | | | |
| 0213 | Rsvd | | | | | | | | |
| 0214 | Rsvd | | | | | | | Rsvd | |
| 0215 | Rsvd | | | | | | | | |
| 0216 | Rsvd | | | | | | | | |
| 0217 | Rsvd | | | | | | | | |
| 0218 | Rsvd | | | | | | | | |

| Digital PLL1 Status Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| EXTLOS1 | R/O | - | External Loopback signal lost for PLL1: 0 = PLL1 has a valid feedback reference signal 1 = PLL1 has lost the external feedback reference signal and is no longer locked |
| NO_REF1 | R/O | - | Valid Reference Status for Digital PLL1: 0 = At least one valid Input Reference is present 1 = No valid Input References present |
| CURR_REF1[2:0] | R/O | - | Currently Selected Reference Status for Digital PLL1: 000 - 011 = No reference currently selected 100 = Input Reference 0 (CLK0, nCLK0) selected 101 = Input Reference 1 (CLK1, nCLK1) selected 110 = Reserved 111 = Reserved |

| Digital PLL1 Status Register Block Field Descriptions | | | |
|---|------------|---------------|--|
| Bit Field Name | Field Type | Default Value | Description |
| PLL1LCK | R/O | - | Digital PLL1 phase error value is less than the LOCK window setting. Not asserted if PLL1 in Synthesizer Mode. |
| SM_STS1[1:0] | R/O | - | Current State of Digital PLL1: 00 = Reserved 01 = Freerun 10 = Normal 11 = Holdover |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Table 6X. General Purpose Input Status Register Bit Field Locations and Descriptions

| Global Interrupt Status Register Block Field Locations | | | | | | | | |
|--|------|----|----|----|--------|--------|--------|--------|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0219 | Rsvd | | | | GPI[3] | GPI[2] | GPI[1] | GPI[0] |

| General Purpose Input Status Register Block Field Descriptions | | | |
|--|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| GPI[3:0] | R/O | - | Shows current values on GPIO[3:0] pins that are configured as General-Purpose Inputs. |

Table 6Y. Global Interrupt Status Register Bit Field Locations and Descriptions

| Global Interrupt Status Register Block Field Locations | | | | | | | | | |
|--|------|------|------|-----------------|----------|------|------|----------|--|
| Address (Hex) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 021A | Rsvd | | | | Rsvd | | | INT | |
| 021B | Rsvd | | | | | | | | |
| 021C | Rsvd | | | CALI_DBIT0[5:0] | | | | | |
| 021D | Rsvd | | | CALI_DBIT1[5:0] | | | | | |
| 021E | Rsvd | | | | | Rsvd | Rsvd | BOOTFAIL | |
| 021F | Rsvd | Rsvd | Rsvd | Rsvd | nEEP_CRC | Rsvd | Rsvd | EEPDONE | |

| Global Interrupt Status Register Block Field Descriptions | | | |
|---|------------|---------------|---|
| Bit Field Name | Field Type | Default Value | Description |
| INT | R/O | - | Device Interrupt Status: 0 = No Interrupt Status bits that are enabled are asserted (nINT pin released) 1 = At least one Interrupt Status bit that is enabled is asserted (nINT pin asserted low) |
| BOOTFAIL | R/O | - | Reading of Serial EEPROM failed. Once set this bit is only cleared by reset. |
| nEEP_CRC | R/O | - | EEPROM CRC Error (Active Low): 0 = EEPROM was detected and read, but CRC check failed - please reset the device via the nRST pin to retry (serial port is locked) 1 = No EEPROM CRC Error |
| EEPDONE | R/O | - | Serial EEPROM Read cycle has completed. Once set this bit is only cleared by reset. |
| CALI_DBITn[5:0] | R/O | - | Indicates current digital bit setting for PLLn. |
| Rsvd | R/W | - | Reserved. Always write 0 to this bit location. Read values are not defined. |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--------------------------------------|
| Supply Voltage, V_{CC} | 3.63V |
| Inputs, V_I OSCI Other Input | 0V to 2V -0.5V to $V_{CC} + 0.5V$ |
| Outputs, V_O (Q[0:7], nQ[0:7]) | -0.5V to $V_{CCOX} + 0.5V$ |
| Outputs, V_O (GPIO[0:3], SDATA, SCLK, nINT) | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, I_O (Q[0:7], nQ[0:7]) Continuous Current Surge Current | 40mA 65mA |
| Outputs, I_O (GPIO[0:3], SDATA, SCLK, nINT) Continuous Current Surge Current | 8mA 13mA |
| Junction Temperature, T_J | 125°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: V_{CCOX} denotes V_{CC00} , V_{CC01} , V_{CC02} , V_{CC03} , V_{CC04} , V_{CC05} , V_{CC06} , V_{CC07} .

Supply Voltage Characteristics

Table 7A. Power Supply Characteristics, $V_{CC} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--|---|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.13$ | 3.3 | V_{CC} | V |
| I_{CC} | Core Supply Current; NOTE 1 | | | 74 | 100 | mA |
| I_{CCA} | Analog Supply Current; NOTE 1 | PLL0 and PLL1 Enabled | | 206 | 265 | mA |
| | | Analog PLL1, Digital PLL1, and Calibration Logic for analog PLL1 Disabled | | 122 | 187 | mA |
| I_{EE} | Power Supply Current; NOTE 2 | Q[0:7] Configured for LVPECL Logic Levels, Outputs Unloaded | | 562 | 735 | mA |

NOTE 1: I_{CC} and I_{CCA} are included in I_{EE} when Q[0:7] configured for LVPECL logic levels.

NOTE 2: Internal dynamic switching current at maximum f_{OUT} is included.

Table 7B. Power Supply Characteristics, $V_{CC} = 2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--|---|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.13$ | 2.5 | V_{CC} | V |
| I_{CC} | Core Supply Current; NOTE 1 | | | 72 | 95 | mA |
| I_{CCA} | Analog Supply Current; NOTE 1 | PLL0 and PLL1 Enabled | | 201 | 260 | mA |
| | | Analog PLL1, Digital PLL1, and Calibration Logic for analog PLL1 Disabled | | 119 | 182 | mA |
| I_{EE} | Power Supply Current; NOTE 2 | Q[0:7] Configured for LVPECL Logic Levels, Outputs Unloaded | | 533 | 695 | mA |

NOTE 1: I_{CC} and I_{CCA} are included in I_{EE} when Q[0:7] configured for LVPECL logic levels.

NOTE 2: Internal dynamic switching current at maximum f_{OUT} is included.

Table 7C. Maximum Output Supply Current, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | $V_{CC0x} = 3.3V \pm 5\%$ | | | | $V_{CC0x} = 2.5V \pm 5\%$ | | | | $V_{CC0x} = 1.8V \pm 5\%$ | Units |
|------------|-------------------------------|------------------|---------------------------|------|------|---------|---------------------------|------|------|---------|---------------------------|-------|
| | | | LVPECL | LVDS | HCSL | LVC MOS | LVPECL | LVDS | HCSL | LVC MOS | LVC MOS | |
| I_{CC00} | Q0, nQ0 Output Supply Current | Outputs Unloaded | 50 | 60 | 50 | 55 | 40 | 50 | 40 | 45 | 35 | mA |
| I_{CC01} | Q1, nQ1 Output Supply Current | Outputs Unloaded | 50 | 60 | 50 | 55 | 40 | 50 | 40 | 45 | 35 | mA |
| I_{CC02} | Q2, nQ2 Output Supply Current | Outputs Unloaded | 80 | 90 | 80 | 80 | 70 | 80 | 70 | 70 | 60 | mA |
| I_{CC03} | Q3, nQ3 Output Supply Current | Outputs Unloaded | 80 | 90 | 80 | 80 | 70 | 80 | 70 | 70 | 60 | mA |
| I_{CC04} | Q4, nQ4 Output Supply Current | Outputs Unloaded | 55 | 65 | 55 | 55 | 45 | 55 | 45 | 45 | 40 | mA |
| I_{CC05} | Q5, nQ5 Output Supply Current | Outputs Unloaded | 55 | 65 | 55 | 55 | 45 | 55 | 45 | 45 | 40 | mA |
| I_{CC06} | Q6, nQ6 Output Supply Current | Outputs Unloaded | 55 | 65 | 55 | 55 | 45 | 55 | 45 | 45 | 40 | mA |
| I_{CC07} | Q7, nQ7 Output Supply Current | Outputs Unloaded | 55 | 65 | 55 | 55 | 45 | 55 | 45 | 45 | 40 | mA |

NOTE: Internal dynamic switching current at maximum f_{OUT} is included.

NOTE: V_{CC0x} denotes V_{CC00} , V_{CC01} , V_{CC02} , V_{CC03} , V_{CC04} , V_{CC05} , V_{CC06} , V_{CC07} .

DC Electrical Characteristics

Table 8A. LVCMOS/LVTTL DC Characteristics, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|---------------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | $V_{CC} = 3.3V$ | 2 | | $V_{CC} + 0.3$ | V |
| | | | $V_{CC} = 2.5V$ | 1.7 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | $V_{CC} = 3.3V$ | -0.3 | | 0.8 | V |
| | | | $V_{CC} = 2.5V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | PLL_BYP, S_A0 | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 150 | μA |
| | | nRST, SDATA, SCLK | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 5 | μA |
| | | GPIO[3:0] | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 1 | mA |
| I_{IL} | Input Low Current | PLL_BYP, S_A0 | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | nRST, SDATA, SCLK | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -150 | | | μA |
| | | GPIO[3:0] | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -1 | | | mA |
| V_{OH} | Output High Voltage | nINT, SDATA, SCLK; NOTE 1 | $V_{CC} = 3.3V \pm 5\%$, $I_{OH} = -5\mu A$ | 2.6 | | | V |
| | | GPIO[3:0] | $V_{CC} = 3.3V \pm 5\%$, $I_{OH} = -50\mu A$ | 2.6 | | | V |
| | | nINT, SDATA, SCLK; NOTE 1 | $V_{CC} = 2.5V \pm 5\%$, $I_{OH} = -5\mu A$ | 1.8 | | | V |
| | | GPIO[3:0] | $V_{CC} = 2.5V \pm 5\%$, $I_{OH} = -50\mu A$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage | nINT, SDATA, SCLK; NOTE 1 | $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $I_{OL} = 5mA$ | | | 0.5 | V |
| | | GPIO[3:0] | $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $I_{OL} = 5mA$ | | | 0.5 | V |

NOTE 1: Use of external pull-up resistors is recommended.

Table 8B. Differential Input DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-------------|---|----------|---------|----------------|---------|
| I_{IH} | Input High Current | CLKx, nCLKx | $V_{CC} = V_{IN} = 3.465V$ or $2.625V$ | | | 150 | μA |
| I_{IL} | Input Low Current | CLKx | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | nCLKx | $V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{PP} | Peak-to-Peak Voltage; NOTE 1 | | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | | V_{EE} | | $V_{CC} - 1.2$ | V |

NOTE: CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

NOTE 1: V_{IL} should not be less than -0.3V. V_{IH} should not be higher than V_{CC} .

NOTE 2: Common mode voltage is defined as the cross-point.

Table 8C. LVPECL DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | $V_{CC0x} = 3.3V \pm 5\%$ | | | $V_{CC0x} = 2.5V \pm 5\%$ | | | Units |
|----------|--------------------------------|------------|-----------------|---------------------------|---------|-------------------|---------------------------|---------|-------------------|-------|
| | | | | Minimum | Typical | Maximum | Minimum | Typical | Maximum | |
| V_{OH} | Output High Voltage; NOTE 1 | Qx, nQx | | $V_{CC0x} - 1.3$ | | $V_{CC0x} - 0.8$ | $V_{CC0x} - 1.4$ | | $V_{CC0x} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | Qx, nQx | | $V_{CC0x} - 1.95$ | | $V_{CC0x} - 1.75$ | $V_{CC0x} - 1.95$ | | $V_{CC0x} - 1.75$ | V |

NOTE: V_{CC0x} denotes V_{CC00} , V_{CC01} , V_{CC02} , V_{CC03} , V_{CC04} , V_{CC05} , V_{CC06} , V_{CC07} .

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

NOTE 1: Outputs terminated with 50Ω to $V_{CC0x} - 2V$.

Table 8D. LVDS DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CC0x} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|---------|
| V_{OD} | Differential Output Voltage | Qx, nQx | | 195 | | 454 mV |
| ΔV_{OD} | V_{OD} Magnitude Change | Qx, nQx | | | 50 | mV |
| V_{OS} | Offset Voltage | Qx, nQx | | 1.1 | | 1.375 V |
| ΔV_{OS} | V_{OS} Magnitude Change | Qx, nQx | | | 50 | mV |

NOTE: V_{CC0x} denotes V_{CC00} , V_{CC01} , V_{CC02} , V_{CC03} , V_{CC04} , V_{CC05} , V_{CC06} , V_{CC07} .

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

NOTE: Terminated 100Ω across Qx and nQx.

Table 8E. LVCMOS DC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | $V_{CC0x} = 3.3V \pm 5\%$ | | | $V_{CC0x} = 2.5V \pm 5\%$ | | | $V_{CC0x} = 1.8V \pm 5\%$ | | | Units |
|----------|---------------------|------------|-----------------|---------------------------|---------|---------|---------------------------|---------|---------|---------------------------|---------|---------|-------|
| | | | | Minimum | Typical | Maximum | Minimum | Typical | Maximum | Minimum | Typical | Maximum | |
| V_{OH} | Output High Voltage | Qx, nQx | $I_{OH} = -8mA$ | 2.6 | | | 1.8 | | | 1.1 | | | V |
| V_{OL} | Output Low Voltage | Qx, nQx | $I_{OL} = 8mA$ | | | 0.5 | | | 0.5 | | | 0.5 | V |

NOTE: Qx denotes Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7. nQx denotes nQ0, nQ1, nQ2, nQ3, nQ4, nQ5, nQ6, nQ7.

NOTE: V_{CC0x} denotes V_{CC00} , V_{CC01} , V_{CC02} , V_{CC03} , V_{CC04} , V_{CC05} , V_{CC06} , V_{CC07} .

Table 9. Input Frequency Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|------------|--|-----------------|--|---------|---------|-------|-----|
| f_{IN} | Input Frequency; NOTE 1 | OSCI, OSCO | Using a crystal (See Table 10 , Crystal Characteristics) | 10 | | 40 | MHz |
| | | | Overdriving Crystal Input, Doubler Logic Enabled; NOTE 2 | 10 | | 62.5 | MHz |
| | | | Overdriving Crystal Input, Doubler Logic Disabled; NOTE 2 | 16 | | 125 | MHz |
| | CLKx, nCLKx | | 0.008 | | 875 | MHz | |
| f_{SCLK} | Serial Port Clock | SCLK | Slave Mode | | 100 | 400 | kHz |

NOTE: CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

NOTE 1: For the input reference frequency, the divider values must be set for the VCO to operate within its supported range.

NOTE 2: For optimal noise performance, the use of a quartz crystal is recommended. Refer to Applications Information, [Overdriving the Crystal Interface](#).

Table 10. Crystal Characteristics

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 10 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | 15 | | Ω |
| Load Capacitance (C_L) | | | 12 | | pF |
| Frequency Stability (total) | | -100 | | 100 | ppm |

AC Electrical Characteristics

Table 11A. AC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CCOx} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$ (1.8V only supported for LVCMOS outputs), $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|-------------|----------------------------|--------------------|--|---------|---------|--------|------|
| f_{VCO} | VCO Operating Frequency | | 3000 | | 4000 | MHz | |
| f_{OUT} | Output Frequency | LVPECL, LVDS, HCSL | Q0, Q1, Q4, Q5, Q6, Q7 Outputs | 0.008 | | 1000 | MHz |
| | | | Q2, Q3 Outputs Integer Divide Ratio & No Added Phase Delay | 0.008 | | 666.67 | MHz |
| | | | Q2, Q3 Outputs Non-integer Divide and/or Added Phase Delay | 0.008 | | 400 | MHz |
| | | LVCMOS | 0.008 | | 250 | MHz | |
| t_R / t_F | Output Rise and Fall Times | LVPECL | 20% to 80% | 145 | 360 | 600 | ps |
| | | LVDS | 20% to 80% | 100 | 230 | 400 | ps |
| | | HCSL | 20% to 80% | 150 | 300 | 600 | ps |
| | | LVCMOS; NOTE 1, 2 | 20% to 80%, $V_{CCOx} = 3.3V$ | 180 | 350 | 600 | ps |
| | | | 20% to 80%, $V_{CCOx} = 2.5V$ | 200 | 350 | 550 | ps |
| | | | 20% to 80%, $V_{CCOx} = 1.8V$ | 200 | 410 | 650 | ps |
| SR | Output Slew Rate; NOTE 3 | LVPECL | Measured on Differential Waveform, $\pm 150mV$ from Center | 1 | | 5 | V/ns |
| | | LVDS | Measured on Differential Waveform, $\pm 150mV$ from Center | 0.5 | | 4 | V/ns |
| | | HCSL | $V_{CCOx} = 2.5V$, $f_{OUT} \leq 125MHz$; Measured on Differential Waveform, $\pm 150mV$ from Center | 1.5 | | 4 | V/ns |
| | | | $V_{CCOx} = 3.3V$, $f_{OUT} \leq 125MHz$; Measured on Differential Waveform, $\pm 150mV$ from Center | 2.5 | | 5.5 | V/ns |

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------------|--|----------------------|---|-----------------|---------|---------|--------|
| tsk(b) | Bank Skew | LVPECL | Q0, nQ0, Q1, nQ1 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q4, nQ4, Q5, nQ5 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q6, nQ6, Q7, nQ7 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | LVDS | Q0, nQ0, Q1, nQ1 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q4, nQ4, Q5, nQ5 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q6, nQ6, Q7, nQ7 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | HCSL | Q0, nQ0, Q1, nQ1 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q4, nQ4, Q5, nQ5 | NOTE 4, 5, 6, 7 | | 75 | ps |
| | | | Q6, nQ6, Q7, nQ7 | NOTE 4, 5, 6, 7 | | 75 | ps |
| LVCMOS | Q0, nQ0, Q1, nQ1 | NOTE 1, 4, 5, 7, 8 | | 80 | ps | | |
| | Q4, nQ4, Q5, nQ5 | NOTE 1, 4, 5, 7, 8 | | 115 | ps | | |
| | Q6, nQ6, Q7, nQ7 | NOTE 1, 4, 5, 7, 8 | | 115 | ps | | |
| odc | Output Duty Cycle; NOTE 9 | LVPECL, LVDS, HCSL | $f_{OUT} \leq 666.667\text{MHz}$ | 45 | 50 | 55 | % |
| | | | $f_{OUT} > 666.667\text{MHz}$ | 40 | 50 | 60 | % |
| | | LVCMOS | 40 | 50 | 60 | % | |
| | Initial Frequency Offset; NOTE 10, 11, 12 | | Switchover or Entering / Leaving Holdover State | -50 | | 50 | ppb |
| | Output Phase Change in Fully Hitless Switching; NOTE 11, 12, 13 | | Switchover or Entering / Leaving Holdover State | | 5 | | ns |
| $\Phi_{SSB}(1k)$ | Single Sideband Phase Noise; NOTE 14 | 1kHz | 122.88MHz Output | | -123 | | dBc/Hz |
| $\Phi_{SSB}(10k)$ | | 10kHz | 122.88MHz Output | | -131 | | dBc/Hz |
| $\Phi_{SSB}(100k)$ | | 100kHz | 122.88MHz Output | | -134 | | dBc/Hz |
| $\Phi_{SSB}(1M)$ | | 1MHz | 122.88MHz Output | | -147 | | dBc/Hz |
| $\Phi_{SSB}(10M)$ | | 10MHz | 122.88MHz Output | | -153 | | dBc/Hz |
| $\Phi_{SSB}(30M)$ | | $\geq 30\text{MHz}$ | 122.88MHz Output | | -154 | | dBc/Hz |
| | Spurious Limit at Offset; NOTE 15 | $\geq 800\text{kHz}$ | 122.88MHz Output | | -83 | | dBc |

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units | |
|----------------------|--|--|--|---------|---------|-------|----|
| t _{startup} | Startup Time | Internal OTP Startup; NOTE 11 | from V _{CC} >80% to First Output Clock Edge | | 110 | 150 | ms |
| | | External EEPROM Startup; NOTE 11, 16 | from V _{CC} >80% to First Output Clock Edge (0 retries); I ² C Frequency = 100kHz | | 150 | 200 | ms |
| | | | from V _{CC} >80% to First Output Clock Edge (0 retries); I ² C Frequency = 400kHz | | 130 | 150 | ms |
| | | | from V _{CC} >80% to First Output Clock Edge (31 retries); I ² C Frequency = 100kHz | | 925 | 1200 | ms |
| | | | from V _{CC} >80% to First Output Clock Edge (31 retries); I ² C Frequency = 400kHz | | 360 | 500 | ms |
| ΔSPO | Static Phase Offset Variation; NOTE 17 | f _{IN} = f _{OUT} = 156.25MHz | -175 | | 175 | ps | |

NOTE: V_{CCOx} denotes V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4}, V_{CCO5}, V_{CCO6}, V_{CCO7}.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Appropriate SE_MODE bit must be configured to select phase-aligned or phase-inverted operation.

NOTE 2: All Q and nQ outputs in phase-inverted operation

NOTE 3: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Measured at the output differential cross point.

NOTE 7: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions running off the same PLL.

NOTE 8: Measured at V_{CCOx}/2 of the rising edge. All Qx and nQx outputs phase-aligned.

NOTE 9: Characterized in synthesizer mode. Duty cycle of bypassed signals (input reference clocks or crystal input) is not adjusted by the device.

NOTE 10: Tested in fast-lock operation after >20 minutes of locked operation to ensure holdover averaging logic is stable.

NOTE 11: This parameter is guaranteed by design.

NOTE 12: Using internal feedback mode configuration.

NOTE 13: Device programmed with SWMODEn = 0 (absorbs phase differences).

NOTE 14: Characterized with 8T49N287B-901 units (synthesizer mode).

NOTE 15: Tested with all outputs operating at 122.88MHz.

NOTE 16: Assuming a clear I²C bus.

NOTE 17: This parameter was measured using CLK0 as the reference input and CLK1 as the external feedback input. Characterized with 8T49N287-908.

Table 11B. HCSL AC Characteristics, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CCOx} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------------|--|-----------------|---------|---------|---------|-------|
| V_{RB} | Ring-back Voltage Margin; NOTE 1, 2 | | -100 | | 100 | mV |
| t_{STABLE} | Time before V_{RB} is allowed; NOTE 1, 2 | | 500 | | | ps |
| V_{MAX} | Absolute Max. Output Voltage; NOTE 3, 4 | | | | 1150 | mV |
| V_{MIN} | Absolute Min. Output Voltage; NOTE 3, 5 | | -300 | | | mV |
| V_{CROSS} | Absolute Crossing Voltage; NOTE 6, 7 | | 230 | | 550 | mV |
| ΔV_{CROSS} | Total Variation of V_{CROSS} Over all Edges; NOTE 6, 8 | | | | 140 | mV |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measurement taken from differential waveform.

NOTE 2: T_{STABLE} is the time the differential clock must maintain a minimum $\pm 150mV$ differential voltage after rising/falling edges before it is allowed to drop back into the $V_{RB} \pm 100mV$ differential range.

NOTE 3: Measurement taken from single ended waveform.

NOTE 4: Defined as the maximum instantaneous voltage including overshoot.

NOTE 5: Defined as the minimum instantaneous voltage including undershoot.

NOTE 6: Measured at crossing point where the instantaneous voltage value of the rising edge of Qn equals the falling edge of nQn.

NOTE 7: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

NOTE 8: Defined as the total variation of all crossing voltages of rising Qn and falling nQn. This is the maximum allowed variance in V_{CROSS} for any particular system.

Table 12A. Typical RMS Phase Jitter (Synthesizer Mode), $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CCOx} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$ (1.8V only supported for LVCMOS outputs), $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | LVPECL | LVDS | HCSL | LVCMOS NOTE 6 | Units |
|----------------|---------------------------|---|--|--------|------|------|------------------|-------|
| tjit(ϕ) | RMS Phase Jitter (Random) | Q0, Q1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz; NOTE 1 | 282 | 299 | 280 | 287 | fs |
| | | | $f_{OUT} = 156.25MHz$, Integration Range: 12kHz - 20MHz; NOTE 2 | 265 | 264 | 263 | 270 | fs |
| | | | $f_{OUT} = 622.08MHz$, Integration Range: 12kHz - 20MHz; NOTE 3 | 289 | 266 | 265 | N/A (NOTE 5) | fs |
| | | Q2, Q3 Integer; NOTE 1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 312 | 326 | 304 | 318 | fs |
| | | Q2, Q3 Fractional; NOTE 4 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 269 | 280 | 261 | 263 | fs |
| | | Q4, Q5, Q6, Q7; NOTE 1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 302 | 321 | 295 | 301 | fs |

NOTE: V_{CCOx} denotes V_{CCO0} , V_{CCO1} , V_{CCO2} , V_{CCO3} , V_{CCO4} , V_{CCO5} , V_{CCO6} , V_{CCO7} .

NOTE: Fox part numbers: 277LF-40-18 and 277LF-38.88-2 used for 40MHz and 38.88MHz crystals, respectively.

NOTE: All outputs configured for the specific output type, as shown in the table.

NOTE 1: Characterized with 8T49N287-901.

NOTE 2: Characterized with 8T49N287-902.

NOTE 3: Characterized with 8T49N287-903.

NOTE 4: Characterized with 8T49N287-900.

NOTE 5: This frequency is not supported for LVCMOS operation.

NOTE 6: Qx and nQx are 180° out of phase.

Table 12B. Typical RMS Phase Jitter (Jitter Attenuator Mode), $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CCOx} = 3.3V \pm 5\%$, $2.5V \pm 5\%$ or $1.8V \pm 5\%$ (1.8V only supported for LVCMOS outputs), $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | LVPECL | LVDS | HCSL | LVCMOS NOTE 6 | Units |
|----------------|---------------------------|---|--|--------|------|------|------------------|-------|
| tjit(ϕ) | RMS Phase Jitter (Random) | Q0, Q1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz; NOTE 1 | 285 | 299 | 280 | 275 | fs |
| | | | $f_{OUT} = 156.25MHz$, Integration Range: 12kHz - 20MHz; NOTE 2 | 261 | 252 | 264 | 274 | fs |
| | | | $f_{OUT} = 622.08MHz$, Integration Range: 12kHz - 20MHz; NOTE 3 | 221 | 203 | 202 | N/A (NOTE 5) | fs |
| | | Q2, Q3 Integer; NOTE 1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 312 | 327 | 306 | 306 | fs |
| | | Q2, Q3 Fractional; NOTE 4 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 271 | 282 | 263 | 267 | fs |
| | | Q4, Q5, Q6, Q7; NOTE 1 | $f_{OUT} = 122.88MHz$, Integration Range: 12kHz - 20MHz | 308 | 320 | 295 | 288 | fs |

NOTE: V_{CCOx} denotes V_{CCO0} , V_{CCO1} , V_{CCO2} , V_{CCO3} , V_{CCO4} , V_{CCO5} , V_{CCO6} , V_{CCO7} .

NOTE: Measured using a Rohde & Schwarz SMA100A as the input source.

NOTE: Fox part numbers: 277LF-40-18 and 277LF-38.88-2 used for 40MHz and 38.88MHz crystals, respectively.

NOTE: All outputs configured for the specific output type, as shown in the table.

NOTE 1: Characterized with 8T49N287-905.

NOTE 2: Characterized with 8T49N287-906.

NOTE 3: Characterized with 8T49N287-907.

NOTE 4: Characterized with 8T49N287-904.

NOTE 5: This frequency is not supported for LVCMOS operation.

NOTE 6: Qx and nQx are 180° out of phase.

Table 13. PCI Express Jitter Specifications, $V_{CC} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_{CCOx} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | PCIe Industry Specification | Units |
|---------------------------------------|---|--|---------|---------|---------|-----------------------------|-------|
| t_j (PCIe Gen 1) | Phase Jitter Peak-to-Peak; NOTE 1, 4, 5 | $f = 100MHz$, 40MHz Crystal Input, Evaluation Band: 0Hz - Nyquist (Clock Frequency/2) | | 8 | 16 | 86 | ps |
| $t_{REFCLK_HF_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4, 5 | $f = 100MHz$, 40MHz Crystal Input, High Band: 1.5MHz - Nyquist (Clock Frequency/2) | | 0.8 | 1.8 | 3.1 | ps |
| $t_{REFCLK_LF_RMS}$ (PCIe Gen 2) | Phase Jitter RMS; NOTE 2, 4, 5 | $f = 100MHz$, 40MHz Crystal Input, Low Band: 10kHz - 1.5MHz | | 0.03 | 0.5 | 3.0 | ps |
| t_{REFCLK_RMS} (PCIe Gen 3) | Phase Jitter RMS; NOTE 3, 4, 5 | $f = 100MHz$, 40MHz Crystal Input, Evaluation Band: 0Hz - Nyquist (Clock Frequency/2) | | 0.2 | 0.5 | 0.8 | ps |

NOTE: V_{CCOx} denotes V_{CCO0} , V_{CCO1} , V_{CCO2} , V_{CCO3} , V_{CCO4} , V_{CCO5} , V_{CCO6} , V_{CCO7} .

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK_HF_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK_LF_RMS}$ (Low Band).

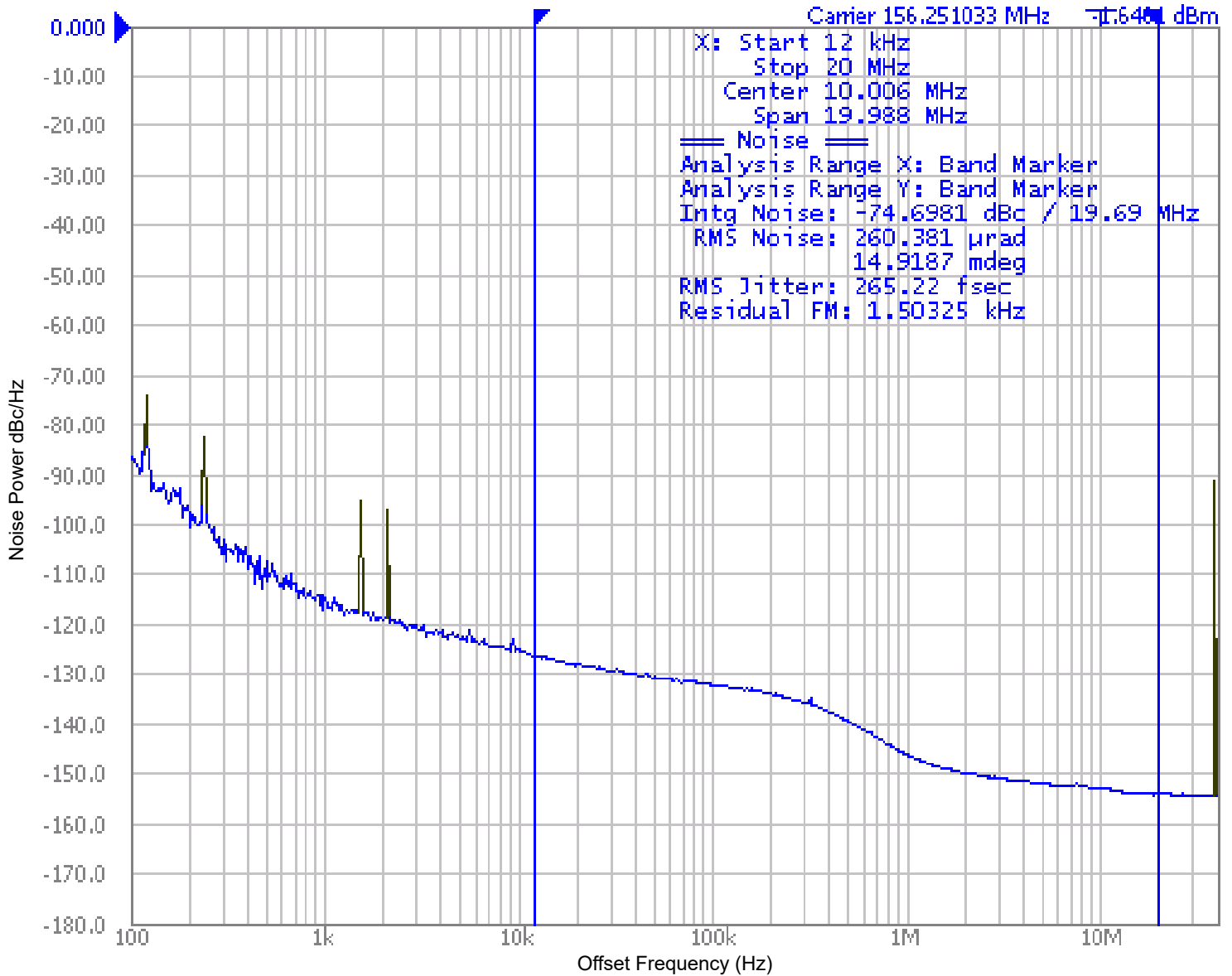
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification Revision 0.7, October 2009 and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

NOTE 5: Outputs configured for HCSL mode. Fox 277LF-40-18 crystal used with doubler logic enabled.

Typical Phase Noise at 156.25MHz

Phase Noise 10.00dB/ Ref 0.000dBc/Hz



Applications Information

Overdriving the Crystal Interface

The OSC1 input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The OSC0 pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise.

Figure 5A shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and changing R_2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 5B shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the OSC1 input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

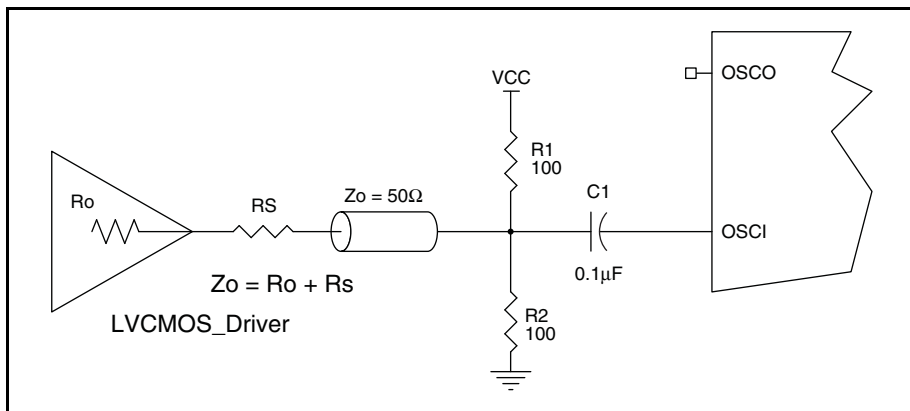


Figure 5A. General Diagram for LVCMOS Driver to XTAL Input Interface

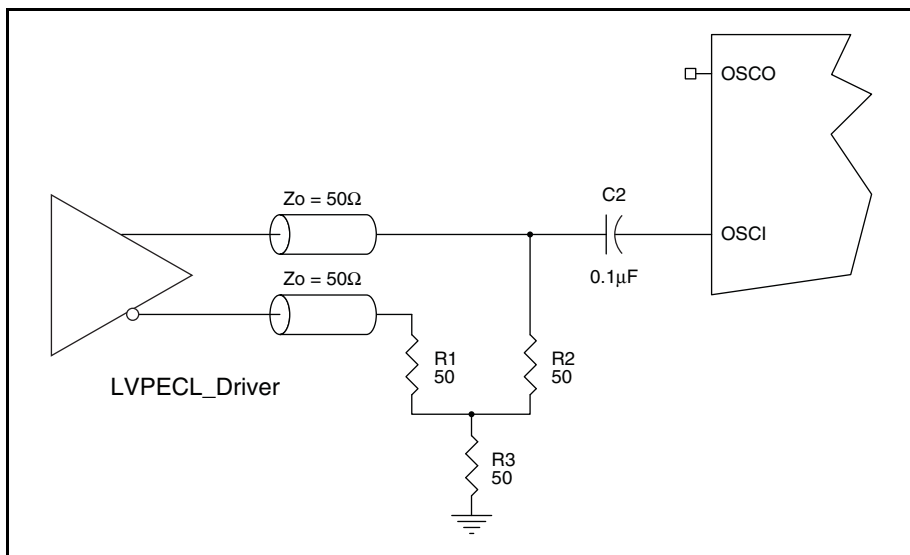


Figure 5B. General Diagram for LVPECL Driver to XTAL Input Interface

Wiring the Differential Input to Accept Single-Ended Levels

Figure 6 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω.

The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than $V_{CC} + 0.3V$. Suggest edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

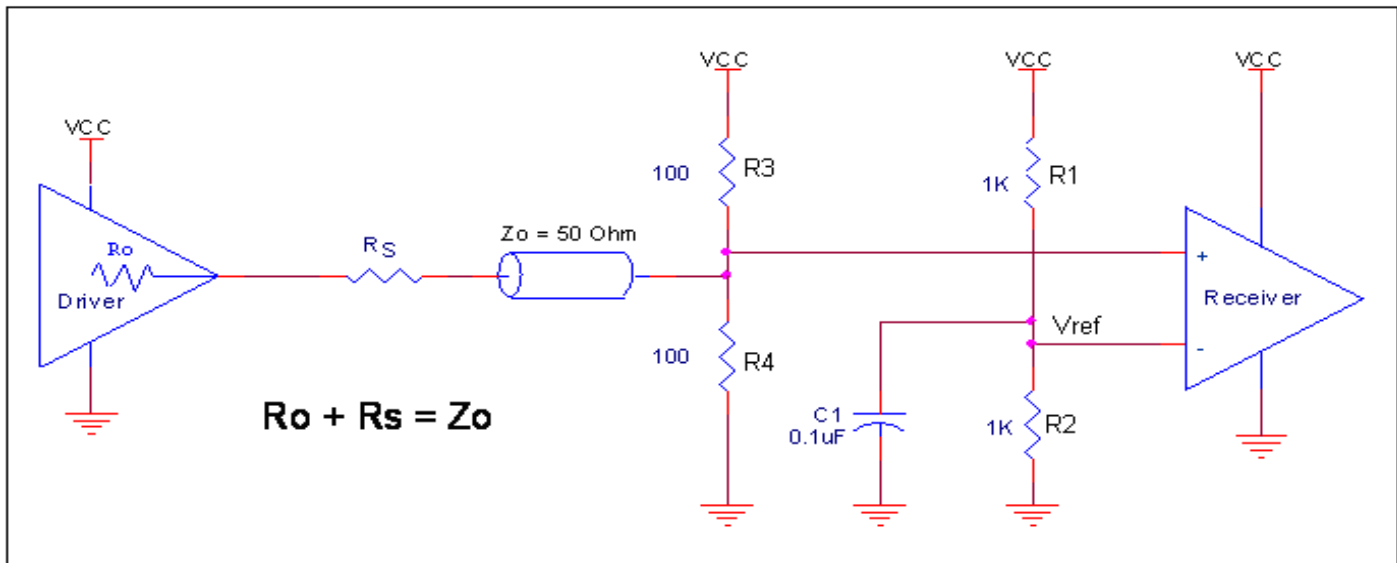


Figure 6. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. [Figure 7A](#) to [Figure 7E](#) show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in [Figure 7A](#), the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

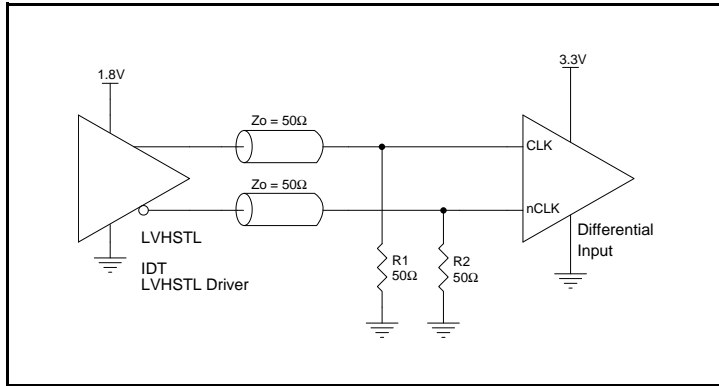


Figure 7A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

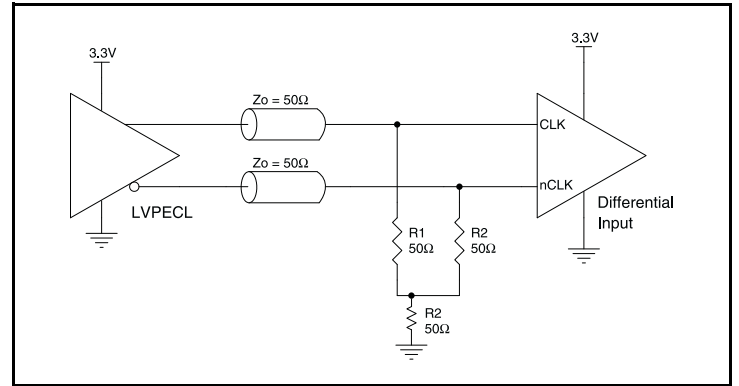


Figure 7D. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

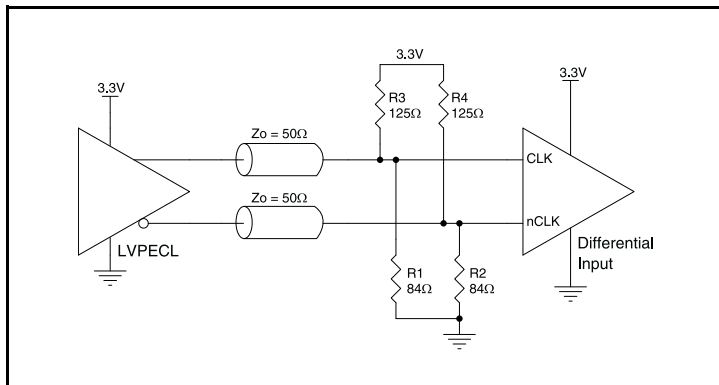


Figure 7B. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

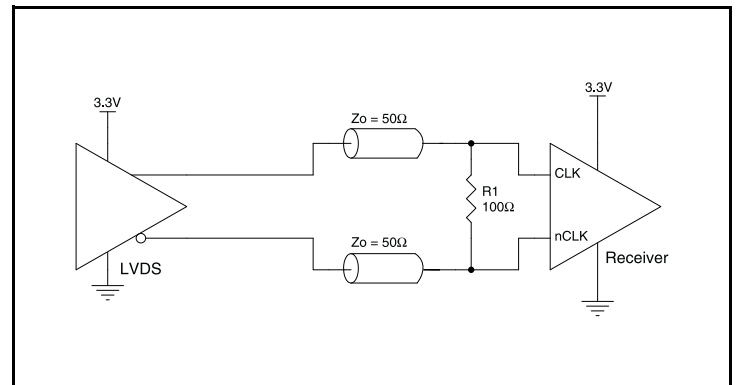


Figure 7E. CLKx/nCLKx Input Driven by a 3.3V LVDS Driver

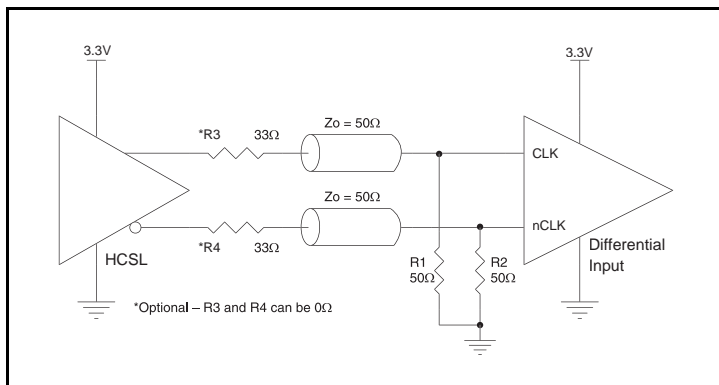


Figure 7C. CLKx/nCLKx Input Driven by a 3.3V HCSL Driver

2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. [Figure 8A](#) to [Figure 8D](#) show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult

with the vendor of the driver component to confirm the driver termination requirements. For example, in [Figure 8A](#), the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

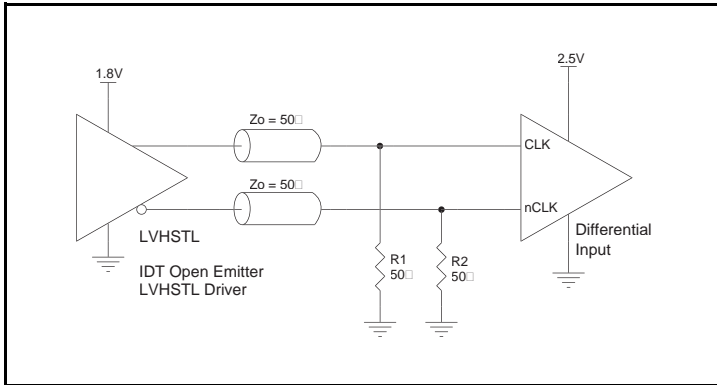


Figure 8A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

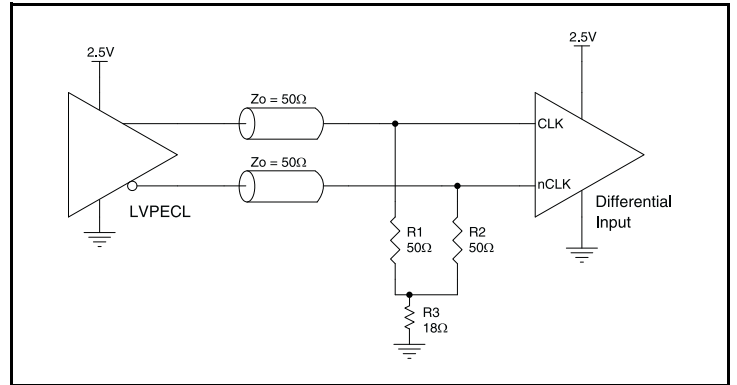


Figure 8C. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

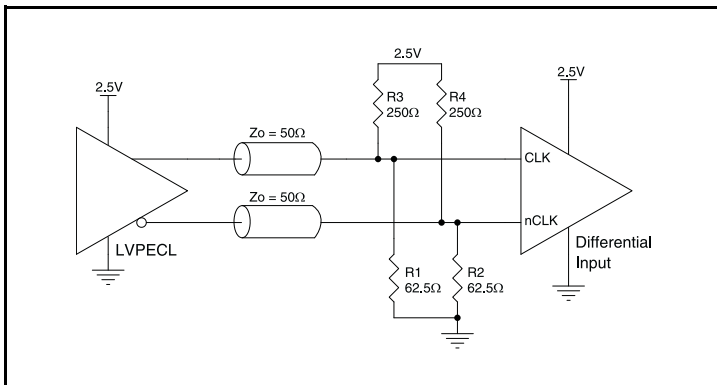


Figure 8B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

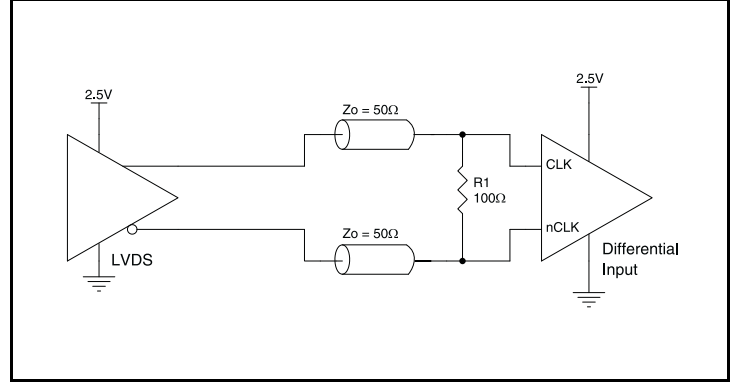


Figure 8D. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Input

For applications not requiring the use one or more reference clock inputs, both CLKx and nCLKx can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground. It is recommended that CLKx, nCLKx not be driven with active signals when not enabled for use.

LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

Any unused LVPECL output pairs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

Any unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating there should be no trace attached.

LVC MOS Outputs

Any LVC MOS output can be left floating if unused. There should be no trace attached.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are

designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. [Figure 9A](#) and [Figure 9B](#) show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

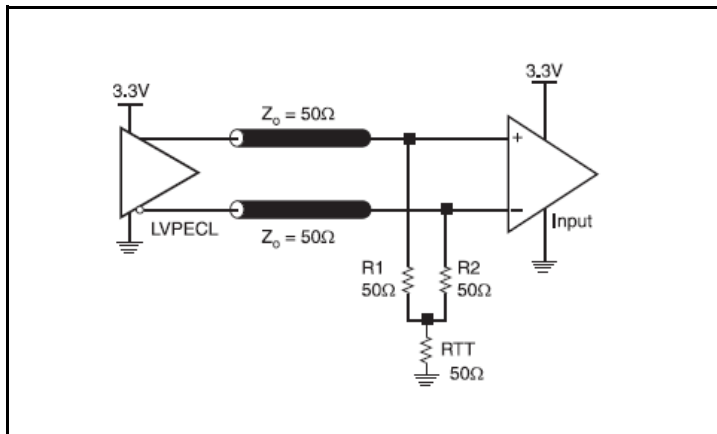


Figure 9A. 3.3V LVPECL Output Termination

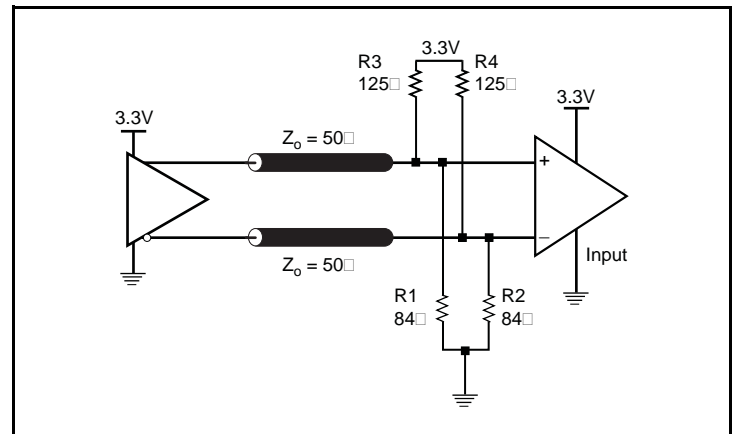


Figure 9B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 10A and Figure 10C show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC0} - 2V$. For $V_{CC0} = 2.5V$, the $V_{CC0} - 2V$ is very close to ground

level. The R3 in Figure 10C can be eliminated and the termination is shown in Figure 10B.

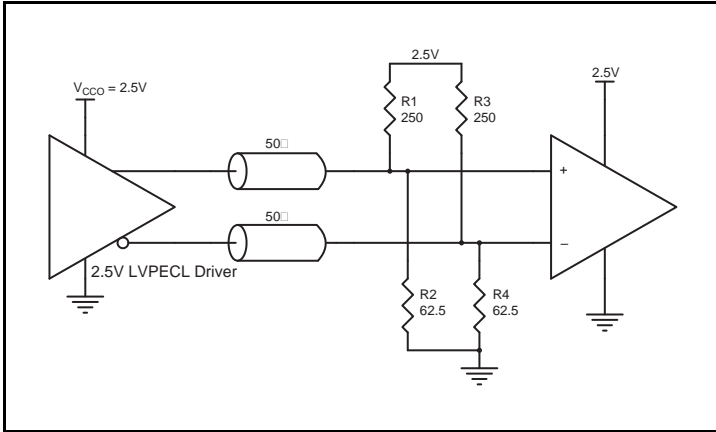


Figure 10A. 2.5V LVPECL Driver Termination Example

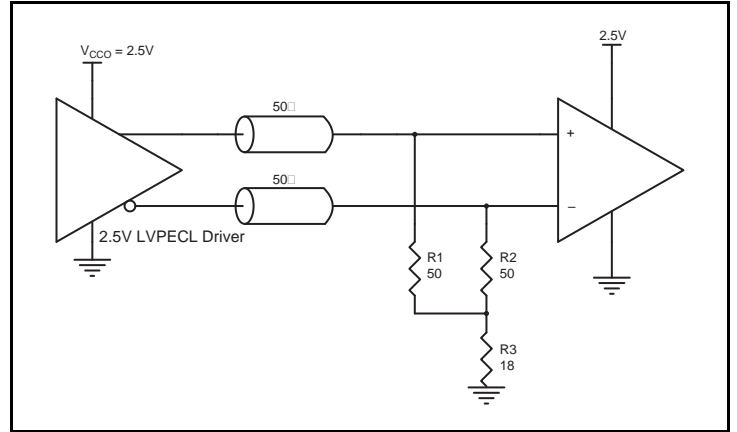


Figure 10C. 2.5V LVPECL Driver Termination Example

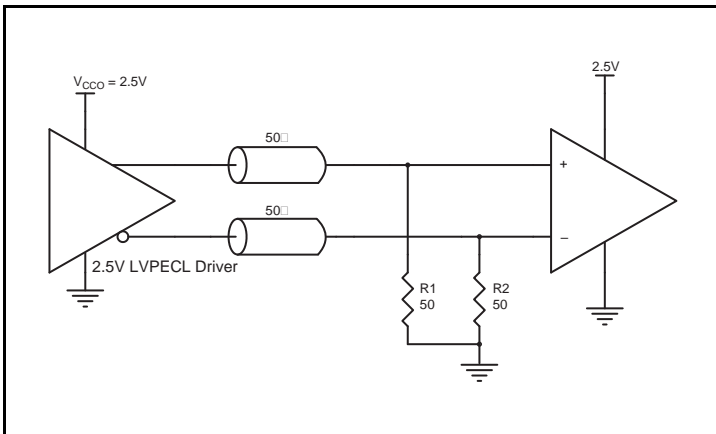


Figure 10B. 2.5V LVPECL Driver Termination Example

2.5V and 3.3V HCSL Recommended Termination

Figure 11A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output

types. All traces should be 50Ω impedance single-ended or 100Ω differential.

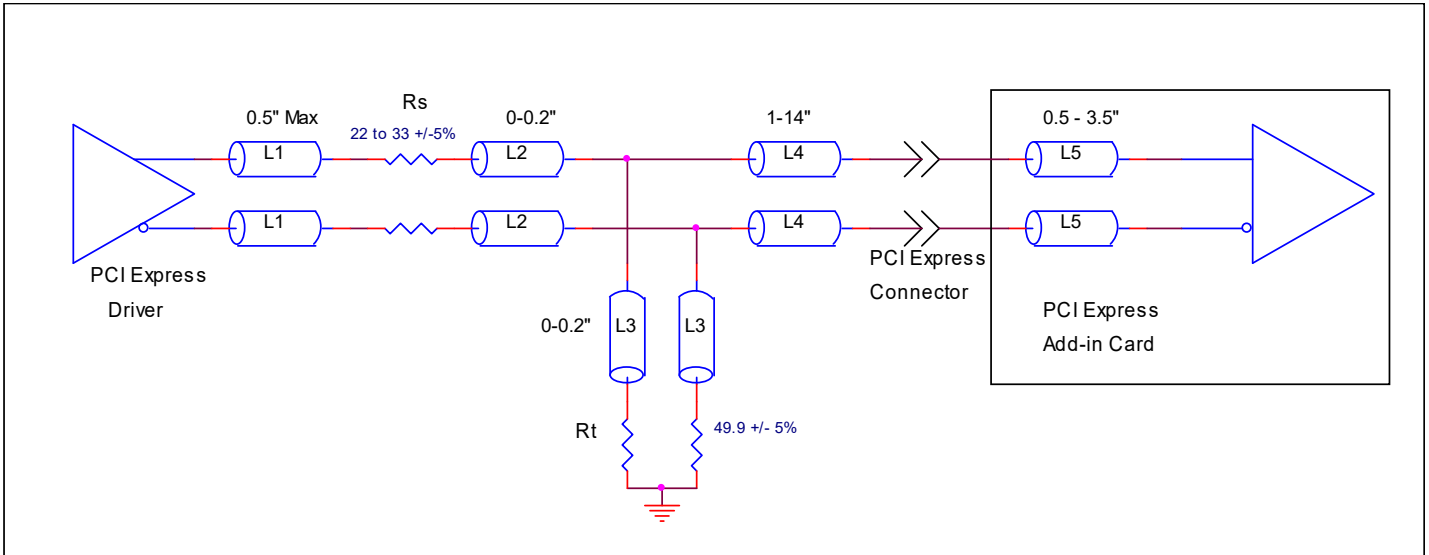


Figure 11A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 11B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

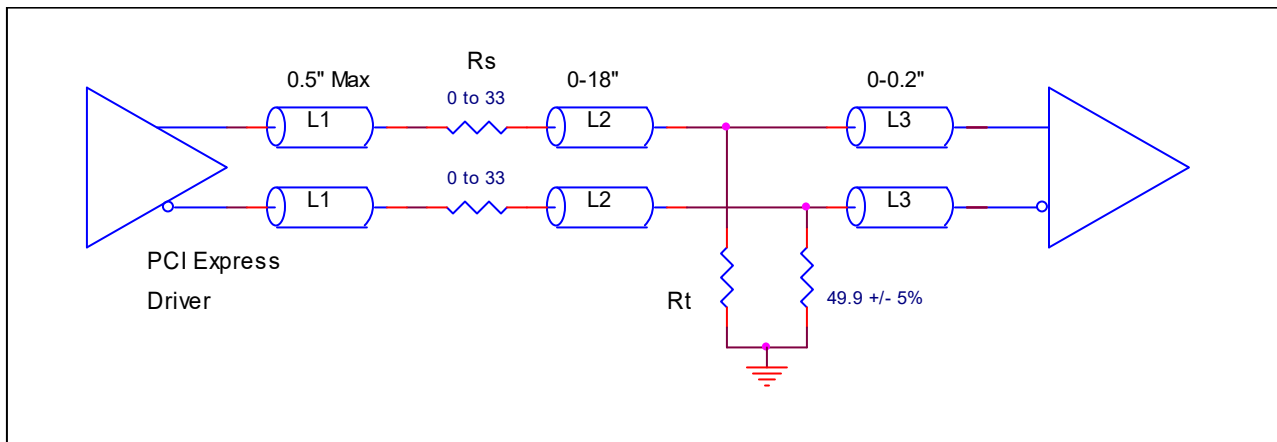


Figure 11B. Recommended Termination (where a point-to-point connection can be used)

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω . The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in [Figure 12A](#) can be used

with either type of output structure. [Figure 12B](#), which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

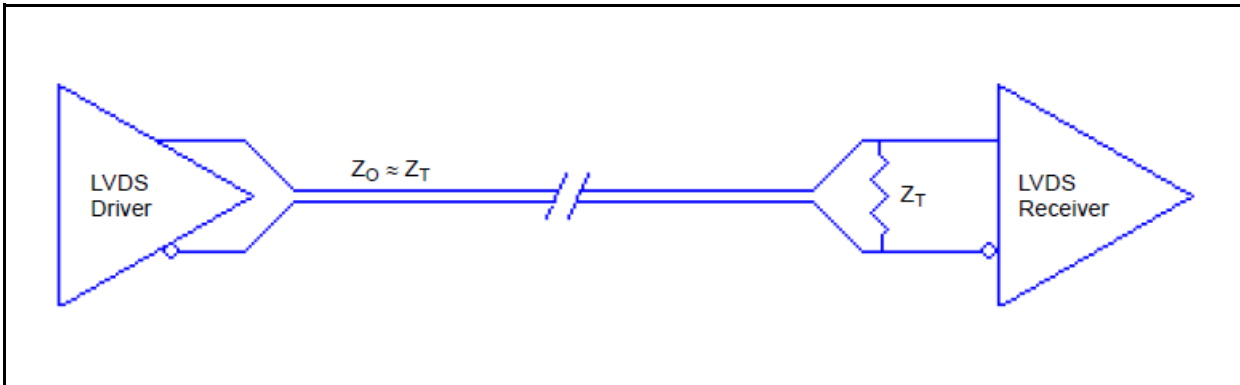


Figure 12A. Standard LVDS Termination

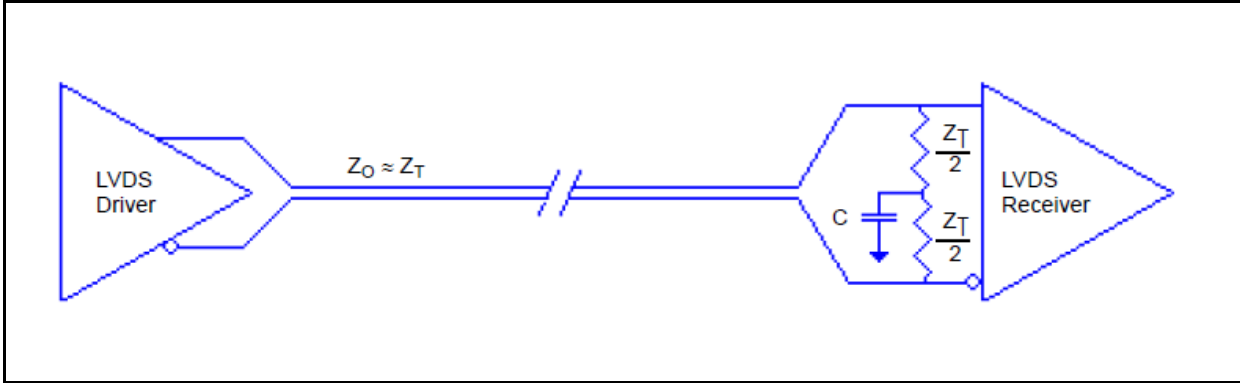


Figure 12B. Optional LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 13*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead frame Base Package, Amkor Technology.

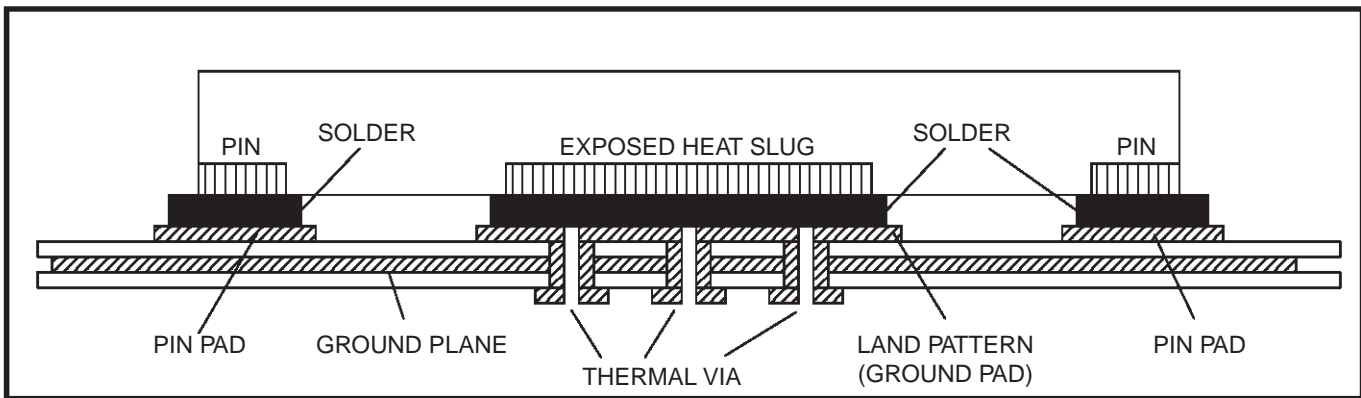


Figure 13. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic and Layout Information

Schematics for 8T49N287 can be found on IDT.com. Please search for the 8T49N287 device and click on the link for evaluation board schematics.

Crystal Recommendation

This device was validated using FOX 277LF series through-hole crystals including part #277LF-40-18 (40MHz) and #277LF-38.88-2 (38.88MHz). If a surface mount crystal is desired, we recommend FOX Part #603-40-48 (40MHz) or #603-38.88-7 (38.88MHz).

I²C Serial EEPROM Recommendation

The 8T49N287 was designed to operate with most standard I²C serial EEPROMs of 256 bytes or larger. Atmel AT24C04C was used during device characterization and is recommended for use. Please contact IDT for review of any other I²C EEPROM's compatibility with the 8T49N287.

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

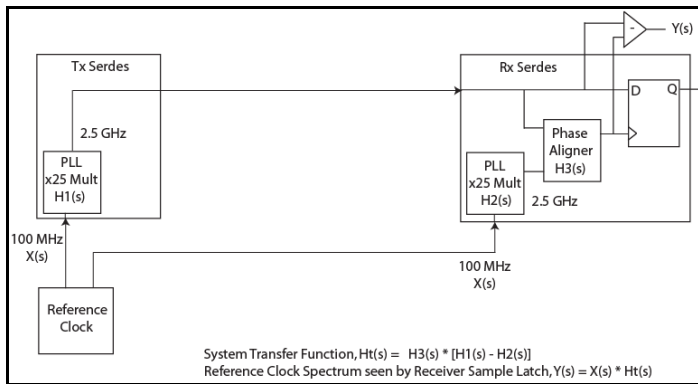
In the jitter analysis, the transmit (Tx) and receive (Rx) SerDes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum $X(s)$ and is:

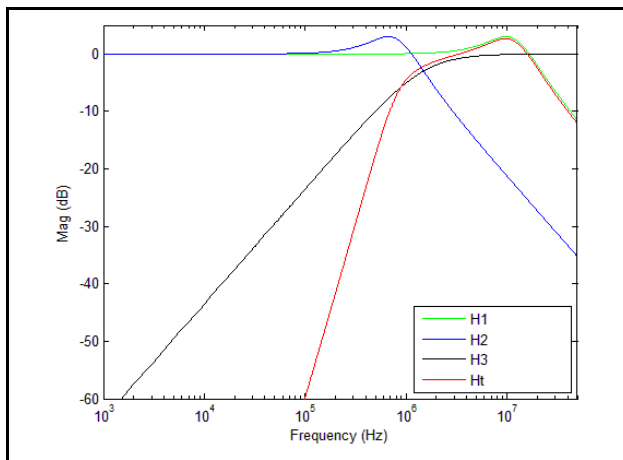
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on $X(s) \cdot H_3(s) \cdot [H_1(s) - H_2(s)]$.



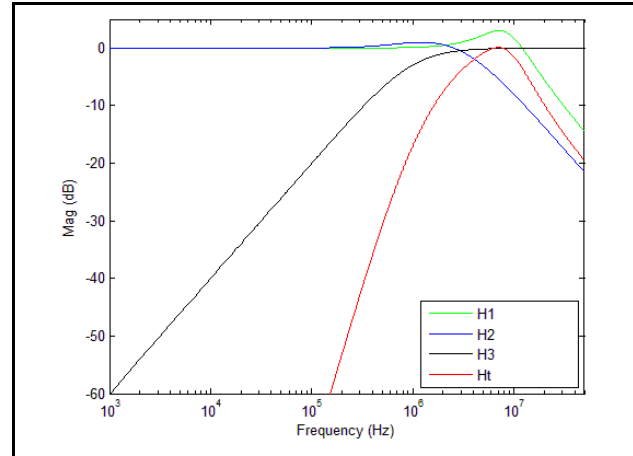
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g., for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

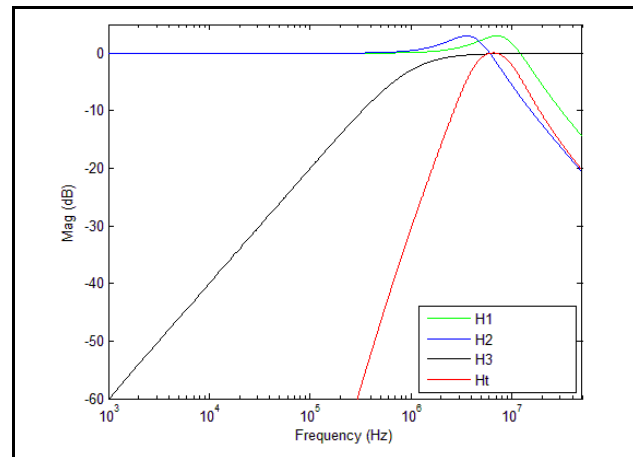


PCI Express Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function H_t .

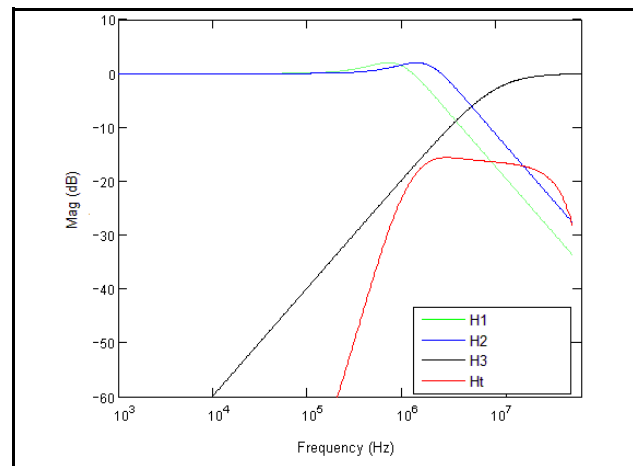


PCI Express Gen 2A Magnitude of Transfer Function



PCI Express Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCI Express Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

Power Dissipation and Thermal Considerations

The 8T49N287 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

The 8T49N287 device was designed and characterized to operate within the ambient industrial temperature range of -40°C to $+85^{\circ}\text{C}$. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact IDT technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8T49N287 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). [Figure 14](#) below indicates the individual domains and the associated power pins.

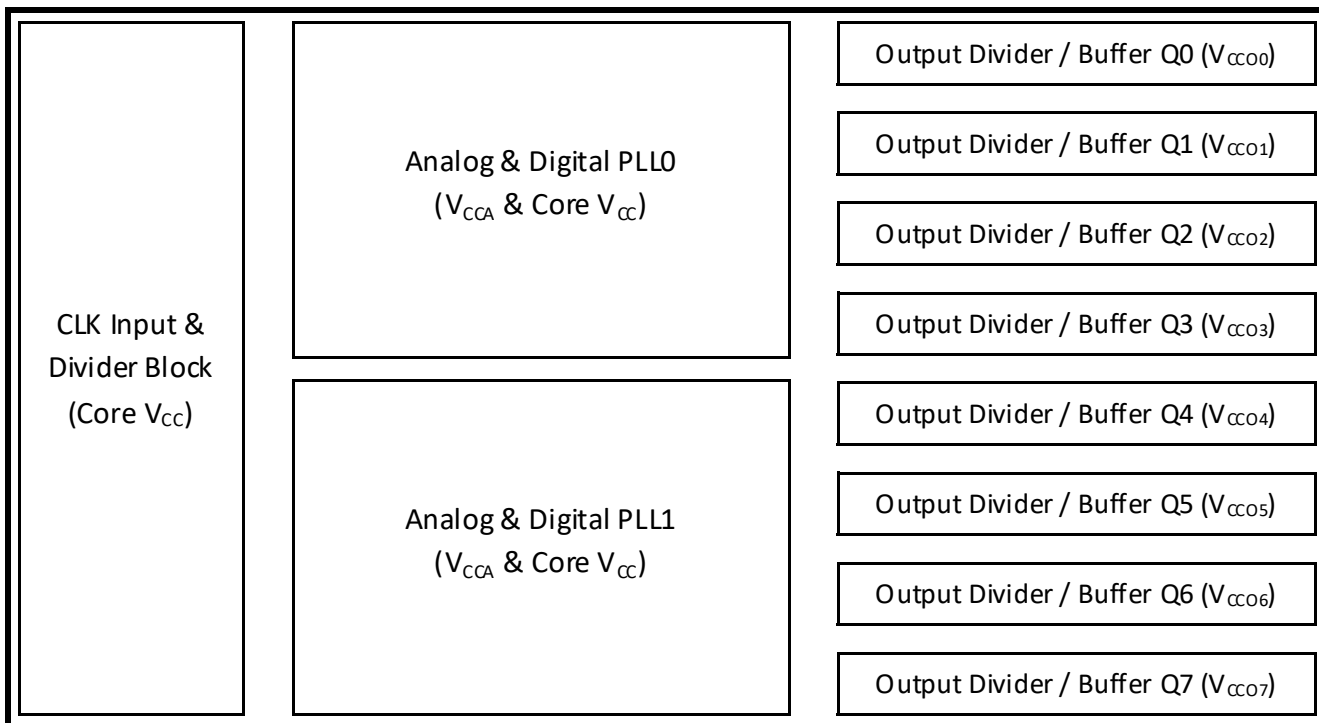


Figure 14. 8T49N287 Power Domains

For the output paths shown above, there are three different structures that are used. Q0 and Q1 use one output path structure, Q2 and Q3 use a second structure and Q[4:7] use a 3rd structure. Power consumption data will vary slightly depending on the structure used as shown in the appropriate tables below.

Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core and analog voltage supplies from [Table 7A](#) and [Table 7B](#).
2. Determine the nominal power consumption of each enabled output path.
 - a. This consists of a base amount of power that is independent of operating frequency, as shown in [Table 15A](#) through [Table 15I](#) (depending on the chosen output protocol).
 - b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in [Table 15A](#) through [Table 15I](#).
3. All of the above totals are then summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heatsink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in [Table 14](#) below. Please contact IDT for assistance in calculating results under other scenarios.

Table 14. Thermal Resistance θ_{JA} for 56-Lead VFQFN, Forced Convection

| θ_{JA} by Velocity | | | |
|---|----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 16.0°C/W | 12.14°C/W | 11.02°C/W |

Current Consumption Data and Equations

Table 15A. 3.3V LVPECL Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00593 | 40.1 |
| Q1 | | |
| Q2 | 0.01363 | 63.8 |
| Q3 | | |
| Q4 | 0.00591 | 42.9 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15D. 2.5V LVPECL Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00373 | 32.8 |
| Q1 | | |
| Q2 | 0.01134 | 56.5 |
| Q3 | | |
| Q4 | 0.00369 | 35.7 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15B. 3.3V HCSL Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00582 | 40.1 |
| Q1 | | |
| Q2 | 0.01358 | 63.8 |
| Q3 | | |
| Q4 | 0.00553 | 43.1 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15E. 2.5V HCSL Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00354 | 32.9 |
| Q1 | | |
| Q2 | 0.01125 | 56.5 |
| Q3 | | |
| Q4 | 0.00353 | 35.7 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15C. 3.3V LVDS Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00627 | 48.6 |
| Q1 | | |
| Q2 | 0.01404 | 72.5 |
| Q3 | | |
| Q4 | 0.00630 | 51.3 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15F. 2.5V LVDS Output Calculation Table

| Output | FQ_Factor (mA/MHz) | Base Current (mA) |
|--------|--------------------|-------------------|
| Q0 | 0.00366 | 40.8 |
| Q1 | | |
| Q2 | 0.01148 | 64.5 |
| Q3 | | |
| Q4 | 0.00367 | 43.7 |
| Q5 | | |
| Q6 | | |
| Q7 | | |

Table 15G. 3.3V LVCMOS Output Calculation Table

| Output | Base Current (mA) |
|--------|-------------------|
| Q0 | 37.4 |
| Q1 | |
| Q2 | 61.6 |
| Q3 | |
| Q4 | 40.6 |
| Q5 | |
| Q6 | |
| Q7 | |

Table 15I. 1.8V LVCMOS Output Calculation Table

| Output | Base Current (mA) |
|--------|-------------------|
| Q0 | 27.4 |
| Q1 | |
| Q2 | 51.4 |
| Q3 | |
| Q4 | 30.3 |
| Q5 | |
| Q6 | |
| Q7 | |

Table 15H. 2.5V LVCMOS Output Calculation Table

| Output | Base Current (mA) |
|--------|-------------------|
| Q0 | 30.8 |
| Q1 | |
| Q2 | 54.8 |
| Q3 | |
| Q4 | 33.7 |
| Q5 | |
| Q6 | |
| Q7 | |

Applying the values to the following equation will yield output current by frequency:

$$Q_x \text{ Current (mA)} = FQ_Factor * \text{Frequency (MHz)} + \text{Base Current}$$

where:

Q_x Current is the specific output current according to output type and frequency

FQ_Factor is used for calculating current increase due to output frequency

Base Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$$T_J = T_A + (\theta_{JA} * Pd_{total})$$

where:

T_J is the junction temperature (°C)

T_A is the ambient temperature (°C)

θ_{JA} is the thermal resistance value from [Table 14](#), dependent on ambient airflow (°C/W)

Pd_{total} is the total power dissipation of the 8T49N287 under usage conditions, including power dissipated due to loading (W)

Note that the power dissipation per output pair due to loading is assumed to be 27.95mW for LVPECL outputs and 44.5mW for HCSL outputs. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using *C_{PD}* (found in [Table 2](#)) and output frequency:

$$Pd_{OUT} = C_{PD} * F_{OUT} * V_{CCO}^2$$

where:

Pd_{out} is the power dissipation of the output (W)

C_{pd} is the power dissipation capacitance (pF)

F_{out} is the output frequency of the selected output (MHz)

V_{CCO} is the voltage supplied to the appropriate output (V)

Example Calculations

Example 1. Common Customer Configuration (3.3V Core Voltage)

| Output | Output Type | Frequency (MHz) | V _{CCO} |
|--------|-------------|-----------------|------------------|
| Q0 | LVPECL | 245.76 | 3.3 |
| Q1 | LVPECL | 245.76 | 3.3 |
| Q2 | LVPECL | 33.333 | 3.3 |
| Q3 | LVPECL | 33.333 | 3.3 |
| Q4 | LVDS | 125 | 3.3 |
| Q5 | LVDS | 125 | 3.3 |
| Q6 | LVC MOS | 25 | 3.3 |
| Q7 | LVC MOS | 25 | 3.3 |
| PLL0 | Enabled | | |
| PLL1 | Enabled | | |

- Core Supply Current, I_{CC} = **100mA (max)**
- Analog Supply Current, I_{CCA} = **265mA (max)**
 - Q0 Current = $0.00593 \times 245.76 + 40.1 = 41.56\text{mA}$
 - Q1 Current = $0.00593 \times 245.76 + 40.1 = 41.56\text{mA}$
 - Q2 Current = $0.01363 \times 33.333 + 63.8 = 64.25\text{mA}$
 - Q3 Current = $0.01363 \times 33.333 + 63.8 = 64.25\text{mA}$
 - Q4 Current = $0.00630 \times 125 + 51.3 = 52.09\text{mA}$
 - Q5 Current = $0.00630 \times 125 + 51.3 = 52.09\text{mA}$
 - Q6 Current = 40.6mA
 - Q7 Current = 40.6mA
- Total Output Current = **397mA (max)**
 - Total Device Current = 100mA + 265mA + 397mA = **762mA**
 - Total Device Power = $3.465\text{V} \times 762\text{mA} = \mathbf{2640.3\text{mW}}$
- Power dissipated through output loading:
 - LVPECL = $27.95\text{mW} \times 4 = \mathbf{111.8\text{mW}}$
 - LVDS = already accounted for in device power
 - HCSL = n/a
 - LVC MOS = $14.5\text{pF} \times 25\text{MHz} \times 3.465\text{V}^2 \times 2 \text{ output pairs} = \mathbf{8.7\text{mW}}$
- Total Power = $2640.3\text{mW} + 111.8\text{mW} + 8.7\text{mW} = \mathbf{2760.8\text{mW or } 2.8\text{W}}$

With an ambient temperature of 85°C and no airflow, the junction temperature is:

$$T_J = 85^\circ\text{C} + 16.1^\circ\text{C/W} \times 2.8\text{W} = \mathbf{130.1^\circ\text{C}}$$

This junction temperature is above the maximum allowable. In instances where maximum junction temperature is exceeded adjustments need to be made to either airflow or ambient temperature. In this case, adjusting airflow to 1m/s ($\theta_{JA} = 12.4^\circ\text{C/W}$) will reduce junction temperature to 119.7C. If no airflow adjustments can be made, the maximum ambient operating temperature must be reduced by a minimum of 5.1°C.

Example 2. High-Frequency Customer Configuration (3.3V Core Voltage)

| Output | Output Type | Frequency (MHz) | V _{CCO} |
|--------|-------------|-----------------|------------------|
| Q0 | LVDS | 625.00 | 2.5 |
| Q1 | LVDS | 625.00 | 2.5 |
| Q2 | LVPECL | 161.133 | 2.5 |
| Q3 | LVPECL | 161.133 | 2.5 |
| Q4 | HCSL | 25 | 3.3 |
| Q5 | HCSL | 25 | 3.3 |
| Q6 | HCSL | 125 | 3.3 |
| Q7 | HCSL | 156.25 | 3.3 |
| PLL0 | Enabled | | |
| PLL1 | Disabled | | |

- Core Supply Current, I_{CC} = **100mA (max)**
- Analog Supply Current, I_{CCA} = **187mA (max, PLL0 path only)**
 - Q0 Current = 0.00366x625 + 40.8 = 43.09mA
 - Q1 Current = 0.00366x625 + 40.8 = 43.09mA
 - Q2 Current = 0.01134x161.133 + 56.5 = 58.3mA
 - Q3 Current = 0.01134x161.133 + 56.5 = 58.3mA
 - Q4 Current = 0.00553x25 + 43.1 = 43.24mA
 - Q5 Current = 0.00553x25 + 43.1 = 43.24mA
 - Q6 Current = 0.00553x125 + 43.1 = 43.79mA
 - Q7 Current = 0.00553x156.25 + 43.1 = 43.96mA
- Total Output Current = **202.8mA** (V_{CCO} = 2.5V), **174.23mA** (V_{CCO} = 3.3V)
 Total Device Power = 3.465V *(100mA + 187mA + 174.23mA) + 2.625V * 202.8mA = **2130.5mW**
- Power dissipated through output loading:
 - LVPECL = 27.95mW * 2 = **55.9mW**
 - LVDS = already accounted for in device power
 - HCSL = 44.5mW * 4 = 178mW
 - LVC MOS = n/a
 Total Power = 2130.5mW + 55.9mW + 178mW = **2364.4mW or 2.36W**

With an ambient temperature of 85°C, the junction temperature is:

$$T_J = 85^\circ\text{C} + 16.1^\circ\text{C/W} * 2.36\text{W} = \mathbf{123^\circ\text{C}}$$

This junction temperature is below the maximum allowable.

Example 3. Low Power Customer Configuration (2.5V Core Voltage)

| Output | Output Type | Frequency (MHz) | V _{CCO} |
|--------|-------------|-----------------|------------------|
| Q0 | LVDS | 156.25 | 2.5 |
| Q1 | LVDS | 156.25 | 2.5 |
| Q2 | LVDS | 161.133 | 2.5 |
| Q3 | LVC MOS | 33.333 | 1.8 |
| Q4 | LVC MOS | 25 | 1.8 |
| Q5 | LVC MOS | 25 | 1.8 |
| Q6 | LVC MOS | 25 | 1.8 |
| Q7 | LVDS | 156.25 | 2.5 |
| PLL0 | Enabled | | |
| PLL1 | Enabled | | |

- Core Supply Current, I_{CC} = **95mA (max)**
- Analog Supply Current, I_{CCA} = **260mA (max)**
 Q0 Current = $0.00366 \times 156.25 + 40.8 = 41.37\text{mA}$
 Q1 Current = $0.00366 \times 156.25 + 40.8 = 41.37\text{mA}$
 Q2 Current = $0.01148 \times 161.133 + 64.5 = 66.35\text{mA}$
 Q3 Current = 51.4mA
 Q4 Current = 30.3mA
 Q5 Current = 30.3mA
 Q6 Current = 30.3mA
 Q7 Current = $0.00367 \times 156.25 + 43.7 = 44.27\text{mA}$
- Total Output Current = **193.36mA** (V_{CCO} = 2.5V), **142.3mA** (V_{CCO} = 1.8V)
 Total Device Power = $2.625\text{V} \times (95\text{mA} + 260\text{mA} + 193.36\text{mA}) + 1.89\text{V} \times 142.3\text{mA} = \mathbf{1708.4\text{mW}}$
- Power dissipated through output loading:
 LVPECL = n/a
 LVDS = already accounted for in device power
 HCSL = n/a
 LVC MOS_33.3MHz = $17\text{pF} \times 33.3\text{MHz} \times 1.89\text{V}^2 \times 1 \text{ output pair} = \mathbf{2.02\text{mW}}$
 LVC MOS_25MHz = $12.5\text{pF} \times 25\text{MHz} \times 1.89\text{V}^2 \times 3 \text{ output pairs} = \mathbf{3.35\text{mW}}$
 Total Power = $1708.4\text{mW} + 2.02\text{mW} + 3.35\text{mW} = \mathbf{1714\text{mW or } 1.7\text{W}}$

With an ambient temperature of 85°C, the junction temperature is:

$$T_j = 85^\circ\text{C} + 16.1^\circ\text{C/W} \times 1.7\text{W} = \mathbf{112.4^\circ\text{C}}$$

This junction temperature is below the maximum allowable.

Reliability Information

Table 16. θ_{JA} vs. Air Flow Table for a 56-Lead VFQFN

| θ_{JA} vs. Air Flow | | | |
|---|----------|-----------|-----------|
| Meters per Second | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 16.0°C/W | 12.14°C/W | 11.02°C/W |

NOTE: Theta JA (θ_{JA}) values calculated using a 4-layer JEDEC PCB (114.3mm x 101.6mm), with 2oz. (70 μ m) copper plating on all 4 layers.

Transistor Count

The transistor count for 8T49N287 is: 998,958

Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

Marking Diagram



1. Line 1 and Line 2 is the part number.
2. "ddd" denotes a configuration-specific number (dash code).
3. "#" denotes stepping.
4. "YYWW" denotes: "YY" is the last two digits of the year, and "WW" is the work week number that the part was assembled.
5. "\$" denotes the mark code.

Ordering Information

Table 17. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|--------------------|----------------------|--------------------------|---|----------------|
| 8T49N287A-dddNLGI | IDT8T49N287A-dddNLGI | 56-Lead VFQFN, Lead-Free | Tray | -40°C to +85°C |
| 8T49N287A-dddNLGI8 | IDT8T49N287A-dddNLGI | 56-Lead VFQFN, Lead-Free | Tape & Reel, Pin 1 Orientation: EIA-481-C | -40°C to +85°C |
| 8T49N287A-dddNLGI# | IDT8T49N287A-dddNLGI | 56-Lead VFQFN, Lead-Free | Tape & Reel, Pin 1 Orientation: EIA-481-D | -40°C to +85°C |

NOTE: For the specific, publicly available -ddd order codes, refer to *FemtoClock NG Universal Frequency Translator Ordering Product Information* document. For custom -ddd order codes, please contact IDT for more information.

Table 18. Pin 1 Orientation in Tape and Reel Packaging

| Part Number Suffix | Pin 1 Orientation | Illustration |
|--------------------|------------------------|--------------|
| NLGI8 | Quadrant 1 (EIA-481-C) | |
| NLGI# | Quadrant 2 (EIA-481-D) | |

Revision History

| Revision Date | Description of Change |
|--------------------|--|
| January 31, 2018 | Updated I2C Mode Operation to indicate support for v2.1 of the I2C specification |
| October 30, 2017 | Added a Marking Diagram |
| September 11, 2017 | <ul style="list-style-type: none"> Added a note before Digital PLL0 Status Register Bit Field Locations and Descriptions and Digital PLL1 Status Register Bit Field Locations and Descriptions Added the following fields to Digital PLL0 Status Register Bit Field Locations and Descriptions and Digital PLL1 Status Register Bit Field Locations and Descriptions: NO_REF, SM_STS, and PLLLCK |
| October 27, 2016 | Crystal Recommendation - deleted IDT crystal reference. |
| February 1, 2016 | <p>T17, Per PCN# W1512-01, Effective Date 03/18/2016 - changed Part/Order Number from 8T49N287-dddNLGI to 8T49N287A-dddNLGI, and Marking from IDT8T49N287-dddNLGI to IDT8T49N287A-dddNLGI.</p> <p>Updated Datasheet header/footer.</p> |
| July 9, 2015 | Device Start-up and Reset Behavior - added second paragraph. |
| June 1, 2015 | <p>AC Characteristics Table - added f_{OUT} minimum parameters.</p> <p>Termination for 3.3V LVPECL Outputs updated Figure 9A.</p> <p>Updated Crystal Recommendation.</p> |
| March 20, 2015 | <p>Table 11A, AC Characteristics Table - updated LVDS Rise/Fall Time maximum spec. from 500 to 400ps.</p> <p>Miscellaneous content enhancement in: Output Phase Control on Switchover section; Table 6A, Table 6C, Table 6E and Table 6G, and Pin Assignment format.</p> |
| November 6, 2014 | <p>Description - first paragraph/last sentence, added HCSSL.</p> <p>Features - added HCSSL in "Accepts up to two LVPECL..." bullet and "Generates 8 LVPECL..." bullet.</p> |



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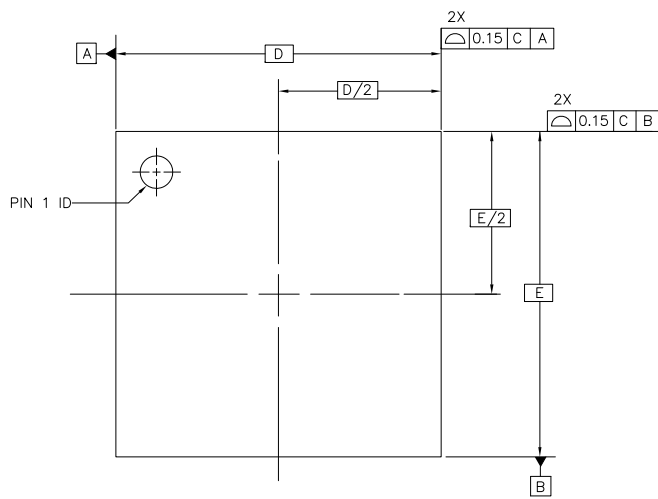
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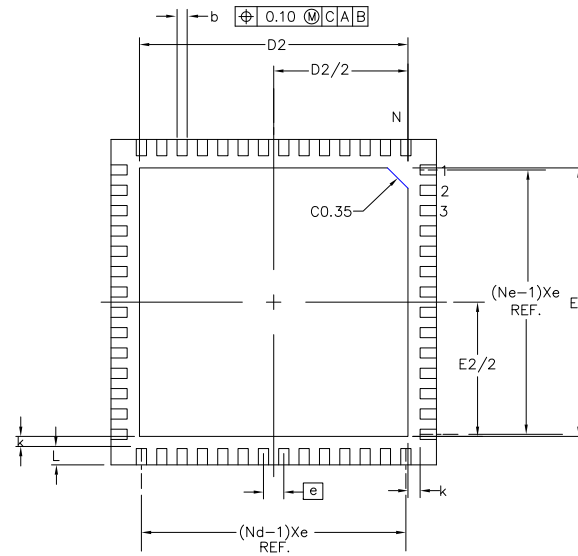
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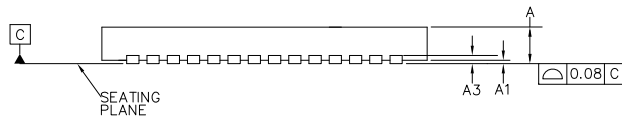
| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/23/16 | JH |



TOP VIEW



BOTTOM VIEW



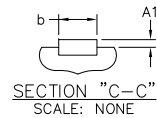
SIDE VIEW

| SYMBOL | DIMENSION | | |
|--------------------------|-----------|------|------|
| | MIN. | NOM. | MAX. |
| $\text{\textcircled{e}}$ | 0.50 BSC | | |
| N | 56 | | |
| Nd | 14 | | |
| Ne | 14 | | |
| L | 0.30 | 0.40 | 0.50 |
| b | 0.18 | 0.25 | 0.30 |
| D2 | 6.45 | 6.60 | 6.75 |
| E2 | 6.45 | 6.60 | 6.75 |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.20 REF. | | |
| D | 8.00 BSC | | |
| E | 8.00 BSC | | |
| θ | - | - | 12° |
| k | - | 0.30 | - |



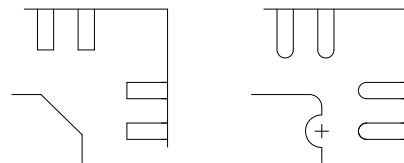
FOR ODD TERMINAL/SIDE

FOR EVEN TERMINAL/SIDE




NOTES:

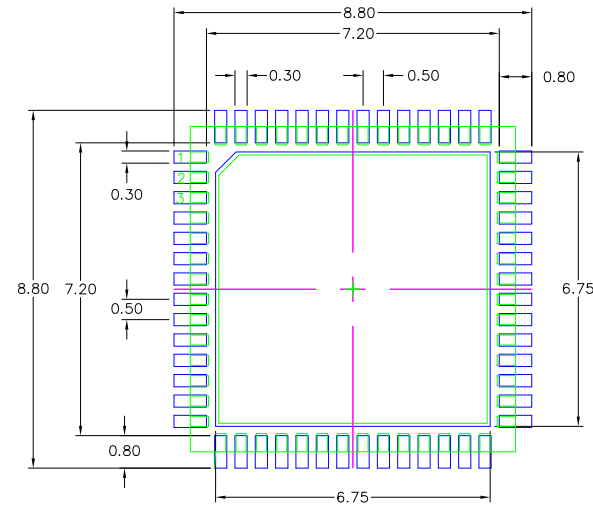
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1994.
2. ALL DIMENSIONS ARE IN mm.



PIN #1 ID AND TIE BAR MARK OPTION

| | | | | |
|-----------------------------|----------|---|---|--------------|
| TOLERANCES UNLESS SPECIFIED | |  www.IDT.com | 6024 SILVERCREEK VALLEY ROAD SAN JOSE CA. 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 | |
| DECIMAL | ANGULAR | | | |
| XX± | ± | | | |
| XXX± | | | | |
| XXXX± | | | | |
| APPROVALS | DATE | TITLE/NLG 56 PACKAGE OUTLINE | | |
| DRAWN <i>PJC/P</i> | 12/07/01 | 8.0 X 8.0 mm BODY, EPAD 6.60mm SQ | | |
| CHECKED | | 0.50 mm PITCH VFQFP-N | | |
| | | SIZE | DRAWING No. | REV |
| | | C | PSC-4110-02 | 00 |
| DO NOT SCALE DRAWING | | | | SHEET 1 OF 2 |


| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/23/16 | JH |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | | |
|--------------------------------|----------|--|---|--------------|
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| APPROVALS | DATE | TITLE NLG 56 PACKAGE OUTLINE | | |
| DRAWN <i>PJP</i> | 12/07/01 | 8.0 X 8.0 mm BODY, EPAD 6.60mm SQ 0.50 mm PITCH VQFP-N | | |
| CHECKED | | SIZE | DRAWING No. | REV |
| | | C | PSC-4110-02 | 00 |
| DO NOT SCALE DRAWING | | | | SHEET 2 OF 2 |



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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