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November 2013

FCP13N60N / FCPF13N60NT N-Channel SupreMOS[®] MOSFET 600 V, 13 A, 258 m Ω

Features

- $R_{DS(on)}$ = 220 $m\Omega$ (Typ.) @ V_{GS} = 10 V, I_D = 6.5 A
- Ultra Low Gate Charge (Typ. Q_q = 30.4 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 145 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

Application

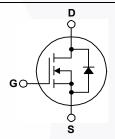
- LCD/LED/PDP TV
- · Lighting
- · Solar Inverter
- · AC-DC Power Supply

Description

The SupreMOS® MOSFET is Fairchild Semiconductor's next generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest Rsp on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.







MOSFET Maximum Ratings $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol		Parameter		FCP13N60N	FCPF13N60NT	Unit	
V_{DSS}	Drain to Source Voltage			6	V		
V_{GSS}	Gate to Source Voltage			±	30	V	
	Drain Current	- Continuous (T _C = 25°C)		13	13*	۸	
ID	- Continuous (T _C = 100°C)			8.2	8.2*	A	
I _{DM}	Drain Current - Pulsed (Note 1)		39	39	Α		
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		2	35	mJ		
I _{AR}	Avalanche Current (Note 1)		(Note 1)	4	Α		
E _{AR}	Repetitive Avalanche Energy (Note 1)		1.16		mJ		
dv/dt	MOSFET dv/dt			1	00	V/ns	
uv/ut	Peak Diode Recovery	lv/dt	(Note 3)	3) 20		V/ns	
D	$(T_C = 25^{\circ}C)$		116	33.8	W		
P_{D}	Power Dissipation - Derate Above 25°C		0.93	0.27	W/°C		
T _J , T _{STG}	Operating and Storage Temperature Range			-55 to	+150	°C	
TL	Maximum Lead Tempe	rature for Soldering, 1/8" from Case for	or 5 Seconds	3	00	°C	

^{*}Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	FCP13N60N	FCPF13N60NT	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.07	3.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	· C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP13N60N	FCP13N60N	TO-220	Tube	N/A	N/A	50 units
FCPF13N60NT	FCPF13N60NT	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions		Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}, T_C = 25^{\circ}\text{C}$	600	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.73	-	V/°C
	Zoro Cata Valtago Drain Current	V _{DS} = 480 V, V _{GS} = 0 V	-	-	10	
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	100	μА
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	2.0	-	4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6.5 A	-	0.220	0.258	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 6.5 \text{ A}$	-	16.3	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 400 V V 0 V	-	1325	1765	pF
C _{oss}	Output Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz		50	65	pF
C _{rss}	Reverse Transfer Capacitance			3	5	pF
C _{oss}	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	30	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	145	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 380 V,I _D = 6.5 A,	-	30.4	39.5	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	6.0	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	9.5	-	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	2.8	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	14.5	39	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_D = 6.5 \text{ A},$	-	10.6	31.2	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	/-	45	100	ns
t _f	Turn-Off Fall Time	(Note 4)	-	9.8	29.6	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode	Maximum Continuous Drain to Source Diode Forward Current		-	13*	Α
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	39	Α
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 6.5 \text{ A}$	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 6.5 A,	-	287	-	ns
Q _{rr}	Reverse Recovery Charge dI _F /dt = 100 A/μs		-	3.5	//-	μC

Notes:

- 1. Repetitive rating: pulse-width limited by maximum junction temperature.
- 2. I_{AS} = 4.3 A, R_{G} = 25 Ω , starting T_{J} = 25°C.
- 3. $I_{SD} \le$ 13 A, di/dt \le 200 A/ μ s, $V_{DD} \le$ BV $_{DSS}$, starting T_J = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

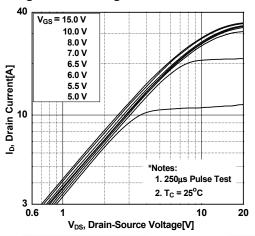


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

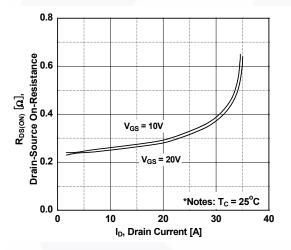


Figure 5. Capacitance Characteristics

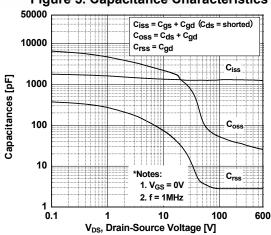


Figure 2. Transfer Characteristics

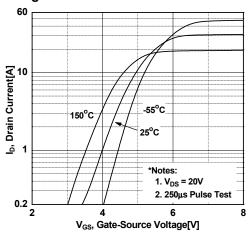


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

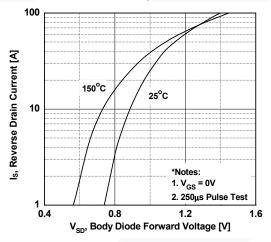
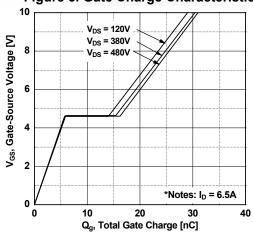


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

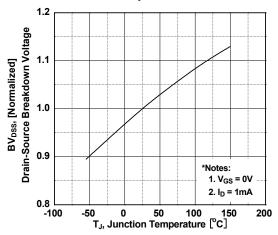


Figure 9. Maximum Safe Operating Area - FCP13N60N

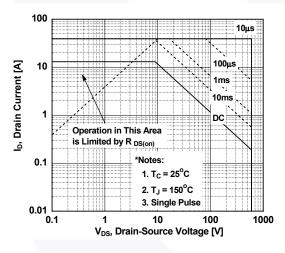


Figure 11. Maximum Drain Current vs. Case Temperature

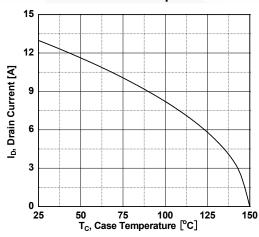


Figure 8. On-Resistance Variation vs. Temperature

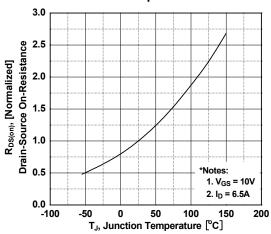
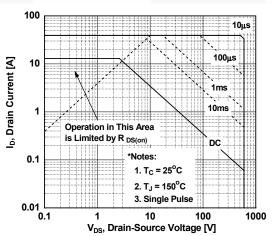


Figure 10. Maximum Safe Operating Area - FCPF13N60NT



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve - FCP13N60N

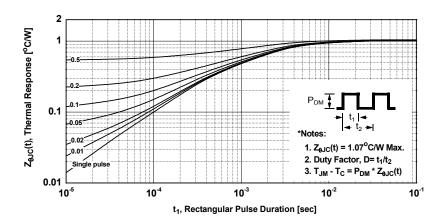
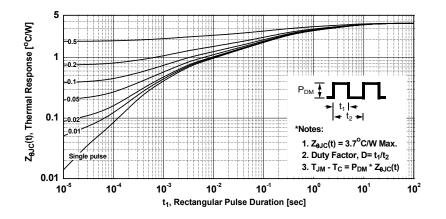


Figure 13. Transient Thermal Response Curve - FCPF13N60NT



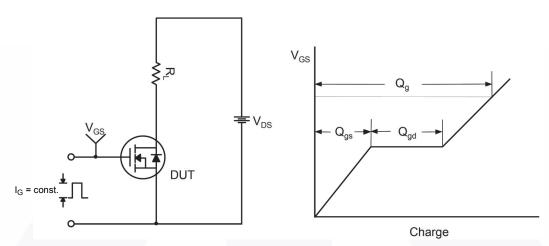


Figure 14. Gate Charge Test Circuit & Waveform

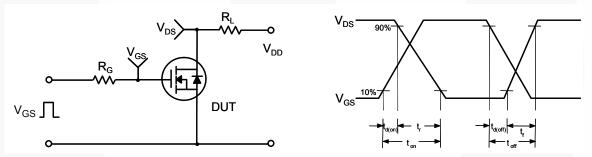


Figure 15. Resistive Switching Test Circuit & Waveforms

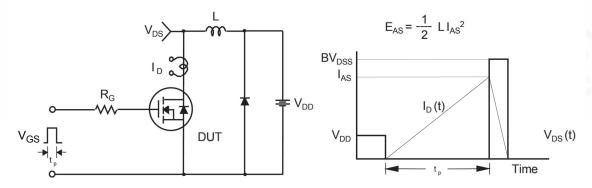


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

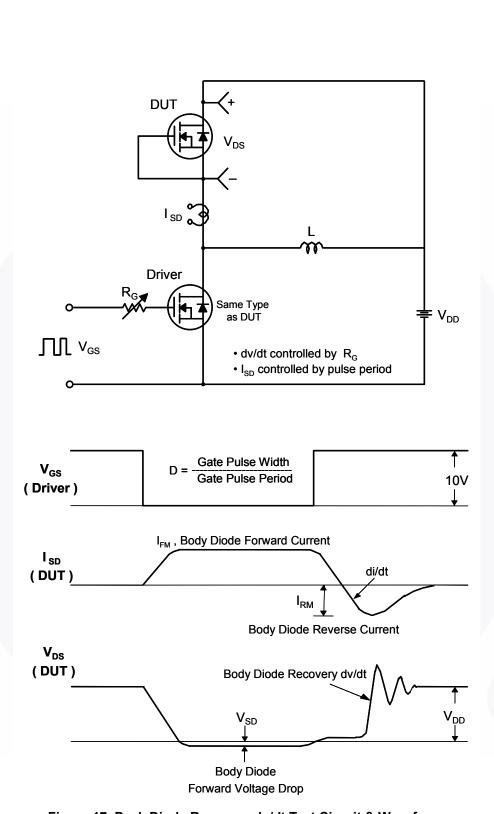


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

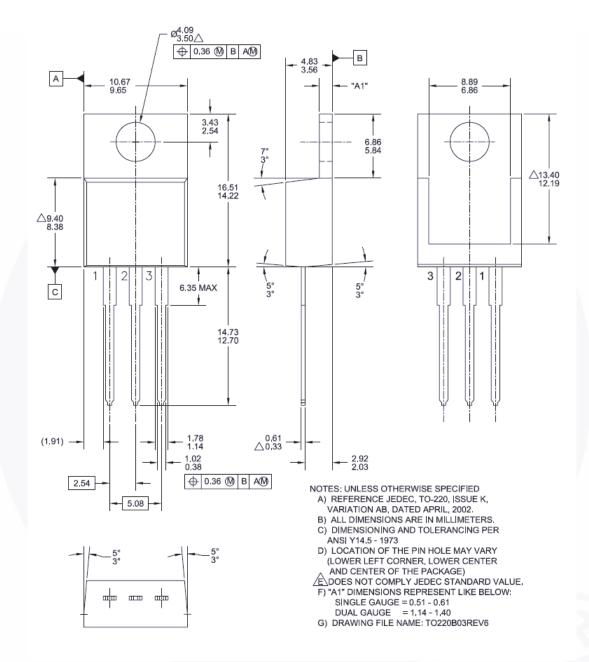


Figure 18. TO-220, Molded, 3-Lead, Jedec Variation AB

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Mechanical Dimensions

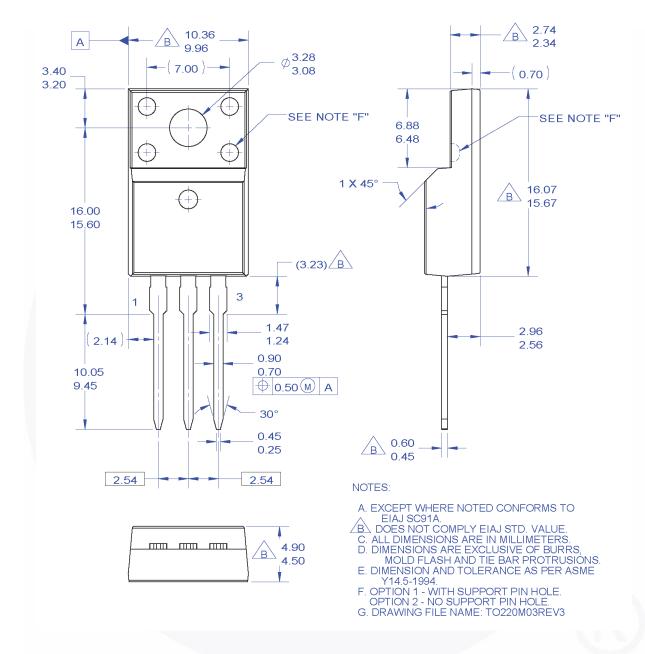


Figure 19. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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