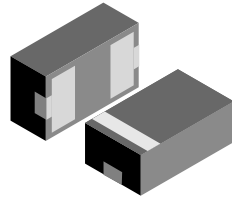
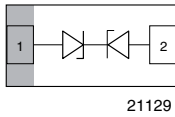




## Ultra Low Capacitance Bidirectional Symmetrical (BiSy) Single Line ESD Protection Diode in LLP1006-2M



20855

### MARKING (example only)



Bar = pin 1 marking  
X = date code  
Y = type code (see table below)

### DESIGN SUPPORT TOOLS click logo to get started



### FEATURES

- Ultra compact LLP1006-2M package
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range  $\pm 5.5$  V
- Low leakage current < 0.01  $\mu$ A
- Ultra low load capacitance  $C_D = 0.36$  pF typ.
- ESD immunity acc. IEC 61000-4-2  
 $\pm 18$  kV contact discharge  
 $\pm 18$  kV air discharge
- Lead plating: Sn (e3); tin plated exposed side wall of leadframe; soldering can be checked by standard vision inspection; (AOI = Automated Outgoing Inspection); no X-ray necessary
- Lead material: Cu
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION			
DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
VBUS05M1-DD1	VBUS05M1-DD1-G3-08	10 000	100 000

PACKAGE DATA				
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	SOLDERING CONDITIONS
VBUS05M1-DD1	LLP1006-2M	5	0.72 mg	260 °C/10 s at terminals reflow soldering according JEDEC® STD-020

ABSOLUTE MAXIMUM RATINGS				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot	$I_{PPM}$	4.5	A
Peak pulse power	Pin 1 to pin 2 Acc. IEC 61000-4-5; $t_p = 8/20$ $\mu$ s; single shot	$P_{PP}$	95	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	$\pm 18$	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		$\pm 18$	
Operating temperature	Junction temperature	$T_J$	-55 to +125	°C
Storage temperature		$T_{stg}$	-55 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.



**ESD PROTECTION FOR HIGH-SPEED SIGNAL OR DATA LINES**

The VBUS05M1-DD1 is a Bidirectional and Symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05M1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny LLP1006 package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots. Due to the very low capacitance the VBUS05M1-DD1 can be used for high speed data ports like HDMI, USB 3.0 or Thunderbolt.

<b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	5.5	V
Reverse voltage	at $I_R = 0.1\text{ }\mu\text{A}$	$V_R$	5.5	-	-	V
Reverse current	at $V_{RWM} = 5.5\text{ V}$	$I_R$	-	-	0.1	$\mu\text{A}$
Reverse breakdown voltage	at $I_R = 1\text{ mA}$	$V_{BR}$	6.0	8.5	10	V
Reverse clamping voltage	at $I_{PP} = 1\text{ A}$	$V_C$	-	11	13	V
	at $I_{PP} = I_{PPM} = 4.5\text{ A}$	$V_C$	-	18	21	V
Capacitance	at $V_R = 0\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	0.36	0.4	pF
	at $V_R = 3.3\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	0.36	-	pF
Clamping voltage	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$ $I_{TLP} = 8\text{ A}$	$V_{C-TLP}$	-	21	-	V
	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$ $I_{TLP} = 16\text{ A}$		-	31	-	
Dynamic resistance	Transmission Line Pulse (TLP); $t_p = 100\text{ ns}$	$R_{DYN}$	-	1.3	-	$\Omega$

**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

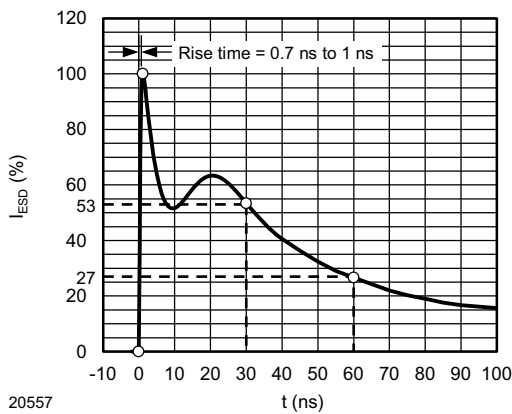


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

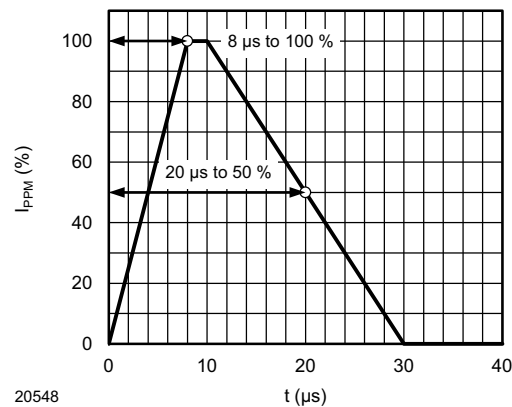


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

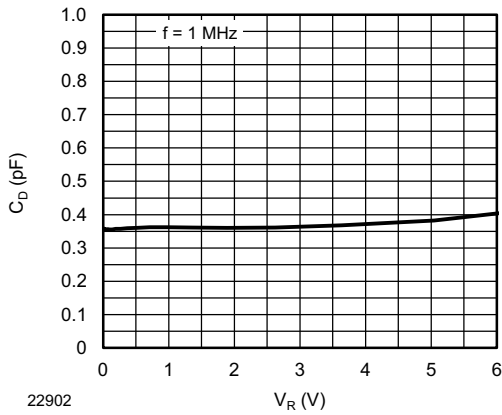


Fig. 3 - Typical Capacitance vs. Reverse Voltage

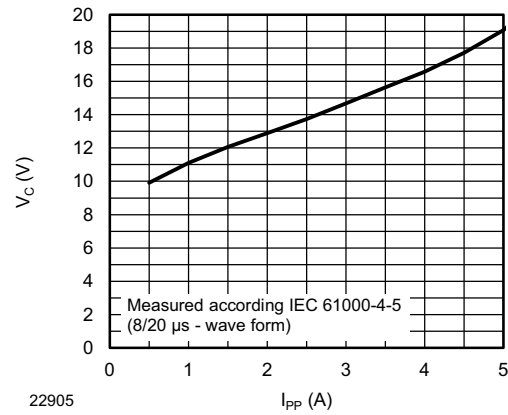


Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current

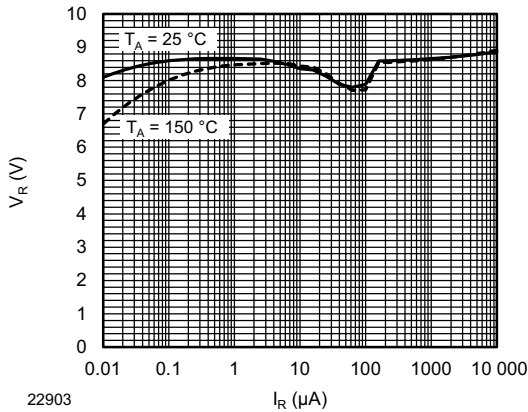


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

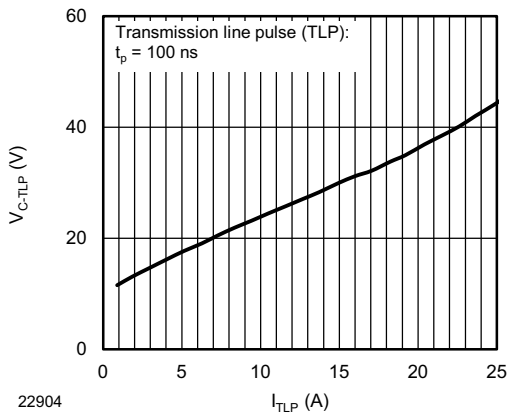
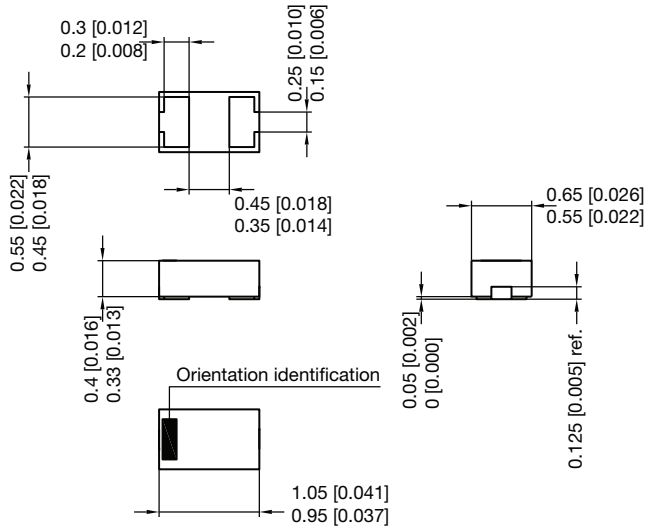


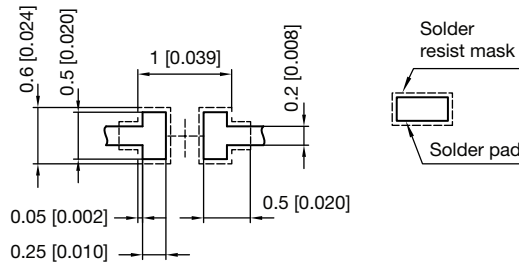
Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current



**PACKAGE DIMENSIONS** in millimeters (inches): **LLP1006-2M**

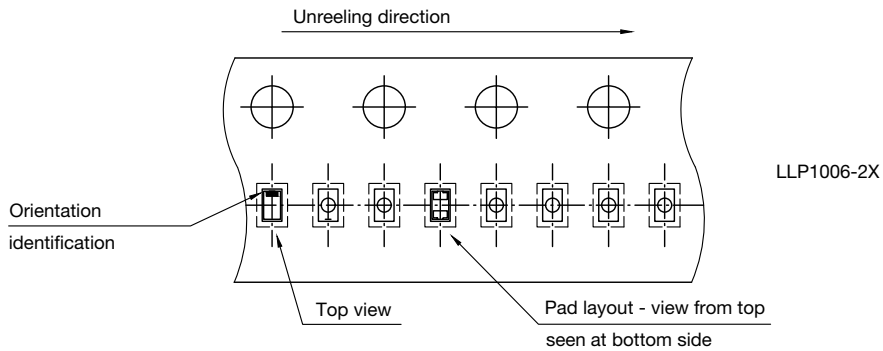


Foot print recommendation:



Pad Design Patented:  
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02.05.2017  
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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