

NTF3055-100, NVF3055-100

Power MOSFET 3.0 Amps, 60 Volts

N-Channel SOT-223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- AEC-Q101 Qualified and PPAP Capable – NVF3055-100
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 10\text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage – Continuous – Non-repetitive ($t_p \leq 10\text{ ms}$)	V_{GS}	± 20 ± 30	Vdc Vpk
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Continuous @ $T_A = 100^\circ\text{C}$ – Single Pulse ($t_p \leq 10\text{ }\mu\text{s}$)	I_D I_D I_{DM}	3.0 1.4 9.0	Adc Adc Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	P_D	2.1	W
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)		1.3	W
		0.014	W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, $I_L(\text{pk}) = 7.0\text{ Apk}$, $L = 3.0\text{ mH}$, $V_{DS} = 60\text{ Vdc}$)	E_{AS}	74	mJ
Thermal Resistance – Junction-to-Ambient (Note 1) – Junction-to-Ambient (Note 2)	$R_{\theta JA}$ $R_{\theta JA}$	72.3 114	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

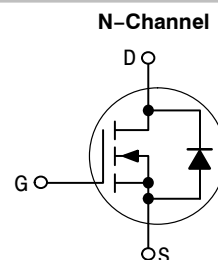
1. When surface mounted to an FR4 board using 1" pad size, 1 oz. (Cu. Area 1.127 sq in).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2–2.4 oz. (Cu. Area 0.272 sq in).



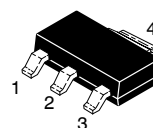
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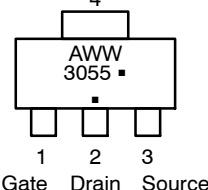
3.0 A, 60 V
 $R_{DS(on)} = 110\text{ m}\Omega$



MARKING DIAGRAM & PIN ASSIGNMENT



**SOT-223
CASE 318E
STYLE 3**



A = Assembly Location
WW = Work Week
3055 = Specific Device Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF3055-100T1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NTF3055-100T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF3055-100T1G	SOT-223 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTF3055-100, NVF3055-100

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\text{ }\mu\text{Adc}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	60 –	68 66	– –	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	–	–	± 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 –	3.0 6.6	4.0 –	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\text{ Adc}$)	$R_{DS(on)}$	–	88	110	m Ω
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.0\text{ Adc}$) ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\text{ Adc}$, $T_J = 150^\circ\text{C}$)	$V_{DS(on)}$	–	0.27 0.24	0.40 –	Vdc
Forward Transconductance (Note 3) ($V_{DS} = 8.0\text{ Vdc}$, $I_D = 1.7\text{ Adc}$)	g_{fs}	–	3.2	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$)	C_{iss}	–	324	455	pF
Output Capacitance		C_{oss}	–	35	50	
Transfer Capacitance		C_{rss}	–	110	155	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$(V_{DD} = 30\text{ Vdc}$, $I_D = 3.0\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$, $R_G = 9.1\text{ }\Omega$) (Note 3)	$t_{d(on)}$	–	9.4	20	ns
Rise Time		t_r	–	14	30	
Turn-Off Delay Time		$t_{d(off)}$	–	21	45	
Fall Time		t_f	–	13	30	
Gate Charge	$(V_{DS} = 48\text{ Vdc}$, $I_D = 3.0\text{ Adc}$, $V_{GS} = 10\text{ Vdc}$) (Note 3)	Q_T	–	10.6	22	nC
		Q_1	–	1.9	–	
		Q_2	–	4.2	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	$(I_S = 3.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$) $(I_S = 3.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 150^\circ\text{C}$) (Note 3)	V_{SD}	– –	0.89 0.74	1.0 –	Vdc
Reverse Recovery Time	$(I_S = 3.0\text{ Adc}$, $V_{GS} = 0\text{ Vdc}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$) (Note 3)	t_{rr}	–	30	–	ns
		t_a	–	22	–	
		t_b	–	8.6	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.04	–	μC

3. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

4. Switching characteristics are independent of operating junction temperatures.

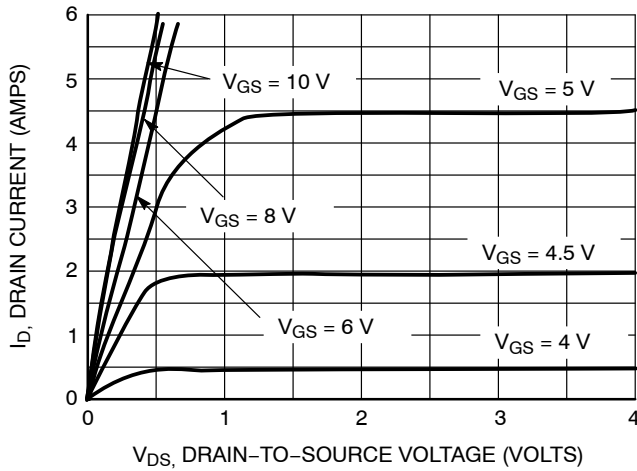


Figure 1. On-Region Characteristics

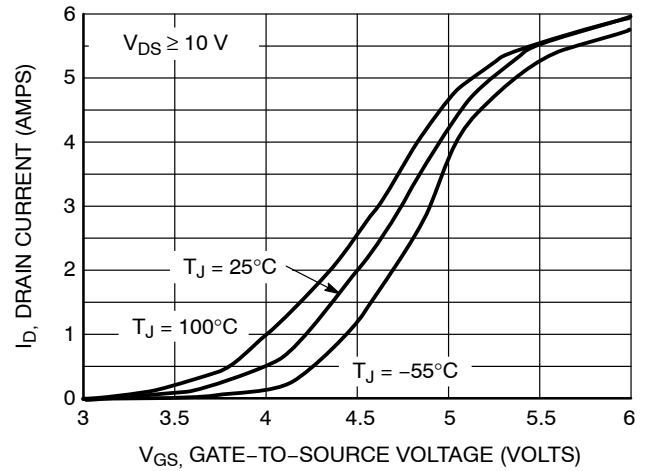


Figure 2. Transfer Characteristics

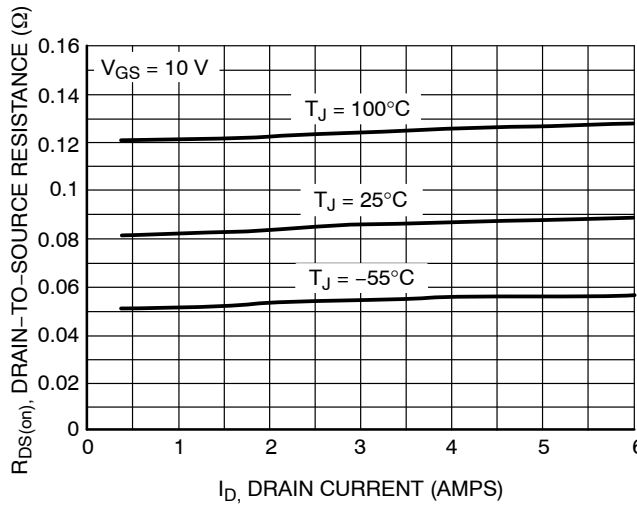


Figure 3. On-Resistance versus Gate-to-Source Voltage

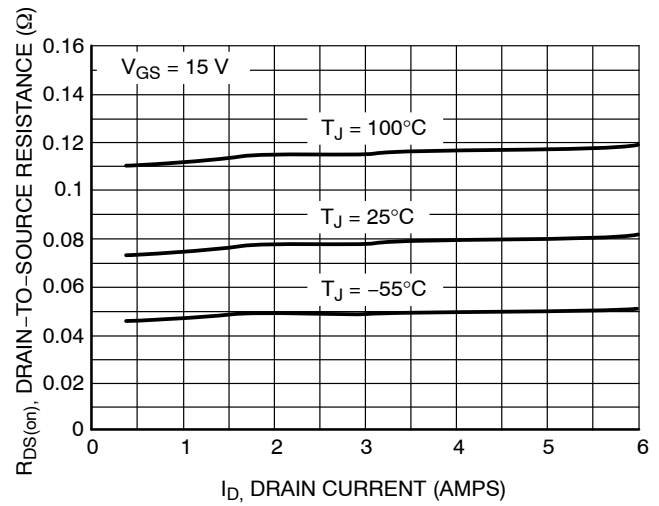


Figure 4. On-Resistance versus Drain Current and Gate Voltage

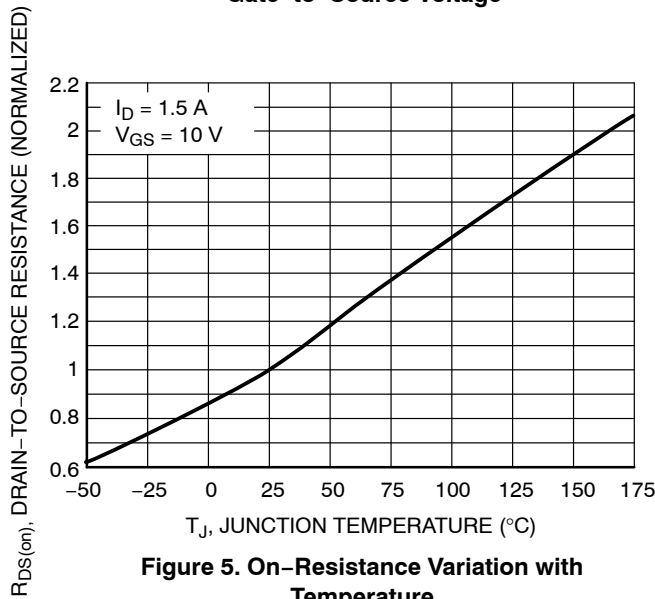


Figure 5. On-Resistance Variation with Temperature

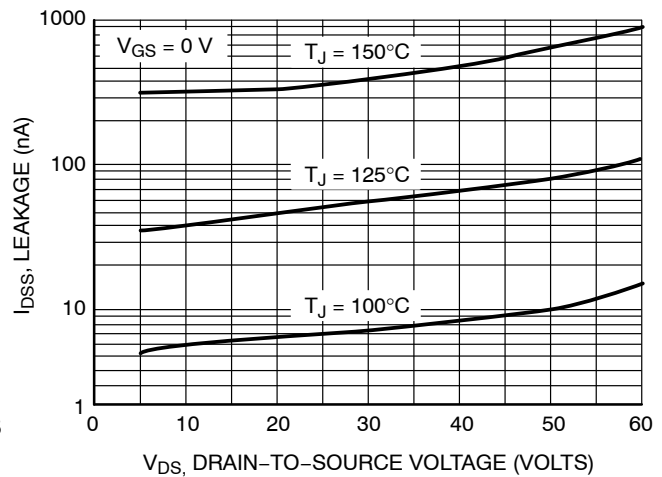


Figure 6. Drain-to-Source Leakage Current versus Voltage

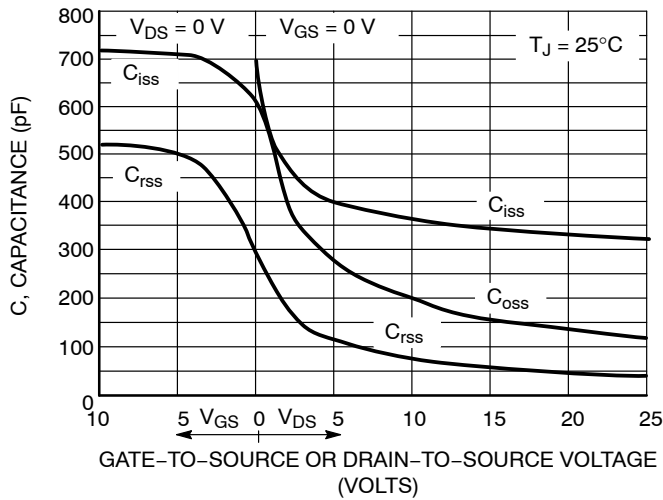


Figure 7. Capacitance Variation

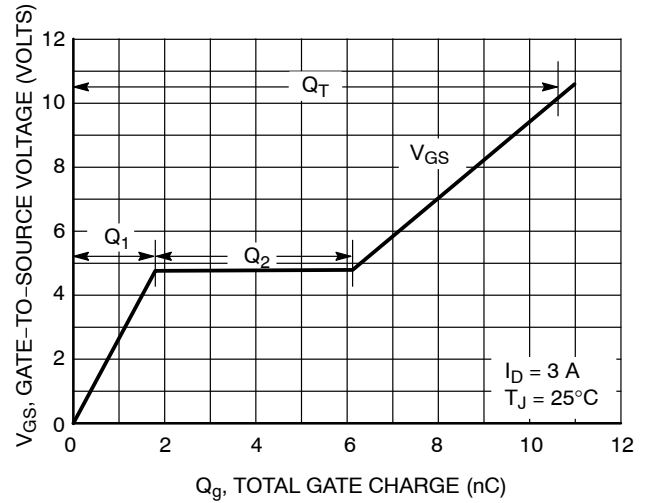


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

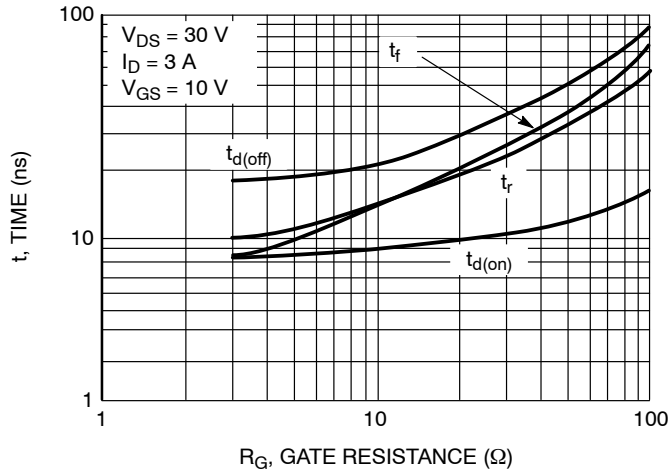


Figure 9. Resistive Switching Time Variation versus Gate Resistance

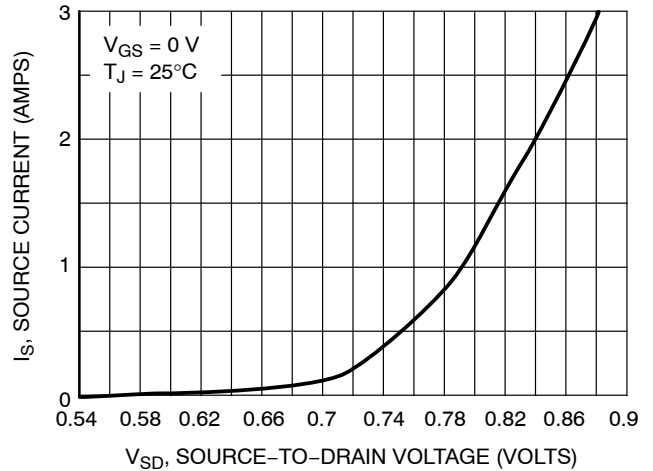


Figure 10. Diode Forward Voltage versus Current

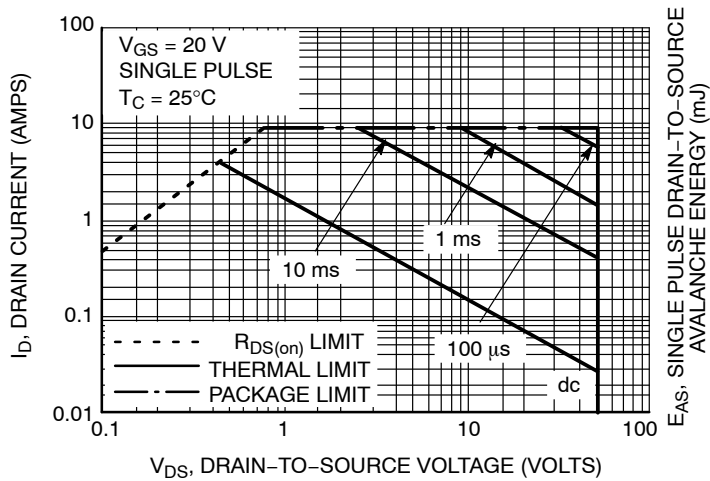


Figure 11. Maximum Rated Forward Biased Safe Operating Area

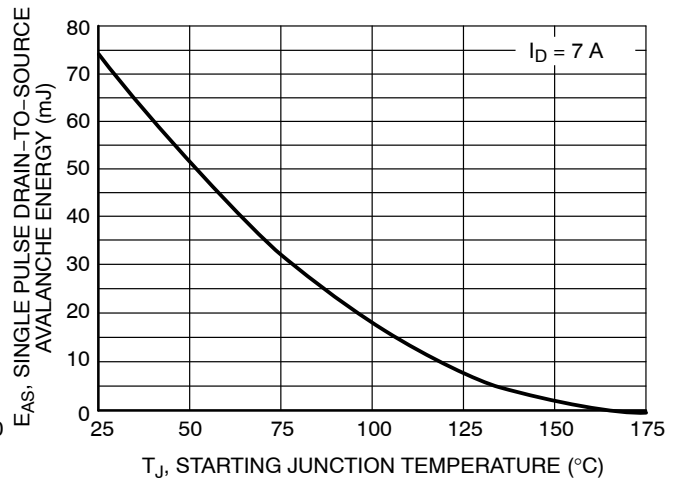


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

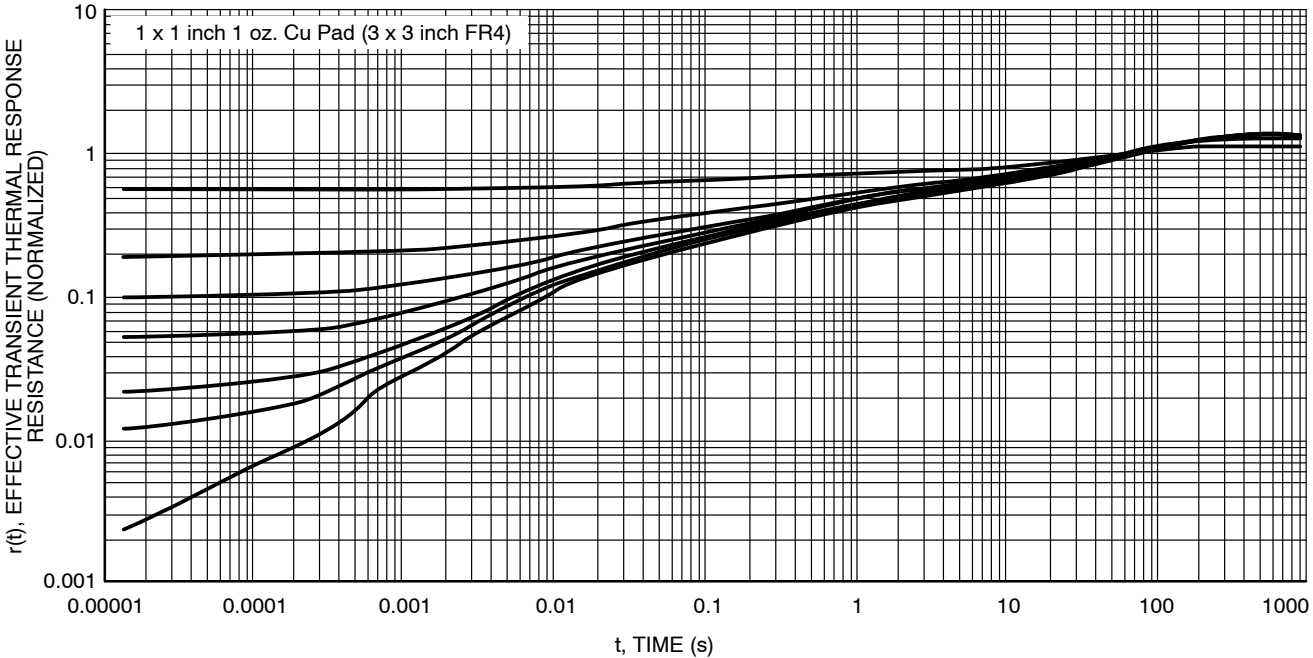
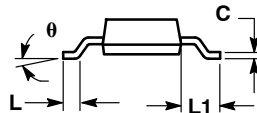
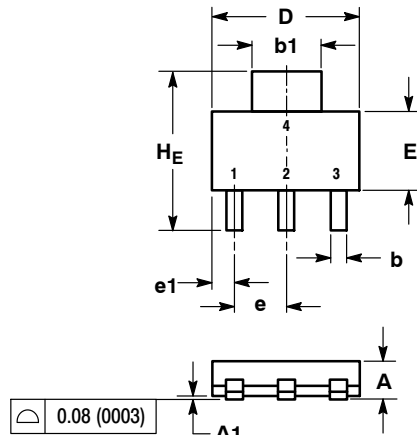


Figure 13. Thermal Response

PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N

NOTES:

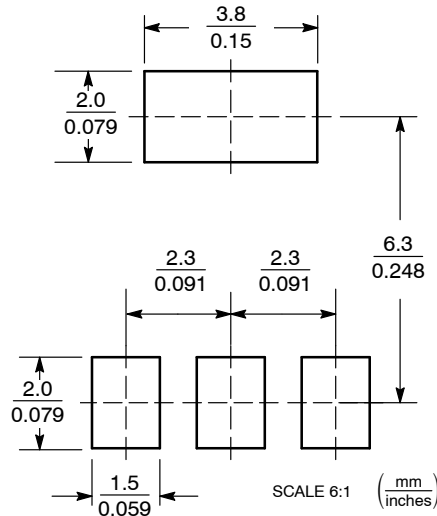
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	---	10°	0°	---	10°

STYLE 3:

- PIN 1: GATE
2: DRAIN
3: SOURCE
4: DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Техническая поддержка проекта;
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