



NX138BKS

60 V, dual N-channel Trench MOSFET

15 June 2016

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

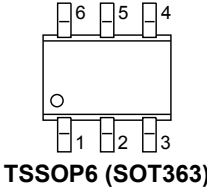
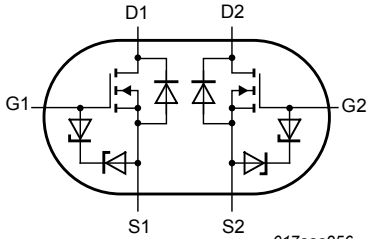
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$		-	-	60	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}$	[1]	-	-	210	mA
Static characteristics (per transistor)							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 200\text{ mA}; T_j = 25\text{ }^{\circ}\text{C}$		-	2.1	3.5	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX138BKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

7. Limiting values

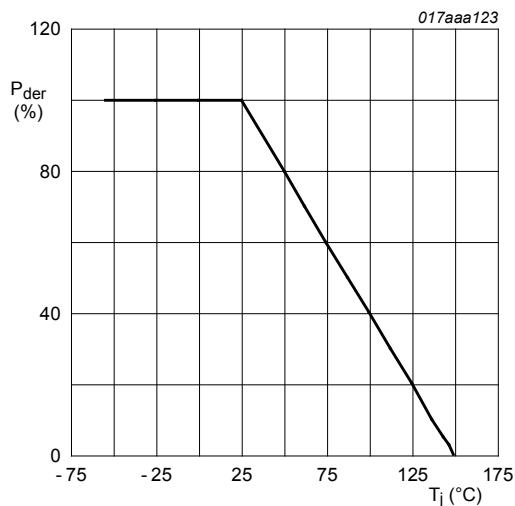
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{DS}	drain-source voltage	T _J = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	210	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	135	mA
		V _{GS} = 10 V; T _{sp} = 25 °C		-	330	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	855	mA
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	285	mW
			[1]	-	320	mW
		T _{sp} = 25 °C		-	860	mW
Per device						
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	170	mA

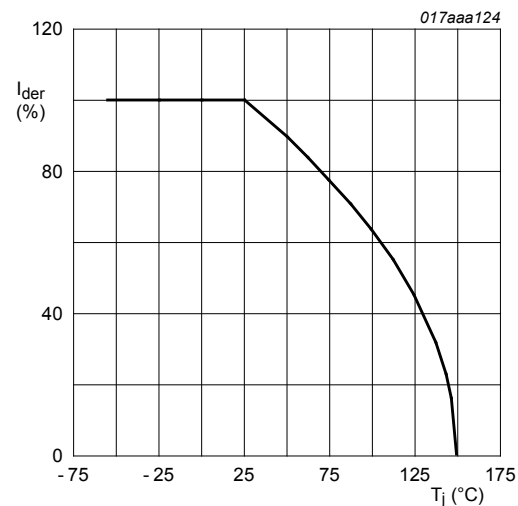
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



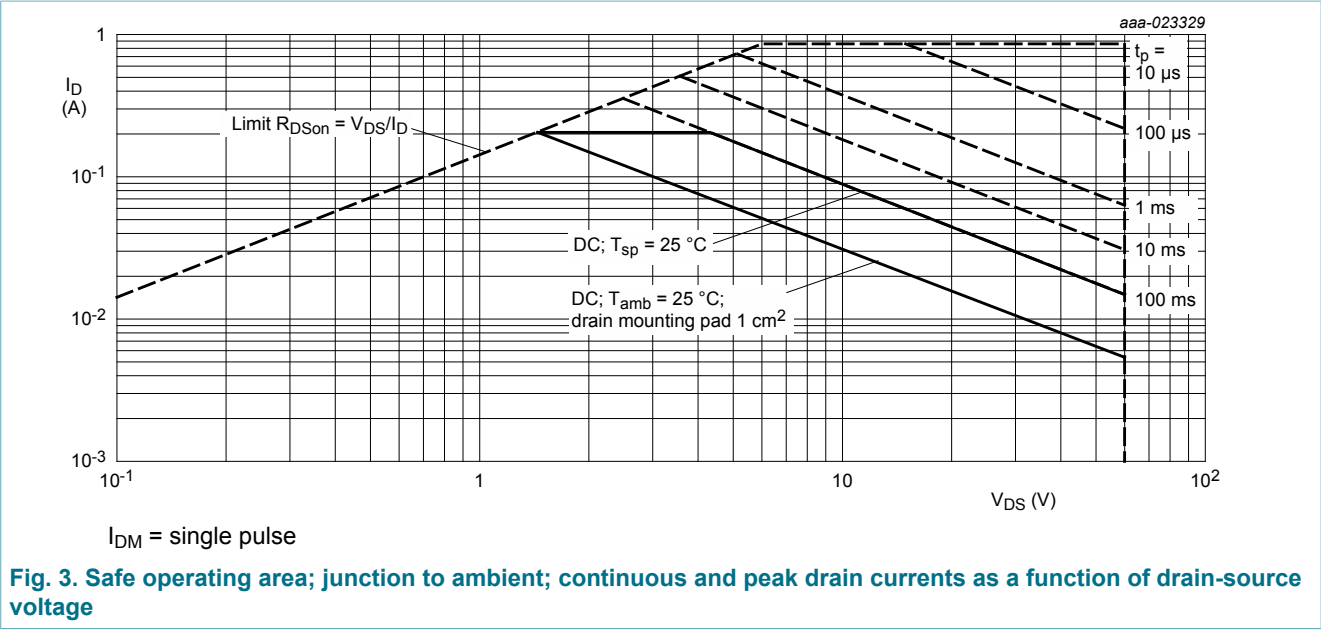
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig. 1. MOSFET transistor: Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig. 2. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

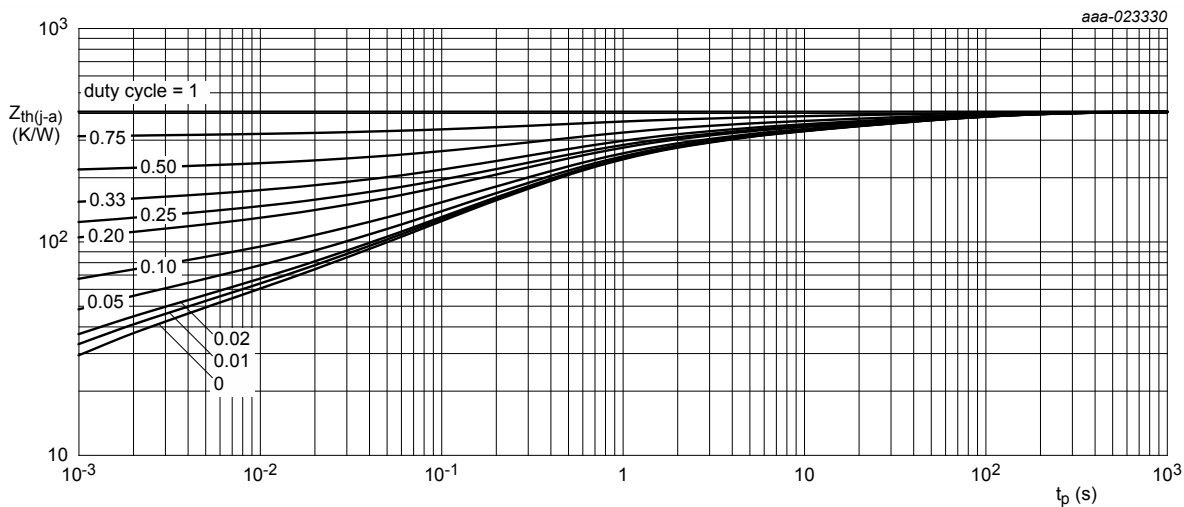


8. Thermal characteristics

Table 5. Thermal characteristics

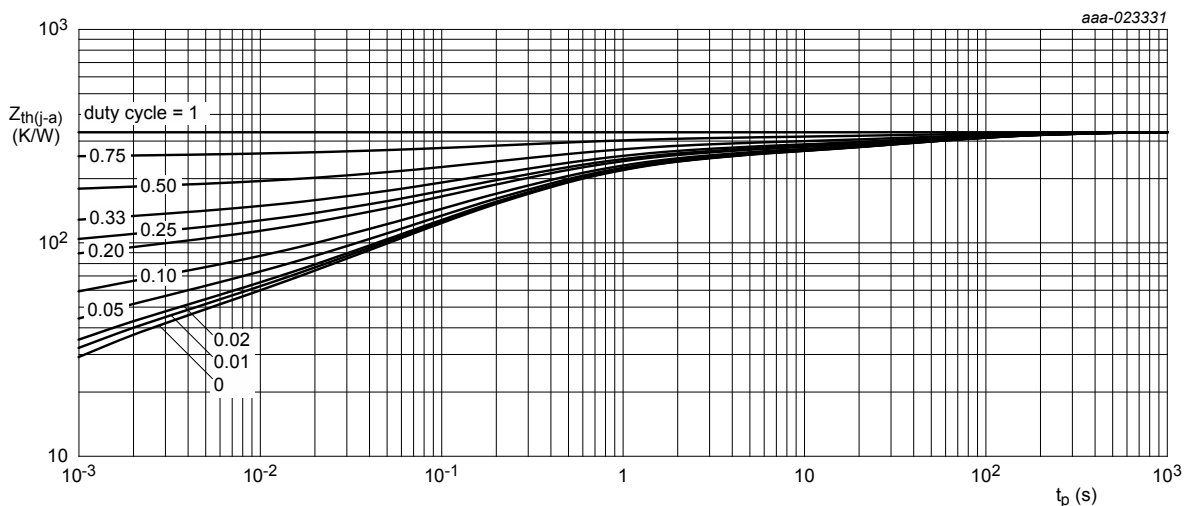
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	380	440	K/W
			[2]	-	340	390	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	125	145	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm^2

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		0.5	1	1.5	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-10	μA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{GS} = 5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	0.3	μA
		V _{GS} = -5 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-0.3	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 200 mA; T _j = 25 °C		-	2.1	3.5	Ω
		V _{GS} = 10 V; I _D = 200 mA; T _j = 150 °C		-	4.3	7.2	Ω
		V _{GS} = 5 V; I _D = 170 mA; T _j = 25 °C		-	2.2	3.8	Ω
		V _{GS} = 2.5 V; I _D = 75 mA; T _j = 25 °C		-	2.6	5	Ω
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 200 mA; T _j = 25 °C		-	0.7	-	S
Dynamic characteristics (per transistor)							
Q _{G(tot)}	total gate charge	V _{DS} = 30 V; I _D = 200 mA; V _{GS} = 10 V; T _j = 25 °C		-	0.5	0.7	nC
Q _{GS}	gate-source charge			-	0.12	-	nC
Q _{GD}	gate-drain charge			-	0.12	-	nC
C _{iss}	input capacitance	V _{DS} = 30 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	20	-	pF
C _{oss}	output capacitance			-	3.1	-	pF
C _{rss}	reverse transfer capacitance			-	2	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; I _D = 200 mA; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	8	-	ns
t _r	rise time			-	8	-	ns
t _{d(off)}	turn-off delay time			-	13	-	ns
t _f	fall time			-	5	-	ns
Source-drain diode (per transistor)							
V _{SD}	source-drain voltage	I _S = 200 mA; V _{GS} = 0 V; T _j = 25 °C		-	0.9	1.2	V

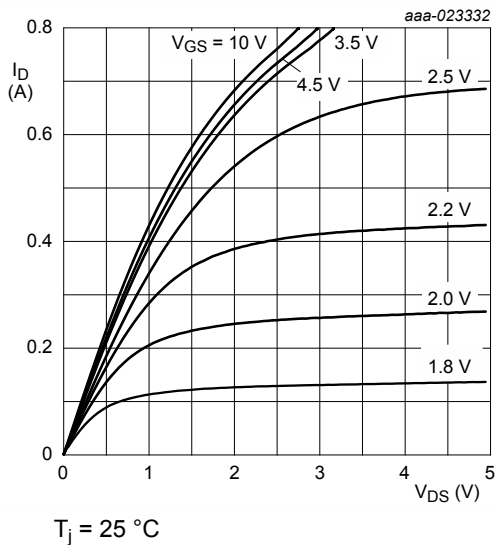


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

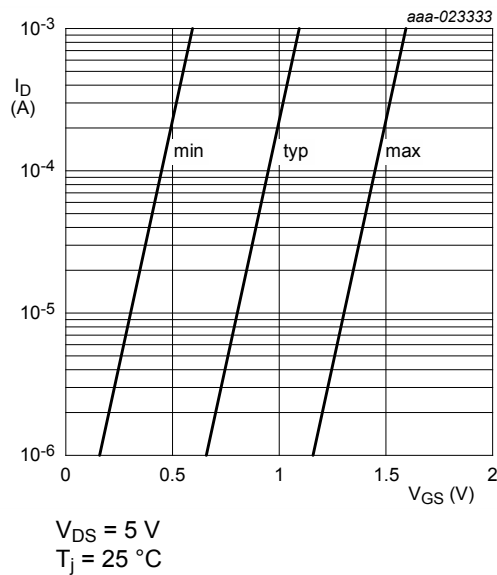


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

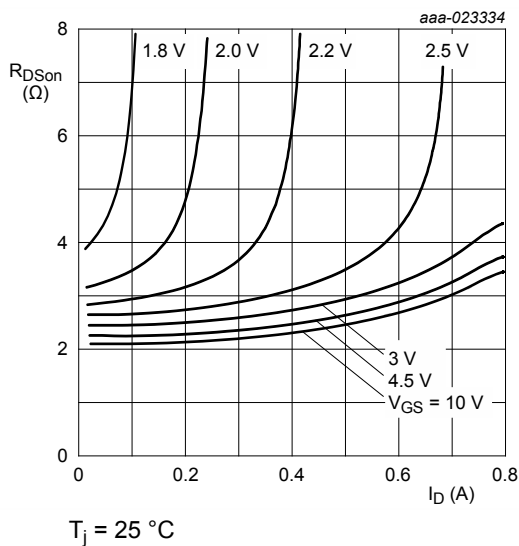


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

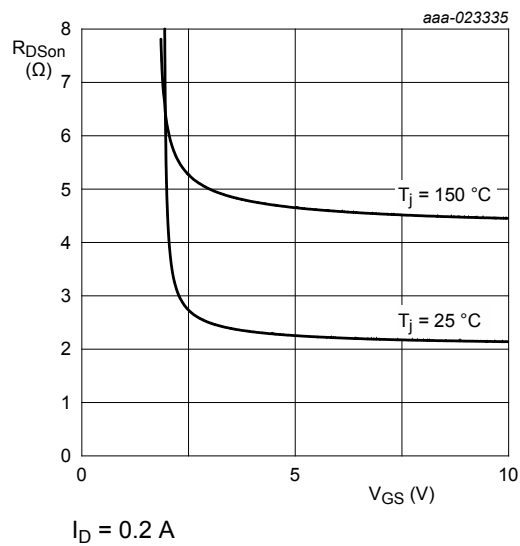


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

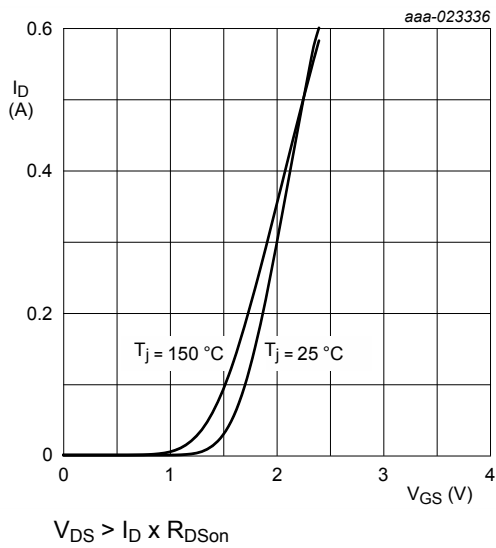


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

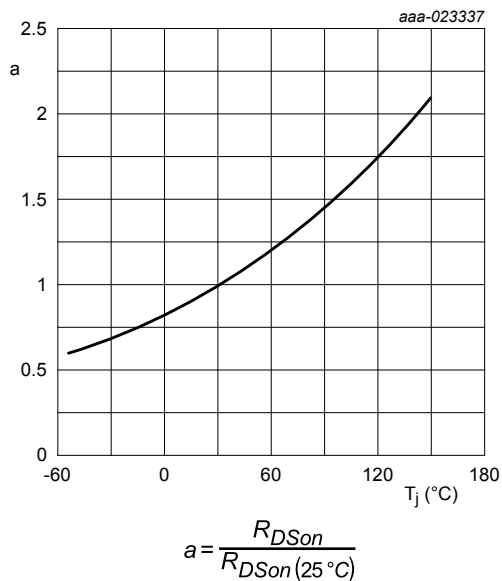


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

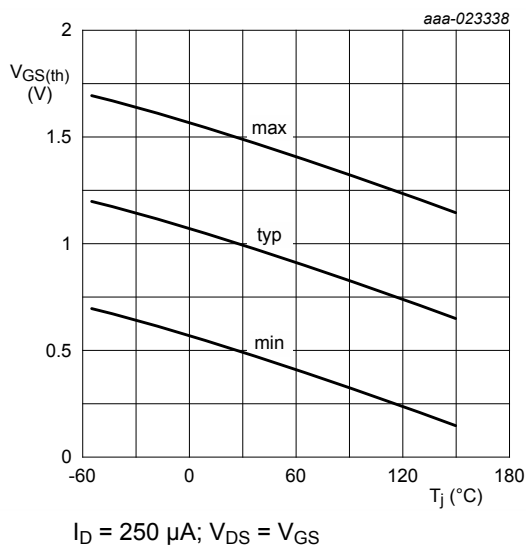


Fig. 12. Gate-source threshold voltage as a function of junction temperature

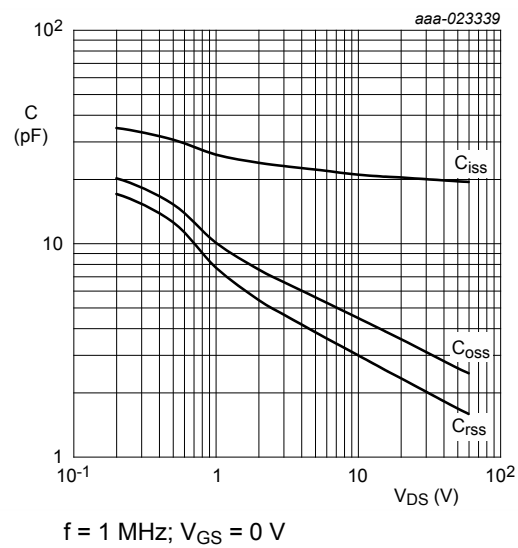


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

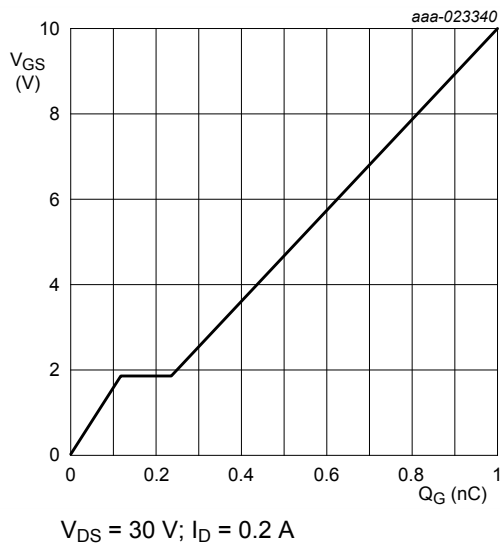


Fig. 14. Gate-source voltage as a function of gate charge; typical values

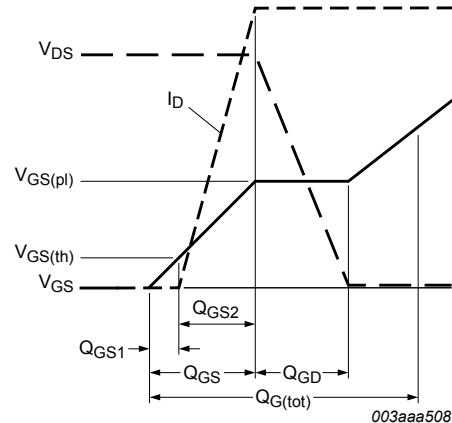


Fig. 15. MOSFET transistor: Gate charge waveform definitions

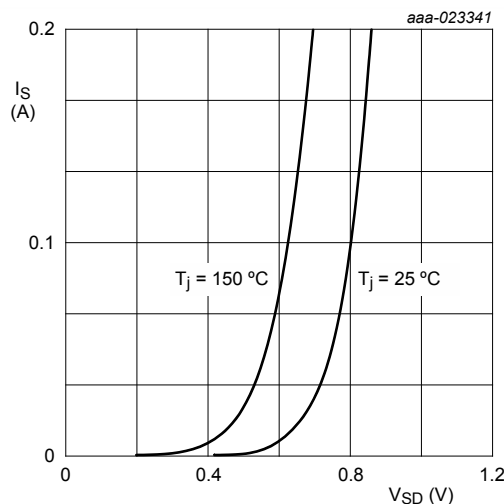


Fig. 16. Source current as a function of source-drain voltage; typical values

10. Test information

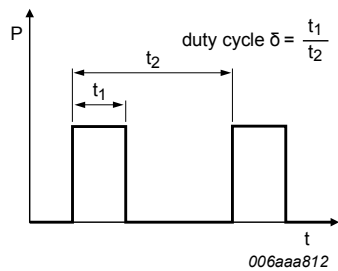
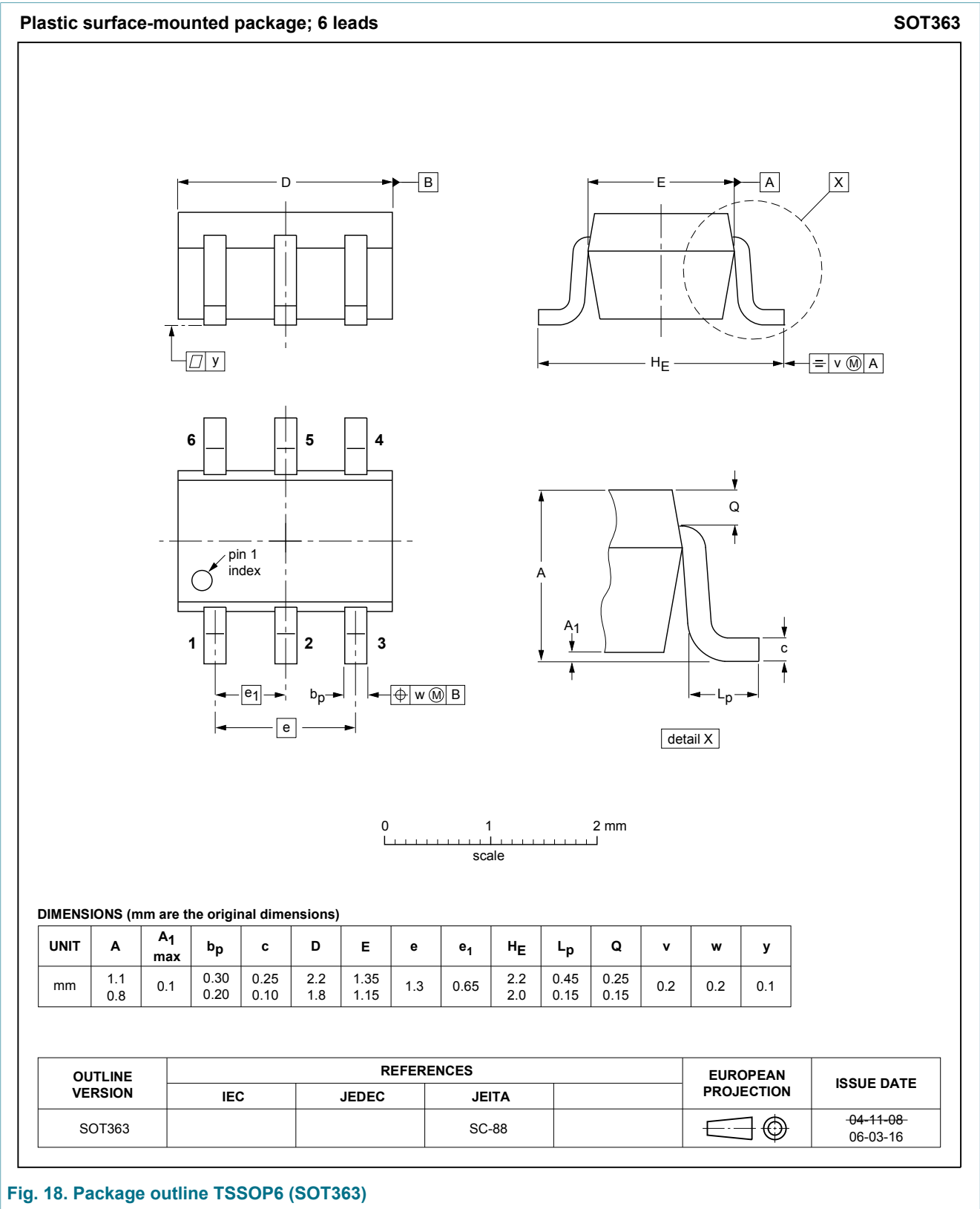


Fig. 17. Duty cycle definition

11. Package outline



12. Soldering

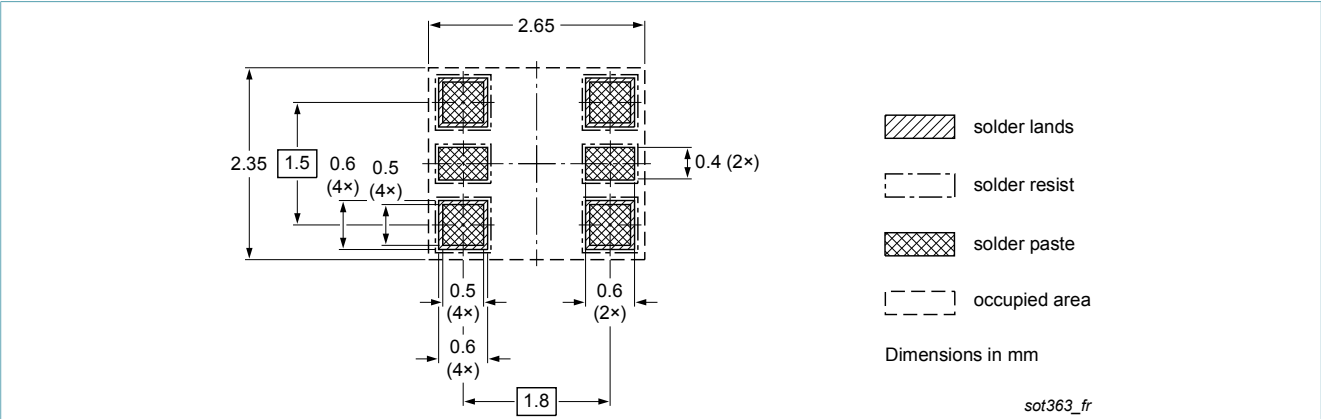


Fig. 19. Reflow soldering footprint for TSSOP6 (SOT363)

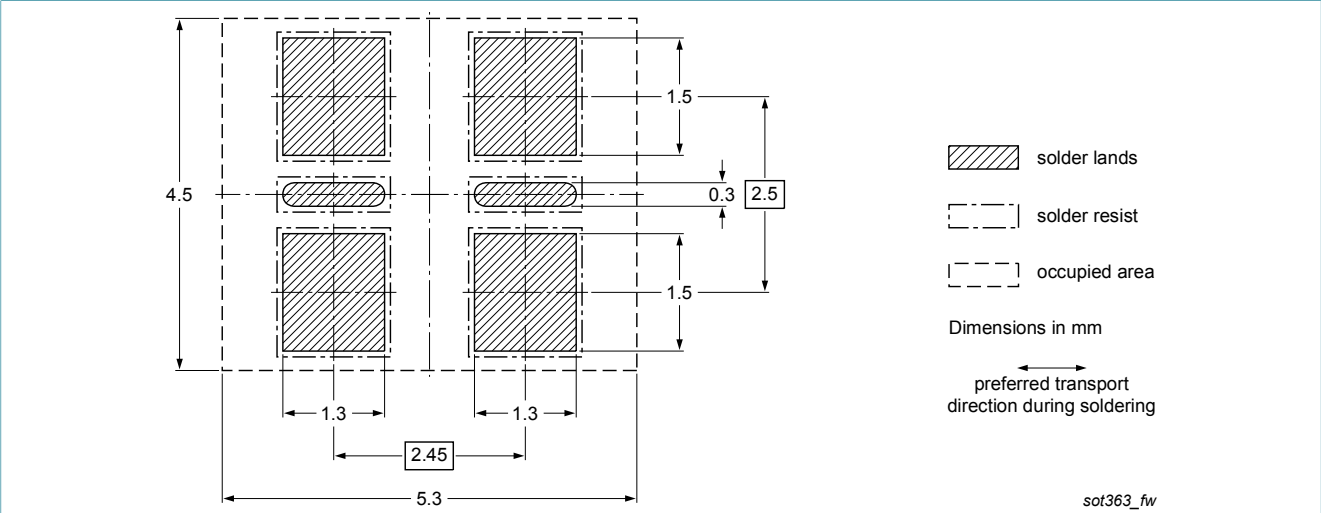


Fig. 20. Wave soldering footprint for TSSOP6 (SOT363)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX138BKS v.1	20160615	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.