SCES843A - JANUARY 2013-REVISED FEBRUARY 2013

16-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: SN74LVC16T245-EP

FEATURES

- Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs and Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly and Test Site
- One Fabrication Site
- Available in Military (-55°C to 125°C)
 Temperature Ranges (1)
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability
- (1) Custom temperature ranges available

DESCRIPTION

This 16-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

1DIR 48 10E 1B1 🛮 2 47 1 1A1 1B2 🛮 3 46 1A2 GND L 45 GND 1B3 44 1 1A3 1B4 ∏ 6 43 | 1A4 42 V_{CCA} V_{CCB} 1B5 📙 8 41 1A5 40 1A6 1B6 **□** 9 GND [] 10 39 GND 1B7 [] 11 38 II 1A7 1B8 🛮 12 37 L 1A8 2B1 13 36 2A1 2B2 14 35 2A2 **GND** 15 34 GND 2B3 L 16 33 L 2A3 17 32 2A4 2B4 🛚 31 V_{CCA} 18 V_{CCB} 2B5 1 19 30 2A5 2B6 20 29 2A6 28 GND GND 21 2B7 🛮 22 27 2A7 2B8 🛮 23 26 2A8 2DIR [24 25 20E

DGG PACKAGE

(TOP VIEW)



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DESCRIPTION (CONTINUED)

The SN74LVC16T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74LVC16T245 is designed so that the control pins (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) are supplied by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 1. ORDERING INFORMATION(1)

T _A	PACKA	AGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
FE°C to 125°C	TOROD DOG	Reel of 2000	CLVC16T245MDGGREP	LVC46T245M	V62/12667-01XE
–55°C to 125°C	o 125°C TSSOP-DGG —		CLVC16T245MDGGEP	LVC16T245M	V62/12667-01XE-T

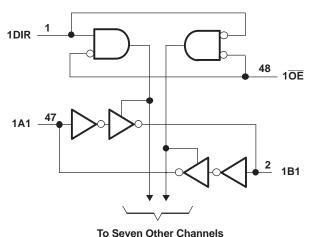
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

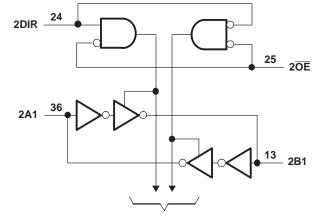
FUNCTION TABLE⁽¹⁾ (EACH 8-BIT SECTION)

CONTRO	L INPUTS	OUTPUT C	IRCUITS	OPERATION
ŌĒ	DIR	A PORT	B PORT	OPERATION
L	L	Enabled	Hi-Z	B data to A bus
L	Н	Hi-Z	Enabled	A data to B bus
Н	Χ	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)





To Seven Other Channels

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Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		-0.5	6.5	V
		I/O ports (A port)	-0.5	6.5	
V_{I}	Input voltage range (2)	I/O ports (B port)	-0.5	6.5	V
		Control inputs	-0.5	6.5	
\/	Voltage range applied to any output	A port	-0.5	6.5	V
Vo	in the high-impedance or power-off state (2)	B port	-0.5	6.5	V
\/	Valtage range applied to any output in the high or law state (2) (3)	A port	-0.5 \	/ _{CCA} + 0.5	V
Vo	Voltage range applied to any output in the high or low state (2) (3)	B port	-0.5 \	/ _{CCB} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CCA} , V _{CCB} , and GND			±100	mA
TJ	Maximum junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

		SN74LVC16T245	
	THERMAL METRIC ⁽¹⁾	DGG	UNITS
		48 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	59.9	
θ_{JCtop}	Junction-to-case (top) thermal resistance (3)	13.9	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	27.1	20044
ΨЈТ	Junction-to-top characterization parameter ⁽⁵⁾	0.5	°C/W
ΨЈВ	Junction-to-board characterization parameter (6)	26.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	N/A	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

⁽²⁾ The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

⁽³⁾ The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.



Recommended Operating Conditions (1)(2)(3)(4)

			V _{CCI}	V _{cco}	MIN	MAX	UNIT
V_{CCA}	0				1.65	5.5	
V _{CCB}	Supply voltage				1.65	5.5	V
			1.65 V to 1.95 V		V _{CCI} × 0.65		
	High-level	5 (5)	2.3 V to 2.7 V		1.7		.,
V_{IH}	input voltage	Data inputs ⁽⁵⁾	3 V to 3.6 V		2		V
			4.5 V to 5.5 V		V _{CCI} × 0.7		
			1.65 V to 1.95 V			V _{CCI} × 0.35	
	Low-level	5 (5)	2.3 V to 2.7 V			0.7	.,
V_{IL}	input voltage	Data inputs ⁽⁵⁾	3 V to 3.6 V			0.8	V
			4.5 V to 5.5 V			V _{CCI} × 0.3	
			1.65 V to 1.95 V		V _{CCA} × 0.65		
	High-level	Control inputs	2.3 V to 2.7 V		1.7		.,
V _{IH}	input voltage	(referenced to V _{CCA}) ⁽⁶⁾	3 V to 3.6 V		2		V
			4.5 V to 5.5 V		V _{CCA} × 0.7		
			1.65 V to 1.95 V			V _{CCA} × 0.35	
	Low-level	Control inputs	2.3 V to 2.7 V			0.7	.,
V_{IL}	input voltage	(referenced to V _{CCA}) ⁽⁶⁾	3 V to 3.6 V			0.8	V
			4.5 V to 5.5 V			$V_{CCA} \times 0.3$	
V _I	Input voltage	Control inputs			0	5.5	V
.,	Innut/output voltogo	Active state			0	V _{cco}	V
V _{I/O}	Input/output voltage	3-State			0	5.5	V
				1.65 V to 1.95 V		-4	
	High-level output cur	rant		2.3 V to 2.7 V		-8	mA
ЮН	nign-ievei output cun	rent		3 V to 3.6 V		-24	MA
				4.5 V to 5.5 V		-32	
				1.65 V to 1.95 V		4	
ı	Low lovel output our	ont		2.3 V to 2.7 V		8	mΛ
OL	Low-level output curr	ent		3 V to 3.6 V		24	mA
				4.5 V to 5.5 V		32	
			1.65 V to 1.95 V			20	·
Δt/Δν	Input transition	Data inputs	2.3 V to 2.7 V			20	ns/V
ΔI/ΔV	rise or fall rate	Data Iliputs	3 V to 3.6 V			10	HS/V
			4.5 V to 5.5 V			5	
T _A	Operating free-air ter	nperature			-55	125	°C

V_{CCI} is the V_{CC} associated with the input port.

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⁽²⁾

 V_{CCO} is the V_{CC} associated with the output port. All unused or driven (floating) data inputs (I/Os) of the device must be held at logic HIGH or LOW (preferably V_{CCI} or GND) to ensure proper device operation and minimize power. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

⁽⁴⁾ All unused data inputs of the device must be held at V_{CCA} or GND to ensure proper device operation.
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.
(6) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

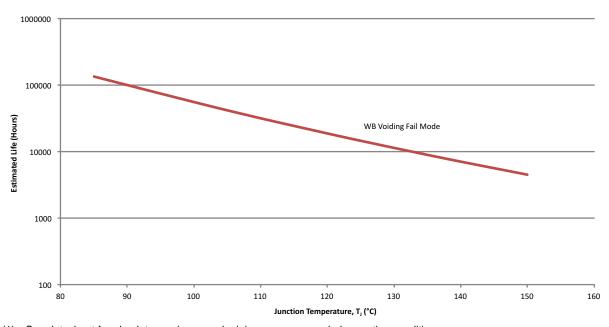
Electrical Characteristics (1)(2)

 $T_A = -55$ °C to 125°C, over recommended input voltage range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
		$I_{OH} = -100 \ \mu A, \qquad V_I = V_{IH}$	1.65 V to 4.5 V	1.65 V to 4.5 V	V _{CCO} - 0.1			
		$I_{OH} = -4 \text{ mA}, \qquad V_I = V_{IH}$	1.65 V	1.65 V	1.2			
V_{OH}		$I_{OH} = -8 \text{ mA}, \qquad V_I = V_{IH}$	2.3 V	2.3 V	1.9			V
		$I_{OH} = -24 \text{ mA}, \qquad V_I = V_{IH}$	3 V	3 V	2.35			
		$I_{OH} = -32 \text{ mA}, \qquad V_I = V_{IH}$	4.5 V	4.5 V	3.75			
		$I_{OL} = 100 \mu A$, $V_I = V_{IL}$	1.65 V to 4.5 V	1.65 V to 4.5 V			0.1	
		$I_{OL} = 4 \text{ mA}, \qquad V_I = V_{IL}$	1.65 V	1.65 V			0.45	
V_{OL}		$I_{OL} = 8 \text{ mA}, \qquad V_I = V_{IL}$	2.3 V	2.3 V			0.3	V
		$I_{OL} = 24 \text{ mA}, \qquad V_I = V_{IL}$	3 V	3 V			0.65	
		$I_{OL} = 32 \text{ mA}, \qquad V_I = V_{IL}$	4.5 V	4.5 V			0.65	
I _I	Control inputs	V _I = V _{CCA} or GND	1.65 V to 5.5 V	1.65 V to 5.5 V			±2	μΑ
	A or B	\\ \cap\\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\	0 V	0 to 5.5 V			±10	
l _{off}	port	V_1 or $V_0 = 0$ to 5.5 V	0 to 5.5 V	0 V			±10	μA
I _{OZ}	A or B port	$\frac{V_O}{OE} = V_{CCO}$ or GND, $\frac{V_O}{OE} = V_{IH}$	1.65 V to 5.5 V	1.65 V to 5.5 V			±10	μΑ
			1.65 V to 5.5 V	1.65 V to 5.5 V			20	
I_{CCA}		$V_I = V_{CCI}$ or GND, $I_O = 0$	5 V	0 V			20	μΑ
		10 - 0	0 V	5 V			-2.5	
			1.65 V to 5.5 V	1.65 V to 5.5 V			20	
I_{CCB}		$V_I = V_{CCI}$ or GND, $I_O = 0$	5 V	0 V			-2.5	μΑ
		10 - 0	0 V	5 V			20	
I _{CCA} + I _C	ССВ	$V_I = V_{CCI}$ or GND, $I_O = 0$	1.65 V to 5.5 V	1.65 V to 5.5 V			30	μΑ
	A port	One A port at $V_{CCA} - 0.6 \text{ V}$, DIR at V_{CCA} , B port = open					50	
ΔI _{CCA}	DIR	DIR at V _{CCA} – 0.6 V, B port = open, A port at V _{CCA} or GND	3 V to 5.5 V	3 V to 5.5 V			50	μΑ
ΔI _{CCB}	B port	One B port at $V_{CCB} - 0.6 V$, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V			50	μΑ
C _i	Control inputs	V _I = V _{CCA} or GND	3.3 V	3.3 V		4		pF
C _{io}	A or B port	$V_O = V_{CCA/B}$ or GND	3.3 V	3.3 V		8.5		pF

 $[\]begin{array}{ll} \hbox{(1)} & V_{CCO} \mbox{ is the } V_{CC} \mbox{ associated with the output port.} \\ \hbox{(2)} & V_{CCI} \mbox{ is the } V_{CC} \mbox{ associated with the input port.} \\ \end{array}$





(1) See datasheet for absolute maximum and minimum recommended operating conditions.

Figure 1. SN74LVC16T245-EP Operating Life Derating Chart

Switching Characteristics

 $T_A = -40$ °C to 85°C, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	FROM TO (INPUT)		V _{CCB} = 1.8 V ± 0.15 V V _{CCB} = 2.5 V ± 0.2 V		V _{CCB} = 3.3 V ± 0.3 V		V _{CCB} = 5 V ± 0.5 V		UNIT	
	(INFO1)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	В	1.7	21.9	1.3	9.2	1	7.4	0.8	7.1	ns
t _{PHL}	Α	5	1.7	21.5	1.0	5.2		7.4	0.0	7.1	113
t _{PLH}	В	Α	0.9	23.8	0.8	23.6	0.7	23.4	0.7	23.4	ns
t _{PHL}	Б	٨	0.9	23.0	0.0	25.0	0.7	25.4	0.7	25.4	113
t_{PHZ}	 OE	Α	1.6	29.6	1.5	29.4	1.5	29.3	1.4	29.2	ns
t_{PLZ}	OL	A	1.0	23.0	1.5	23.4	2.9	29.5	1.4	23.2	113
t_{PHZ}	 OE	В	2.4	32.2	1.9	13.1	1.7	12	1.3	10.3	ns
t_{PLZ}	OL	В	2.4	52.2	1.3	13.1	1.7	12	1.5	10.5	113
t_{PZH}	 OE	Α	0.4	24	0.4	23.8	0.4	23.7	0.4	23.7	ns
t _{PZL}	OE	^	0.4	24	0.4	23.0	0.4	23.1	0.4	23.1	115
t_{PZH}	 OE	В	1.8	32	1.6	16	1.2	12.6	0.9	10.8	ns
t _{PZL}	OL	В	1.0	32	1.0	10	1.2	12.0	0.9	10.0	115

Switching Characteristics

 $T_A = -55$ °C to 125°C, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.8 V ± 0.15 V			V _{CCB} = 5 V ± 0.5 V	UNIT						
	(1141 01)	(0011 01)	MIN MAX	MIN MAX	MIN MAX	MIN MAX							
t _{PLH}	A	В	25.9	13.2	11.4	11.1	ns						
t _{PHL}	A	Ь	25.9	13.2	11.4	11.1	115						
t _{PLH}	В	^	27.8	27.8	27.4	27.4	ns						
t _{PHL}	Ь	Α	21.0	27.0	27.4	27.4	115						
t_{PHZ}	ŌĒ	А	33.6	33.4	33.3	33.2	ns						
t_{PLZ}	OL	A	A	Λ	Α	A	A	Λ	33.0	33.4	33.3	33.2	115
t_{PHZ}	ŌĒ	В	36.2	17.1	16	14.3	ns						
t_{PLZ}	OL	В	30.2	17.1	10	14.3	115						
t _{PZH}	ŌĒ	А	28	27.8	27.7	27.7	20						
t _{PZL}	OE .	A	26	27.0	21.1	21.1	ns						
t _{PZH}	ŌĒ	В	36	22	16.6	14.8	20						
t _{PZL}	OE .	В	36	22	10.0	14.0	ns						



Switching Characteristics

 $T_A = -40$ °C to 85°C, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO	V _{CCB} = ± 0.1			= 2.5 V .2 V	V _{CCB} = ± 0.	: 3.3 V 3 V	V _{CCB} 0.5		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	В	1.6	21.4	1.2	9	0.8	6.2	0.6	4.8	ns
t _{PHL}	A	Ь	1.0	21.4	1.2	9	0.0	0.2	0.0	4.0	115
t _{PLH}	В	Α	1.2	9.3	1	9.1	1	8.9	0.9	8.8	ns
t _{PHL}	Ь	Α	1.2	9.5		9.1		0.9	0.9	0.0	115
t_{PHZ}	 OE	Α	1.4	9	1.4	9	1.4	9	1.4	9	ns
t_{PLZ}	OL	^	1.4	<u> </u>	1.4	9	1.4	3	1.4	3	113
t_{PHZ}	 OE	В	2.3	29.6	1.8	11	1.7	9.3	0.9	6.9	ns
t_{PLZ}	OL	Ь	2.5	23.0	1.0		1.7	9.0	0.5	0.9	113
t_{PZH}	OE	Α	1	10.9	1	10.9	1	10.9	1	10.9	ns
t_{PZL}	OL.	Α	'	10.9	'	10.9	'	10.9	!	10.9	115
t_{PZH}	<u>OE</u>	В	1.7	28.2	1.6	12.9	1.2	9.4	1	6.9	ns
t_{PZL}	OL .	В	1.7	20.2	1.0	12.5	1.2	9.4	'	0.9	115

Switching Characteristics

 $T_A = -55$ °C to 125°C, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CCB} = 1.8 V ± 0.15 V	V _{CCB} = 2.5 V ± 0.2 V	V _{CCB} = 3.3 V ± 0.3 V	V _{CCB} = 5 V 0.5 V	UNIT
	(INPUT)	(OUTPUT)	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _{PLH}	A	В	25.4	13	10.2	8.8	ns
t _{PHL}	^	Б	25.4	13	10.2	0.0	113
t _{PLH}	В	Α	13.3	13.1	12.9	12.8	ns
t _{PHL}	В	A	13.3	13.1	12.9	12.0	115
t_{PHZ}	ŌĒ	Α	13	13	13	13	ns
t_{PLZ}	OL	A	13	13	13	13	115
t _{PHZ}	ŌĒ	В	33.6	14	14.3	10.9	ns
t_{PLZ}	OL	В	33.0	14	14.5	10.9	115
t _{PZH}	ŌĒ	^	14.9	14.9	14.9	14.9	no
t _{PZL}	OE	Α	14.9	14.9	14.9	14.9	ns
t _{PZH}	ŌĒ	В	32.2	16.9	13.4	10.9	20
t _{PZL}	OE .	В	32.2	16.9	13.4	10.9	ns

Product Folder Links: SN74LVC16T245-EP

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Switching Characteristics

 $T_A = -40$ °C to 85°C, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CCB} = ± 0.1	: 1.8 V I5 V	V _{CCB} = ± 0.	= 2.5 V 2 V	V _{CCB} = ± 0.3		V _{CCB} ± 0.		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	В	1.5	21.2	1.1	8.8	0.8	6.1	0.5	4.4	ns
t _{PHL}	^	ь	1.5	21.2	1.1	0.0	0.6	0.1	0.5	4.4	115
t _{PLH}	В	Α	0.9	7.2	0.8	6.2	0.7	6.1	0.6	6	ns
t _{PHL}	В	Α	0.9	1.2	0.0	0.2	0.7	0.1	0.0	O	115
t _{PHZ}	ŌĒ	А	1.6	8.2	1.6	8.2	1.6	6.2	1.6	8.2	ns
t_{PLZ}	OL	Λ	1.0	0.2	1.0	0.2	1.0	0.2	1.0	0.2	113
t_{PHZ}	ŌĒ	В	2.1	29	1.7	10.3	1.5	8.6	0.8	6.3	ns
t_{PLZ}	OL	<u> </u>	2.1	23	1.7	10.5	1.0	0.0	0.0	0.5	113
t _{PZH}	ŌĒ	Α	0.8	7.8	0.8	7.8	0.8	7.8	0.8	7.8	ns
t_{PZL}	OL .	Λ	0.0	7.0	0.0	7.0	0.6	7.0	0.0	7.0	115
t _{PZH}	ŌĒ	В	1.6	27.7	1.4	12.4	1.1	8.5	0.9	8.4	ns
t_{PZL}	JL	נ	1.0	21.1	1.4	12.4	1.1	0.5	5.9	0.4	113

Switching Characteristics

 $T_A = -55$ °C to 125°C, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO	V _{CCB} = 1.8 V ± 0.15 V	V _{CCB} = 2.5 V ± 0.2 V	V _{CCB} = 3.3 V ± 0.3 V	V _{CCB} = 5 V ± 0.5 V	UNIT
	(INPUT)	(OUTPUT)	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _{PLH}	A	В	25.2	12.8	10.2	8.4	ns
t _{PHL}	Λ	Ь	25.2	12.0	10.2	0.4	113
t _{PLH}	В	А	11.2	10.2	10.1	10	ns
t _{PHL}	Б	A	11.2	10.2	10.1	10	115
t_{PHZ}	ŌĒ	А	12.2	12.2	12.2	12.2	ns
t_{PLZ}	OL	A	12.2	12.2	12.2	12.2	115
t_{PHZ}	ŌĒ	В	33	14.3	12.8	10.3	ns
t_{PLZ}	OL	Ь	33	14.5	12.0	10.5	115
t_{PZH}	ŌĒ	^	11.0	12.1	12.1	10.1	no
t _{PZL}	OE .	A	11.8	12.1	12.1	12.1	ns
t _{PZH}	ŌĒ	В	31.7	16.4	12.9	10.4	ns
t_{PZL}	OE .	Б	31.7	10.4	12.9	10.4	115



Switching Characteristics

 $T_A = -40$ °C to 85°C, $V_{CCA} = 5$ V \pm 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)		V _{CC} = 1.8 V V _{CC} = 2 ± 0.15 V ± 0.2			V _{CC} = 3.3 V ± 0.3 V		V _{CC} : ± 0.		UNIT
	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	В	1.6	21.4	1	8.8	0.7	6	0.4	4.2	ns
t _{PHL}	^	В	1.0	21.4		0.0	0.7		0.4	4.2	113
t _{PLH}	- В	А	0.7	6.8	0.4	4.8	0.3	4.5	0.3	4.3	ns
t _{PHL}	В		0.7	0.0	0.4	4.0	0.5	4.5	0.3	4.3	115
t_{PHZ}	- ŌE	А	0.3	5.4	0.3	5.4	0.3	5.4	0.3	6.4	ns
t _{PLZ}	OL	^	0.5	5.4	0.5	5.4	0.5	5.4	0.5	0.4	113
t_{PHZ}	- OE	В	2	28.7	1.6	9.7	1.4	8	0.7	5.7	ns
t_{PLZ}	OL	В		20.7	1.0	9.1	1.4		0.7	5.7	115
t_{PZH}	- OE	А	0.7	5.5	0.7	5.5	0.7	5.5	0.7	5.5	ns
t _{PZL}	OL	A	0.7	5.5	0.7	5.5	0.7	5.5	0.7	5.5	115
t _{PZH}	- <u>0E</u>	В	1.6	27.6	1.3	11.4	1	8.1	0.9	6	ns
t _{PZL}	JL	В	1.0	27.0	1.3	11.4		0.1	0.9	O	115

Switching Characteristics

 $T_A = -55$ °C to 125°C, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see Figure 2)

PARAMETER	FROM	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V	V _{CC} = 2.5 V ± 0.2 V	V _{CC} = 3.3 V ± 0.3 V	V _{CC} = 5 V ± 0.5 V	UNIT
	(INPUT)	(OUTPUT)	MIN MAX	MIN MAX	MIN MAX	MIN MAX	
t _{PLH}	A	В	25.4	14.3	10	8.2	ne
t _{PHL}	^	Б	25.4	14.5	10	0.2	ns
t_{PLH}	В	Α	11	8.8	8.5	8.3	ns
t _{PHL}	В	Α	11	0.0	6.5	0.5	115
t_{PHZ}	ŌĒ	A	9.4	9.4	9.4	9.4	ns
t_{PLZ}	OL	Λ	5.4	9.4	9.4	3.4	115
t_{PHZ}	ŌĒ	В	32.7	13.7	12	9.7	ns
t_{PLZ}	OL	В	32.1	13.7	12	3.1	113
t_{PZH}	ŌĒ	Α	10.4	10.4	10.4	10.4	ns
t _{PZL}	OE .	A	10.4	10.4	10.4	10.4	115
t_{PZH}	 	В	31.6	19.3	12.6	10	ns
t _{PZL}	OE .	Б	31.0	19.5	12.0	10	115

Operating Characteristics

 $T_{\Delta} = 25^{\circ}C$

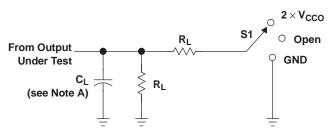
1A - 20	<u> </u>						
PARAMETER		TEST CONDITIONS	V _{CCA} = V _{CCB} = 1.8 V TYP	$V_{CCA} = V_{CCB} = 2.5 V$	V _{CCA} = V _{CCB} = 3.3 V	V _{CCA} = V _{CCB} = 5 V	UNIT
a (1)	A-port input, B-port output		2	2	2	3	
C _{pdA} (1)	B-port input, A-port output	$C_L = 0$,	18	19	19	22	
c (1)	A-port input, B-port output	f = 10 MHz, $t_r = t_f = 1 \text{ ns}$	18	19	20	22	pF
C _{pdB} ⁽¹⁾	B-port input, A-port output		2	2	2	2	

(1) Power dissipation capacitance per transceiver

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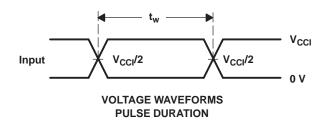
PARAMETER MEASUREMENT INFORMATION



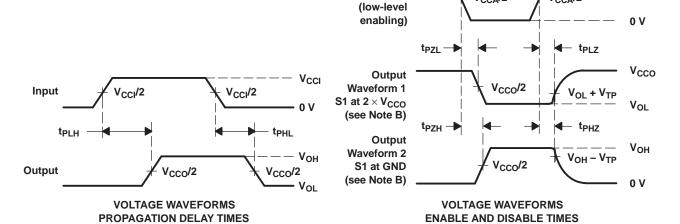
TEST	S 1
t _{pd} t _{PLZ} /t _{PZL}	Open 2 × V _{CCO}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

V _{CCO}	CL	R _L	V _{TP}
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V
5 V \pm 0.5 V	15 pF	2 k Ω	0.3 V



V_{CCA}/2



Output Control

- NOTES: A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $dv/dt \geq$ 1 V/ns.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. V_{CCO} is the V_{CC} associated with the output port.
 - J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

Product Folder Links: SN74LVC16T245-EP

 V_{CCA}

CCA/2





21-Mar-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
CLVC16T245MDGGEP	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
CLVC16T245MDGGREP	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
V62/12667-01XE	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples
V62/12667-01XE-T	ACTIVE	TSSOP	DGG	48	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	LVC16T245M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74LVC16T245-EP:

● Catalog: SN74LVC16T245

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVC16T245MDGGREP	TSSOP	DGG	48	2000	367.0	367.0	45.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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